A Design Methodology to Enable Sampling PLLs to Synthesise Fractional-N Frequencies

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***Abstract*—A novel design methodology is proposed to enable sampling phase-locked loops (SPLL) to synthesise fractional-N frequencies. To date, SPLL can only generate integer-N frequencies. The benefit is that the proposed SPLL has the advantages of both fractional-N phase-locked loop (FN-PLL) and SPLL, such as the faster frequency switching, a smaller phase jump and a larger loop gain. Since the frequency divider can be omitted in SPLL, the associated phase noise, power and hardware consumption can be ignored. Also, the design work is simplified, since the complex multi-phase frequency divider is not needed in the proposed fractional-N sampling phase-locked loop (FN-SPLL).**

I. Introduction

Phase-locked loop (PLL) based frequency synthesizers are widely used in modern RF/microwave systems. In general, they are employed as clock generators or local oscillators (LO) to supply exactly the required frequencies. In comparison with integer-N PLLs, the fractional-N PLLs permit higher reference frequencies, faster frequency switching and lower phase noise [1]. Thus they are employed in modern communication systems more and more frequently, although the structure of the integer-N PLLs is simpler.

The pulse removal technique is one method to synthesise fractional-N frequencies. However, it produces too many fractional spurs [2]. Digital delta-sigma modulators (DDSM) [3] [4] are used to solve this problem. PLLs with DDSM are termed Delta-Sigma Fractional-N PLLs [5]. C. Park [6] introduced a new architecture for fractional-N PLL, which used a multi-phase voltage-controlled oscillator (MP-VCO) and a multi-phase frequency divider to do phase interpolation. This new architecture achieves a smaller phase jump and less phase noise than the traditional delta-sigma fractional-N PLLs. C.-H. Heng [7] used a DDSM as the controller of the multi-phase frequency divider to randomise the interpolated phases. Then the problem of phase mismatching and spurs is effectively reduced. S. Pamarti [8] added an FIR filter in the divider controller to eliminate spurs in the multi-phase fractional-N PLLs.

The design of frequency dividers has become more and more difficult and complex, especially with the inclusion of the multi-phase interpolation technique. Fortunately, frequency dividers may be omitted in sampling PLLs. Thus the noise, power and hardware consumption of frequency dividers can be ignored in the design process or analysis. Also, the noise from the phase detector and the charge pump will be reduced to $1/N^2$ of the original noise density [9], where N is the divisor of a frequency divider in the conventional PLL. However, the conventional SPLL is not able to synthesise fractional-N frequencies and thus cannot achieve the advantages of fractional-N synthesizers just mentioned. Consequently, it is to overcome this stumbling block for SPLLs that the work in this paper is addressed.

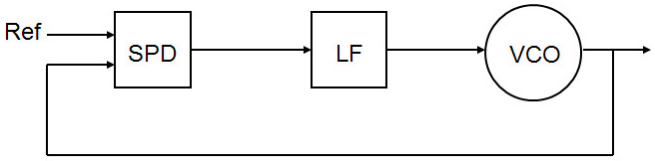

Fig. 1. Sampling phase-locked loop.

The paper is arranged as follows. In Section II, the operation of the conventional integer-N sampling PLL is described. The condition required to synthesise fractional-N frequencies is introduced in Section III-A. The method to achieve the condition by using the phase interpolation technique is proposed in Section III-B. In Section III-C, an example is given to further illustrate the proposed design method. In Section IV, simulation results are shown to demonstrate the proposed design method. The conclusion is given in Section V.

II. Background to Sampling PLL

The diagram of the SPLL is illustrated in Fig. 1. The key difference between the SPLL and the conventional PLL is that the SPLL exploits a sample & hold as the sampling phase detector (SPD) [10]. The SPLLs have three advantages [11]: Firstly, the frequency divider and loop filter can be omitted. Thus their phase noise, power and hardware consumption can be ignored. Secondly, the spectral purity is quite good, since the SPD output is a pure DC signal, which reduces the reference frequency modulation. Thirdly, the SPLL has no dead zone when it is locked.

As shown in Fig. 2(a), the VCO output and reference signal are the two inputs of the SPD, and V_{sam} is the output. It is assumed that a PMOS transistor works as the analog switch,

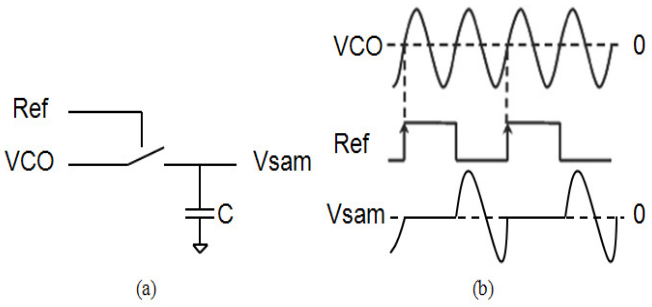

Fig. 2. Sampling phase detector: (a)diagram (b)waveform.

then the rising edge of the Ref is the sampling edge. At this instant, the sampling switch is opened and the sine wave V_{VCO} is sampled by the square wave Ref, i.e., V_{sam} is kept at a constant value equal to the value of V_{VCO} at the Ref rising edge. The falling edge of the Ref is the tracking edge. The switch is closed at this instant, and V_{sam} equals to V_{VCO}, as shown in Fig. 2(b).

Generally, the zero-crossing point of the V_{VCO} is a DC voltage, it is assumed as 0 here to aid understanding. If $V_{sam} \neq 0$, it will adjust the VCO frequency until the zero-crossing point of V_{VCO} and the rising edge of Ref are aligned, i.e., V_{sam} always equals to 0 when it is sampled as shown in Fig. 2(b). At this moment, the VCO frequency will not be changed, and the SPLL is locked. Note that they will be aligned only if the frequency ratio of V_{VCO} and Ref

$$\lambda = f_{VCO}/f_{Ref} \tag{1}$$

is an integer.

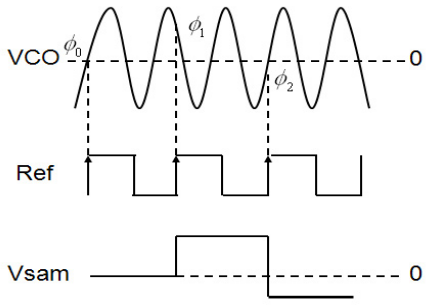

Fig. 3. Waveform of fractional-N frequency.

III. Fractional-N Sampling PLL

A novel design methodology is proposed in this section to enable the SPLL to generate fractional-N frequencies.

A. Fractional-N Frequencies

As illustrated in Fig. 3, if the frequency ratio of VCO and Ref is a fraction

$$\lambda = f_{VCO}/f_{Ref} = N + \alpha \tag{2}$$

where N is an integer and $0 < \alpha < 1$, the value of V_{sam} changes at every rising edge of Ref. If the phase of V_{VCO} at the first rising edge of Ref is assumed as 0, then the phases at the later rising edges are

$$\phi_n = (N + \alpha) \cdot 2\pi \cdot n \tag{3}$$

where $n = 1, 2, 3, ...$ The differences between any two adjacent phases are same:

$$\begin{aligned} \phi_n =& \phi_{n-1} + (N + \alpha) \cdot 2\pi \\ =& \phi_{n-1} + 2\pi N + \Delta_\phi \end{aligned} \tag{4}$$

where

$$\Delta_\phi = 2\pi\alpha. \tag{5}$$

If every ϕ_n is changed to ϕ'_n manually in order to achieve

$$\sin(\phi'_n) = \sin(\phi_{n-1}) \tag{6}$$

the zero-crossing point of V_{VCO} and rising edge of Ref are aligned[1] without changing the value of λ, as shown in Fig. 4. Then ϕ'_n is obtained as

$$\phi'_n = \phi_{n-1} + 2\pi \cdot i \tag{7}$$

where $i = 0, 1, 2....$ Since ϕ'_n should be the nearest value to ϕ_n, here i is set as

$$i = N. \tag{8}$$

Substitute (8) into (7) and combine with (4) and (5), it is obtained

$$\phi'_n = \phi_n - \Delta_\phi. \tag{9}$$

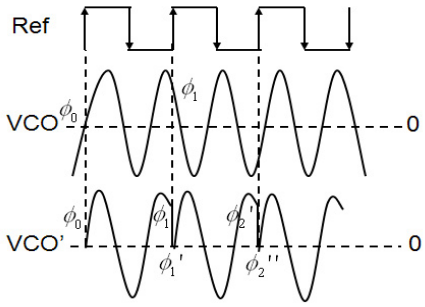

Fig. 4. Waveform of the modified VCO output.

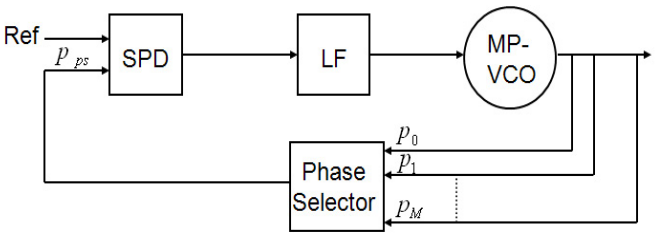

Fig. 5. Fractional-N sampling phase-locked loop.

[1] V_{sam} has two solutions here, since V'_{VCO} has two values at the Ref rising edge, as shown in Fig. 4. This issue will be resolved in Sec. III-B.

B. Phase Interpolation

Equation (9) can be achieved by the phase interpolation technique. The diagram of the proposed architecture is shown in Fig. 5. A multi-phase voltage-controlled oscillator (MP-VCO) with $(M+1)$ outputs is employed instead of the conventional single-phase VCO. The expression for the outputs of the MP-VCO is

$$p_m = A\sin(\omega t + \theta_m) \tag{10}$$

where A and ω are the amplitude and angular velocity, respectively, θ_m denotes the initial phase of the mth output signal and $m = 0, 1, ..., M$. Note that the $(M+1)$ output signals have the same amplitude and angular velocity, and their initial phases form an arithmetic progression

$$\begin{aligned}\theta_m - \theta_{m-1} =& \theta_{m-1} - \theta_{m-2} \\ =& \Delta_\theta\end{aligned} \tag{11}$$

where

$$\Delta_\theta = \frac{2\pi}{M+1}. \tag{12}$$

The waveform of the outputs of an 8 outputs MP-VCO is illustrated in Fig. 6. In this case, $M = 7$ and $\Delta_\theta = \pi/4$.

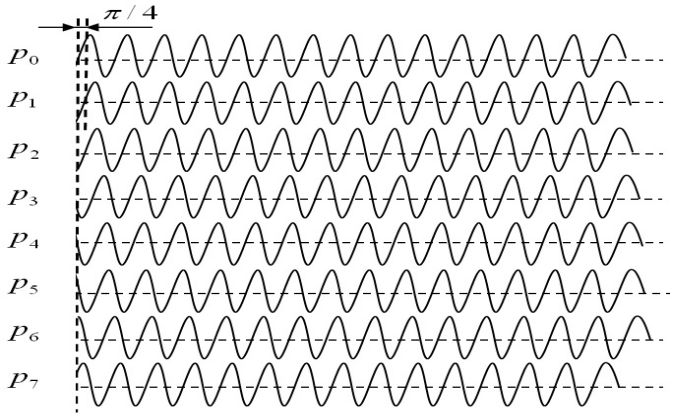

Fig. 6. Outputs of the 8 phase MP-VCO.

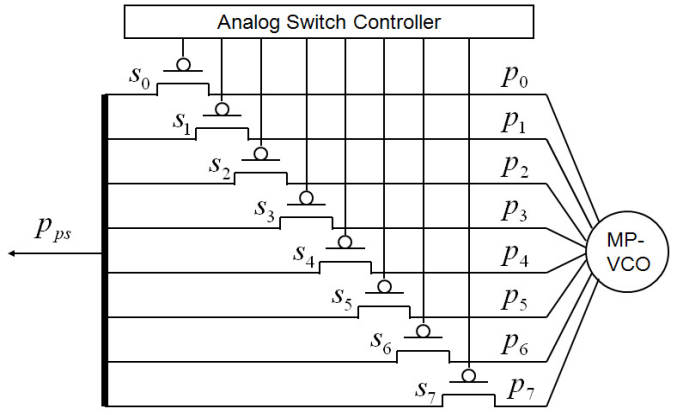

Fig. 7. The phase selector with 8 inputs.

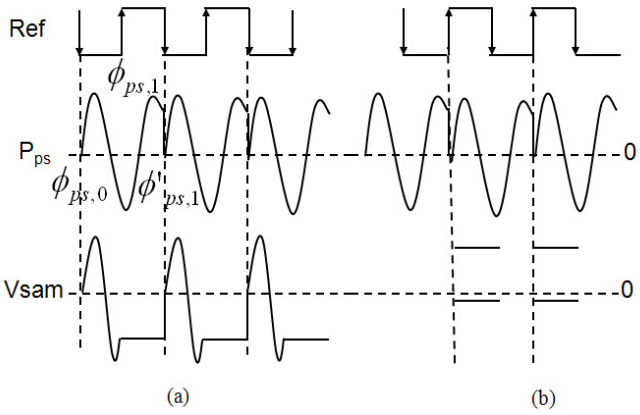

Fig. 8. Waveform of the SPD: the switches are switched at (a) tracking edges (b) sampling edges.

A phase selector is used to sort and align the $(M+1)$ signals as shown in Fig. 5. Then it is possible that the different outputs of the MP-VCO are sampled at each rising edge of the reference signal in the required order. The diagram of a phase selector with 8 inputs is illustrated in Fig. 7. There are 8 PMOS transistors used as the analog switches. They are all switched by the controller. The controller turns on different switches in the required order at each Ref falling edge as shown in Fig. 8(a). The order is arranged according to the value of the fractional factor α. Note that there is only one analog switch turned on at one moment and the switches must be switched at the tracking edges (falling edges). Since the 8 signals have the same amplitude and angular velocity, if they are aligned well at the Ref falling edges, the phases at the Ref rising edges are the same. If the analog switches are switched at the sampling edge (rising edge), the V_{sam} has two values as shown in Fig. 8(b). Hence, it is preferable to switch at the falling edge.

C. Case Study

A simple example is given here to illustrate the arrangement of the order to turn the different switches on. The MP-VCO has 8 outputs in this example. The frequency ratio of the VCO output and referent signal is set as 1.25, i.e., $N = 1$ and $\alpha = 0.25$. Firstly, the first switch s_0 is switched on, then $p_{ps} = p_0$. The phase of p_{ps} at the first rising edge of Ref, $\phi_{ps,0}$ equals to that of p_0 at the same moment. Recall equation (4) and (5), the phase of p_{ps} at the second rising edge is

$$\begin{aligned}\phi_{ps,1} =& \phi_{p0,1} \\ =& \phi_{p0,0} + 2\pi + \Delta_\phi\end{aligned} \tag{13}$$

where

$$\Delta_\phi = \frac{\pi}{2} \tag{14}$$

as shown in Fig. 8(a). Substitute (13) into (9), the phase of p_{ps} at this moment should be modified to

$$\phi'_{ps,1} = \phi_{p0,0} + 2\pi \tag{15}$$

equalling,

$$\phi'_{ps,1} = \phi_{p0,1} - \Delta_\phi \tag{16}$$

such that the frequency ratio is kept as 1.25. Since the phase difference between the adjacent VCO outputs is $\Delta_\theta = \pi/4$ due to (12) in this case, the phase difference between p_0 and p_2 can achieve the required Δ_ϕ

$$\begin{aligned}\phi_{p2,1} =& \phi_{p0,1} - 2\Delta_\theta \\ =& \phi_{p0,1} - \Delta_\phi.\end{aligned} \tag{17}$$

Combining (16) and (17), it follows:

$$\phi'_{ps,1} = \phi_{p2,1}. \tag{18}$$

Thus the analog switch s_2 should be turned on at the second falling edge of Ref. With the same method, it follows that the switches should be turned on in the following order, $s_0 \longrightarrow s_2 \longrightarrow s_4 \longrightarrow s_6 \longrightarrow s_0$.... Note that the fractional factor α has to be the multiple of $1/(M+1)$. Otherwise, a solution of (18) cannot be found. This is the disadvantage of all phase interpolation based multi-phase fractional-N phase-locked loops.

IV. Simulation Results

The proposed method is verified by simulation in Matlab/Simulink. The reference frequency is 5 MHz and the desired VCO frequency is 6.25 MHz. Thus their frequency ratio is 1.25, $M = 1$ and $\alpha = 0.25$, as in the example above. Fig. 9 shows the frequency spectrum prior to locking and there are a lot of undesired frequencies, since the VCO frequency is being adjusted by V_{sam} at this stage. When the zero-crossing point of the phase selector output p_{ps} and the rising edge of reference signal are aligned, the SPLL is locked as shown in Fig. 10.

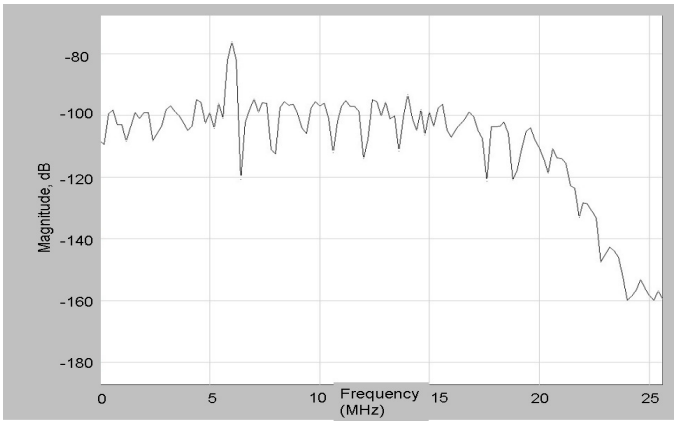

Fig. 9. Spectrum of the non-locked fractional-N SPLL.

V. Conclusion

A methodology has been proposed to enable sampling phase-locked loops to synthesise fractional-N frequencies. The novel PLL then has the advantages of both conventional SPLLs and fractional-N PLLs. The multi-phase frequency divider with a quite complex architecture can be omitted, and its phase noise, power and hardware consumption is ignored. The SPLL can achieve a smaller phase jump and faster frequency switching as is the case with multi-phase fractional-N PLLs. The disadvantage is that the fractional factor α depends on the number of VCO outputs. This issue will be addressed in future work.

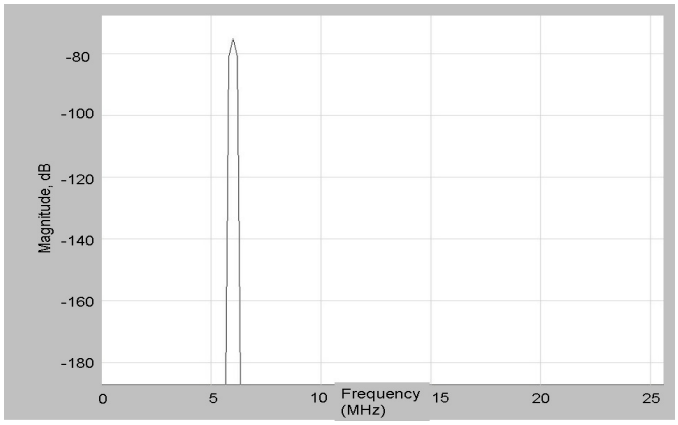

Fig. 10. Spectrum of the locked fractional-N SPLL.

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