The Development and Characterization of Novel Pd/Sn Ohmic Contacts to n-type GaAs

Thesis

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by

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DECLARATION

I hereby certify that this material, which I now submit for assessment on the programme of study leading to the award of Doctor of Philosophy is entirely my own work and has not been taken from the work of others save and to the extent that such work has been cited and acknowledged within the text of my work.

Signed: _____ **Date:** 25 February 1997.

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DEDICATION

To my parents
and
To my wife

Contents

List of Symbols

A	contact area
Å	metallization thickness
d	channel depth
E_C	conduction band minimum
E_F	Fermi level
E_V	valence band maximum
E_g	band gap
E_{oo}	tunneling parameter
g_m	transconductance
g_m(int)	intrinsic transconductance
g_{max}	maximum transconductance
h	Planck's constant
I_{GS}	gate current
I_{DS}	dram current
I_{DSS}	drain saturation current
J	current density
k	Boltzmann constant
L	separation between the contacts
L_c	contact length
L_T	transfer length
L_G	gate length
L_{GS}	gate-to-source distance
L_{GD}	gate-to-drain distance
m^*	electron effective mass
m	Sn to Pd thickness ratio
N_D	donor concentration
q	electronic charge
R_c	contact resistance
R_T	total resistance
R_{sh1}	sheet resistance of the active layer under the contact
R_{sh2}	sheet resistance of the active layer between the contacts
R_p	resistance of the interconnect wires

R_a	average surface roughness
R_S	series resistance
T	temperature
TIR	maximum peak-to-valley distance of the scanned surface
T_m	melting point
T_{an}	annealing temperature
V	voltage
V_P	pinch off voltage
V_B	built in potential
V_{DS}	drain-to-source voltage
V_{GS}	gate-to-source voltage
V_F	diode forward voltage
W	contact width
ρ_c	contact resistivity
$\Delta\rho_c$	measurement error
Ω	resistance
ϕ_B	barrier height
ε	dielectric constant of the semiconductor
ϕ_m	metal work function
ϕ_s	semiconductor work function

List of Abbreviations

AES	Auger Electron Spectroscopy
CHINT	Charge injection transistor
cTLM	Conventional transmission line model
DI	De-ionized
EDAX	Energy Dispersive Analysis of X-rays
FE	Field emission
FEM	Field Emission SEM
HEMT	High electron mobility transistor
HBT	Heterojunction bipolar transistor
I-V	current-voltage
LPMOCDV	Low pressure organometallic chemical vapor deposition
LED	Light emitting diode
MESFET	Metal semiconductor field-effect transistor
MQW	Multiple quantum-well
MODFET	Modulation doped field-effect transistor
MOVPE	Metal-organic vapor phase epitaxy
NERFET	Negative differential resistance field-effect transistor
RTA	Rapid thermal annealing
RTP	Rapid thermal processing
SEB	Scanned electron beam
SLS	Strained layer superlattice
SD	Switching diode
STM	Scanning Tunneling Microscopy
SEM	Scanning Electron Microscopy
SIMS	Secondary Ion Mass Spectrometry
SI	Semi-insulating
SDSR	Standard deviation of surface roughness
TE	Thermionic emission
TFE	Thermionic field emission
TEM	Transmission Electron Microscopy
TLM	Transmission line model
2DEG	Two-dimensional electron gas
XRD	X-ray diffraction

The Development and Characterization of Novel Pd/Sn Ohmic Contacts to n-type GaAs

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Abstract

A novel Ohmic contact system comprising of Pd/Sn metallizations has been developed for n-GaAs and systematically characterized using Scanning Tunneling Microscopy (STM), Scanning Electron Microscopy (SEM), Surface Profilometry measurements, Secondary Ion Mass Spectrometry (SIMS), Energy Dispersive Analysis of X-rays (EDAX) and current-voltage (I-V) measurements. Contact resistivities, ρ_c, of the proposed metallizations are measured utilizing a conventional Transmission Line Model (cTLM) method. The Pd/Sn metallizations show lowest ρ_c in the range of low 10^{-5} Ω-cm^2 on Si-doped ($2x10^{18}$ cm^{-3}) n-GaAs. A Au overlayer improves the characteristics of the Pd/Sn Ohmic contacts. The Pd/Sn/Au contacts display lowest ρ_c in the range of low 10^{-6} Ω-cm^2. The Pd/Sn and Pd/Sn/Au Ohmic contacts are very adhesive to the substrates. Both Pd/Sn and Pd/Sn/Au contacts exhibit improved characteristics when compared with alloyed Au/Ge/Au/Ni/Au contacts.

The Pd/Sn and Pd/Sn/Au metallizations show better thermal stability at 410 ^{0}C than non-alloyed Pd/Ge contacts. The Pd/Sn/Au metallizations also display better thermal stability than alloyed eutectic Au-Ge/Ni and Ni/Au-Ge/Ni contacts. However, at this temperature thermal stability of the Pd/Sn/Au metallizations is comparable to that of alloyed Au/Ge/Au/Ni/Au contacts. Long-term stability of the Pd/Sn/Au metallizations at 300 ^{0}C is comparable to non-alloyed Pd/Ge contacts. No change in surface morphology is observed after having been annealed at 300 ^{0}C for 400 h. At 300 ^{0}C, the Pd/Sn/Au metallization exhibits ρ_c which is slightly higher than those of the alloyed Au-Ge/Ni, Ni/Au-Ge/Ni and Au/Ge/Au/Ni/Au contacts.

GaAs Metal Semiconductor Field-Effect Transistors (GaAs MESFETs) have been fabricated using Pd/Sn and Pd/Sn/Au metallizations as source/drain contacts. MESFETs fabricated with Pd/Sn/Au Ohmic contacts display improved characteristics when compared to Pd/Sn contacts. MESFETs fabricated with Pd/Sn/Au contacts show comparable edge uniformity to non-alloyed Pd/Ge metallizations which is very important for VLSI GaAs devices. The newly developed, thermally stable, Pd/Sn and Pd/Sn/Au metallizations appear to be promising candidates for future GaAs device technology.

CHAPTER 1

Introduction

1.1 Introduction

The purpose of an Ohmic contact to a semiconductor is to allow electrical current to flow into or out of the semiconductor The contact should have a linear I-V characteristic, be stable over time and temperature, and contribute as little resistance as possible Simply placing a metal in contact with a wide bandgap III-V compound semiconductor, such as GaAs generally results in a rectifying contact (a diode) rather than an Ohmic one Therefore, achieving a stable, low-resistance Ohmic contact has been as much technical art as science, and this problem generated a large amount of research over several decades

Recent remarkable progress in semiconductor technology has made it possible to fabricate high performance GaAs devices [1] Although many useful contact schemes have been developed, further improvements in contact resistance are still necessary in order to keep pace with developments in the novel device design The primary requirements of Ohmic contacts are a low contact resistivity, an insignificant contact metal diffusion into the semiconductor both laterally and vertically, reproducibility, thermal stability and reliability

Advances in ultra-fast electronics and optoelectronics have considerably accelerated demand for GaAs devices in recent years This has been achieved through an improvement in GaAs device fabrication and processing techniques, new device structures and new circuit designs The need for a reliable and well-controlled Ohmic contact is central to the successful operation of almost all GaAs devices Achieving a low resistance Ohmic contact to GaAs is not trivial, and requiring in addition that the contact be thermally stable during subsequent processing at temperatures up to 400 ^{0}C (about 800 ^{0}C if the contact is to be used as a mask for dopant implants), morphologically uniform on the 0 1 μm scale and compatible with conventional lithographic patterning techniques, presents a formidable challenge Yet the development of low resistance contacts that meet these requirements is necessary for further miniaturization of devices such as the GaAs metal-semiconductor field-effect transistor (MESFET) shown in Fig 1 1 In this device, lateral encroachment of the

source and drain Ohmic contacts towards gate contact can occur during the contact annealing treatment, thereby limiting the minimum gate-to-source and gate-to-drain separation

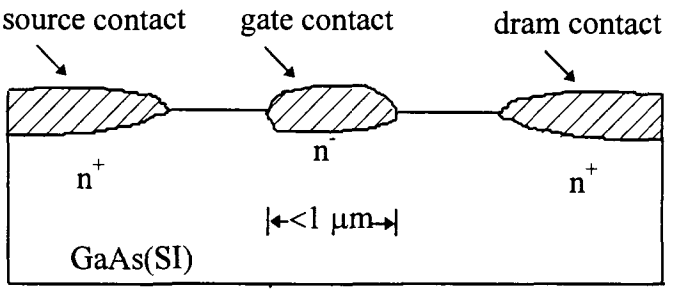


Fig 1 1 Schematic diagram of sub-μm GaAs-MESFET illustrating the demands on contact metallizations [2]

In the MESFET, the source and dram resistances are key parameters that determine its performance The source resistance strongly affects the device transconductance and noise figure An increase in both source and dram resistances tends to increase the power consumption and slow down device operation Low contact resistivity is also required in efficient optoelectronic devices both from the point of view of power consumption and heat dissipation

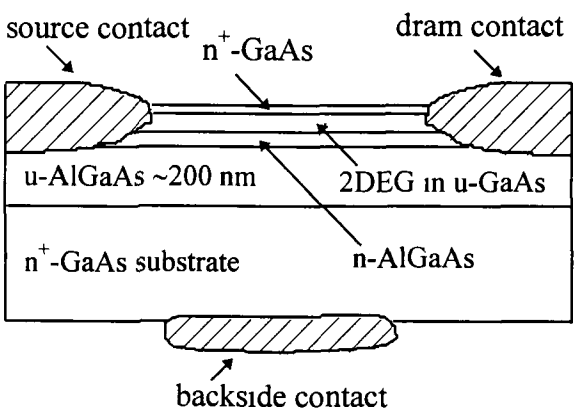


Fig 1 2 Schematic diagram of the NERFET illustrating the demands on contact metallizations [3]

The scaling of GaAs devices to submicrometre dimensions imposes more stringent requirements on the electrical and metallurgical characteristics of Ohmic contacts The morphological constrains on low resistance contacts are even more severe for heterojunction devices in which the current is confined in the form of a two-dimensional electron gas (2DEG) at the buried interface (e g GaAs-$Al_{1-x}Ga_xAs$) For example, the source and dram contacts in the negative differential resistance field-effect transistor (NERFET) [3] (Fig 1 2) must make contact with the buried 2DEG without

penetrating the thin (about 200 nm) $Al_{1-x}Ga_xAs$ barrier layer Even a localized penetration will introduce a path for excessive leakage current and render the device inoperable

Smaller intrinsic resistances make the problem of low contact resistivity more acute For Gunn diodes and LEDs, contact resistivity, $\rho_c = 10^{-3}$-10^{-5} Ω-cm^2 has been adequate since the Ohmic contacts employed in these devices are realtively large in area and the resulting contact resistivity can easily be smaller than a few Ohms For MESFETs with 1 μm gate, a ρ_c of mid 10^{-6} Ω-cm^2 may suffice, but for sub-μm devices, where the semiconductor channel resistance is lower by more than a factor of two, the ρ_c should be reduced to low 10^{-6} Ω-cm^2

From the point of view of metallurgical characteristics, requirements for fine pattern capability and precise control of the penetration depth of the Ohmic contact have become crucial Modern device designs require contacts with morphological uniformity such that lateral depth definition and depth of penetration of the metallization can be controlled to within tens of nanometres Fine pattern capability is necessary for minimizing gate-to-source spacing in all types of field-effect transistors To realize the high dc current gain, high speed and high microwave cut-off frequency capabilities of thin base heterojunction bipolar transistors (HBTs), vertical scaling of the Ohmic contact is necessary to avoid contact penetration into the adjacent active region of the HBT In the case of a high electron mobility transistor (HEMT), a rigid control is required on the vertical scaling of source and drain contacts providing an Ohmic contact directly to the 2DEG channel [1]

It is clear therefore that with ongoing miniaturization and integration of GaAs devices, the ever-increasing demand for high performance Ohmic contacts is one of the more challenging problems in GaAs IC technology Many reports describing Ohmic contacts to GaAs already exist in literature, including a number of reviews The reviews by Rideout [4], Popovic [5] and Piotrowska [6] present a theoretical treatment as well as a summary of research activities prior to 1983 Shen et al [7] very concisely treated a number of basic issues related to Ohmic contacts on GaAs The role of interfacial reactions in Ohmic contact formation is described by Piotrowska [8] and Sands [2] Additionally, information regarding Ohmic contacts can also be found in a number of reference books [9-12]

The remainder of this chapter is concerned with a brief discussion of Ohmic contact formation mechanisms This will be followed by a detailed review of recent and important research activities related to Ohmic metallizations for n-GaAs Different

Ohmic contact schemes will also be summarized for various GaAs device applications The relative advantages and disadvantages of each contact scheme will be pointed out Finally, the organisation of this thesis will be presented

1.2 Ohmic Contact Formation Mechanisms

An Ohmic contact is defined as a metal-semiconductor (M-S) contact that has a linear current-voltage (I-V) characteristics and also has a negligible contact resistance relative to the bulk or spreading resistance of the semiconductor A satisfactory Ohmic contact should not significantly perturb device performance and it can supply the required current with a voltage drop that is sufficiently small compared with the drop across the active region of the device If R_c is the contact resistance and A is the contact area then the contact resistivity ρ_c is given by the product of R_c and A When evaluated at zero bias, this ρ_c is an important figure of merit for Ohmic contacts A formal definition of ρ_c is usually given as

$$\rho_c = \left\{ \left(\frac{\partial J}{\partial V} \right)_{V=0} \right\}^{-1} \quad (\Omega\text{-cm}^2), \tag{1 1}$$

where J=current density (ampere/cm^2) and V=applied voltage across the contact (volts)

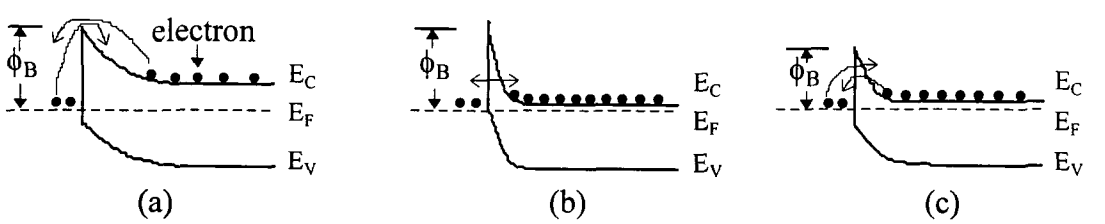


Fig 1 3 Ohmic contact formation mechanisms (a) TE, (b) FE and (c) TFE The conduction band minimum, Fermi level and valence band maximum are indicated by E_C, E_F and E_V, respectively

Basically, there are three mechanisms [9] which govern the current flow in a M-S contact These mechanisms are described below very concisely

- **Thermionic emission (TE):** dominant in moderately doped semiconductors, N_D<(~10^{17} cm^{-3}) In this case, the width of depletion region is relatively wide, implying that the probability of electrons tunneling through the barrier is rather small If the barrier height (ϕ_B) is small, the electrons can easily surmount the top of the low barrier by thermionic emission (Fig 1 3(a)) For low doped or high-barrier

semiconductors, the vast majority of electrons are unable to overcome this barrier in either direction and result in non-Ohmic (rectifying) contacts

- **Field emission (FE):** effective in heavily doped semiconductors, N_D>(~10^{18} cm^{-3}) For this situation, the depletion region is so narrow that electrons can easily tunnel through the barrier and tunneling is the dominant transport mechanism (Fig 1 3(b))
- **Thermionic-field emission (TFE):** applicable for intermediately doped semiconductors, (~10^{17} cm^{-3})<N_D<(10^{18} cm^{-3}) Both thermionic and tunneling are significant as shown m Fig 1 3(c)

For each of these three mechanisms, the contact resistivity ρ_c can be calculated with the help of a very useful parameter kT/E_{oo} introduced by Yu [13], where

$$E_{oo} = \frac{qh}{4\pi}\sqrt{\frac{N_D}{\varepsilon m^*}} \tag{1 2}$$

E_{oo} is the tunneling parameter, q is the electronic charge, h is the Planck's constant, N_D is the donor concentration, ε is the dielectric constant of the semiconductor, and m^* is the electron effective mass

For kT/E_{oo}>>1, i e for moderate N_D, the TE mechanism dominates the current conduction and the contact resistivity is given by

$$\rho_c \propto \exp\frac{q\phi_B}{kT} \tag{1 3}$$

From eqn (1 3), it is clear that the contact resistivity is dependent on temperature At higher temperatures, the thermionic emission current increases resulting m a smaller ρ_c

For kT/E_{oo}≈1, i e for intermediate N_D, a mixure of both thermionic and tunneling mechanisms (TFE) is observed and the contact resistivity is

$$\rho_c \propto \exp\frac{q\phi_B}{E_{oo}\coth\frac{E_{oo}}{kT}} \tag{1 4}$$

It is seen that the contact resistivity depends on both the temperature and the transmission coefficient for tunneling

For kT/E_{oo}<<1, i.e for heavy doping concentrations, contact resistivity becomes

$$\rho_c \propto \exp\frac{q\phi_B}{E_{oo}} \tag{1 5}$$

In this case, ρ_c depends strongly on doping concentration and the field emission (FE) mechanism prevails As the doping concentration is increased further, the depletion width of the Schottky junction decreases resulting in an increase of the tunneling transmission coefficient Hence, even a metal with a high barrier to the semiconductor can form an Ohmic contact

If a large number of surface states exists in the semiconductor, the Fermi level is pinned and the barrier height is independent of the metal work function This is the Bardeen limit [14] which stands in contrast to the Schottky limit where the metal-semiconductor contact is assumed ideal and the surface states are ignored In practice, the surface Fermi levels of most III-V compound semiconductors are pinned somewhere in the gap, which is what determines the barrier height It can then be concluded that the barrier height depends not only on the gap of the semiconductor, but also on the surface state density

Three main approaches have been used to obtain low ρ_c Ohmic contacts on n-GaAs These three approaches are described below very briefly

- **Contacts to very small band gap semiconductors:** When a metal is brought into contact with a semiconductor, the Fermi levels in the metal and semiconductor must align under equilibrium conditions (Fig 1 4(a)) If the work function of the metal (ϕ_m) is smaller than the work function of the semiconductor (ϕ_s), the Fermi levels are aligned by transferring electrons from the metal to the semiconductor This raises the semiconductor electron energy relative to the energy of electrons in the metal at equilibrium The Fermi level is pinned in the conduction band of the small band gap material, for example InAs (E_g~0 36 eV) (Fig 1 4(b)), therefore, the junction has a very small ρ_c, in the range of 10^{-7}-10^{-8} Ω-cm^2 (TE mechanism) [15]
- **Contacts in the case of low barrier height and heavily doped semiconductors:** This approach is also successful for attaining low ρ_c (TFE mechanism) For example, contacts made on n^+-InGaAs (E_g~0 75 eV)/GaAs exhibit a contact resistivity in the range of 10^{-6}-10^{-8} Ω-cm^2 (Fig 1 4(c)) [16,17]
- **Contacts in the case of heavily doped semiconductors:** The heavier the doping at the semiconductor surface, the thinner the barrier width, and carriers can tunnel more easily between the metal and the semiconductor (FE mechanism) (Fig 1 4(d)) Contacts made on GaAs (E_g~1 42 eV) with a surface doping of 10^{18}-10^{20} cm^{-3} fall into this category Contact resistivities in the range of 10^{-5}-10^{-7} Ω-cm^2 are generally obtained [18-21]

In particular, the contact resistivity depends greatly on the doping level in the semiconductor, the barrier height of the metal-semiconductor combination, carrier effective mass, dielectric constant and temperature

In practice, the most widely used Ohmic contacts to GaAs today involve multicomponent metallization systems prepared by conventional deposition and annealing techniques Heat treatment is used to drive a suitable dopant from the metallization into the GaAs surface region to form a tunneling junction and/or to fabricate, in contact reaction, a suitable heterojunction with low effective barrier height

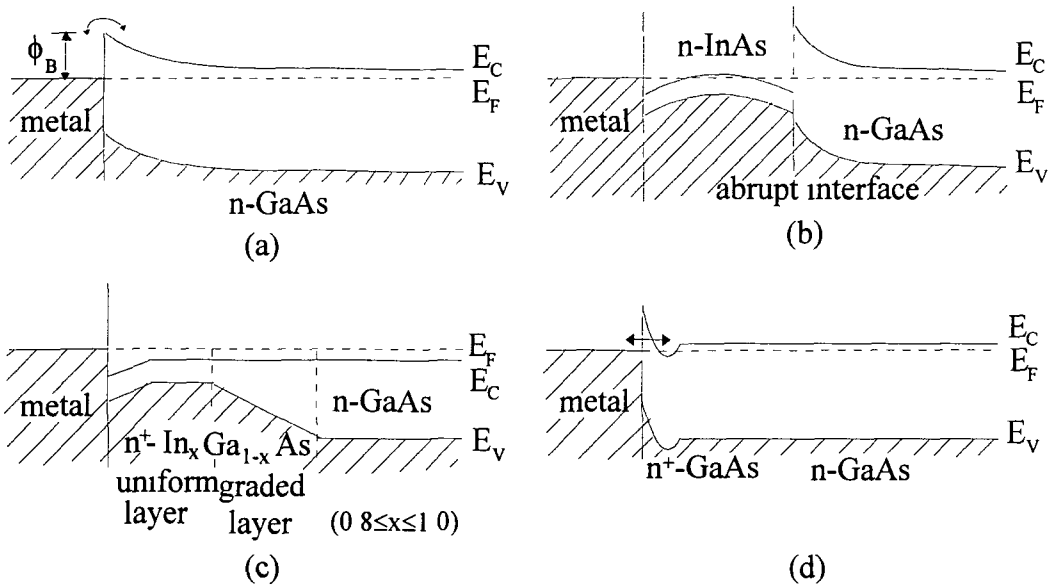


Fig 1 4 Schematic diagrams of band bending for various metal/semiconductor interfaces The conduction band minimum, Fermi level and valence band maximum are indicated by E_C, E_F and E_V, respectively

(a) The typical band line-up for metals deposited on air exposed n-GaAs {100} Under bias, electrons are transported by thermionic emission over the ~0 8 eV energy barrier [2]
(b) Band diagram for metal/n-InAs/n-GaAs [7]
(c) Band diagram for metal/n^+-$In_xGa_{1-x}As$ (0 8≤x≤1 0)/n-GaAs [17]
(d) Band diagram for metal/n^+-GaAs (heavily doped) [2]

1.3 Recent Developments of Ohmic Contacts

The most important areas of recent investigations into Ohmic contacts to n-GaAs are those involving the use of rapid thermal annealing (RTA) or rapid thermal processing (RTP), scanned electron beam (SEB) annealing, electroless deposition of metals, the δ-doped epilayer technique, development of refractory metallizations and the application of heavily doped and/ or small band gap materials [17, 18, 22-28] Metallizations containing dopant elements, such as Si, Ge and Sn for n-GaAs are preferred in order to

form heavily doped surface layers that are essential for low ρ_c contacts [19, 20, 29, 30] At high temperatures, out-diffusion of GaAs constituents occur Therefore, it is necessary to incorporate a barrier layer to reduce this outdiffusion A variety of materials have been used as barrier layers refractory metals (platinum, palladium, chromium, molybdenum, tungsten, etc) and related alloys (TiW, MoW, etc), and above all, low resistivity compounds (borides, nitrides, silicides, etc) [27, 31-35]

1.3.1 Pd/Ge and Ge/Pd metallizations

The Pd/Ge metallization scheme can provide Ohmic contacts with a low ρ_c similar to that obtained in AuGeNi contact systems Furnace annealing at 325 ^{0}C for 30 min is usually used to form Pd/Ge Ohmic contacts [18] However, it is often desirable to use an annealing process with shorter duration The Ohmic contact formation mechanism for the non-alloyed Pd/Ge or Ge/Pd contact can be explained by a solid-phase regrowth mechanism [19,36] The regrowth process begins with a limited low-temperature (~100 ^{0}C) reaction between the Pd and GaAs substrate to produce an intermediate Pd_4GaAs phase (Figs 1 5(a) and 1 5(b)) A subsequent reaction at a high temperature (~300 ^{0}C) between the Ge overlayer and the intermediate Pd_4GaAs phase results in the decomposition of the Pd_4GaAs phase and the epitaxial regrowth of a Ge-doped n^+-GaAs surface layer (Fig 1 5(c)) The excess Ge is then transported across the PdGe layer and epitaxially grows on the GaAs substrate (Fig 1 5(d))

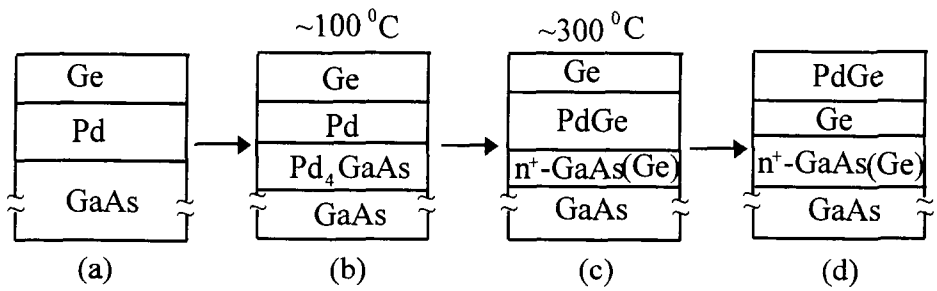


Fig 1 5 Shematic diagram of the regrowth mechanism using the Pd/Ge system [20]

Since Ge creates an n^+ doping on the GaAs surface upon annealing and Pd can decompose Ga and As oxides, Pd/Ge or Ge/Pd metallization systems have been extensively investigated on n-GaAs as possible Ohmic contacts [18, 20, 22, 31, 32, 37-49] There are additional but less notable advantages such as a lower barrier height for Ge/GaAs heterojunctions (~0 5 eV), compared to Pd/n-GaAs junctions where the Fermi level is generally pinned at ~0 8 eV In general, research has concluded that for a doping level in the low 10^{18} cm^{-3} range and a heat treatment of 325-375 ^{0}C up to 30 mm, a solid-phase reaction takes place producing contacts with ρ_c~10^{-6} Ω-cm^2 RTA or

RTP was reported to form good Ge/Pd and Pd/Ge contacts, having better surface morphology, better edge definition, lower ρ_c, high reliability for aging and exhibiting a shallow (non-spiking) nature [22, 37, 38].

Since Ge and Pd form compounds at low temperatures, the Pd/Ge or Ge/Pd contacts also exhibit $\rho_c \sim 10^{-6}$ Ω-cm^2 for doping concentrations of $\sim 10^{18}$ cm^{-3} [18, 40, 41, 44, 50]. The addition of a Au overlayer reduces sheet resistance of the metallization and facilitates Au wire bonding [51]. An optimum Ge/Pd metallization thickness with excess Ge (Pd~500Å, Ge~1265Å) can result in better ρ_c [18]. The same author found an increase in ρ_c, about one order of magnitude when the contacts were treated at 400 ^{0}C for 5 h. Scanned electron beam (SEB) annealing contacts [23, 52] gave better results than those of furnace annealing.

A number of fabrication techniques have been reported for improving the thermal stability of Ohmic contacts to GaAs. These approaches invariably depend on the use of a suitable Au diffusion barrier such as TiN [33], TiW [27], WSi [34], WN [35] and Pd [23]. Thermal stability and long-term stability of Pd/Ge Ohmic contacts have been studied by many authors [23, 31, 32, 38, 44, 51]. Ti/Pt/Au [31, 32], WN/Au [31], Ti/Pd/Au [53] and Ti/Au [21] overlayers improve the thermal stability of the Pd/Ge metallization. The Ge/Pd contact [44] was found to be stable at 300 ^{0}C for at least 50 h. An interdiffusion degradation model of this contact [44] was also proposed. Long-term stability was investigated by annealing the Pd/Ge/Au and Ge/Pd/Au contacts at 180 ^{0}C for 280 h [51]. No change in contact resistance or surface morphology was observed. The SEB annealed Au/Pd/Ge Ohmic contact exhibited good thermal stability after 25 h of aging at 500 ^{0}C [23]. Tsuchimoto et al. [38] investigated the long-term stability of Pd/Ge contacts and observed an increase in ρ_c from 1×10^{-5} to 1.2×10^{-5} Ω-cm^2 at 300 ^{0}C after 1000 h. This degradation is equivalent to a 10% deterioration in 10^9 years at 70 ^{0}C. Another model for the aforementioned degradation was also proposed [42].

The presence of Ni in Au/Pd/Ge contacts results in a reduction in the ρ_c and good surface morphology [23, 52]. This is because Ni by itself forms some Ni-Ge intermetallics and is known to enhance Ge diffusion into GaAs [54]. In addition, Ni prevents any interaction between Pd and Ge thereby enabling the Pd layer to effectively act as a Au diffusion barrier. The effectiveness of polyimide and rf sputtered SiO_2 passivation layers on the stability of a Au/Pd/Ni/Ge Ohmic contact [52] shows that both types of passivation provide good thermal stability. The operating life of this Ohmic contact for an eightfold increase in ρ_c is in excess of 100 000 h at room temperature

(300 K) High-temperature (800-900 °C) RTA is used to form Ge/Pd/W/Au Ohmic contacts [55] which are compatible with ion implantation activation processes

1.3.2 Pd/Ge/Ti/Pt metallizations

Pd/Ge/Ti/Pt appears to be an excellent candidate as an Ohmic contact for both n- and p-GaAs [56, 57] Contact resistivities in the range of mid 10^{-7} Ω-cm^2 are obtained for both n- and p-GaAs using RTA The Ti was added to the Pd/Ge contact primarily to promote the adhesion of the Pt to the contact and act as a diffusion barrier for the Pt The Pt layer was protected from the Pd and Ge layers so that it would not participate in the contact forming reactions and would therefore retain its smooth morphology Thermal stability of the contacts has also been studied [56, 57] The contact is stable at 300 °C for 20 h, but at 400 °C it is stable for only about 35 s

1.3.3 Pd/AuGe/Ag/Au metallizations

Shallow Ohmic contacts have been developed using Pd/AuGe/Ag/Au metallizations [58,59] The structure offers low resistivity (ρ_c~2x10^{-6} Ω-cm^2) Ohmic contacts with good adherence to the substrate in the temperature range from 400 to 500 °C The limited metal-GaAs reaction and the uniform interface morphology make the structure very attractive in large-scale integrated circuits The same metallization can be used for $Al_xGa_{1-x}As$ [58] which is very important for light-emitting diodes, laser diodes and other heterostructures

1.3.4 Pd/Si metallizations

This metallization system is in many ways similar to Pd/Ge, including a low ρ_c~10^{-6} Ω-cm^2 for similar doping levels if the Si/Pd ratio is equal to or greater than 0 65 [19] The Ohmic contact formation mechanism is described by many authors [2,7,8,19,40,44] The regrowth mechanism can be briefly summarized as shown in Fig 1 6 With a layer structure of Si/Pd/GaAs (Fig 1 6(a)), the regrowth mechanism begins with a low-temperature (~100 °C) reaction between a Pd layer and GaAs to form a stable Pd_xGaAs (x~4) ternary compound (Fig 1 6(b)) The reaction

$$xPd + GaAs \rightarrow Pd_xGaAs \qquad (1\ 6)$$

starts at the Pd/GaAs interface and at higher temperatures (about 200-275 °C) the reaction

$$Si + 2Pd \rightarrow Pd_2Si \qquad (1\ 7)$$

starts at the Si/Pd interface (Fig 1 6(c)) Since Pd_xGaAs and Pd_2Si have almost identical crystal structures, the ternary compound is loaded with Si via diffusion of Si atoms (Fig 1 6(d)) When Pd_xGaAs and Pd_2Si meet, the thermal stability of Pd_2Si then drives the reaction

$$2Si + Pd_4GaAs \rightarrow 2Pd_2Si + GaAs \qquad (1\ 8)$$

to the right in the presence of excess Si at the subsequent higher temperatures (≥300 °C) This reaction results in the epitaxial regrowth of a thin GaAs layer as a product of the above reaction on the GaAs substrate [36] During the regrowth process, Si atoms incorporated in the Pd_4GaAs layer are carried along into the GaAs lattice in this process In this manner, the regrowth layer is doped with Si atoms Equation (1 8), thus, is modified to be

$$2Si + Pd_4GaAs(Si) \rightarrow 2Pd_2Si + GaAs(Si) \qquad (1\ 9)$$

where $Pd_4GaAs(Si)$ and GaAs(Si) signify the doping of Si in these layers (Fig 1 6(e)) The thickness of this regrown layer is about 100Å In order for this regrown layer to be strongly n-type (≥$2x10^{19}$ cm^{-3}), Si atoms must preferentially occupy Ga vacant sites

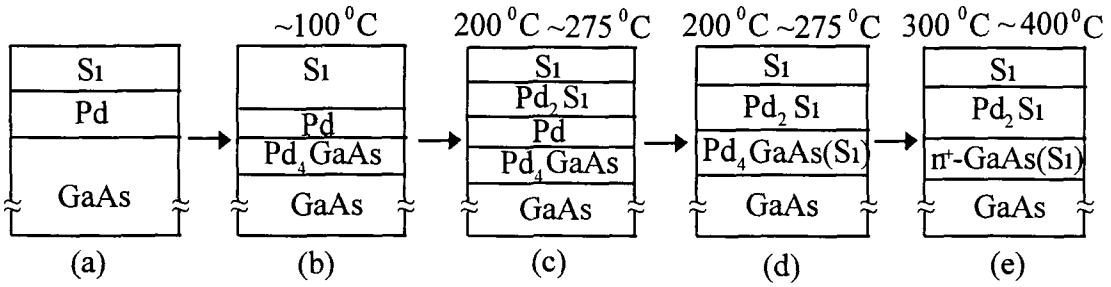


Fig 1 6 Schematic diagram of the regrowth mechanism using the Pd/Si system [40]

In terms of this regrowth mechanism, the significance of excess Si is evident Significant interaction between Pd_2Si and GaAs was observed at temperatures above 400 °C for the samples without excess Si [60] However, the presence of excess Si tends to drive eqn (1 9) to the right hand side, thus leading to Ohmic behaviour as well as forming a stable contact by preventing the Pd_2Si layer from reacting with GaAs The major difference between the Si/Pd/GaAs and Ge/Pd/GaAs systems is that epitaxial Ge is in contact with GaAs in the Ge/Pd/GaAs system, whereas Pd_2Si is in contact with GaAs in the Si/Pd/GaAs system However, both systems can result in Ohmic contact behaviour on n-GaAs with ρ_c in the range of 10^{-6} Ω-cm^2 on $1x10^{18}$ cm^{-3} n-GaAs From

this fact, it is clear that the epitaxial Ge (or a possible low barrier height at the Ge-GaAs heterojunction) is not essential for the Ohmic behaviour, but it may be responsible for reducing the contact resistance

The Pd/Si contact is stable at 300 °C for at least 50 h [44] The final layer sequence of Si/Pd/GaAs system is Si/Pd_2Si/GaAs The thermal stability of this system is related to the stability of the Pd_2Si/GaAs interface The importance of excess Si in the Pd/Si metallization is also reported [44] Excess Si is needed to form the n^+ layer for the contact to become Ohmic Excess Si also stabilizes the Pd_2Si/GaAs interface The excess Si may also stop the Ga and As out-diffusion because Si has been shown to be a good annealing cap for implanted GaAs [61]

1.3.5 Pd/In metallizations

The main motivation for considering In-based metallization is the resultant formation of the small band gap material InGaAs on GaAs which can improve ρ_c However, the reaction between In and GaAs without surface oxides starts above the melting point of In (156 °C), hence, formation of the liquid phase and possible oxides may lead to poor interface and surface morphologies Palladium forms several refractory compounds with Indium, such as InPd, In_3Pd, and In_3Pd_2, whose melting points lie between 700 °C and 1300 °C [62,63] Thus the thermal stability and morphology of Pd/In metallizations are improved Moreover, palladium deposited on GaAs increases the out-diffusion of gallium when heated, which facilitates the in-diffusion of doping species like Zn or Ge The same behaviour is expected for indium [47,63,64]

Ohmic contacts to n-GaAs based on Pd/In metallizations are reported by many authors [50, 65-69] The Ohmic contact formation mechanism of Pd/In metallization starts at low temperatute (~100 °C) At this temperature, a limited reaction occurs between Pd and GaAs to form Pd_4GaAs and between Pd and In to form $PdIn_3$ During subsequent exposure to high temperatures (>550 °C), the high melting point phase, PdIn, nucleates The reaction continues at higher temperatures to form PdIn resulting in the extraction of Pd from the interfacial layer of Pd_4GaAs and the regrowth of $In_xGa_{1-x}As$ The sequence of solid-phase reactions are as follows

$$4Pd + GaAs \rightarrow Pd_4GaAs \qquad (1\ 10)$$

(~100 °C, at the Pd/GaAs interface) and

$$3In + Pd \rightarrow PdIn_3 \qquad (1\ 11)$$

(~100 °C, at the Pd/In interface).
At higher temperatures (≥300 °C)

$$PdIn_3 + Pd_4GaAs \rightarrow PdIn + In_xGa_{1-x}As. \qquad (1.12)$$

(The In fraction x is significantly greater than 0 only above ~550 °C). Equation (1.12) is not balanced since the exact stoichiometry of the ternary compound Pd_4GaAs and the growth $In_xGa_{1-x}As$ layers are not known, although x is estimated to be ~0.4 for temperatures above 550 °C.

The effect of a thin Ge layer (2 nm) on Pd in Pd/In Ohmic contacts was investigated by Wang et al. [65]. Both contacts with and without Ge are stable in the low 10^{-6} Ω-cm² range at 400 °C for 48 h. Since the localized oxides prior to In deposition represent a problem, the use of a Pd, Ni, or Pt thin film to reduce the oxides has met with good results [66,67]. Formation of small band gap InAs on the GaAs was found in one In/Pt contact study [67]. A thermal study of the Pd/In contact [66] was carried out and the contact was seem to be relatively stable during anneals at 400 °C. A unique electroless method [63] which co-deposits Au-Pd-In and Pd-In onto an n-GaAs substrate has also lead to Ohmic contacts with ρ_c~$6x10^{-6}$ Ω-cm² in this case only for Pd-In after annealing at 470 °C for 2 min. A ρ_c of the order of ~10^{-6} Ω-cm² was obtained using both SEB and RTA processed Pd/In Ohmic contacts [68] with SEB annealed contacts exhibiting a superior surface morphology and thermal stability.

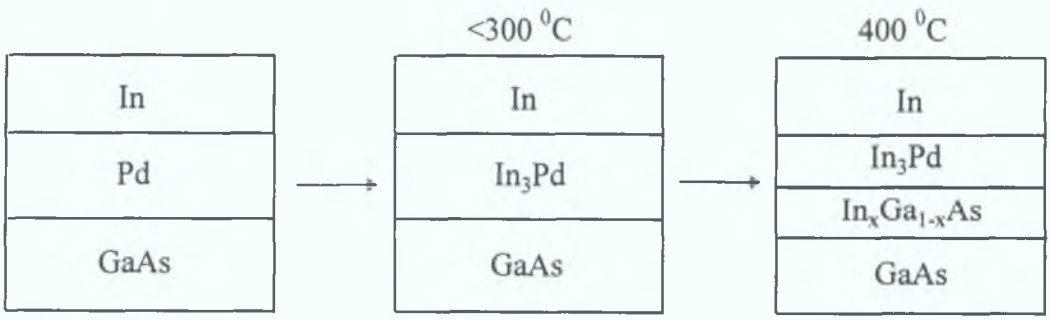


Fig.1.7.Schematic diagram of alloying sequence of Pd/In metallization to n-GaAs [70].

Very recently, Ma et al. [70] presented a growth mechanism for Pd/In contacts as depicted in Fig.1.7. Below 400 °C, it is proposed that In first reacts with Pd, developing a stable In_3Pd compound on the GaAs layer. This reaction continues until the Pd is entirely consumed. At 400 °C, solid-state diffusion occurs as excess In diffuses through the In_3Pd, forming a low resistive $In_xGa_{1-x}As$ compound with GaAs. The

$In_xGa_{1-x}As$ compound is believed to form an abrupt heterojunction with GaAs which restricts carrier transport more than the metal-$In_xGa_{1-x}As$ barrier and hence reduces the ρ_c values. Wang et al. [69] investigated Pd-In-Ge non-spiking Ohmic contacts to n-GaAs (10^{18} cm^{-3}). They observed that a layered structure of Pd/In/Pd/n-GaAs with 10-20Å of Ge embedded in the Pd layer adjacent to the GaAs can lead to a hybrid contact. When the Ohmic formation temperature was above 550 ^{0}C, a layer of $In_xGa_{1-x}As$ doped with Ge was formed between the GaAs structure and the metallization. When the annealing temperature was below 550 ^{0}C, a regrown layer of GaAs doped with Ge was formed at the PdIn/GaAs interface, giving rise to an n^+ surface layer and a tunneling junction as shown in Fig.1.8. The ρ_c of (2-3)x10^{-7} Ω-cm^2 for this contact structure is nearly independent of the contact area from 900 to 0.2 μm^2. This contact has been shown to be thermally stable up to a temperature as high as 600 ^{0}C.

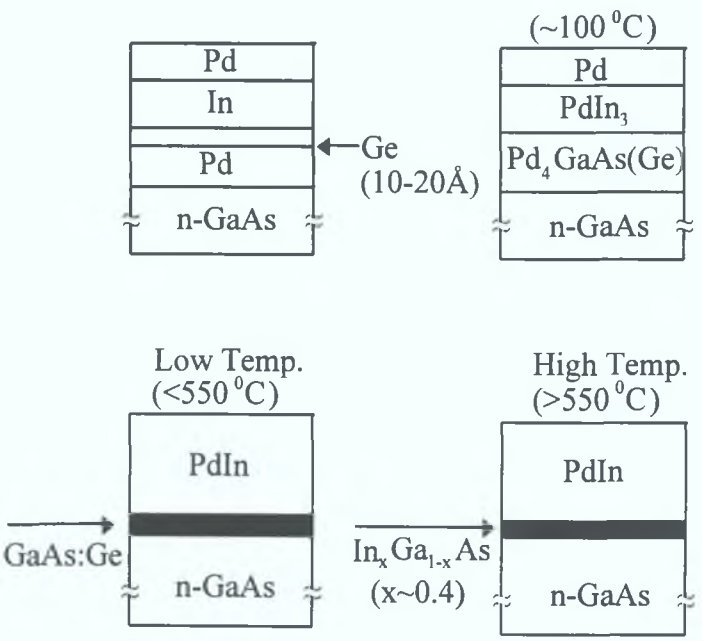


Fig.1.8. Schematic diagram showing the solid-phase reaction of the Pd/In/Pd(Ge) contact [69].

1.3.6 AuGe/Ni metallizations

Among Ni-based metallizations, eutectic AuGe/Ni is the most common contact material for n-GaAs [52, 71-80]. In this contact system, Ge serves to increase the surface doping, while Ni forms a barrier and a conductive NiAs compound. Two-stage annealing techniques can improve the overall performance of AuGeNi-based Ohmic contacts [71]. A pre-anneal can remove the inhomogeneity of the metal/GaAs interface [71]. Melting has been attributed to the β-AuGa phase modified by the other elements present. The addition of a Ti/Au cap also improves the topography of the annealed metallization but

contact resistivities are poorer [71]. RTP (RTA) is also a popular means to improve Au-based contacts [78-80]. AuGe/Ni non-alloyed Ohmic contacts have been formed on heavily doped n-GaAs layers activated by SiO_xN_y-capped infrared rapid thermal annealing (RTA) [78]. A further reduction in ρ_c has been accomplished by low-temperature (300 ^{0}C) alloying without melting the AuGe eutectic. Both conventional annealed and RTA AuGe/Ni contacts [80] have identical ρ_c values, but the interface reacted layer was wider for the first process.

Scanned electron beams (SEBs) have also been used for the alloying of AuGe/Ni metallization [52,77]. Capped alloyed AuGe/Ni contacts were found to have a higher resistance to degradation than uncapped alloyed AuGe/Ni contacts [52]. Capped AuGe/Ni contacts also exhibited longer operating life than uncapped contact structures for twofold, fourfold and eightfold increases in their ρ_c values. Cohen et al. [77] fabricated AuGe/Ni Ohmic contacts utilizing furnace and SEB annealing techniques. They observed that SEB-alloyed contacts exhibited less redistribution of contact constituents compared with furnace-alloyed contacts.

The importance of Ni to Ge ratio and of annealing cycle for the resistivity and morphology of AuGeNi Ohmic contacts to n-GaAs was investigated by Procop et al. [73]. The morphology of the contact layer at the minimum ρ_c was determined by the selected annealing cycle and by the Ni to Ge ratio. Goronkin et al. [72] used Ni/Ge/Au Ohmic contacts on GaAs and GaAs/AlGaAs. They did not observe any melting and lateral encroachment of the Ohmic metals alloyed at 460 ^{0}C. The use of Ni/Ge/Au Ohmic contacts on GaAs/AlGaAs with 460 ^{0}C, 8 min alloying cycles produced low-resistance contacts, no lateral encroachment, and sharp edge acuity. The AuGe/Ni contacts to n-GaAs [74] have mixed structure, composed of about 84% of n^+ n-contact and about 16% of the Schottky contact. The results obtained with AuGe/Ni and Ni/AuGe/Ni Ohmic contacts [75] indicate that the incorporation of Ge into GaAs occurs via solid-state diffusion and Ge distribution within the metallization layer differs in the two systems.

The effect of Ni as a first layer in the AuGeNi Ohmic contact was also reported [81]. The uniformity of the interface structure was greatly improved by the deposition of a 5 nm-thick Ni first layer due to its effects on kinetics of the alloying reaction (Fig.1.9). For sample A (without an initial Ni layer) Ni_3Ge is formed between AuGe and Au at temperatures below 420 ^{0}C. When the annealing temperature is higher than 440 ^{0}C, a reaction between Au and GaAs is initiated, followed by the diffusion of Ni_3Ge or the remaining Ni to the GaAs interface and the formation of a protruded NiAs(Ge) phase. The top layer is binary Au-Ga consisting of β-AuGa and β′-AuGa

phases with melting points of 375 °C and 347 °C, respectively The interface in this particular sample is nonplanar By contrast, in sample B (with an initial Ni first layer), the first layer Ni reacts with GaAs and forms Ni_2GaAs or Ni_3GaAs compounds at ~200 °C Above 400 °C, NiGa and NiAs develop An initial Ni layer clearly optimizes the alloying kinetics Alloying at a higher temperature, such as 600 °C, causes NiAs(Ge) grains to grow, resulting in dilution of Ge in the grains which then causes an increase in ρ_c The effect of the AuGe thickness in this metallization was also reported to have an impact on ρ_c [82] The same metallization has been utilized to find out the effect of AlAs mole fraction (x) on $Al_xGa_{1-x}As$ [43]

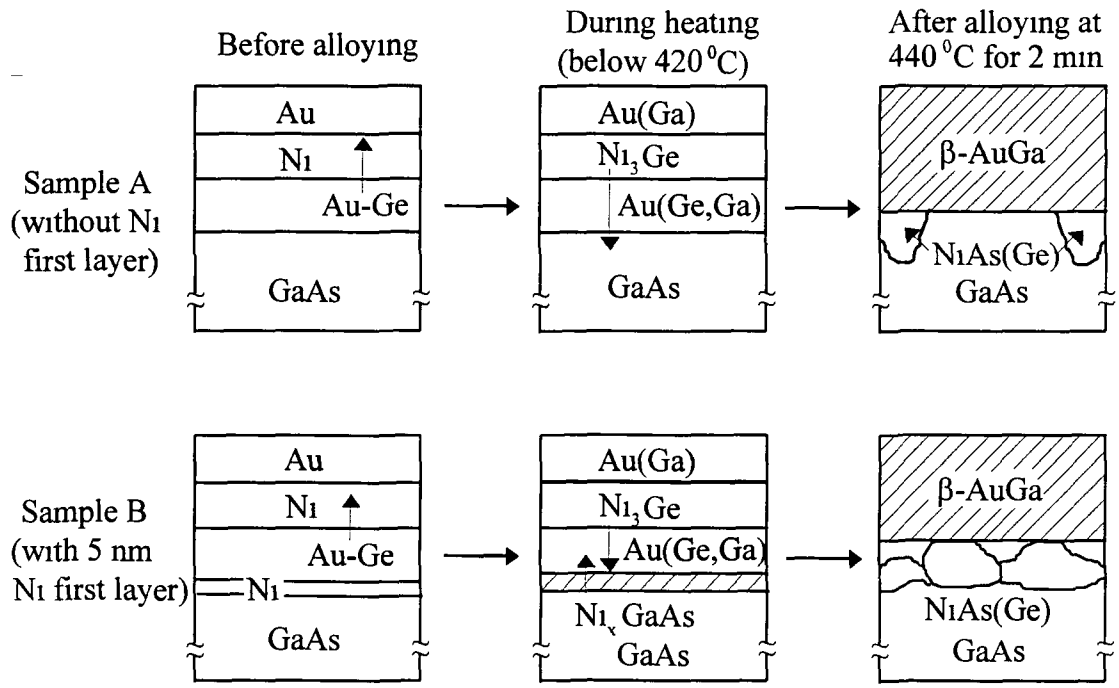


Fig 1 9 Schematic illustration of the sequence of alloying reactions for sample A and B, respectively [81]

A novel theoretical model for electron transport has been presented by Shenai [29] and extremely low ρ_c is reported using Ni/Ge/Au metallizations in Sn-doped n^+-GaAs layers The Ni/Ge/Au contact revealed extensive GaAs consumption [50] The ρ_c of Au/AuGeNi contacts formed by rapid electron-beam annealing [83] is much lower than that formed by other techniques The contacts formed by this technique are found to be considerably stable with thermal aging Ion beam mixing has been utilized to produce morphologically improved Ohmic contacts to n-GaAs using Ge/Ni/Au metallization [84] The values of ρ_c depend both on ion dose and ion implant temperature.

Solid-state and alloyed AuGeNi/ZrB_2/Au Ohmic contacts to n-$In_{0.53}Ga_{0.47}As$ have been investigated for optoelectronic integrated circuits [85] ZrB_2 acted as a diffusion barrier in these contacts Non-alloyed, high-temperature stable Ge-Ni-Au Ohmic contacts to n-GaAs with a LaB_6 diffusion barrier are also reported [86] The stable WSiN diffusion barrier (against gold) in Au/WSiN/(Au,Ge,Ni) metallization [87] resulted in alloying depth less than 10 nm and values of ρ_c in mid 10^{-7} Ω-cm^2 range The influence of the internal layer (Au,Ge,Ni) sequences on ρ_c is optimized and it is found that a combination of 25 nm Au, 5 nm Ni, 20 nm Ge resulted in lower ρ_c values Reproducible and thermally stable non-alloyed Ohmic contacts are achieved by interposing a $W_{60}N_{40}$ diffusion barrier between the Ni/Ge and the Au in Ni/Ge/Au system [35]

Both the contact uniformity and the resistivity of Ge/Au/Ni/Au Ohmic contacts may be greatly improved when a thin Ti/Au layer is deposited on the GaAs wafer backside prior to alloying [88] Ti/Au cap also improves the topography of Ni/AuGe/Ni/Au metallization [71] Very small area Ge/Au/Ni/Au contacts on GaAs have been reported [89] The proportions of Ni and AuGe in RTA AuGe/Ni/Au Ohmic contacts have also been optimized for low-temperature annealing [90] The annealing temperature for forming low ρ_c contacts to thin n^+ GaAs epilayers can be reduced from the standard 420 ^{0}C to 300-320 ^{0}C by varying the percentage of Ni in the contact Non-alloyed and alloyed low resistance Ni/Ge/Au/Ti/Au Ohmic contacts with good morphology for GaAs using a graded InGaAs cap layer have been developed [91] A low ρ_c of $4x10^{-8}$ Ω-cm^2 for a Ni/Au-Sn/Ni contact on n-GaInAs has also been obtained and compared with a Ni/Au-Ge/Ni contact [92] The Au-Ge contact shows better results than that of Au-Sn contact The contact resistivity and thermal stability of NiGe(Au)W Ohmic contacts were studied as a function of the Au layer thickness between 0 and 75 Å [93] A gold layer of ~60 Å produced a minimum contact resistance of 0 15 Ω-mm

1.3.7 Multilayer Au/Ge/Au/Ni/Au metallizations

A five-layer Ohmic contact structure [41,94] (Fig 1 10) annealed at 425 ^{0}C for 60 s using a RTA has the following advantages compared to conventional approaches

- The donor/acceptor layer is separated from the barrier layer This prevents undesired chemical reactions between the dopants and the barrier
- Evaporation of eutectic alloys containing the dopants is not necessary Thus fractional distillation in the evaporation process is avoided and the resulting contacts show better reproducibility.
- The top gold layer is sufficiently thick to permit bonding A post evaporation of gold over the alloyed area is not needed

- Only three metal evaporation sources are required to create the five-layer structure

Using this metallization contact resistivities in the 10^{-7} Ω-cm^2 range on both n- and p-type materials are obtained This metallization technique is applicable for fabricating a wide variety of microwave and lightwave devices including switching diodes and field effect transistors

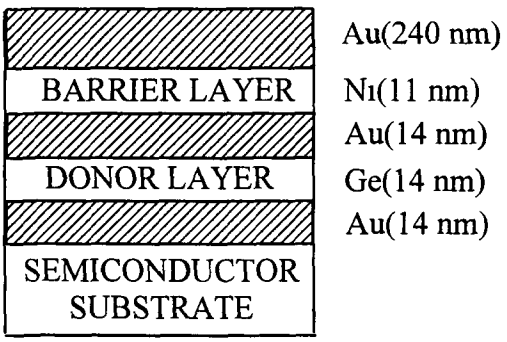


Fig 1 10 Cross-sectional view of five-layer Au/Ge/Au/Ni/Au metallization [94]

1.3.8 Ni/AuGe/Ag/Au metallizations

Silver (Ag) barrier Ohmic contacts are very important for GaAs based HEMT structures, such as AlGaAs/GaAs, AlGaAs/InGaAs and AlInAs/InGaAs It has been found that the Ohmic contact to GaAs based HEMTs requires high alloying temperature because the Ohmic metal has to penetrate the high band gap AlGaAs to reach the low band gap GaAs (or InGaAs) channel layer The conventional AuGe based Ohmic schemes (Ni/AuGe/Au) can not withstand high temperatures above 450 °C The sample alloyed at high temperature, in order to diffuse Ohmic metal deeply into the HEMT layer, may exhibit very rough morphology and high contact resistivity due to the interdiffusion between the top Au layer and substrate [95] To allow higher temperature alloying, researchers have added different diffusion barriers such as silicon nitride, TiW and silver to this alloyed metal system Among them the Ag diffusion barrier is one of the most popular approaches and has been used in most of the reported state-of-the-art HEMTs [96-99] Low resistance (≤0 1 Ω-mm) Ohmic contacts to the lower band gap material in both AlGaAs/GaAs and AlInAs/GaInAs MODFET structures can be fabricated using slightly different metallizations based on AuGeNi/Ag/Au [100] Ag in an AlGaAs/GaAs MODFET creates an Ag/Au alloy that reduces Ga outdiffusion from the semiconductor at temperatures up to ~570 °C In this way the GaAs stochiometry beneath the metallization is well maintained

1.3.9 Au/Ni/NiSn metallizations

These metallizations are electroplated to n-GaAs. Kelly and Wrixon [101] developed low temperature electroplated alloyed Au/SnNi/Au Ohmic contacts in 1978. They observed that layer thicknesses of 4000Å Au, 5000Å SnNi and 3500Å Au gave minimum ρ_c after alloying at 300 °C for 3 min. Tin (Sn) in a shallow donor and is 0.006 eV from the edge of conduction band in GaAs. This results in a barrier with a high tunneling probability. A SnNi/Ni/Au Ohmic contact scheme to n-GaAs has also been proposed [102]. Inclusion of a Pt layer to reduce Au (acceptor) diffusion into the contact results in higher ρ_c. In Au/Ni/SnNi/GaAs junctions, Sn is expected to diffuse into Au-induced Ga vacancies thereby producing an excess electron concentration [103]. Ni is expected to provide good wetting so that Sn does not "ball up" during the alloying process. This process is similar to that occuring for Au/Ni-Ge/GaAs contacts with Sn taking the place of Ge. The addition of Sn to Au/Ni/n-GaAs system lowers ρ_c by at least two orders of magnitude [103].

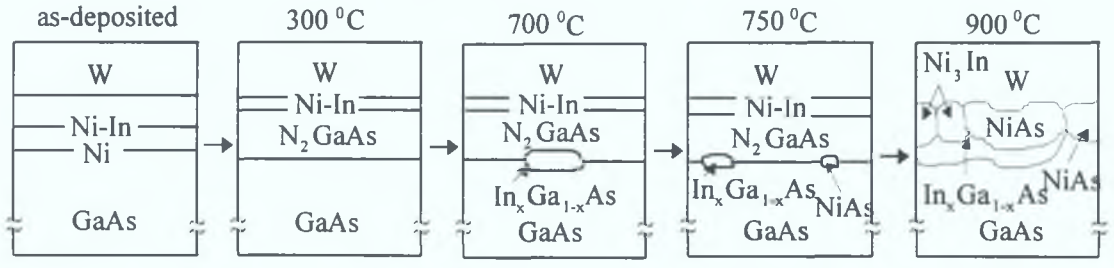


Fig.1.11. Schematic illustration of alloying sequence of Ni/Ni-In/Ni/W metallizations to n^+-GaAs [105].

1.3.10 NiInW metallizations

Rough surfaces and deteriorated contact edge profiles are observed in AuGeNi Ohmic contacts after annealing in forming gas at 440 °C for 2 min needed to form an Ohmic contact [81,104]. This limits extendability of this contact for use in submicron devices. NiInW Ohmic contacts have been developed which are very attractive for GaAs MESFETs because of improved morphology and thermal stability after Ohmic contact formation [105-109]. A typical example of the alloying sequence in the Ni/Ni-In/Ni/W metallization system [105] is illustrated in Fig.1.11. Initially, Ni from the upper layer diffuses into the Ni-In layer, forming a mixture of amorphous Ni-In and polycrystalline Ni phases. Under heat treatment at 300 °C for 30 min, an epitaxial Ni_2GaAs phase forms at the Ni/GaAs interface while In partially intermixes with W and Ni_2GaAs. At 700 °C, broad areas of $In_xGa_{1-x}As$ phase, with x=0.6, form at the Ni_2GaAs/GaAs interface.

Heating to 750 °C produces additional NiAs precipitates under Ni_2GaAs Further annealing at 900 °C leads to interfacial microstructures with large grains of regrown $In_xGa_{1-x}As$ with x=0 3 covering ~90% of the interface, the other 10% comprising of NiAs phase Ni_3In forms on top of the $In_xGa_{1-x}As$ phase, while the W layer remains above the NiAs and Ni_3In phases The W layer is usually inert and causes no electromigration problems in applications

A reduction in ρ_c for the NiInW metallizations has been obtained by adding donors to the contact material The Ni(Si)InW contacts with various Si concentrations were prepared and annealed at temperatures in the range of 750-900 °C for 2 s The lowest ρ_c value reached $8x10^{-7}$ Ω-cm² at 5% Si and an approximately 50% increase in the Si doping at the $In_xGa_{1-x}As$ (x=0 4) layer was believed to be achieved [106] Excellent stability in MESFETs with the NiInW Ohmic contacts was observed [105] No deterioration was observed at 400 °C for 180 h, 450 °C for 18 h and 500 °C for 2h The role of Ni on NiInW contacts was investigated [107] and it was found that Ni contributed to both a reduction of ρ_c and to improved thermal stability

The unreacted In after annealing is of great concern for thermal stability The unreacted In melts above 156 °C and the electrical properties of the contacts deteriorate To deposit In at the critical thickness is extremely difficult and is not practical The addition of an element which forms high melting point (T_m) compounds with the unreacted In improves thermal stability after contact formation and is attractive from the view point of the fabrication process Nickel is observed to form various Ni_xIn_y compounds which have T_m higher than 900 °C Ni_3In (T_m=908 °C), NiAs (T_m=962 °C) and $In_xGa_{1-x}As$ (T_m>900 °C) were observed in the Ni/Ni-In/Ni/W contacts and no evidence for the existence of unreacted In was obtained [107] A very low ρ_c in the range of 10^{-7} Ω-cm² was obtained with NiInW metallizations after annealing under As overpressure [108] Glas et al [109] reported a $Ni_4(GaAs)_3$ annealing product for the first time in NiInW contacts

1.3.11 Ni-based non-gold metallizations

Thermal instability is of serious concern for AuGeNi contacts utilized in very large scale integration (VLSI) devices As previously noted, this undesirable instability is due to formation of low melting point (T_m~375 °C) β-AuGa phases during contact annealing In order to improve the thermal instability of the AuGeNi contacts, Ni-based non-gold Ohmic contacts have been developed [110,111] The removal of Au from the AuGeNi contacts is effective in improving the thermal instability after contact formation as seen in NiGe contacts [110] The thermal stability of NiGe contacts is

strongly influenced by the compounds that are formed at the interface between the NiGe and the GaAs after contact annealing The compound formation is controlled by the Ge concentration in the NiGe contacts and the annealing temperature A contact with 38% Ge prepared by annealing at 600 °C had a smooth surface and yielded good thermal stability at 400 °C, which was due to the formation of refractory NiGe compounds with a melting point (T_m) of 850 °C

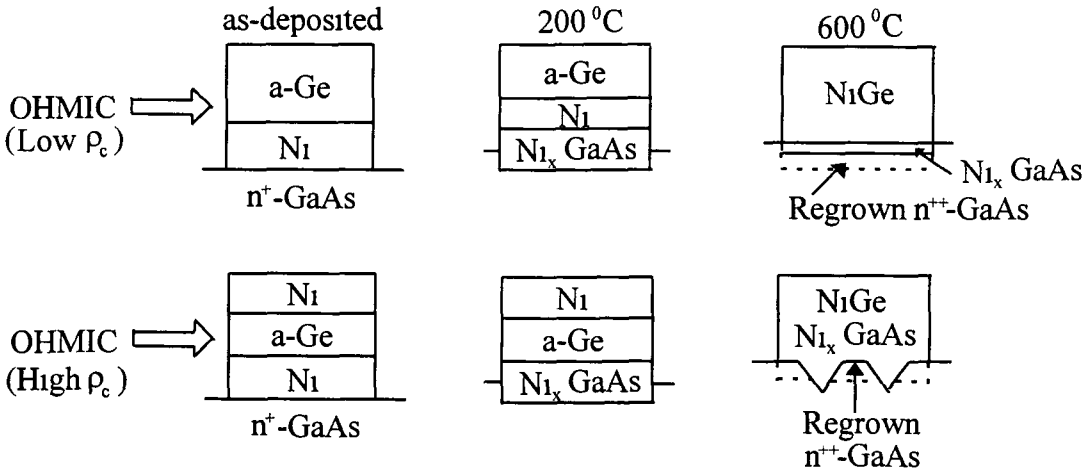


Fig 1 12 Schematic illustration of microstructural changes of NiGe Ohmic contacts, where a-Ge represents amorphous Ge [110]

A model for the electron transport mechanism through the GaAs/NiGe interface was also proposed by correlating the electrical properties and the microstructure The interfacial microstructure of the NiGe Ohmic contact with low ρ_c is discussed by referring to Fig 1 12 At the initial stages of annealing at 200 °C, Ni reacts with GaAs to form a ternary Ni_xGaAs compound by

$$xNi + GaAs \rightarrow Ni_xGaAs \qquad (1\ 13)$$

The thickness of the Ni_xGaAs layer increases with increasing the thickness of the Ni layer deposited directly on the GaAs After annealing at temperatures above 300 °C, Ni and Ge start to react, forming NiGe compounds When Ni in the Ni_xGaAs layer reacts with Ge, the thickness of the Ni_xGaAs layer reduces, leaving the regrown GaAs layer as shown by a dashed line in the bottom of Fig 1 12 This reaction is expressed by

$$Ni_xGaAs + Ge \rightarrow NiGe + GaAs \text{ (regrowth) [110]} \qquad (1\ 14)$$

When Ni reacts with GaAs forming the Ni_xGaAs layer, a small amount of Ge atoms diffuse to this ternary layer Some of the Ge atoms remain in the regrown GaAs,

resulting in formation of a n^{++}-GaAs layer The Ge-doped n^{++}-GaAs layer enhances carrier tunneling probability and Schottky behaviour transforms to Ohmic behaviour, leading to a reduction in ρ_c Thermally stable NiSiW Ohmic contacts to n-GaAs have been developed [111] Ohmic behaviour was found to have dependencies on the Si concentration of the NiSiW contacts and the annealing condition Ohmic contacts with 40% Si, prepared by annealing at 650 °C, had smooth surfaces and yielded excellent thermal stability during subsequent annealing at 400 °C after contact formation The cross sections of the NiSiW Ohmic contacts before and after annealing are shown in Fig 1 13 When the NiSiW contacts are annealed at temperatures above 300 °C, the Si atoms diffuse into the crystalline Ni layers to form amorphous nickel-silicon layers (indicated by a-Ni-Si) At higher temperatures, the a-Ni-Si layer close to the GaAs surface transforms into the crystalline structure that is indicated by c-Ni-Si The best candidate for this crystalline structure as determined by XRD measurements and TEM observation is δ-Ni_2Si

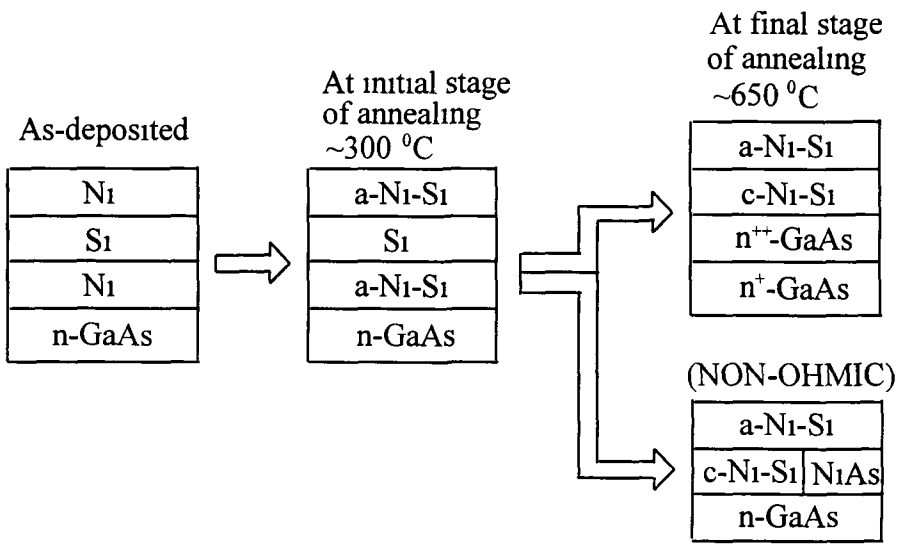


Fig 1 13 Schematic illustration of microstructural changes of NiSiW Ohmic contacts, where a-Ni-Si and c-Ni-Si indicate amorphous-nickel-silicon and crystalline-nickel-silicon, respectively [111]

The Ni_xGaAs phases were not detected in the NiSiW Ohmic contacts even at the initial stages (≅300 °C) of RTA Therefore, the n^{++}-GaAs layers for the NiSiW Ohmic contacts were believed to be formed by in-diffusing Si atoms The growth of the NiAs compounds results in non-Ohmic behaviour, which is schematically shown in Fig 1 13 The formation of NiAs is found to be suppressed by increasing the Si concentration and decreasing the annealing time using RTA The top W layer reduces the sheet resistance of the contact metal, improves the surface morphology of the NiSi contacts and also reduces the formation of NiAs compounds

The kinetic effects of a layering sequence in Al-Ge-Ni Ohmic contact components on (001)GaAs were investigated by Lampert et al. [112]. Al-Ge-Ni metallizations have been successfully fabricated on both n- and p-type GaAs [113]. For n-type GaAs, the thickness of Ge deposited and the alloying time have a large influence over the degree of Ohmicity observed. The contact interface is extremely flat and uniform with a continuous single phase polycrystalline layer of Al_3Ni adjacent to the semiconductor. Kalkur et al. [79] have analyzed the microstructure of Al-Ge-Ni RTA Ohmic contacts. Epitaxial GaAs/NiAl/GaAs heterostructures consisting of buried NiAl layers and GaAs overlayers that are monocrystalline and well aligned were also reported [114].

The Al-Sn-Ni [115] metallizations can produce Ohmic contacts to both n- and p-type GaAs and they have morphological characteristics superior to the Al-Ge-Ni contacts [79, 112, 113]. It is easy to pattern Al-Sn-Ni with the lift-off process and the surface remains remarkably smooth and planar after alloying. Contact resistivities in the range of 10^{-4} Ω-cm^2 are obtained for both n- and p-type GaAs [115]. The homogeneity of alloyed Ni-Sn Ohmic contacts to n-GaAs was investigated by Nikolaev et al. [116]. They reported intermediate phases NiAs, NiGa, and SnAs for the inhomogeneity of these contacts. Similarly, the role of Ge in NiAs/n-GaAs, NiAs/Ge/n-GaAs and Ge/NiAs/n-GaAs structures have been investigated [117].

1.3.12 Au-Ge metallizations

Most commonly employed Ohmic contacts to n-type GaAs are based on the Au-12wt.%Ge eutectic alloy [118,119]. A minimum ρ_c of 9×10^{-7} Ω-cm^2 is obtained for an epilayer doping of 3×10^{17} cm^{-3} after annealing at 450 ^{0}C for 2½ min [119]. Melting of this eutectic alloy at a temperature of about 360 ^{0}C causes the localized dissolution of GaAs (presumably at pinholes in the native oxide). The higher solubility of Ga in the Au-Ge melt encourages the solidification of As-rich GaAs during cooling. Ge is thus incorporated preferentially on the Ga site in the precipitated GaAs, resulting in n-type GaAs and a tunneling Ohmic contact. Iliadis and Singer [119] observed that the role of Ge in Au-Ge metallization is not simply as dopant, but it is also the key element in initiating the melting. Barrier height reduction in Au-Ge metallization is investigated by Iliadis [118]. A massive reduction in barrier height [ϕ_B (TFE)=0.34 eV] at a 300 ^{0}C heat treatment is due to the large fraction of Ge atoms that is not accommodated in Ga vacant sites and indiffuses along with the Au atoms.

Recently, non-alloyed Au-Ge Ohmic contacts to n-GaAs have gained significant research interest [120-123] Low emperature, non-alloyed Au-Ge contact formation is a multi-step process [121] Ohmic behaviour was observed after 3 hrs of annealing at 320 ^{0}C and a Au_2Ga phase was found at this stage Samples annealed with Si_3N_4 cap layers to prevent As sublimation resulted in higher ρ_c values than uncapped samples [121] A novel model was presented for single crystal, non-alloyed epitaxial Au-Ge Ohmic contacts in Ref [120] According to this model, Au first comes in contact with the GaAs at points where the Ge layer is either very thin or nonexistent It reacts with the GaAs to form AuGa phases which results in the formation of free As and/or vacancies in the GaAs lattice The Ge then rapidly mdiffuses substantially via Ga vacancies forming GeAs related phases Heavy Ge doping may then occur, leading to Ohmic contact formation Isothermal regrowth of doped, smooth and planar Ohmic contacts with low ρ_c using Au-Ge metallization has also been reported [122] This procedure is suitable for forming Ohmic contacts on shallow junction devices Extremely low resistance non-alloyed Au-Ge Ohmic contacts on δ-doped GaAs have also been developed [123] and recently, properties of Au-Ge Ohmic contacts after the alloying process have been studied [124]

1.3.13 Au/Te/Au metallizations

In Au/Te/Au metallizations, Te is used as the dopant to form an Ohmic contact to n-GaAs Te atoms become electrically active donors only when occupying As sites Therefore, As vacancies must be created during metallization Although reports on Au/Te/Au/GaAs contacts are scarce, several mechanisms have been invoked to explain their Ohmic behaviour In particular, Wuyts and co-workers attributed the formation of an Ohmic contact to the formation of either a metal/Te/Ga_2Te_3(Au)/GaAs or a metal/(Te)/Ga_2Te_3(As)/GaAs heterostructure [125-127]

Munder et al [128] investigated pulsed laser beam and furnace annealed Au/Te/Au metallizations For furnace annealed contacts the mechanism responsible for the Ohmic behaviour was dominated by the formation of a Ga_2Te_3, polycrystalline Te and a highly disordered GaAs layer [125,129] For laser annealed contacts electron tunneling through the potential barrier involving localized gap states was postulated for Ohmic behaviour The effects of an Al_2O_3 cap on the structural and electrical properties of Au/Te/Au contacts on n-GaAs were also ameliorated [130,131] Contacts annealed without the capping layer became Ohmic after annealing at 420 ^{0}C for 3 mm with a ρ_c of ~1 6x10^{-4} Ω-cm^2 [130] In the uncapped system, the contact reaction is dominated by the Au-GaAs interaction, as indicated in TABLE I by the appearance of Au_7Ga_2 phase and large arsenic losses

Annealing under a capping layer changes the kinetics of the contact reaction. For sealed GaAs/Au/Te/Au contacts, the losses of both Te and As are limited. Suppression of As vapourisation restrains the Au-GaAs reaction, while reduction of Te sublimation activates the Te-GaAs reaction. Ga_2Te_3 and As_2Te_3 are the main products of the interaction, apart from unreacted Au. Such interactions, however, do not lead to the formation of Ohmic contacts to n-GaAs. The results indicated do not support the heterojunction model of Ohmic contact, but rather testify in favour of the doping model.

TABLE I. The influence of Al_2O_3 capping layer on the outcome of n-GaAs/Te and n-GaAs/Au/Te/Au contact reaction [131].

Contact material	Annealing		Phase composition	As loss	Te loss
	T(^{0}C)	t(min)		$N_{As}x10^{15}$ (atom/cm^2)	$N_{Te}x10^{15}$ (atom/cm^2)
Te	As-deposited		Te		
	380	3	Te (small amount)		
	420	3	Te (traces)		300
	460	3	Te (traces)		310
Te/Al_2O_3	380	3	Ga_2Te_3		
	420	3	Ga_2Te_3 , As_2Te_3 (traces)		10
	460	3	Ga_2Te_3, As_2Te_3 (traces)		33
Au/Te/Au	As-deposited		Au+Te		
	380	3	Au+AuGa(50 at. %)		
	420	3	$Au+Au_7Ga_2$	139	45.5
	460	3	$Au+Au_7Ga_2$	320	50.4
Au/Te/Au/	380	3	$Au+Ga_2Te_3+As_2Te_3$(traces)		
Al_2O_3	420	3	$Au+Ga_2Te_3+As_2Te_3$(traces)	17.3	0.5
	460	3	$Au+Ga_2Te_3+As_2Te_3$(traces)	53	0.7

1.3.14 High-temperature refractory metallizations

The main reason for using refractory metals, e.g., W, Ti and Mo, is to achieve thermal stability of the contact both during processing and in real applications. Refractory metal contacts are expected to withstand high temperatures encountered during device

processing such as those used to activate the ion implanted dopants. In addition, the metals/alloys can act as a barrier against Ga and As out-diffusion. Since the refractory metals/alloys are good alternatives to Ni/AuGe metallization, many research groups have attempted to exploit these high-temperature metallization schemes.

Among the composites recently investigated are [27,28,86,105,107-109, 132-142] as follows: Au/TiW/Ge/Pd, NiInW, MoGeW, MoGe, Ge-Mo-LaB_6-Au, Ge-WSi_2-Au, WGe, W-In, $TiWSi_x$, TiW/Ge, $Ti_xW_ySi_z$, Ti/Pt/Au, Ti/Pt and Ti/Mo (with Si & Ge). In most of these investigations, W is common and chosen over other high temperature metals because of its compatibility with processes used in dry etching (reactive ion), its thermal stability (ϕ_B on GaAs is stable up to 700 ^{0}C) and its compatibility with AlCu wiring. Refractory NiInW metallizations [105,107-109] have already been discussed. Arsenic(As)-doped GeMoW i.e., Ge(As)MoW refractory Ohmic contacts can be fabricated for n-GaAs using different annealing techniques [108,132]. Very low contact resistivities, in the range of a few 10^{-7} Ω-cm^2, have been obtained when annealed under an As overpressure. Without As doping, the same metallization gives higher ρ_c values.

A minimum ρ_c of $5x10^{-6}$ Ω-cm^2 has been obtained without arsenic doping in the GeMoW contacts annealed at 800 ^{0}C for 7 min [132,134]. As the arsenic doping is increased, the ρ_c values are decreased with $\rho_c \sim 2x10^{-7}$ Ω-cm^2 for an arsenic doping of 10^{20} cm^{-3} (800 ^{0}C, 10 min). A minimum ρ_c of 0.176 Ω-mm is obtained at an annealing temperature of 500 ^{0}C using GeMoW contacts to n-GaAs with a $In_{0.5}Ga_{0.5}As$ cap layer [133]. The $In_{0.5}Ga_{0.5}As$ cap layer significantly widens the range over which the n-GaAs is Ohmic (300-700 ^{0}C). Merkel et al. [28] applied GeMoW metallization as source/drain contacts to GaAs-MESFETs with Al and TiPtAu as gate contacts. Both GeMoW/TiPtAu and GeMoW/Al are thermally stable up to 450 ^{0}C. Thermal cycling at 500 ^{0}C resulted in degradation of both contacts with GeMoW/Al exhibiting less degradation. Furthermore, self-aligned high-temperature MoGe Ohmic contacts for HBTs have been fabricated by Ketata et al. [135].

Refractory metallizations incorporating diffusion barriers [86] or refractory metallization diffusion barriers [27,136] can improve the overall thermal stability of Ohmic contacts. The choice of WSi_2, which also acts as a diffusion barrier, is due to its phase stability with GaAs [136]. TiW and LaB_6 diffusion barriers are also utilized in PdGe and GeMoAu metallizations, respectively [27,86]. Thermally stable WGe Ohmic contacts for GaAs/AlGaAs HBTs have also been reported [137]. W-In-(Ge, Si or Te) Ohmic contacts to n-GaAs show thermal stability up to 500 ^{0}C with good surface morphology [138]. The W-In-Si/n-GaAs structure shows a ρ_c of $3x10^{-6}$ Ω-cm^2. Ohmic

contacts to n-GaAs using graded-band-gap layers of low pressure organometallic chemical vapor deposition (LPMOCVD)-grown $In_xGa_{1-x}As$ and sputter-deposited $TiWSi_x$ films were investigated [139]. The as-deposited contacts exhibited ρ_c values of $1x10^{-5}$ Ω-cm² and $9x10^{-7}$ Ω-cm² for $In_{0.5}Ga_{0.5}As$ and InAs caps, respectively. Ti/Pt/Au non-alloyed source and drain contacts to Sn or Si doped AlGaAs/GaAs HEMTs were fabricated without additional intermediate InGaAs or InAs layers [140]. Ti/Pt metallization has been utilized to form contacts on both n^+-InAs emitter cap and p^+ base layers of HBTs [141]. Comparison of Ti, Mo and Cr metallizations with Ge- or Si-doped GaAs have been reported [142]. TABLE II summarizes the results obtained with many of these refractory metals. One can clearly see that all of these refractory contacts have very low ρ_c and are stable at ~400 °C. This temperature is compatible with the wiring and packaging process.

TABLE II. Summary of refractory metallizations to n-GaAs.

Metallization	Doping concentration (cm^{-3})	Contact resistivity (Ω-cm²)	Thermal stability	Application	Ref. No.
Au/TiW/Ge/Pd	$2x10^{18}$	$1.45x10^{-6}$	410 °C, 1h	MESFET	[27]
GeMoW	$3x10^{18}$	0.21 Ω-mm*	Up to 450 °C, 10 min	MESFET	[28]
Ge(As)MoW	$4x10^{18}$	~$4x10^{-7}$	----------	HBT	[132]
GeMoW	$5x10^{18}$	0.176 Ω-mm*	----------	-------	[133]
GeMoW	$1x10^{18}$	$2x10^{-7}$	----------	HBT	[134]
MoGe	$1x10^{18}$	--------	----------	HBT	[135]
Au/WSi_2/Ge	$1x10^{16}$	$5x10^{-5}$	460 °C, 1h	MESFET	[136]
WGe	-------	$7.5x10^{-7}$	----------	HBT	[137]
W-In-Si	-------	$3x10^{-6}$	Up to 500 °C	-------	[138]
TiW/Si/Au	$3x10^{18}$	~$9x10^{-7}$	Up to 500 °C	-------	[139]
Ti/Pt/Au	$1x10^{19}$	~$1.1x10^{-6}$	----------	HEMT	[140]
Ti/Pt	-------	~$3x10^{-7}$	----------	HBT	[141]

*Ω-mm and Ω-cm^2 can be correlated if the contact width is known.

1.3.15 InAs-based metallizations

In forming good Ohmic contacts to large band gap GaAs, narrow band gap InAs has been used as a cap layer sandwiched between the metal and GaAs. Since the Fermi

level of metals is normally pinned in the conduction band of InAs (Fig 1 14(a)), the conduction barrier at metal-GaAs interface can be drastically reduced However, due to the relatively large band gap difference between GaAs and InAs (Fig 1 4(b)), only a reasonable value with non-alloyed ρ_c of about 10^{-6} Ω-cm^2 has been obtained in a nearly abrupt layer of n^+-InAs [143] To eliminate this band discontinuity and thus the high barrier for carrier transport, an epitaxial layer of $In_xGa_{1-x}As$ with the In mole fraction graded from x=0 at the GaAs interface to x=1 at the surface contacting metal has been proposed [16] and ρ_c values in the range from $5x10^{-7}$ to $5x10^{-6}$ Ω-cm^2 are obtained This graded metal/n-InAs/n-$In_xGa_{1-x}As$/n-GaAs (x=0-0 53) structure is shown in Fig 1 14(b) Applying a graded InGaAs cap layer has also led to ρ_c of $5x10^{-8}$ Ω-cm^2 for non-alloyed Ti/Pt/Au contacts [17]

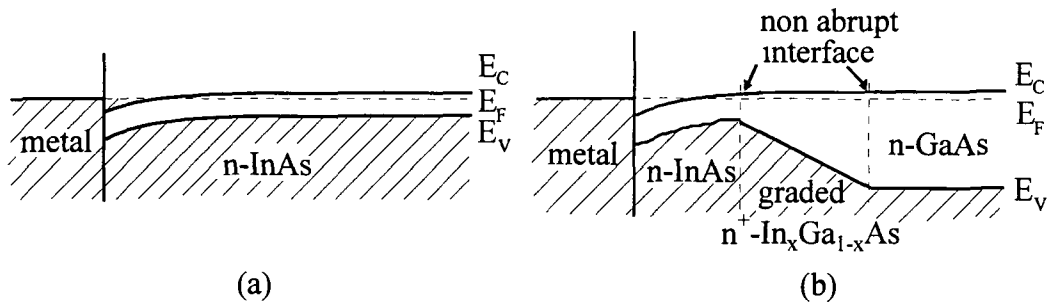


Fig 1 14 Band-bending diagrams for (a) metal on n-InAs and (b) metal on n-InAs on graded n^+-$In_xGa_{1-x}As$/n-GaAs [144]

A refinement to the InAs on GaAs procedure is to replace the thick and cumbersome InGaAs graded layer with a thin superlattice structure In doing so, the refinement resulted in dramatic reductions of ρ_c (1 $5x10^{-8}$ Ω-cm^2) on n-GaAs as demonstrated by Peng et al [15] using an strained layer superlattice (SLS) structure Ohmic contacts using an SLS structure have many advantages Firstly, the SLS scheme requires a smaller overall layer thickness than the graded structure Secondly, a SLS is easier to fabricate and pliable for different structures Hence it is convenient to incorporate this structure in devices and optimize it to obtain even lower ρ_c The implementation of this SLS scheme m a GaAs-MESFET has been demonstrated [144] Huang et al [145] have concluded that quantum tunneling through SLS conduction bands plays an essential role in the effective barrier lowering leading to extremely low contact resistance

1.4 Applications of Ohmic Contacts to n-GaAs

Ongoing miniaturization of GaAs devices requires Ohmic contacts having very low ρ_c ($\leq 10^{-6}$ Ω-cm^2), easy reproducibility, a shallow (non-spiking) interface, smooth surface morphology and thermal stability Many devices based on GaAs and its alloys, such as the high electron mobility transistor (HEMT), heterojunction bipolar transistor (HBT), charge injection transistor (CHINT)/negative resistance field-effect transistor (NERFET), metal-semiconductor field-effect transistor (MESFET), modulation doped field-effect transistor (MODFET) and multiple quantum-well (MQW) superlattice devices require reliable planar low-resistance Ohmic contacts Nonspiking Ohmic contacts are essential to GaAs-based very large scale integration (VLSI) technology Three of the most important issues are (i) achievement of low-resistance Ohmic behaviour with a wide processing window, (ii) thermal stability at temperatures up to ~500 ^{0}C and (iii) applicability to small contact areas (down to sub-μm sizes) Thermal stability of Pd/In Ohmic contacts [65,66,68,69] is more than sufficient to meet the demands of subsequent device and circuit fabrication steps Pd/Ge Ohmic contacts for GaAs MESFETs [21,31,32,38,53] are an even better alternative to conventional AuGeNi ones, with a fabrication process fully compatible with standard MESFET technology Moreover, these contacts are obtained by a solid-phase interaction at a lower temperature allowing easier control of the process, better flatness and edge definition

AlGaAs/GaAs heterojunction structures are extensively used in fabricating HBTs, HEMTs and CHINT/NERFETs Rapid thermal annealed (RTA) Pd/Ge [38] and Ge/Pd/W/Au [55] contacts have already been utilized in fabricating HBTs The successful application of Pd/Ge contacts is also reflected in multiple quantum-well (MQW) structures [18,39] Chen et al [146] found that the Pd/Ge/Au contact is not suitable for the HEMT structure, but it could be useful in some heterojunction devices, such as MQW structures, in which the apparent inability of the Pd-Ge to diffuse beyond the AlGaAs/GaAs interface could be used to advantage Based on the above assumption Wang et al [20] have successfully applied the Pd/Ge Ohmic scheme to an AlGaAs/GaAs HEMT Han et al [56] developed a non-alloyed Pd/Ge/Ti/Pt Ohmic contact for optical switch (OS) CHINT/NERFET devices require shallower Ohmic contacts Lai and Lee very recently developed even shallower RTA Ohmic contacts for CHINT/NERFET devices using Pd/Ge metallizations [22,37] Using this process technology, the fabrication tolerances for the CHINT/NERFET become much less critical

TABLE III. Summary of Pd-based metallizations to n-GaAs.

Metallization	Doping concentration (cm^{-3})	Annealing condition	Contact resistivity (Ω-cm^2)	Application	Ref. No.
Pd/Ge	$1x10^{18}$	325 °C, 30 min	$\sim 1x10^{-6}$	MQW	[18]
Pd/Ge	$4x10^{18}$	325 °C, 30 min	$\sim 3x10^{-7}$	HEMT	[20]
Pd/Ge	$2x10^{18}$	RTA, 450-500 °C, 60s	$\sim 1x10^{-6}$	CHINT/NERFET	[22]
Pd/Ge	$2x10^{17}$	RTA, 450-500 °C, 60s	$\sim 1x10^{-6}$	CHINT/NERFET	[37]
Pd/Ge	$1.5x10^{17}$	325 °C in forming gas	0.16 Ω-mm*	MESFET	[31]
Pd/Ge	$1.5x10^{17}$	325 °C, 30 min	0.16 Ω-mm*	MESFET	[32]
Pd/Ge	$3x10^{18}$	RTA, 500-750 °C, 10s	$\sim 7.5x10^{-6}$	HBT/MESFET	[38]
Pd/Ge	$4.5x10^{18}$	250-500 °C, 1-5 min	$\sim 1.25x10^{-6}$	MQW	[39]
Pd/Ge/Ti/Au	$1.5x10^{17}$	325 °C, 30 min	$4x10^{-6}$	MESFET	[53]
Pd/Ge/Ti/Au	$1x10^{17}$	340 °C, 2 min	$\sim 1x10^{-5}$	MESFET	[21]
Ge/Pd/W/Au	$1x10^{17}$	RTA, 800-900 °C, 10s	$\sim 5x10^{-6}$	HBT	[55]
Pd/Ge/Ti/Pt	$2x10^{18}$	RTA, 450-450 °C	$4.7x10^{-7}$	OS	[56]
Pd/Ge/Au	$1x10^{18}$	450 °C, 30s	$\sim 1x10^{-6}$	HEMT	[146]

*Ω-mm and Ω-cm^2 can be correlated if the contact width is known.

HEMTs are also fabricated on n-GaAs by incorporating diffusion barriers [87,99] and capping layers [71] to AuGeNi Ohmic contacts. Two-stage annealing incorporating a Ag barrier in AuGeNi contacts is used to fabricate conventional HEMTs (CHEMTs) [99]. This Ag barrier is also used in fabricating AlGaAs/GaAs and AlInAs/GaInAs MODFETs [100]. Rapid thermal annealed (RTA) AuGeNi contacts with a WSiN barrier are utilized to fabricate MESFETs as well as HBTs and HEMTs [87]. Goronkin et al. [72] found that AuGe/Ni Ohmic contacts are more suitable for GaAs MESFETs than for GaAs/AlGaAs MODFETs. Multilayer AuGeNi Ohmic contacts [94] are very attractive for fabricating a wide variety of microwave and lightwave devices including switching diodes (SDs) and MESFETs. GaAs MESFETs with AuGeNi and NiInW metallizations have been successfully fabricated [105] and their characteritics were evaluated. NiInW contacts have improved thermal stability compared to AuGeNi contacts and the fabrication process is compatible with the current GaAs MESFET technology. Thermally stable non-gold NiGe and NiSiW Ohmic contacts for MESFETs are reported by Takata et al. [110,111]. Al-Sn-Ni Ohmic contacts [115] on both types of GaAs with $\rho_c \sim 10^{-4}$ Ω-cm^2 are very cost effective in a rapid turnaround fabrication procedure. Refractory metallizations (TABLE II) are very attractive for the fabrication of thermally stable, high-speed, self-aligned GaAs devices. The applications of Pd- and

Ni-based Ohmic contacts, along with other useful parameters, are listed in TABLE III and TABLE IV, respectively

TABLE IV Summary of Ni-based metallizations to n-GaAs

Metallizations	Doping concentration (cm^{-3})	Annealing condition	Contact resistivity (Ω-cm^2)	Application	Ref No
AuGe/Ni	(2-7)x10^{17}	340 °C, 30 min	--------	HEMT	[71]
Au/Ge/Ni	2x10^{18}	460 °C, 8 min	--------	MESFET, MODFET	[72]
Au/WSiN/ Au/Ni/Ge	(1-2)x10^{17}	430-470 °C, 150s	~5x10^{-7}	MESFET, HEMT & HBT	[87]
Au/Ge/Au/ Ni/Au	2x10^{18}	425 °C, 1 min	8 8x10^{-7}	SD, MESFET	[94]
Au/Ag/AuGe/Ni-------		250 °C, 20s + 400 °C, 40s	~0 1 Ω-mm*	HEMT	[99]
Au/Ag/AuGe/Ni~2x10^{18}		540-600 °C	0 06-0 2 Ω-mm*	MODFET	[100]
NiInW	--------	RTA, 800 °C, ~7s	--------	MESFET	[105]
NiInW	--------	RTA	--------	MESFET	[107]
Ni/Ge/Ni	1x10^{18}	200-700 °C, 5 min	0 78 Ω-mm*	MESFET	[110]
Ni/Sn/Al	1 9x10^{18}	505-605 °C, 1-4 min	1x10^{-4}	HBT	[115]

*Ω-mm and Ω-cm^2 can be correlated if the contact width is known

1.5 Conclusions

From the above discussions it is evident that thermally stable, non-spiking Ohmic contacts are necessary to meet device miniaturization and speed requirements Special attention is given to rapid thermal annealed (RTA) Ohmic contacts because the RTA process often gives better results than those of conventional furnace annealing It is found that the scanned electron beam (SEB) annealing process is more advantageous than the RTA process Refractory Ohmic contacts have been developed to meet the demands of self-aligned fabrication process of GaAs devices

The highlights of the most recent developments in Ohmic contacts are summarized as follows

- Metallizations such as Ge/Pd, Ge/Pd/Au, Pd/Ge/Ti/Pt, Pd/AuGe/Ag/Au, Si/Pd, In/Pd, etc to n-GaAs have low contact resistivities of ~10^{-6} Ω-cm^2 and are good

alternatives to the AuGeNi metallization But their thermal and long-term stabilities at and above 400 °C still require further studies

- High-temperature (refractory) contacts have both thermal stability and low ρ_c However, other properties such as thermal expansion coefficients compared to GaAs and adhesion to GaAs should be investigated
- RTA is an excellent means of limiting interfacial reactions and has distinct advantages over conventional alloying procedures
- Several techniques such as the use of capping layers, diffusion barriers and GaAs surface treatments, have been used extensively to reduce ρ_c

The advantages of high-speed GaAs devices can only be exploited if adequate and reliable Ohmic contacts are available For this reason, efforts should be directed towards the fabrication of new thermally stable Ohmic contacts to n-GaAs More fundamental interface studies of the interactions between metals and GaAs, along with their long-term reliability, are necessary Moreover, further investigations are required to optimize various metallizations for the fabrication of high-speed, sub-μm size GaAs devices for both present and future requirements

1.6 Organisation of This Thesis

This thesis is organised into nine chapters The theoretical background and research survey related to Ohmic contacts to n-GaAs have been described in this introductory chapter

- Chapter 2 presents the objectives of this research and brief highlights of the characterization techniques to be employed

- Chapter 3 presents the optimisation of Pd and Sn evaporation rates for better surface morphology of Pd/Sn contacts on GaAs(SI) using Scanning Tunneling Microscopy (STM)

- Chacter 4 introduces the conventional Transmission Line Model (cTLM) method employed to determine the ρ_c of the contacts on n-GaAs This chapter also presents the effects of metallization thickness on the characteristics of Pd/Sn Ohmic contacts to n-GaAs

- Chapter 5 describes the effects of a Au overlayers on the characteristics of Pd/Sn Ohmic contacts A comparative study of non-alloyed Pd/Sn and Pd/Sn/Au and alloyed Au/Ge/Au/Ni/Au Ohmic contacts will also be presented in this chapter

- Chapter 6 compares the electrical and morphological characteristics of non-alloyed Pd/Ge and alloyed Au-Ge/Ni Ohmic contacts with those of non-alloyed Pd/Sn and Pd/Sn/Au metallizations

- Chapter 7 presents a study of the thermal stability of the contacts at temperatures of 300 ^{0}C and 410 ^{0}C Long-term stability of the contacts is carried out for 400 h at 300 ^{0}C

- Chapter 8 examines the characteristics of GaAs-MESFETs fabricated using Pd/Sn, Pd/Ge and Pd/Sn/Au Ohmic contacts

- Chapter 9 presents the conclusions of this research and offers suggestions for further study

CHAPTER 2

Objectives of this research

2.1 Introduction

Because Ohmic contacts are so important to GaAs devices (section 1.1), substantial experimental effort has been directed toward developing practical metallization and processing procedures. Of all the metallizations investigated, none has proven superior to Au-Ge based systems for contacting n-GaAs. However, as device dimensions have shrunk into the sub-μm and even toward the nanometre regime, the shortcomings of Au-Ge based Ohmic metallization have become serious. These deficiencies are:

- **High contact resistivity** ρ_c. A typical Au-Ge $\rho_c \approx 10^{-6}$ Ω-cm^2 produces a 5Ω contact resistance to a 10 μm diameter diode but a 50KΩ contact resistance to a 100 nm diameter diode. Contact resistance [147] in modern GaAs FETs may comprise at least half the total parasitic source resistance and noise figures are particularly sensitive to such resistances. Parasitic resistance is likely to be the limitation in high frequency exploitation of vertical transport devices.
- **Poor morphology.** During annealing the typical AuGeNi eutectic mix is in the liquid phase which can result in *balling-up* and surface roughness or patchiness.
- **Thermal instability.** The Au-Ge system is not thermally stable [118-121], due to the formation low melting point (~375 ^{0}C) β-AuGa phase [104], so cannot be used for high temperature applications or be subjected to subsequent high temperature (400 ^{0}C) processing steps.
- **Metal diffusion.** The alloying steps necessary to contact formation results in the component metals, particularly Au, moving both vertically and laterally into the underlying semiconductor over distances that can be several thousand Angstroms. This necessitates the growth of thick contact layers on epitaxial structures and imposes a lower limit on lateral separation. Furthermore, metal migration during device operation compromises device reliability causing shorts and other failure modes.

To overcome the aforementioned disadvantages of Au-Ge based contact systems, nonalloyed Pd/Ge contacts have been developed [38,148]. Nonalloyed Pd/Ge

contacts have low ρ_c in the range of ~10^{-6} Ω-cm^2 [22,39,148]. Pd/Ge contacts are also very shallow in nature and therefore can be used for GaAs based heterojunction devices [148-150].

One of the most important criteria for an Ohmic contact is its thermal stability. Although a suitable Au diffusion barrier is used to improve the thermal stability of Pd/Ge contacts (section 1.3.1), thermal stability of this contact system at and above 400 ^{0}C still requires further study [31,148,151].

2.2 Objectives

Pd/Ge Ohmic contacts are extensively used to fabricate GaAs devices. To our knowledge, Pd/Sn Ohmic contacts to n-GaAs have yet to be developed. Ni-Sn based alloyed Ohmic contacts are reported [102,115], but their contact resistivities are very high and surface morphology is poor. Although both Ge and Sn are shallow amphoteric dopants in GaAs and are 0.006 eV from the edge of the conduction band, Sn has a distinct advantage over Ge. Sn is a less-compensated amphoteric dopant compared to Ge [152] which results higher net doping concentration and thus lowers ρ_c values. Although little work has been carried out on the Pd/Sn metallization system [153], there is enough information to suggest that this system could withstand the elevated temperatures associated with modern GaAs device processing.

Anticipating the above facts, a novel potentially non-alloyed Pd/Sn Ohmic contact system is fabricated on n-GaAs. The objectives of the present research are:

1) to undertake the development of a new contact to n-GaAs comprising a Pd/Sn mix undergoing a solid-phase reaction. The successful completion of this undertaking would place the users at the forefront of a whole new contact technology for the microwave and optoelectronic industries.
2) the design, fabrication, testing and modelling of the contact having target properties of
   - ⇨ contact resistivity $\rho_c \leq 10^{-6}$ Ω-cm^2
   - ⇨ thermal stability up to 410 ^{0}C
   - ⇨ smooth morphology on a sub-μm scale
   - ⇨ abruptness i.e. having a vertical and lateral penetration of metal in the semiconductor of <50 nm.

In addition, the effects of a Au overlayer on the properties of Pd/Sn contacts i e the properties of Pd/Sn/Au contacts will also be investigated A comparative study among the characteristics of Pd/Sn, Pd/Sn/Au, Pd/Ge and conventional Au-Ge/Ni contacts will be performed Finally, GaAs-MESFETs will be fabricated utilizing Pd/Sn, Pd/Ge and Pd/Sn/Au Ohmic contacts

2.3 Characterization of the Contacts

The metallization would be deposited by thermal (resistance heating) evaporation (Appendix A) onto n-GaAs bulk and epitaxial wafers patterned with test structures by photolithography Lift-off techniques will produce the required metal test structures which will then undergo the annealing steps by conventional graphite strip annealer (Appendix B) and rapid thermal annealer (RTA) Experimental design principles will be applied in the optimisation of metal component relative proportions, order of deposition, thicknesses and annealing conditions A furnace will be employed to characterize the long-term thermal stability of the contacts

In addition, the characterization of the contact and evaluation of the contact structure and chemistry will be undertaken by

- ⇨ Current-Voltage (I-V) measurements to examine conversion from Schottky to Ohmic behaviour of the contacts
- ⇨ Transmission Line Model (TLM) to determine the contact resistivity ρ_c
- ⇨ Scanning Tunneling Microscopy (STM) to study surface morphology
- ⇨ Tencor surface profilometry measurements to determine surface roughness
- ⇨ Scanning Electron Microscopy (SEM) to study surface morphology
- ⇨ Energy Dispersive Analysis of X-rays (EDAX) to study phase formation before and after annealing the contacts
- ⇨ Secondary Ion Mass Spectrometry (SIMS) to evaluate the phase and component chemistry of the contacts and movement of the metals into the substrate

CHAPTER 3

Optimization of Pd and Sn evaporation rates for better surface morphology of the Pd/Sn contacts

3.1 Introduction

Conventionally alloyed Au-Ge/Ni is the most common Ohmic contact material regime for n-GaAs [38,72,73,78] After alloying, this contact system gives very rough surface morphology which is detrimental for VLSI GaAs devices Once Ohmic contact is formed, a second metallization (e g TiAu) for bonding is required to connect the Ohmic contact to the outside environment If the surface morphology of the contacts is very bumpy or rough, it is difficult to define a small area bonding pad, which imposes geometrical constraints on VLSI GaAs devices Rough surface morphology Ohmic contacts may also be of a spiking nature Spiking contacts cannot be used for GaAs based heterojunction devices One of the most important reasons for the development of non-alloyed Pd/Ge Ohmic contacts [22,53,148] is to overcome the rough surface morphology of conventional alloyed Au-Ge/Ni contacts Since Pd/Ge contacts are non-alloyed, they show better surface morphology and a non-spiking nature which can be used for GaAs based VLSI devices [31,53,149,154]

In this chapter, a non-alloyed contact system comprising of Pd/Sn metallization is fabricated on GaAs Considering the aforementioned importance of the surface morphology of an Ohmic contact, the morphology of the proposed metallization is optimized using Scanning Tunneling Microscopy (STM) for various evaporation rates of Pd and Sn The effect of **Sn to Pd thickness ratio (m)** is investigated for both as-deposited and annealed contacts Metallizations are deposited using a resistance heating evaporator (Appendix A) and annealing is carried out in a conventional graphite strip annealer (Appendix B)

3.2 Experiments

Undoped semi-insulating (SI) GaAs substrates of (001) surface orientation were sequentially cleaned in trichloroethylene, acetone, methanol and de-ionized (DI) water each for 10 min. The substrates were blow-dried immediately using dry N_2. Prior to loading into an evaporator, the substrates were soaked in a solution of DI H_2O:HCl (15:1 by volume) for at least 2 min and then blow dried to remove native oxides. Samples (GaAs/Pd/Sn structures) listed in TABLE V were prepared by sequential deposition of Pd and Sn in a resistance heating evaporator without breaking vacuum. The base pressure was ~$4x10^{-7}$ Torr and pressure during evaporation was ~$1x10^{-6}$ Torr. Samples A to J were then annealed in a conventional graphite strip annealer with a flowing forming gas (5% H_2 + 95% N_2) ambient at 200-400 ^{0}C for 5 or 10 min. Surface morphology of samples A to J was investigated using STM.

TABLE V. Summary of GaAs/Pd/Sn samples used in STM.

Sample	Pd evaporation rate (Å/s)	Sn evaporation rate (Å/s)	Contact structures	Value of m
A	5	5	GaAs/Pd(466Å)/Sn(2726Å)	5
B	5	8	GaAs/Pd(530Å)/Sn(2694Å)	5
C	5	10	GaAs/Pd(638Å)/Sn(2734Å)	5
D	5	12	GaAs/Pd(532Å)/Sn(2646Å)	5
E	5	5	GaAs/Pd(532Å)/Sn(1924Å)	3
F	5	8	GaAs/Pd(624Å)/Sn(1640Å)	3
G	5	10	GaAs/Pd(570Å)/Sn(1688Å)	3
H	5	12	GaAs/Pd(568Å)/Sn(1796Å)	3
I	8	10	GaAs/Pd(540Å)/Sn(1862Å)	3
J	7	15	GaAs/Pd(588Å)/Sn(2800Å)	5

3.3 Results

A surface area of 60000Åx60000Å was scanned using STM. TABLE VI summarizes the surface morphology of samples A to J before and after annealing at 200 ^{0}C for 10 min. In the as-deposited state, samples A, E and G exhibit smooth surface morphology compared to other samples. After annealing at 200 ^{0}C for 10 min, all samples, except sample H show rough surface morphology. Further annealing of samples B, C, D, F, G,

I and J at temperatures above 200 ^{0}C result in a very rough surface Therefore, surface roughness of samples A, E, and H was further investigated Fig 3 1 shows the standard deviation of surface roughness (SDSR) of metallizations as a function of Sn evaporation rate for the as-deposited condition with m=3 and m=5 From Fig 3 1, it is clear that for better surface morphology in the as-deposited state the evaporation rates of both Pd and Sn should be around 5 Å/s It is also noted that m=3 gives better surface morphology under these conditions The STM photographs of samples A, E, G and H before and after annealing at 200 ^{0}C for 10 min are shown in Fig 3 2 and Fig 3 3 The results, summarized in TABLE VI, are also confirmed from these photographs

TABLE VI Summary of surface morphology before and after annealing at 200 ^{0}C for 10 mm

Sample	Pd evaporation rate (Å/s)	Sn evaporation rate (Å/s)	Value of m	Surface condition before annealing	Surface condition after annealing
A	5	5	5	Smooth	Worse
B	5	8	5	Rough	Worse
C	5	10	5	Rough	Worse
D	5	12	5	Rough	Worse
E	5	5	3	Smooth	Worse
F	5	8	3	Rough	Worse
G	5	10	3	Smooth	Worse
H	5	12	3	Rough	Better
I	8	10	3	Rough	Worse
J	7	15	5	Rough	Worse

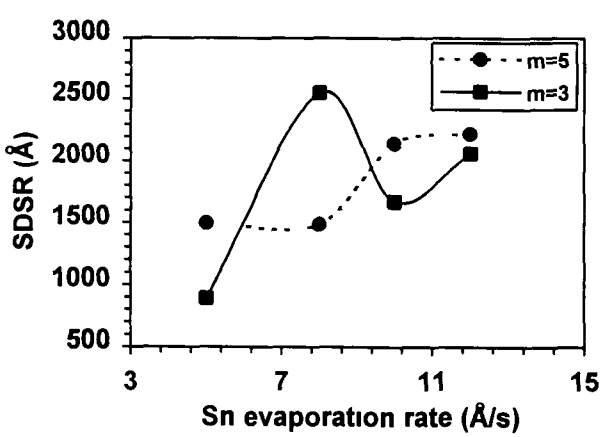


Fig 3 1 Standard deviation of surface roughness (SDSR) as a function of Sn evaporation rate of samples A, B, C, D, E, F, G and H under as-deposited condition, Pd evaporation rate being constant at 5 Å/s Data points are connected for visual aid

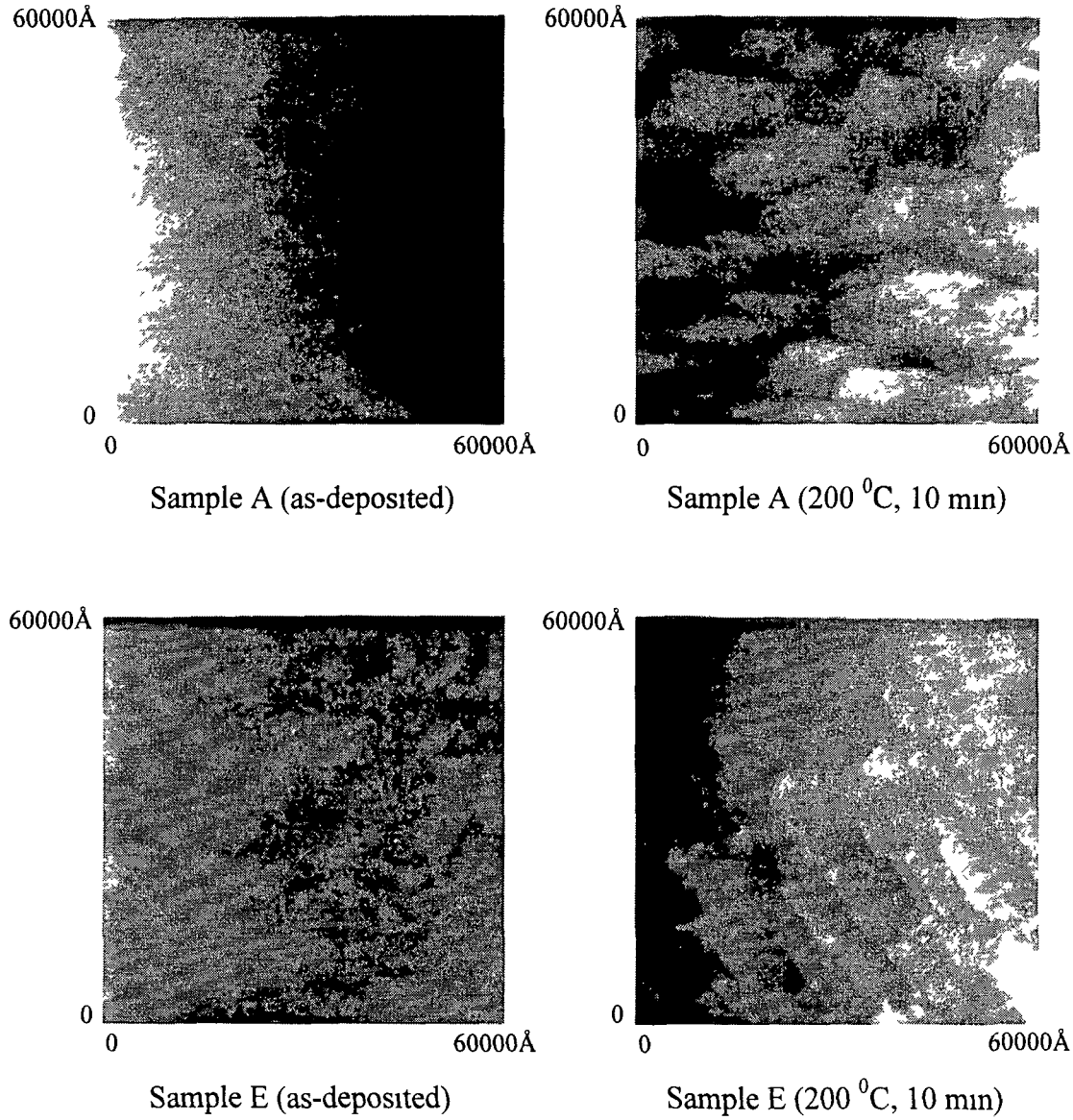


Fig 3 2 STM photographs of samples A and E under both as-deposited and annealed (at 200 ^{0}C for 10 min) conditions Original photographs are given in Appendix C

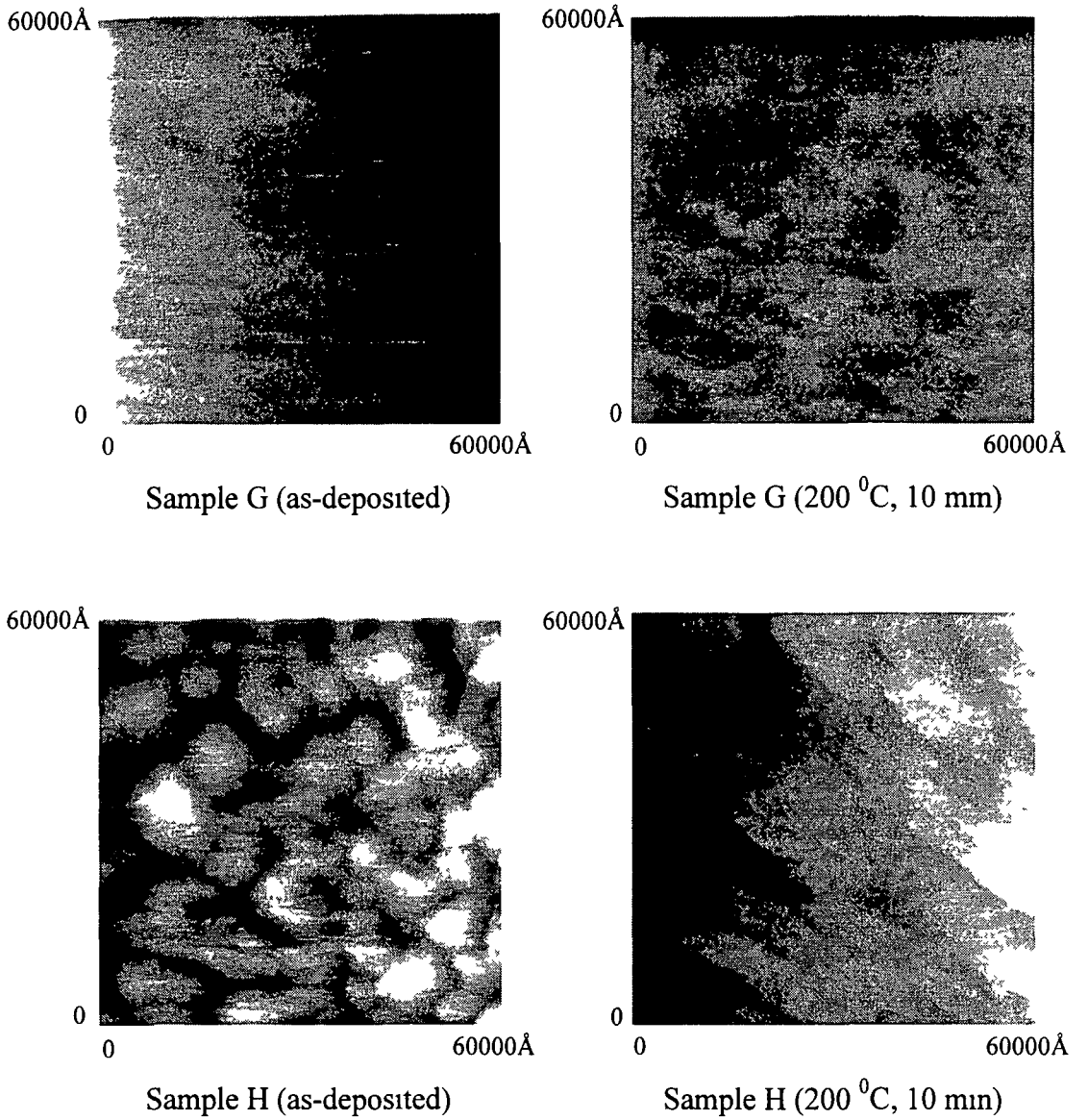
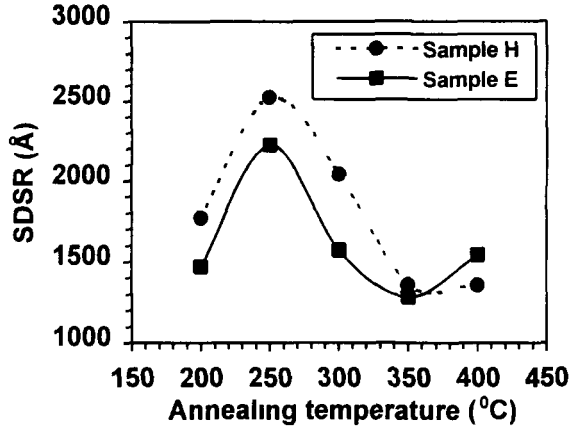
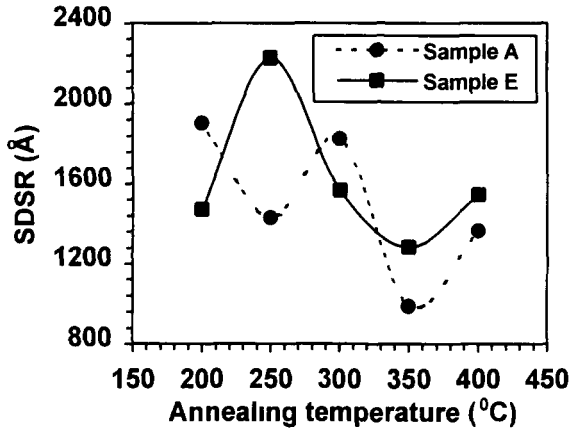


Fig 3 3 STM photographs of samples G and H under both as-deposited and annealed (at 200 ^{0}C for 10 mm) conditions Original photographs are given in Appendix C

The SDSR of samples A, E and H as a function of various annealing temperatures is shown in Fig 3 4 Annealing time is 10 min for all temperatures except at 300 ^{0}C where annealing time is 5 mm Both samples E and H have m=3, but sample E shows better surface morphology than that of sample H at almost all annealing temperatures investigated (Fig 3 4(a)) The SDSR of samples A and E is shown in Fig 3 4(b) For annealing temperatures above 300 ^{0}C, all samples give better surface morphology (Fig 3 4(a) and Fig 3 4(b)) This behaviour is significant because Ohmicity of Pd/Sn metallization is expected to occur at and above 300 ^{0}C In this region, sample A (with m=5) exhibits better surface morphology than that of sample E (Fig 3 4(b))



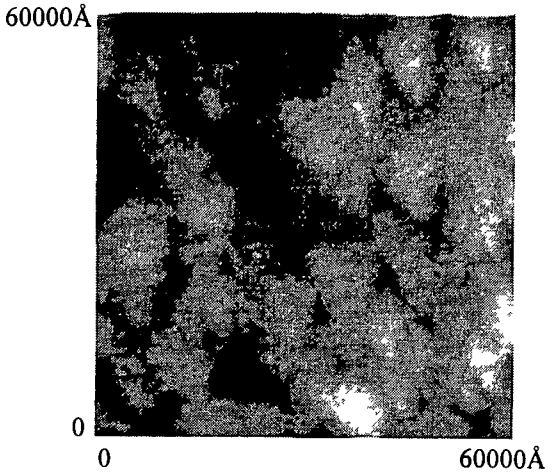
(a)



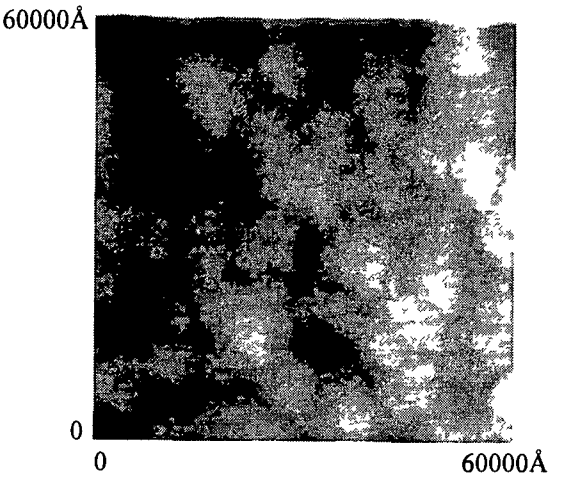
(b)

Fig 3 4 Standard deviation of surface roughness (SDSR) as a function of annealing temperature of (a) samples E and H, (b) samples A and E Data points are connected for visual aid

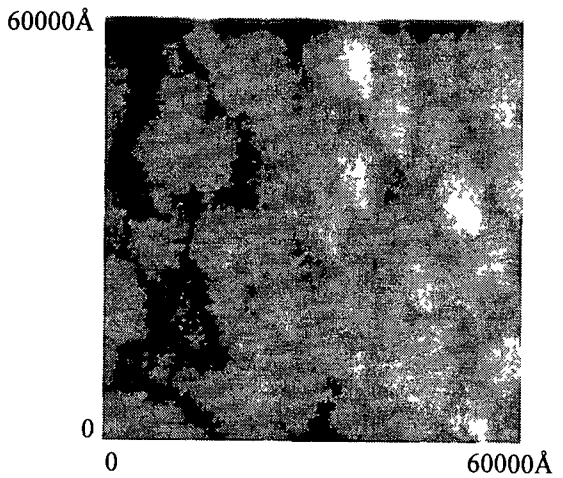
Fig 3 5 shows the STM results for samples E and H after annealing at temperatures of 350 ^{0}C and 400 ^{0}C for 10 mm At 350 ^{0}C, both samples show almost identical surface morphology After annealing at 400 ^{0}C, the surface morphology of sample E deteriorates when compared to that of sample H Fig 3 4(a) also confirms these results At these temperatures, the STM photographs of sample A are shown in Fig 3 6 Sample A shows a slightly deteriorated surface morphology at 400 ^{0}C compared to that at 350 ^{0}C However, at these temperatures, sample A shows the best surface morphology among all of the samples investigated These results are also confirmed from Fig 3 4(b)



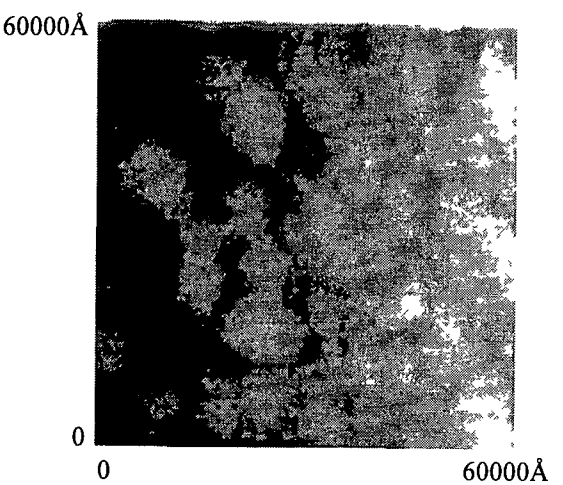
Sample E (350 ^{0}C, 10 mm)



Sample E (400 ^{0}C, 10 min)

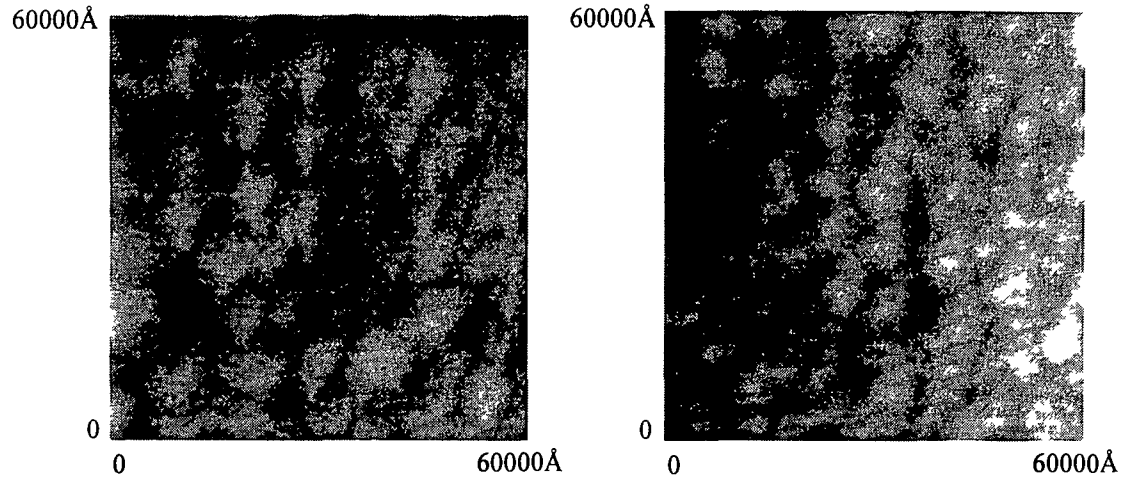


Sample H (350 ^{0}C, 10 mm)



Sample H (400 ^{0}C, 10 min)

Fig 3 5 STM photographs of samples E and H annealed for 10 mm at temperatures of 350 ^{0}C and 400 ^{0}C Original photographs are given in Appendix C



Sample A (350 ^{0}C, 10 mm) Sample A (400 ^{0}C, 10 mın)

Fıg 3 6 STM photographs of sample A annealed for 10 mm at temperatures of 350 ^{0}C and 400 ^{0}C Orıgınal Photographs are gıven ın Appendıx C

3.4 Summary

Surface morphology of the Pd/Sn contacts on GaAs(SI) has been optımısed for varıous evaporatıon rates of Pd and Sn utılızıng STM The effects of Sn to Pd thıckness ratıo (m) on the morphologıcal characterıstıcs of Pd/Sn contacts are also presented From the results, the followıng conclusıons can be drawn

- Evaporatıon rates of both Pd and Sn should be around 5 Å/s for better surface morphology
- For the ınıtıal evaporatıon, m=3 gıves best results under almost all evaporatıon rates ınvestıgated
- For annealıng temperatures, T_{an}>300 ^{0}C the surface morphology of the contacts ımproves
- Sample A wıth a contact structure of GaAs/Pd(466Å)/Sn(2726Å) shows the best surface morphology among all of the contacts ınvestıgated at T_{an}>300 ^{0}C

CHAPTER 4

Pd/Sn Ohmic contacts to n-GaAs

4.1 Introduction

An Ohmic contact system comprising of Pd/Sn metallization has been developed for n-GaAs for the first time [155-157] Metallizations are deposited using a resistance heating evaporator and annealing is carried out in a conventional graphite strip annealer Metallization thickness and annealing cycles are optimized to reduce ρ_c values The effects of layering sequencing on the Ohmicity of the Pd/Sn contact are reported The effects of two-step annealing on the characteristics of Pd/Sn contacts are also investigated

Pd/Sn contacts are systematically characterized using Surface Profilometry measurements, Scanning Electron Microscopy (SEM), Energy Dispersive Analysis of X-rays (EDAX), Secondary Ion Mass Spectrometry (SIMS) and current-voltage (I-V) measurements Surface Profilometry measurements and SEM are utilized to investigate surface morphology of the contacts Conversion from Schottky to Ohmic behaviour of the contacts is confirmed by I-V measurements Contact resistivities, ρ_c, of the proposed metallizations are measured using the conventional Transmission Line Model (cTLM) method which will be described in Section 4 2 EDAX is used to determine the various signal peaks of the contacts at different annealing temperatures These signal peaks will be correlated with the measured ρ_c values Contact depth profiles are analyzed by SIMS The formation of various compounds at different annealing temperatures will be determined by mass spectrometer analysis

4.2 Conventional TLM (cTLM) Method

The TLM pattern used for the contact resistance measurements is shown in Fig 4 1 The total resistance between two adjacent Ohmic pads of width W separated by a distance L is given by

$$R_T = 2R_c + \frac{R_{sh2}}{W} L + R_p \qquad (4\ 1)$$

where R_{sh2} is the sheet resistance of the active layer between the contacts (i.e., the film resistance per square), R_c is the contact resistance and R_p is the resistance of the interconnect wires. If $R=R_T - R_p$ then equation (4.1) may be written as

$$R = \frac{2R_{sh1}L_T}{W} + \frac{R_{sh2}}{W}L \tag{4.2}$$

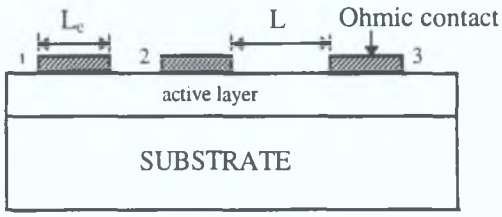


Fig.4.1. TLM pattern. Three or more Ohmic contacts with different distances between adjacent contacts are used in TLM measurement.

where R_{sh1} is the sheet resistance of the active layer under the contacts and L_T is the transfer length [12]. For the non-alloyed contact it is assumed that $R_{sh1}=R_{sh2}$. For the alloyed contact, $R_{sh1}\neq R_{sh2}$.

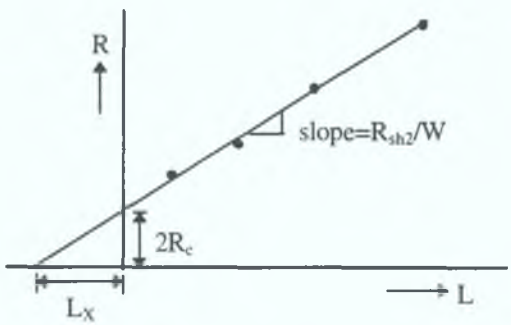


Fig.4.2. Plot of measured resistance as a function of contact separation yields sheet resistance, contact resistance and other parameters.

Assuming that sheet resistance is constant, a plot of R as a function of L will yield a straight line, as shown in Fig.4.2. The slope of the line gives the value R_{sh2}/W and the intercept with the R axis gives the value $2R_c$. The intercept with the L axis, $-L_X$, is related to the transfer length, L_T:

$$L_X = \frac{2R_cW}{R_{sh2}} = \frac{2R_{sh1}L_T}{R_{sh2}}. \tag{4.3}$$

Thus the L-axis intercept would give the value of L_T if $R_{sh1}=R_{sh2}=R_{sh}$. Equation (4.1) gives unequivocal answers for R_{sh2} and R_c; these are the experimentally determined variables. Additional data is needed to accurately determine the quantities ρ_c, R_{sh1} or L_T.

Technically, the end resistance measurement [10] can supply the necessary information if the length, L_c, of the contact is known. The end resistance measurement is useful only if L_c is not greatly larger than L_T. Usually, $L_c >> L_T$, so that R_c is independent of L_c. Under these circumstances the area WL_c does not have much significance, but W itself still does, of course. The effective area of the contact is WL_T and the contact resistivity is given by

$$\rho_c = WL_T R_c = R_{sh} L_T^2 . \tag{4.4}$$

4.3 Experiments

Contacts were fabricated on a Si-doped ($2x10^{18}$ cm^{-3}) n-GaAs epitaxial layer grown by metal-organic vapor phase epitaxy (MOVPE) in a metal-semiconductor field-effect transistor (MESFET) structure. The starting material for this MESFET structure was semi-insulating (SI) GaAs substrate of (100) surface orientation. The epitaxial structure consists of the following layers: a 50 nm AlAs undoped barrier layer, a 2500 nm GaAs undoped channel layer, a 200 nm n-GaAs ($5x10^{17}$ cm^{-3}) layer for recessed gate metallization, and a 100 nm n-GaAs ($2x10^{18}$ cm^{-3}) layer for Ohmic contacts (Fig.4.3). The top 100 nm GaAs heavily doped layer is used to reduce contact resistivity and the 50 nm AlAs barrier layer is used to confine electrons in the channel layer.

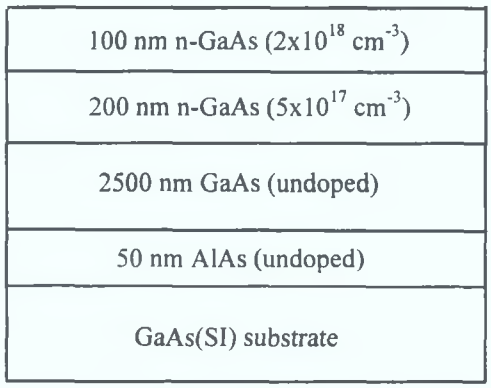


Fig.4.3. Schematic diagram of the GaAs MESFET substrate.

The GaAs substrates were sequentially cleaned and degreased in trichloroethylene, acetone, methanol and de-ionized water (DI H_2O), each for 10 min. The substrates were blow-dried immediately using dry nitrogen (N_2). Ohmic test, morphology and TLM patterns were defined by standard photolithography and lift-off processes. A solution of H_2O_2:NH_4OH:DI H_2O (1:3:15 by volume) was used as an etchant for mesa definition.

Prior to loading into an evaporator, the wafers were soaked in a solution of DI H_2O:HCl (15:1 by volume) for at least 2 min and then blow dried using dry N_2 to remove native oxides. The n-GaAs/Pd(30 nm)/Sn(90 nm), n-GaAs/Pd(30 nm)/Sn(150 nm), n-GaAs/Pd(40 nm)/Sn(120 nm) and n-GaAs/Pd(50 nm)/Sn(125 nm) samples were prepared by a sequential deposition of Pd and Sn in a resistance heating evaporator without breaking vacuum. In addition, n-GaAs/Sn(25 nm)/Pd(25 nm) and n-GaAs/Pd(25 nm)/Sn(25 nm) samples were prepared in order to investigate the effect of the layering sequence on Ohmic behaviour. The base pressure was ~$4x10^{-7}$ Torr and pressure during evaporation was between $1.5x10^{-6}$ Torr and $3.5x10^{-6}$ Torr.

All samples were then annealed by a conventional graphite strip annealer in a flowing forming gas (5% H_2 + 95% N_2) ambient. The n-GaAs/Pd(30 nm)/Sn(90 nm) and n-GaAs/Pd(30 nm)/Sn(150 nm) contacts are annealed in the temperature range of 300-400 ^{0}C for 30 min, whereas the n-GaAs/Pd(40 nm)/Sn(120 nm) and n-GaAs/Pd(50 nm)/Sn(125 nm) contacts are annealed in the temperature ranges of 330-400 ^{0}C for 30 min and 360-425 ^{0}C for 30 min, respectively. The n-GaAs/Pd(25 nm)/Sn(25 nm) contact is annealed at 390 ^{0}C for 20 min, whereas the n-GaAs/Sn(25 nm)/Pd(25 nm) contact is annealed at 400 ^{0}C for 5 min. For two-step annealing, the samples were first annealed in a rapid thermal annealer (RTA), and then in a conventional graphite strip annealer under the same ambient condition.

Surface morphology of the contacts was investigated using a Tencor Instruments Surface Profilometer and a Hitachi S-4000 FESEM (FEM). A Cameca IMS3f SIMS intrument using an O_2^+ primary ion beam with an impact energy of 12.5 keV was used in depth profiling studies. Conversion from Schottky to Ohmic behaviour of the contacts was examined by I-V measurements. Contact resistivity was measured utilizing the cTLM method.

4.4 Results and Discussions

4.4.1 Electrical characteristics

The ρ_c of the Pd/Sn Ohmic contacts are measured in a test pattern conforming to the TLM (Fig.4.1), with the pad spacing ranging from 2 to 128 μm. The width of the Ohmic pad, W, is 140 μm. The transfer length method [12] is utilized to measure ρ_c values of the contacts. It is assumed that the sheet resistance of the semiconductor under the contacts, R_{sh}, is equal to the sheet resistance of the semiconductor between the contacts,

R_{sh2} Fig 4 4 shows the measured average contact resistivity vs annealing temperature curves for 4 TLM patterns The measured current-voltage curves show rectifying behaviour when the annealing temperature is ≤300 °C The Pd(30 nm)/Sn(150 nm) contact shows a lowest ρ_c of 3 26x10^{-5} Ω-cm^2 after annealing at 360 °C for 30 mm, whereas the Pd(30 nm)/Sn(90 nm) contact shows a lowest ρ_c of 6 05x10^{-5} Ω-cm^2 for the same annealing condition However, both Pd(40 nm)/Sn(120 nm) and Pd(50 nm)/Sn(125 nm) contacts exhibit a lowest ρ_c of 2 38x10^{-5} Ω-cm^2 and 2 07x10^{-5} Ω-cm^2, respectively after annealing at 400 ^{0}C for 30 mm Thus, metallization thickness has a significant effect on annealing cycles for the Pd/Sn contacts It is also clear that excess Sn does not lower the ρ_c values significantly Measurement errors, $\Delta\rho_c$, of the Pd/Sn Ohmic contacts at the lowest ρ_c points are shown in TABLE VII The Pd(50 nm)/Sn(125 nm) Ohmic contact appears to have excellent reproducibility with a $\Delta\rho_c$ of ±0 92x10^{-5} Ω-cm^2 among all metallizations investigated

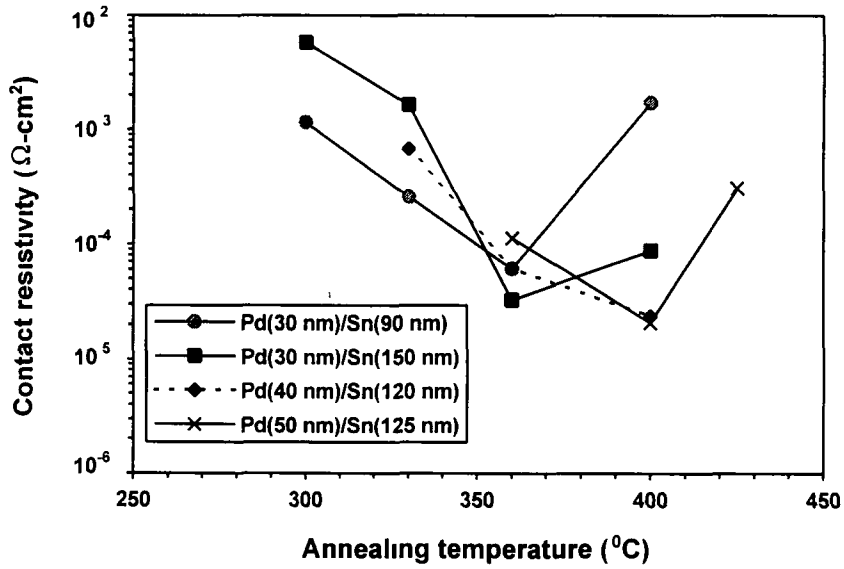


Fig 4 4 Contact resistivity vs annealing temperature curves of the Pd/Sn contacts to n-GaAs All contacts are annealed for 30 min

TABLE VII Summary of contact resistivity, ρ_c, and measurement error, $\Delta\rho_c$, of the Pd/Sn Ohmic contacts to n-GaAs

Contact structure	Annealing condition	ρ_c (Ω-cm^2)	$\Delta\rho_c$ (Ω-cm^2)
Pd(30 nm)/Sn(150 nm)	360 ^{0}C, 30 mm	3 26x10^{-5}	±2 50x10^{-5}
Pd(30 nm)/Sn(90 nm)	360 ^{0}C, 30 mm	6 05x10^{-5}	±1 63x10^{-5}
Pd(40 nm)/Sn(120 nm)	400 ^{0}C, 30 mm	2 38x10^{-5}	±1 25x10^{-5}
Pd(50 nm)/Sn(125 nm)	400 ^{0}C, 30 mm	2 07x10^{-5}	±0 92x10^{-5}

TABLE VIII Summary of calculated sheet resistance, R_{sh}, and transfer length, L_T, parameters of the Pd(30 nm)/Sn(150 nm) contact to n-GaAs under various annealing temperatures

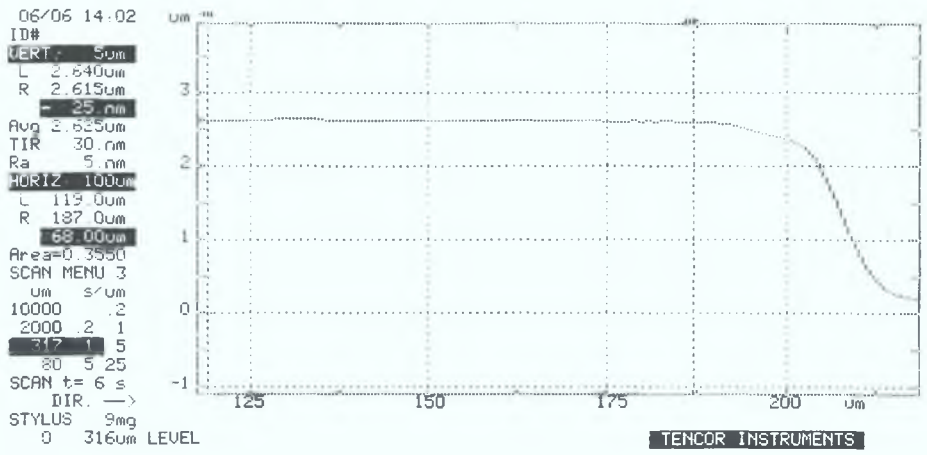
Annealing condition	R_{sh} (Ω/□)	L_T (μm)
300 ^{0}C, 30 min	191 49	54 91
330 ^{0}C, 30 min	192 80	29 18
360 ^{0}C, 30 min	165 00	04 45
400 ^{0}C, 30 min	288 08	05 53

TABLE VIII summarizes the calculated sheet resistance, R_{sh} and transfer length, L_T, parameters of the Pd(30 nm)/Sn(150 nm) contact under different annealing temperatures Both R_{sh} and L_T decrease up to an annealing temperature of 360 ^{0}C where the minimum ρ_c value occurs Above 360 ^{0}C, both R_{sh} and L_T tend to increase At 360 ^{0}C, L_T is 4 45 μm which is much lower than the length of contact, L_c (100 μm) This validates the application of the transfer length method for the Pd/Sn contacts

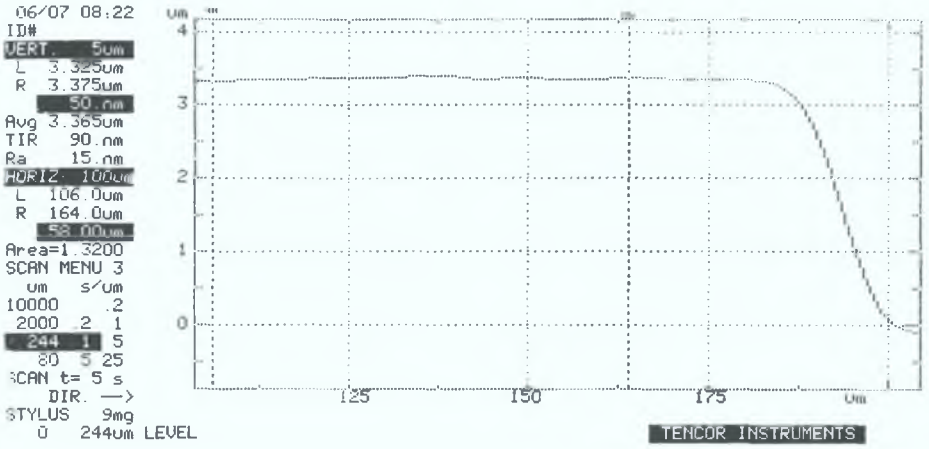
4.4.2 Surface profilometry measurements

Surface profiles of the Pd(30 nm)/Sn(150 nm) contacts under both as-deposited and lowest ρ_c conditions are shown in Fig 4 5 In the as-deposited condition, the maximum peak-to-valley distance, TIR, of the scanned surface is 30 nm and the average surface roughness, Ra, is 5 nm (Fig 4 5(a)) At the lowest ρ_c condition (360 ^{0}C, 30 min), these values are 90 nm and 15 nm, respectively (Fig 4 5(b)) TABLE IX summarizes the surface profiles of all Pd/Sn contacts under both as-deposited and at the lowest ρ_c conditions In the as-deposited state, the Pd(30 nm)/Sn(90 nm) contact shows a TIR of 30 nm and a Ra of 5 nm For the Pd(40 nm)/Sn(120 nm) contact, these values are 45 nm and 5 nm, respectively The Pd(50 nm)/Sn(125 nm) contact shows better surface profiles under as-deposited condition with a TIR of 24 5 nm and a Ra of 3 5 nm

At the lowest ρ_c point, the Pd(30 nm)/Sn(90 nm) contact displays a TIR of 10 nm and a Ra of 0 nm, whereas for the Pd(40 nm)/Sn(120 nm) contact these values are 60 nm and 10 nm, respectively The Pd(50 nm)/Sn(125 nm) contact shows a TIR of 33 nm and a Ra of 5 nm at the lowest ρ_c condition (400 ^{0}C, 30 min) Therefore, the Pd(30 nm)/Sn(90 nm) contact exhibits best surface profiles among all the contacts investigated at the lowest ρ_c conditions



(a)



(b)

Fig.4.5. Surface profiles of the Pd(30 nm)/Sn(150 nm) contact to n-GaAs: (a) as-deposited and (b) annealed at 360 ^{0}C, 30 min.

TABLE IX. Summary of surface profiles of the Pd/Sn contacts to n-GaAs under both as-deposited and lowest ρ_c conditions.

Contact structure	Annealing condition	TIR (nm)	Ra (nm)
Pd(30 nm)/Sn(150 nm)	as-deposited	30.0	5.0
Pd(30 nm)/Sn(150 nm)	360 ^{0}C, 30 min	90.0	15.0
Pd(30 nm)/Sn(90 nm)	as-deposited	30.0	5.0
Pd(30 nm)/Sn(90 nm)	360 ^{0}C, 30 min	10.0	0.0
Pd(40 nm)/Sn(120 nm)	as-deposited	45.0	5.0
Pd(40 nm)/Sn(120 nm)	400 ^{0}C, 30 min	60.0	10.0
Pd(50 nm)/Sn(125 nm)	as-deposited	24.5	3.5
Pd(50 nm)/Sn(125 nm)	400 ^{0}C, 30 min	33.0	5.0

4.4.3 Surface morphology using SEM

SEM micrographs of the Pd(30 nm)/Sn(150 nm) and Pd(30 nm)/Sn(90 nm) contacts under both as-deposited and lowest ρ_c conditions are shown in Fig.4.6. Micro-crystals of the order of ~1.0 μm in diameter are observed on the surface with the Pd(30 nm)/Sn(150 nm) contacts under both as-deposited (Fig.4.6(a)) and at the lowest ρ_c (Fig.4.6(b)) conditions. However, metallizations are more uniformly distributed at the lowest ρ_c point compared to the as-deposited state. The Pd(30 nm)/Sn(90 nm) contact shows micro-crystals of the order of ~0.5 μm in diameter under the as-deposited state (Fig.4.6(c)). After annealing at 360 ^{0}C for 30 min, the size of these micro-crystals does not change appreciably (Fig.4.6(d)) but the metallizations seems to be more uniformly distributed compared to the as-deposited condition. Therefore, excess Sn appears to have a significant effect on the surface morphology of the Pd/Sn contacts.

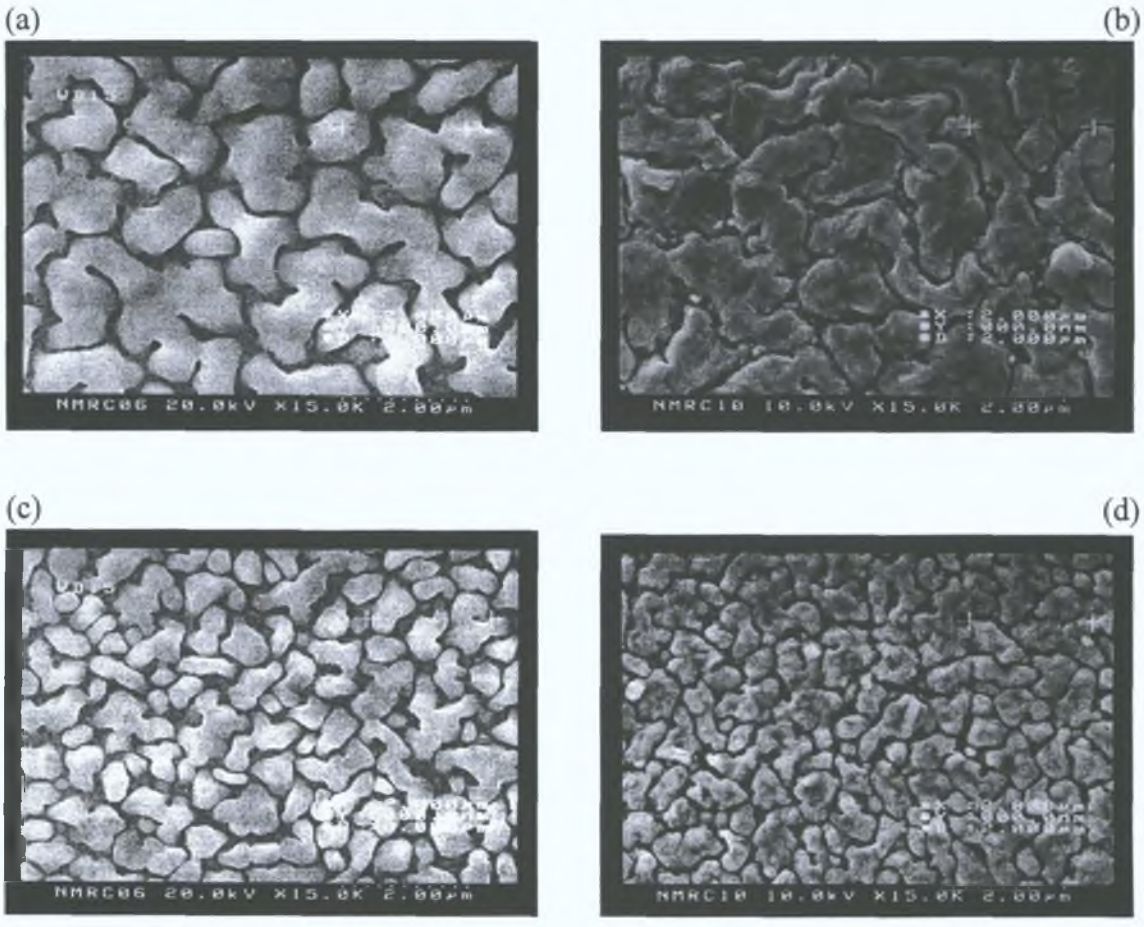


Fig.4.6. SEM micrographs of the Pd/Sn contacts to n-GaAs: (a) Pd(30 nm)/Sn(150 nm), as-deposited; (b) Pd(30 nm)/Sn(150 nm), 360 ^{0}C, 30 min; (c) Pd(30 nm)/Sn(90 nm), as-deposited and (d) Pd(30 nm)/Sn(90 nm), 360 ^{0}C, 30 min.

The size of micro-crystals improves significantly after annealing at the lowest ρ_c point for both Pd(40 nm)/Sn(120 nm) and Pd(50 nm)/Sn(125 nm) contacts (Fig 4 7) In the as-deposited state, Pd(40 nm)/Sn(120 nm) and Pd(50 nm)/Sn(125 nm) contacts show micro-crystals of the order of ~1 0 μm and ~0 75 μm diameters, respectively (Figs 4 7(a) & 4 7(c)) At the lowest ρ_c point, the size of micro-crystals decreases to ~0 5 μm for both contacts (Figs 4 7(b) & 4 7(d)) Thus, excess Pd shows little effect on the surface morphology of the Pd/Sn contacts

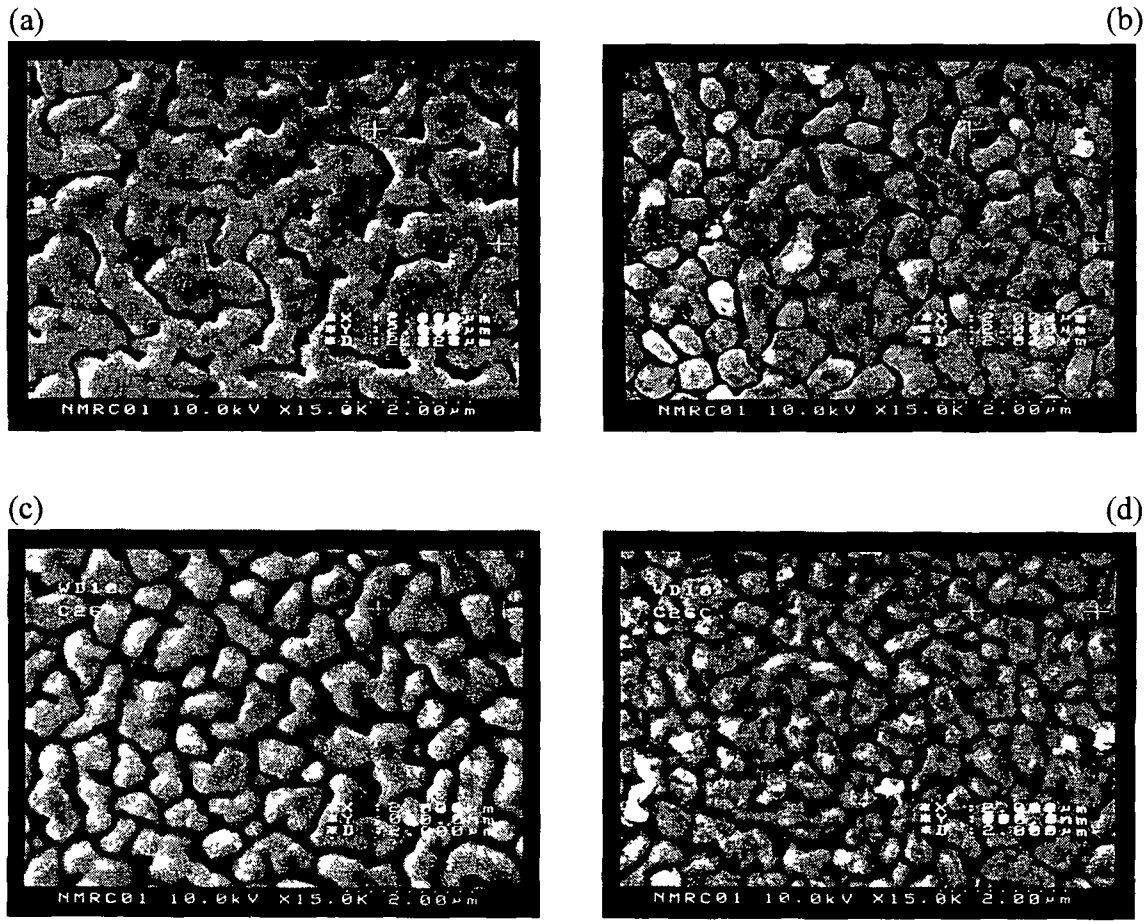


Fig 4 7 SEM micrographs of the Pd/Sn contacts on n-GaAs (a) Pd(40 nm)/Sn(120 nm), as-deposited, (b) Pd(40 nm)/Sn(120 nm), 400 ^{0}C, 30 min, (c) Pd(50 nm)/Sn(125 nm), as-deposited and (d) Pd(50 nm)/Sn(125 nm), 400 ^{0}C, 30 mm

It is postulated that the Ohmic contact formation mechanism of the Pd/Sn metallization to n-GaAs is similar to that which occurs in the Pd/Ge metallization (Fig 1 5), with Sn taking the place of Ge and is shown schematically in Fig 4 8 In Pd/Sn metallization, Sn dopes n-GaAs at temperatures T≥300 ^{0}C (Fig 4 8) and consequently a low resistance Ohmic contact is obtained At the lowest ρ_c point, all of the Pd could react to form the compound PdSn which is comparable to PdGe formation

for the Pd/Ge metallization scheme annealed at 325 ^{0}C for 30 min [18] This layer is at the sample surface It is believed that excess Sn is now transported through the PdSn layer to dope the n-GaAs to form n^+-GaAs layer resulting in the lowering of ρ_c values

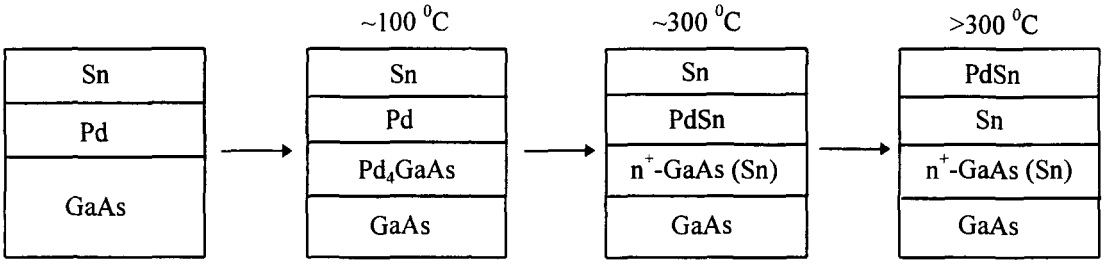


Fig 4 8 Schematic representation of regrowth mechanisms using the Pd/Sn metallization to n-GaAs (postulated)

4.4.4 Contact depth profiles using SIMS

SIMS depth profiling shows how metallizations penetrate into the underlying GaAs Due to the 'knock-on' effect of the primary O_2^+ ion on the contact constituent elements, it is difficult to determine the exact penetration depths of metals into the underlying GaAs using SIMS In the as-deposited sample, knock-on produces "metal tails" Preferential knock-on of species is not responsible for the shape changes of profiles, rather they reflect genuine diffusion Therefore, the best approach is to compare shapes (e g peaks) and look for relative changes between profiles

The SIMS depth profiles of Pd(30 nm)/Sn(150 nm) and Pd(30 nm)/Sn(90 nm) contacts at the lowest ρ_c point are shown in Fig 4 9 and Fig 4 10, respectively The depth profiles for Pd and Sn of the former contact (Fig 4 9) have lower slopes than those of the latter contact (Fig 4 10) However, the Ga and As profiles are identical for both contacts Therefore, a Pd(30 nm)/Sn(90 nm) contact is more abrupt than that of a Pd(30 nm)/Sn(150 nm) contact

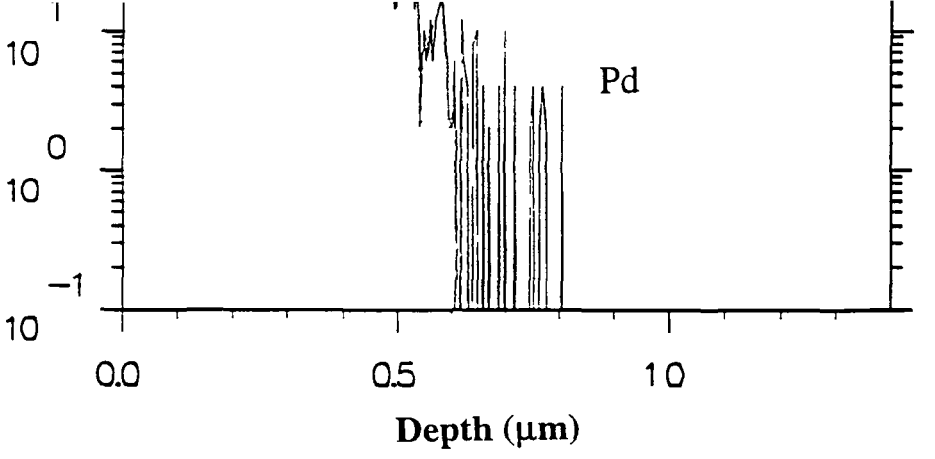
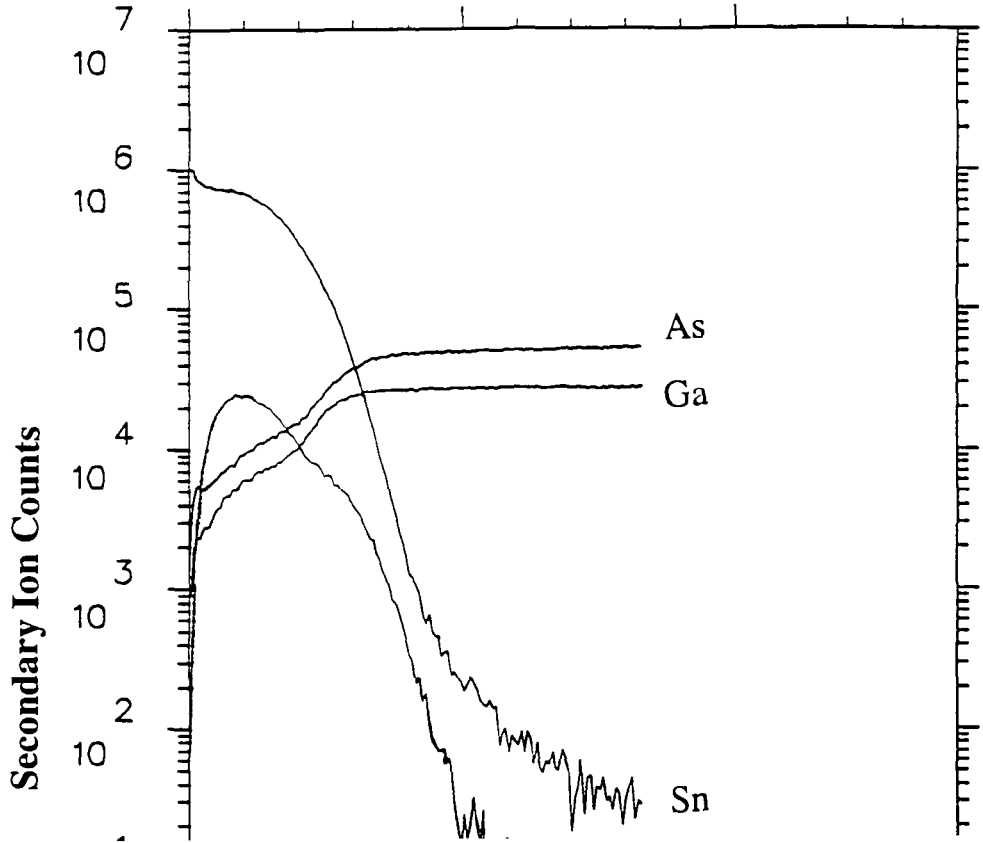


Fig 4 9 SIMS depth profiles of the Pd(30 nm)/Sn(150 nm) contact annealed at 360 ^{0}C, 30 min


Secondary Ion Counts
7
10
6
10
5
10
4
10
3
10
2
10
As
Ga
Sn

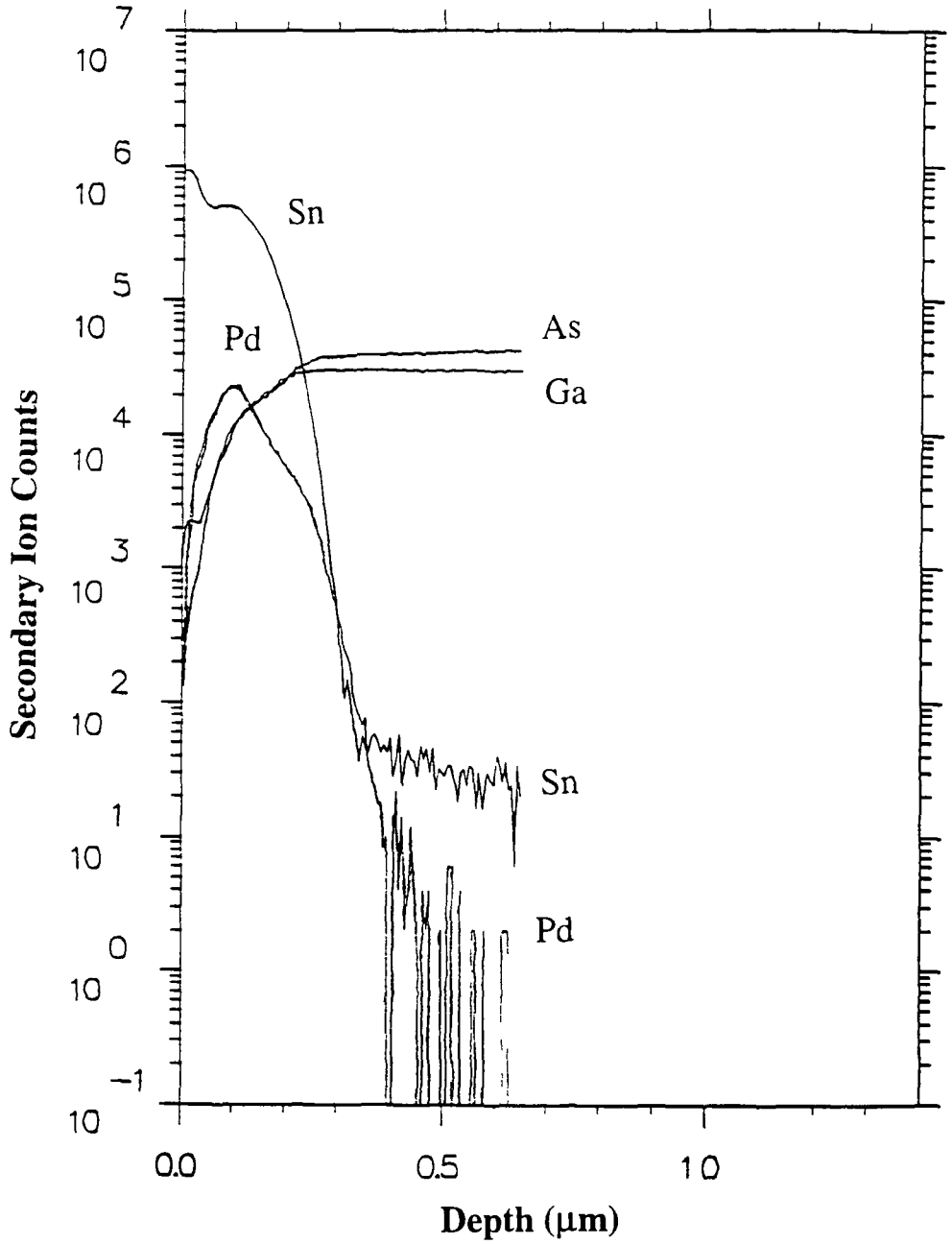


Fig 4 10 SIMS depth profiles of the Pd(30 nm)/Sn(90 nm) contact annealed at 360 ^{0}C, 30 min

SIMS depth profiles of the Pd(40 nm)/Sn(120 nm) contact under both as-deposited and lowest ρ_c (400 ^{0}C, 30 min) conditions are shown in Fig 4 11 and Fig 4 12, respectively The metal/GaAs interface is well defined in the as-deposited state (Fig 4 11) After annealing at 400 ^{0}C for 30 min, Ga and As profiles remain almost identical as those in as-deposited state, although slight outdiffusion of Ga and As is observed at this temperature (Fig 4 12) The slopes of Pd and Sn profiles decrease

significantly after annealing The widths of both Pd and Sn profiles are almost doubled at the lowest ρ_c point (Fig 4 12) compared to the as-deposited state (Fig 4 11) indicating significant metal penetration into the underlying GaAs substrate However, the exact penetration depth can not be determined due to the 'knock-on' effect as described earlier

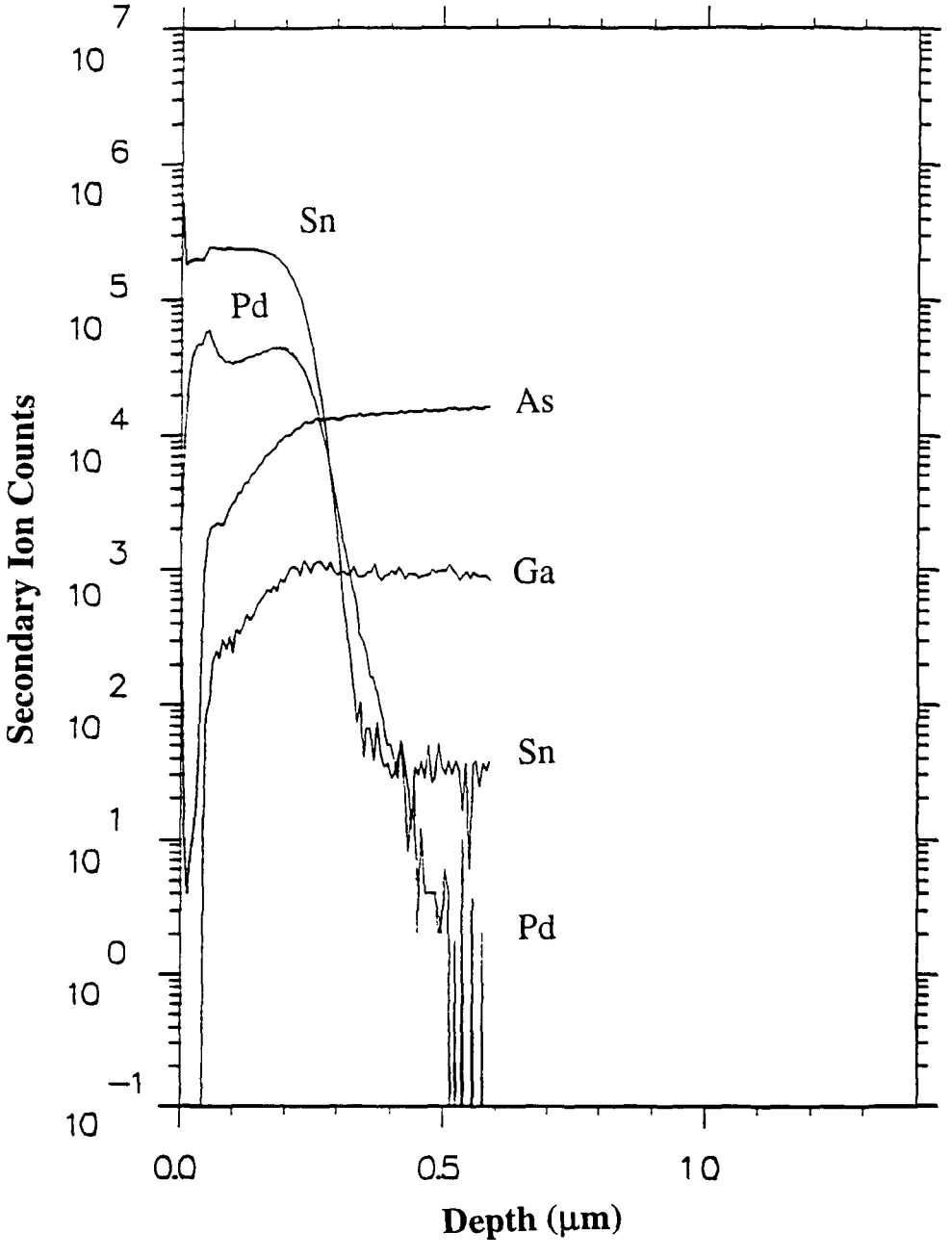


Fig 4 11 SIMS depth profiles of the Pd(40 nm)/Sn(120 nm) contact under as-deposited condition

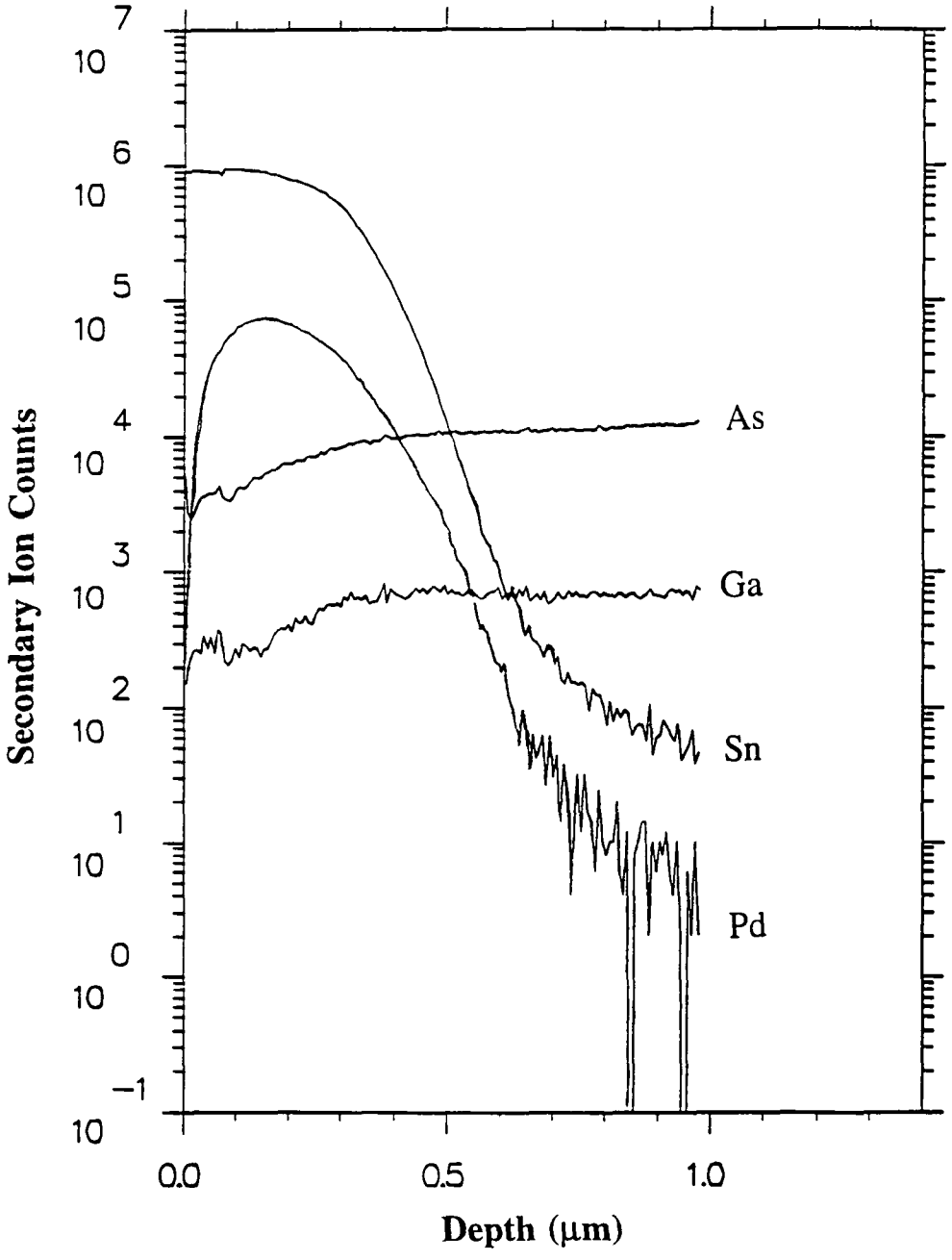
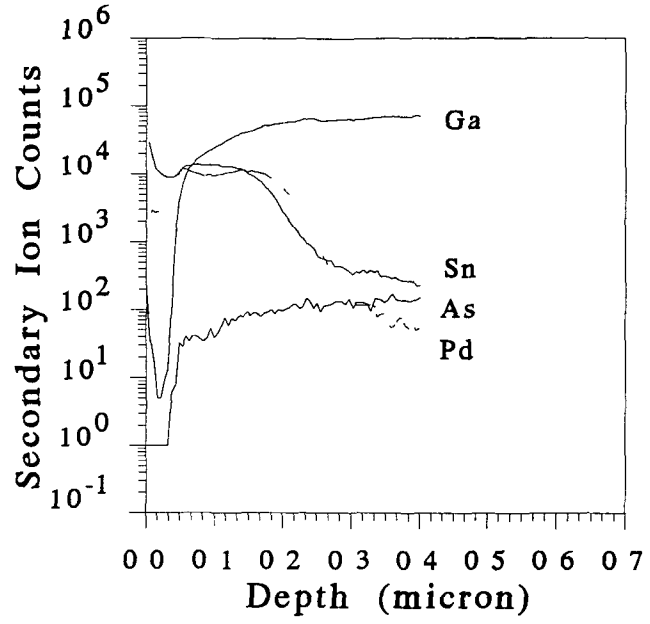


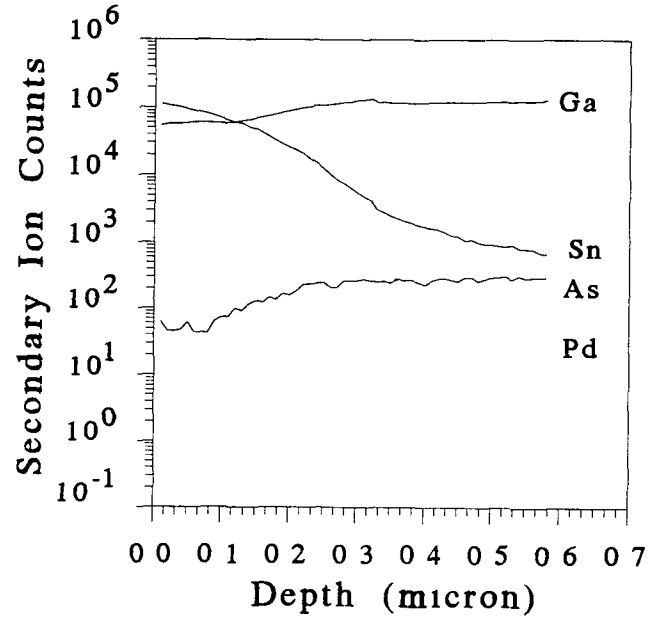
Fig 4 12 SIMS depth profiles of the Pd(40 nm)/Sn(120 nm) contact annealed at 400 ^{0}C, 30 min

Fig 4 13 shows the SIMS depth profiles of the Pd(50 nm)/Sn(125 nm) contact under both as-deposited (Fig 4 13(a)) and annealed at 400 ^{0}C for 30 mm (Fig 4 13(b)) conditions Outdiffusions of Ga and As are observed after annealing at 400 ^{0}C for 30 mm The shape of Pd profile does not change appreciably after annealing However, the shape of Sn profile changes significantly indicating Sn penetration into underlying GaAs substrate

From the SIMS depth profiles (from Fig 4 9 to Fig 4 13) it is clear that both Pd(40 nm)/Sn(120 nm) and Pd(50 nm)/Sn(125 nm) contacts have wider depth profiles compared to both Pd(30 nm)/Sn(150 nm) and Pd(30 nm)/Sn(90 nm) contacts at the lowest ρ_c points This is due to a higher temperature (400 ^{0}C) requirement at the lowest ρ_c point for both Pd(40 nm)/Sn(120 nm) and Pd(50 nm)/Sn(125 nm) contacts The Pd(30 nm)/Sn(90 nm) contact shows the most abrupt metal/GaAs interface among all Pd/Sn contacts investigated

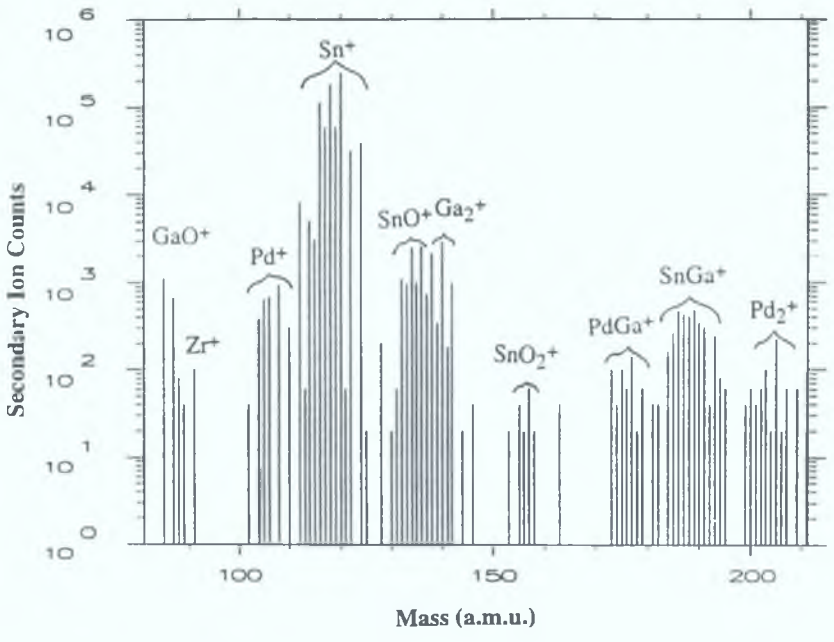


(a)

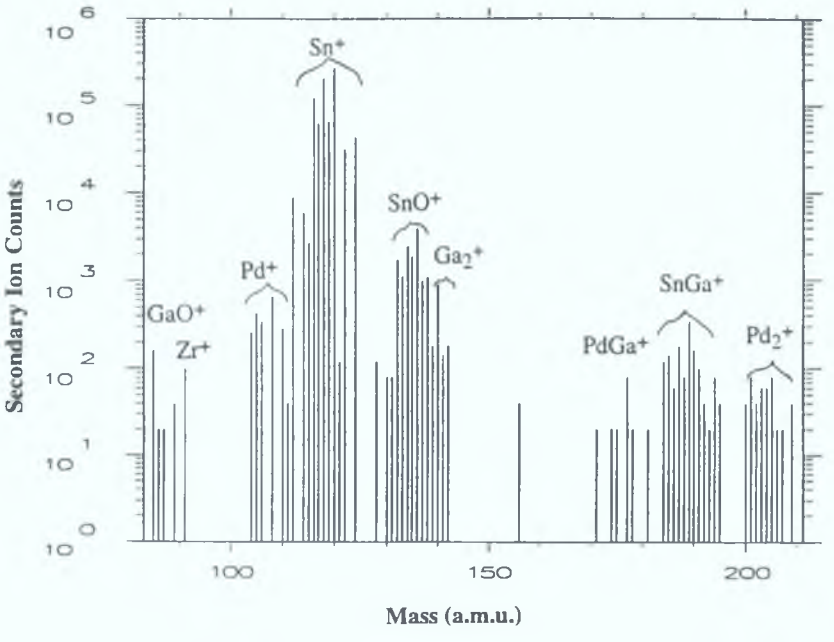


(b)

Fig 4 13 SIMS depth profiles of the Pd(50 nm)/Sn(125 nm) contact (a) as-deposited and (b) annealed at 400 ^{0}C, 30 min



(a)



(b)

Fig.4.14. Mass spectra of positive secondary ions for (a) Pd(30 nm)/Sn(150 nm) and (b) Pd(30 nm)/Sn(90 nm) contacts, both annealed at 360 ^{0}C, 30 min.

4.4.5 Mass spectrometer analysis

Fig.4.14 shows the mass spectrometer analysis of positive secondary ions for the Pd(30 nm)/Sn(150 nm) and Pd(30 nm)/Sn(90 nm) contacts at the lowest ρ_c point. Positive secondary ions of Pd^+, Sn^+, Si^+, As^+, Ga^+, Ga_2^+, GaO^+, SnO^+, SnO_2^+, $PdGa^+$, $SnGa^+$ and

Pd_2^+ are monitored in the ion microanalyzer for both contacts. Mass spectrometer analysis of the Pd(50 nm)/Sn(125 nm) contact at the lowest ρ_c point is shown in Fig.4.15. The observed secondary ions are identical to those found with both Pd(30 nm)/Sn(150 nm) and Pd(30 nm)/Sn(90 nm) contacts (Fig.4.14).

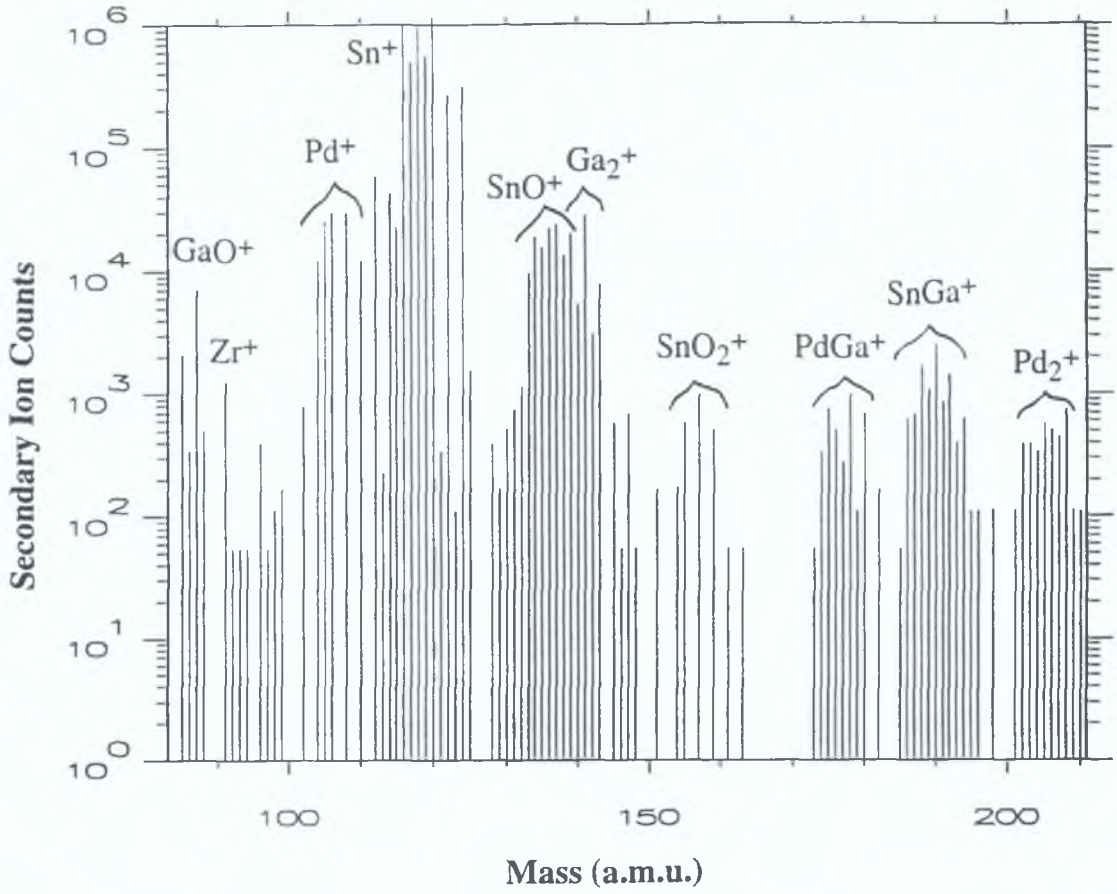


Fig.4.15. Mass spectra of positive secondary ions for the Pd(50 nm)/Sn(125 nm) contact annealed at 400 ^{0}C, 30 min.

At the lowest ρ_c point, $SnPd^+$ ions should be monitored in the microanalyzer and they will have an atomic mass unit (amu) of ~226. SIMS is not very chemically sensitive to $SnPd^+$ species and these species will be formed in the plasma within the instrument. At high amu the noise increases and weak signals are unreliable. For this reason, $SnPd^+$ ions are not detected. The detection of PdSn compound formation would support the non-alloying behaviour of the contacts. Since we failed to detect PdSn compound formation due to SIMS insensitivity as described above, the non-alloying behaviour of the contacts could not be confirmed. However, the detection of $PdGa^+$ and $SnGa^+$ ions indicates the outdiffusion of Ga into the metallization.

4.4.6 Correlation between Ga signal and contact behaviour

Fig 4 16 shows the EDAX spectra of the Pd(30 nm)/Sn(150 nm) contacts at various annealing temperatures TABLE X also summarizes the calculated various signal peaks from EDAX spectra at different annealing temperatures As the annealing temperature increases from 300 ^{0}C (Fig 4 16(a)) to 360 ^{0}C (Fig 4 16(b)), the peak of the Ga signal also increases This signifies Ga outdiffusion into the metallization and formation of more Ga vacant sites in n-GaAs The dopant Sn now occupies these Ga vacant sites to dope the n-GaAs resulting in the formation of epitaxial n^+-GaAs and thus lowers ρ_c values This Ga signal peak is highest at 360 ^{0}C which correlates with the lowest ρ_c value at that temperature The signal peaks of As decreases with increasing annealing temperature Since annealing is carried out in an open system where As vaporizes through the metallization into the surrounding atmosphere or to vacuum, the loss of As increases with the increase in annealing temperatures The diffusivity and or solubility of Ga in Pd is greater than that of As [2] The Pd/Sn metallization serves as a sink for Ga in much the same way that Au acts as a sink for Ga in Au-Ge based Ohmic contacts [120,121] The Pd and Sn signal peaks decrease with increasing temperature This type of behaviour is anticipated since more reactions are expected at increased temperatures indicating more compound (e g PdGa and SnGa) formation as evidenced by mass spectrometer analysis (Fig 4 14)

TABLE X Summary of calculated signal peaks from EDAX spectra of the Pd(30 nm)/Sn(150 nm) contacts after annealing for 30 mm at different temperatures

Annealing temperature	Peak counts of Ga (a u)	Peak counts of As (a u)	Peak counts of Pd (a u)	Peak counts of Sn (a u)
300 ^{0}C	265	372	620	1389
360 ^{0}C	354	377	593	1293
400 ^{0}C	339	320	594	1090

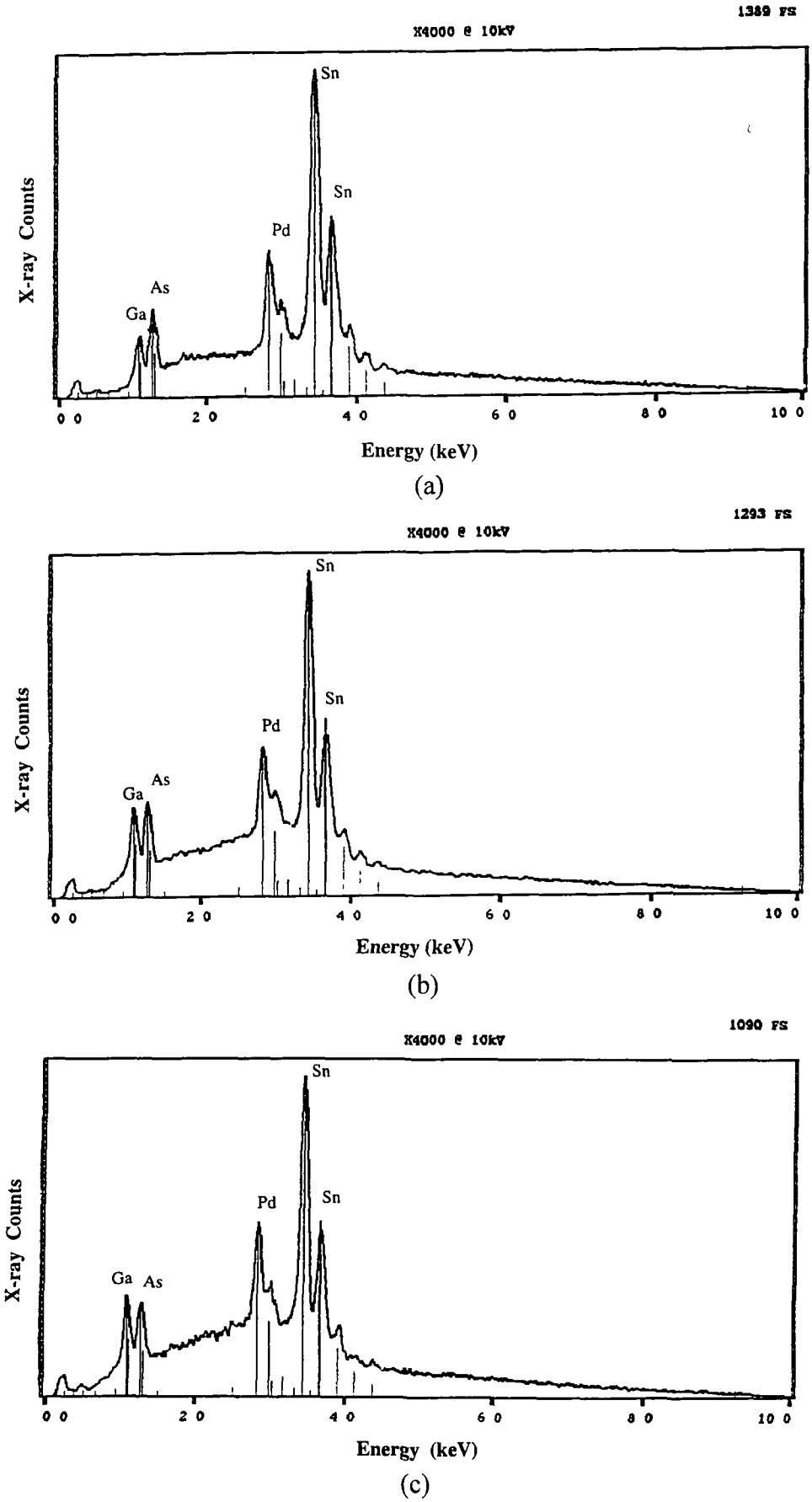
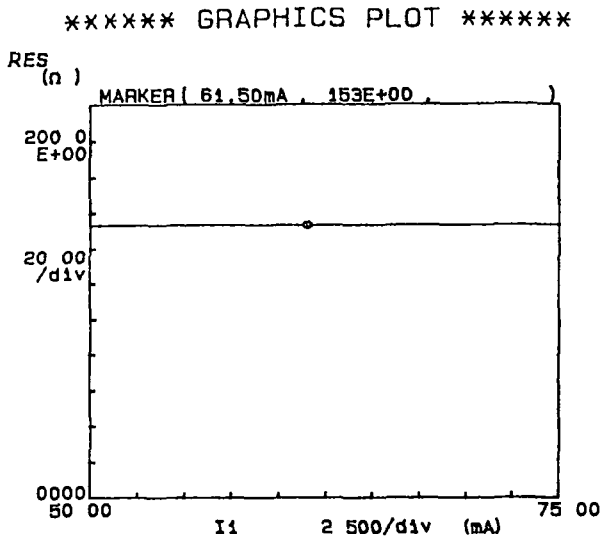


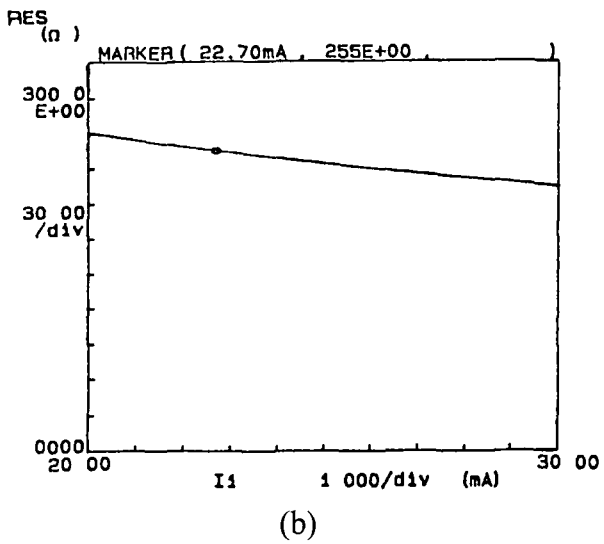
Fig 4 16 EDAX spectra of the Pd(30 nm)/Sn(150 nm) contacts after annealing for 30 min at (a) 300 ^{0}C, (b) 360 ^{0}C and (c) 400 ^{0}C

4.4.7 Effect of layering sequence

Plots of the I-V behaviour of the Pd(25 nm)/Sn(25 nm) and Sn(25 nm)/Pd(25 nm) metallizations to n-GaAs are shown in Fig 4 17 The n-GaAs/Pd(25 nm)/Sn(25 nm) contact shows Ohmic behaviour (constant resistance) after annealing at 390 ^{0}C for 20 min (Fig 4 17(a)), whereas the n-GaAs/Sn(25 nm)/Pd(25 nm) contact shows rectifying behaviour (variable resistance) after annealing at 400 ^{0}C for 5 min This result indicates that Pd must be the first layer deposited on chemically cleaned n-GaAs in order to fabricate Ohmic contacts using the Pd/Sn metallization This is consistent with the idea that Pd disperses the native oxides from the n-GaAs surface in order that the epitaxial growth of Sn can occur during the annealing treatment [2]



(a)



(b)

Fig 4 17 Graphics plots of (a) n-GaAs/Pd(25 nm)/Sn(25 nm) contact annealed at 390 ^{0}C for 20 min and (b) n-GaAs/Sn(25 nm)/Pd(25 nm) contact annealed at 400 ^{0}C for 5 min

4.4.8 Effects of two-step annealing on the characteristics of Pd/Sn Ohmic contacts

Two-step annealing can improve the overall properties of Ohmic contacts [71] In order to investigate the effects of two-step annealing, the Pd(30 nm)/Sn(150 nm) contacts are first annealed in a RTA and then in a conventional graphite strip annealer TABLE XI summarizes the measured ρ_c and R_{sh} values under both single-step and two-step annealing conditions A ρ_c of 3 26x10^{-5} Ω-cm^2 is obtained after single-step annealing at 360 ^{0}C for 30 min The same contact shows ρ_c of 1 49x10^{-5} Ω-cm^2 and 1 53x10^{-5} Ω-cm^2 after two-step annealing of 225 ^{0}C, 50 s + 350 ^{0}C, 15 min and 225 ^{0}C, 2 mm + 350 ^{0}C, 10 min, respectively After annealing at 200 ^{0}C, 2 min + 400 ^{0}C, 15 mm, the Pd(30 nm)/Sn(150 nm) contact displays a ρ_c of 3 35x10^{-5} Ω-cm^2 Therefore, two-step annealing improves the electrical characteristics of the Pd/Sn contacts very slightly In addition, two-step annealing has almost insignificant effect on R_{sh}

TABLE XI Summary of measured contact resistivity, ρ_c, and sheet resistance, R_{sh}, of the Pd(30 nm)/Sn(150 nm) contacts to n-GaAs under both single-step and two-step annealing conditions

Annealing condition	ρ_c (Ω-cm^2)	R_{sh} (Ω/□)
360 ^{0}C, 30 min	3 26x10^{-5}	165 00
225 ^{0}C, 50 s + 350 ^{0}C, 15 min	1 49x10^{-5}	160 00
225 ^{0}C, 2 mm + 350 ^{0}C, 10 min	1 53x10^{-5}	159 35
200 ^{0}C, 2 min + 400 ^{0}C, 15 min	3 35x10^{-5}	133 82

TABLE XII Summary of surface profiles of the Pd(30 nm)/Sn(150 nm) contacts to n-GaAs under different annealing conditions

Annealing conditions	TIR (nm)	Ra (nm)
360 ^{0}C, 30 min	90	15
225 ^{0}C, 50 s + 350 ^{0}C, 15 min	20	0
225 ^{0}C, 2 mm + 350 ^{0}C, 10 min	85	10
200 ^{0}C, 2 min + 400 ^{0}C, 15 min	90	15

TABLE XII summarizes the surface profiles of the Pd(30 nm)/Sn(150 nm) contacts under both types of annealing Single-step annealing (360 ^{0}C, 30 mm) shows a maximum peak-to-valley distance of the scanned surface, TIR, of 90 nm and average

surface roughness, Ra, of 15 nm. Two-step annealing conditions exhibit better surface profiles compared to single-step annealing. Annealing at 225 ^{0}C, 50 s + 350 ^{0}C, 15 min shows the best results with a TIR of 20 nm and a Ra of 0 nm. Therefore, two-step annealing improves the surface profiles of the Pd/Sn Ohmic contacts significantly.

SEM micrographs of the Pd(30 nm)/Sn(150nm) contacts are shown in Fig.4.18. Micro-crystals of the order of ~1.0 μm in diameter are observed after annealing at 360 ^{0}C for 30 min (Fig.4.18(a)). The size of micro-crystals decreases to ~0.75 μm in diameter when annealed at 225 ^{0}C, 50 s + 350 ^{0}C, 15 min (Fig.4.18(b)) and 225 ^{0}C, 2 min + 350 ^{0}C, 10 min (Fig.4.18(c)). However, two-step annealing at 200 ^{0}C, 2 min + 400 ^{0}C, 15 min (Fig.4.18(d)) shows micro-crystals of the order of ~1.0 μm in diameter. Surface profilometry measurements (TABLE XII) also reveal these results. Therefore, judicious choice of two-step annealing can improve the morphological characteristics of the Pd/Sn Ohmic contacts.

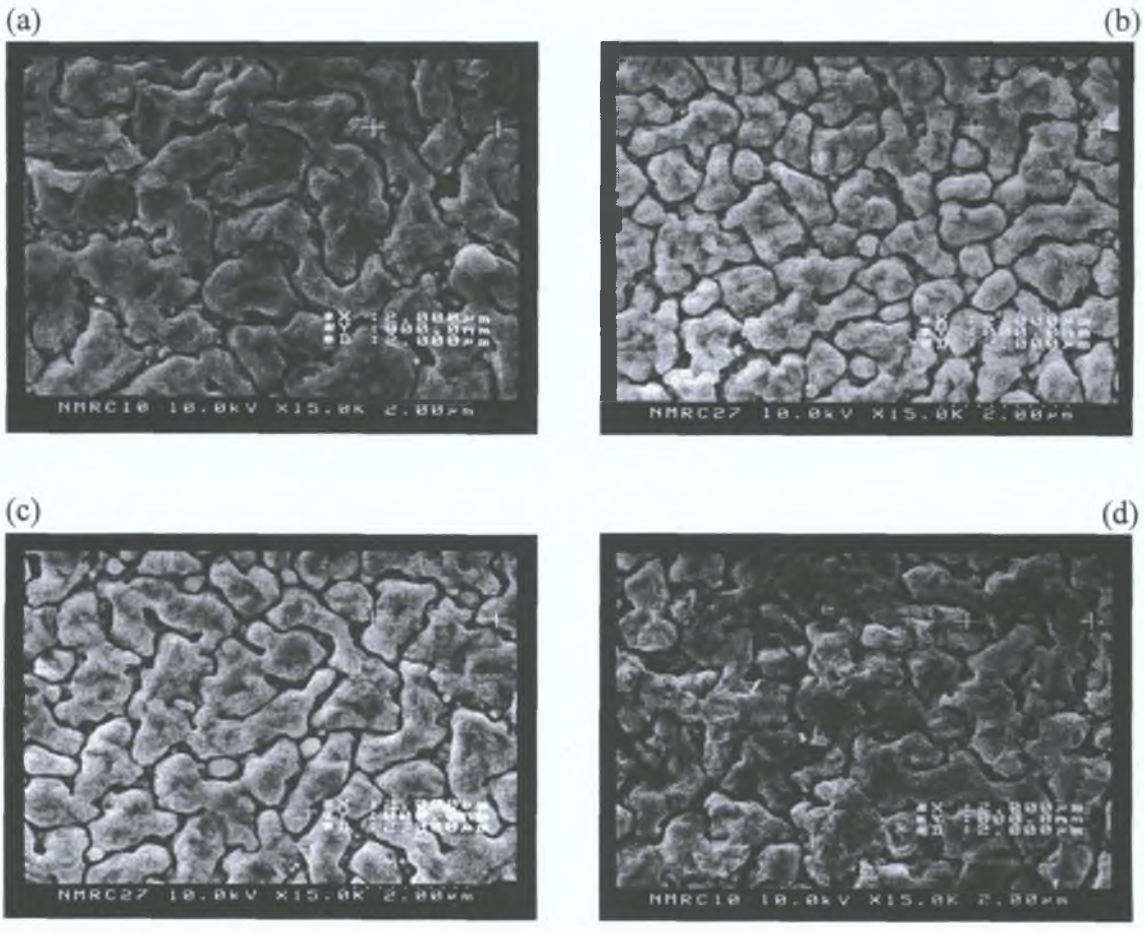


Fig.4.18. SEM micrographs of the Pd(30 nm)/Sn(150 nm) contacts at various annealing conditions: (a) 360 ^{0}C, 30 min; (b) 225 ^{0}C, 50 s + 350 ^{0}C, 15 min; (c) 225 ^{0}C, 2 min + 350 ^{0}C, 10 min and (d) 200 ^{0}C, 2 min + 400 ^{0}C, 15 min.

Fig 4 19 and Fig 4 20 show the SIMS depth profiles of the Pd(30 nm)/Sn(150 nm) contact after annealing at 225 ^{0}C, 50 s + 350 ^{0}C, 15 min and 225 ^{0}C, 2 min + 350 ^{0}C, 10 min, respectively The depth profiles of Pd and Sn are almost identical to those found in single-step annealing at 360 ^{0}C, 30 mm (Fig 4 9) However, the signal peaks of Ga and As are higher in single-step annealing (Fig 4 9) than those of two-step annealing (Fig 4 19 & Fig 4 20) Therefore, aforementioned two-step annealings do not improve the abruptness of the Pd(30 nm)/Sn(150 nm) contacts However, two-step annealing at 225 ^{0}C, 50 s + 350 ^{0}C, 15 min (Fig 4 19) shows higher slopes of Pd and Sn profiles compared to two-step annealing at 225 ^{0}C, 2 min + 350 ^{0}C, 10 min (Fig 4 20) with almost identical ρ_c values (TABLE XI)

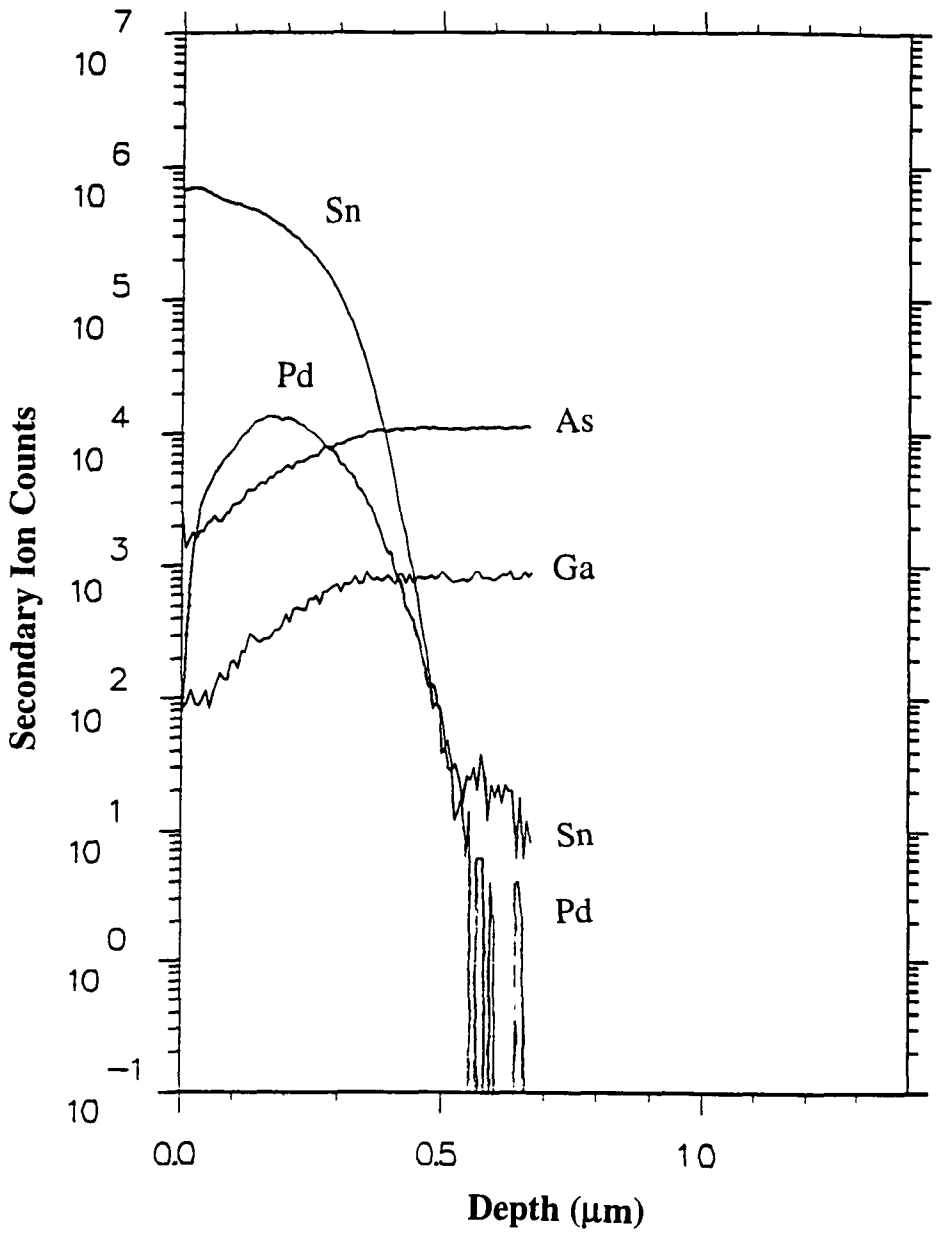


Fig 4 19 SIMS depth profiles of the Pd(30 nm)/Sn(150 nm) Ohmic contact annealed at 225 ^{0}C, 50 s + 350 ^{0}C, 15 min

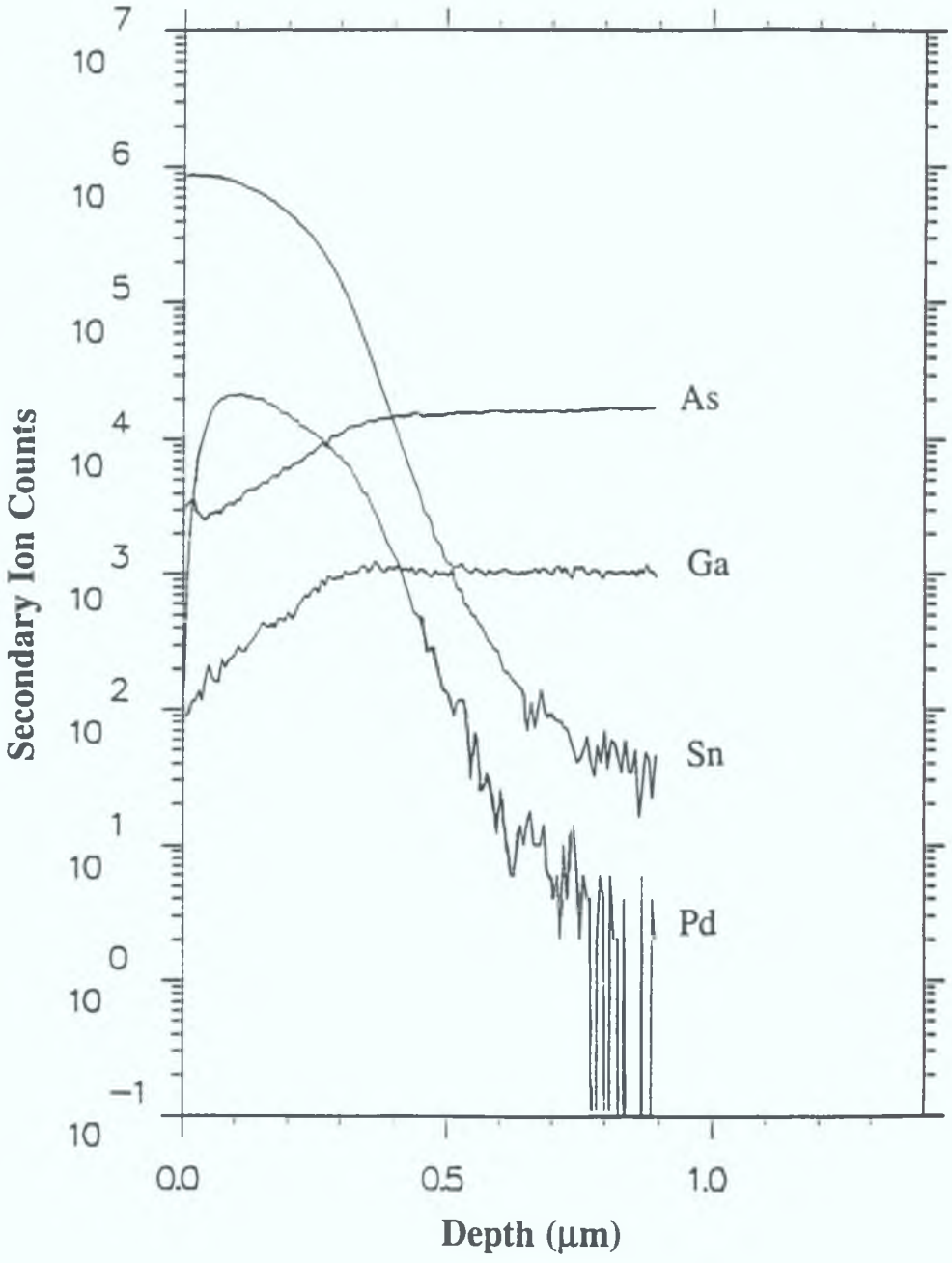


Fig.4.20. SIMS depth profiles of the Pd(30 nm)/Sn(150 nm) Ohmic contact after annealed at 225 ^{0}C, 2 min + 350 ^{0}C, 10 min.

Fig.4.21 shows the SIMS depth profiles of the Pd(30 nm)/Sn(150 nm) Ohmic contact annealed at 200 ^{0}C, 2 min + 400 ^{0}C, 15 min. The Pd and Sn profiles are wider and have lower slopes than those of single-step annealing at 360 ^{0}C, 30 min (Fig.4.9). However, peak counts of both Ga and As profiles are identical in both types of annealing. Thus two-step annealing at 200 ^{0}C, 2 min + 400 ^{0}C, 15 min deteriorates the abruptness of the contact. This is due to higher temperature (400 ^{0}C) used in the case of this annealing.

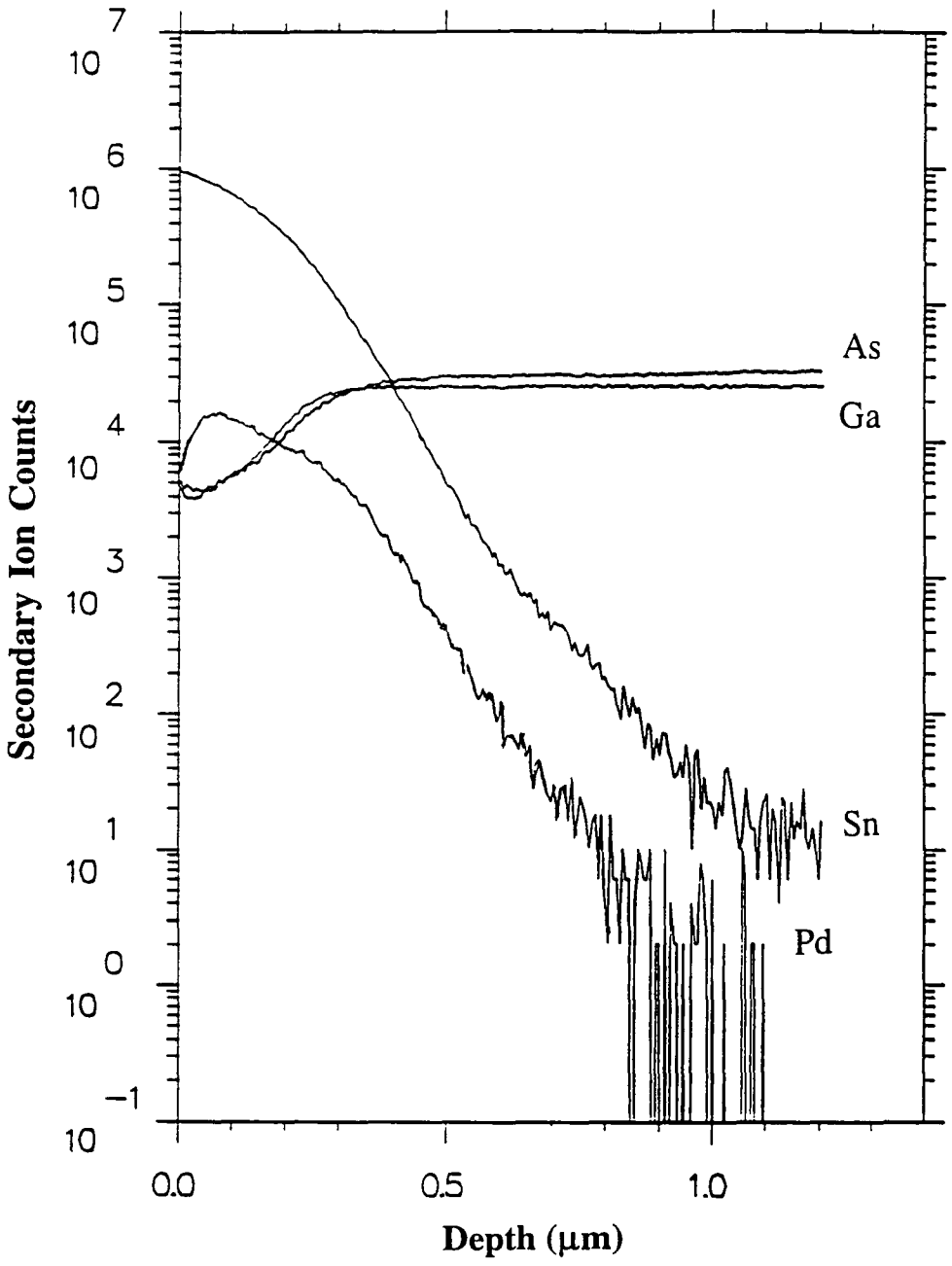


Fig 4 21 SIMS depth profiles of the Pd(30 nm)/Sn(150 nm) Ohmic contact annealed at 200 ^{0}C, 2 min + 400 ^{0}C, 15 min

4.5 Summary

In summary, a novel Ohmic contact system comprising of Pd/Sn metallization has been developed for n-GaAs The effects of metallization thickness on the characteristics of Pd/Sn Ohmic contacts are reported Metallization thickness shows little effect on the

electrical characteristics of the contacts A lowest ρ_c of 3 26x10^{-5} Ω-cm^2 is obtained for a substrate doping of 2x10^{18} cm^{-3} with a Pd(30 nm)/Sn(150 nm) contact after annealing at 360 ^{0}C for 30 mm, whereas the Pd(30 nm)/Sn(90 nm) contact shows a lowest ρ_c of 6 05x10^{-5} Ω-cm^2 at the same annealing condition Thus excess Sn does not lower the ρ_c values significantly Metallization thickness has a significant effect on the annealing cycles at the lowest ρ_c points The Pd(40 nm)/Sn(120 nm) contact produces a lowest ρ_c of 2 38x10^{-5} Ω-cm^2 at 400 ^{0}C, 30 mm, whereas a lowest ρ_c of 2 07x10^{-5} Ω-cm^2 is obtained with the Pd(50 nm)/Sn(125 nm) contact under the same annealing condition The Pd(50 nm)/Sn(125 nm) contact exhibits excellent reproducibility among all metallizations investigated

The Pd(30 nm)/Sn(90 nm) Ohmic contact appears to have the best surface morphology and least metal penetration into the underlying GaAs among all contacts investigated as evidenced by Surface Profilometry measurements, SEM and SIMS Two-step annealing has little effect on the electrical characteristics of the Pd/Sn Ohmic contacts Two-step annealing at 225 ^{0}C, 50 s + 350 ^{0}C, 15 min gives a ρ_c of 1 49x10^{-5} Ω-cm^2 with a Pd(30 nm)/Sn(150 nm) Ohmic contact Proper choice of two-step annealing cycles improves the morphological characteristics of the contacts However, two-step annealing does not improve the abruptness of the contacts

The EDAX spectra indicate an increase in Ga out-diffusion with an increase in annealing temperatures This behaviour is correlated with the calculated ρ_c values Mass spectrometer analysis indicates the formation of PdGa and SnGa compounds at the lowest ρ_c conditions However, the formation of PdSn compounds could not be identified due to SIMS insensitivity as described in 4 4 5 For this reason the non-alloymg behaviour of the contact could not be confirmed Pd must be the first layer deposited on n-GaAs in order to fabricate Ohmic contacts using the Pd/Sn metallization All evidence is consistent with a replacement mechanism in which an n$^+$-GaAs surface region is formed when Sn occupies excess Ga vacant sites resulting in higher tunneling probability and lower ρ_c values

CHAPTER 5

Effects of Au overlayers on the characteristics of Pd/Sn Ohmic contacts to n-GaAs

5.1 Introduction

The effects of Au overlayers on the characteristics of non-alloyed Pd/Sn Ohmic contacts have been studied Metallizations are deposited using a resistance heating evaporator and annealing is carried out in a conventional graphite strip annealer Surface morphology of the contacts is investigated using Surface Profilometry measurements and Scanning Electron Microscopy (SEM) The contact depth profiles are analyzed by Secondary Ion Mass Spectrometry (SIMS) Conversion from Schottky to Ohmic behaviour of the contacts is confirmed by I-V measurements Contact resistivities, ρ_c, of the proposed metallizations are measured using the conventional Transmission Line Model (cTLM) method The formation of various compounds at the lowest ρ_c point will be determined by mass spectrometer analysis Finally, a comparison will be made among non-alloyed Pd/Sn and Pd/Sn/Au and alloyed five-layer Au/Ge/Au/Ni/Au contacts

5.2 Experiments

Contacts were fabricated on a Si-doped ($2x10^{18}$ cm^{-3}) n-GaAs epitaxial layer grown by metal-organic vapor phase epitaxy (MOVPE) in a metal-semiconductor field-effect transistor (MESFET) structure shown previously in Fig 4 3 The GaAs substrates were sequentially cleaned and degreased in trichloroethylene, acetone, methanol and de-ionized water (DI H_2O), each for 10 mm The substrates were blow-dried immediately using dry nitrogen (N_2) Ohmic test, morphology and TLM patterns were defined by standard photolithography and lift-off processes A solution of H_2O_2 NH_4OH DI H_2O (1.3:15 by volume) was used as an etchant for mesa definition

Prior to loading into an evaporator, the wafers were soaked in a solution of DI H_2O:HCl (15:1 by volume) for at least 2 min and then blow dried using dry N_2 to remove native oxides. Samples consisting of n-GaAs/Pd(30 nm)/Sn(150 nm)/Au(40 nm), n-GaAs/Pd(30 nm)/Sn(150 nm)/Au(100 nm), n-GaAs/Pd(50 nm)/Sn(125 nm)/Au(40 nm), n-GaAs/Pd(50 nm)/Sn(125 nm)/Au(100 nm), n-GaAs/Pd(25 nm)/Sn(102 nm)/Au(100 nm) and n-GaAs/Au(14 nm)/Ge(14 nm)/Au(14 nm)/Ni(11 nm)/Au(200 nm) structures were prepared by sequential deposition of metallizations in a resistance heating evaporator without breaking vacuum. The base pressure was ~$4x10^{-7}$ Torr and pressure during evaporation was between $1x10^{-6}$ Torr and $6x10^{-6}$ Torr.

All samples with n-GaAs/Pd/Sn/Au structures were then annealed in the temperature range of 300-360 ^{0}C for 30 min by a conventional graphite strip annealer in a flowing forming gas (5% H_2 + 95% N_2) ambient. The five-layer Au(14 nm)/Ge(14 nm)/Au(14 nm)/Ni(11 nm)/Au(200 nm) contacts were alloyed at 430 ^{0}C for 6 min under the same forming gas ambient in a graphite strip annealer.

Surface morphology of the contacts was investigated using a Tencor Instruments Surface Profilometer and a Hitachi S-4000 FESEM (FEM). A Cameca IMS3f SIMS intrument using an O_2^+ primary ion beam with an impact energy of 12.5 keV was used in depth profiling studies. Conversion from Schottky to Ohmic behaviour of the contacts was examined by I-V measurements. Contact resistivity was measured utilizing the cTLM method.

5.3 Results and Discussions

5.3.1 Electrical characteristics

The ρ_c of the contacts are measured in a test pattern conforming to the TLM (Fig.4.1), with the pad spacing ranging from 2 to 128 μm. The width of the Ohmic pad, W, is 140 μm. The transfer length method [12] is utilized to measure ρ_c values of the contacts. The Pd/Sn/Au contacts are annealed for 30 min. It is assumed that the sheet resistance of the semiconductor under the contacts, R_{sh1}, is equal to the sheet resistance of the semiconductor in between the contacts, R_{sh2}. Fig.5.1 shows the measured average contact resistivity vs. annealing temperature curves for 4 TLM patterns. A lowest ρ_c of $3.89x10^{-6}$ Ω-cm^2 is obtained at 330 ^{0}C for the Pd(30 nm)/Sn(150 nm)/Au(100 nm) contacts, whereas the Pd(30 nm)/Sn(150 nm)/Au(40 nm) contacts show a lowest ρ_c of $2.05x10^{-5}$ Ω-cm^2 at 360 ^{0}C.

The Pd(50 nm)/Sn(125 nm)/Au(40 nm) contacts show a lowest ρ_c of 5.10×10^{-6} Ω-cm^2 at 330 ^{0}C, whereas the Pd(50 nm)/Sn(125 nm)/Au(100 nm) contacts have a lowest ρ_c of 1.29×10^{-6} Ω-cm^2 at the same annealing temperature. However, the Pd(25 nm)/Sn(102 nm)/Au(100 nm) contacts display a lowest ρ_c of 2.27×10^{-5} Ω-cm^2 at 330 ^{0}C. In the previous chapter (Section 4.4.1), it is seen that the Pd(30 nm)/Sn(150 nm) contacts produce a minimum ρ_c of 3.26×10^{-5} Ω-cm^2 after annealing at 360 ^{0}C for 30 min, whereas the Pd(50 nm)/Sn(125 nm) contacts give a lowest ρ_c of 2.07×10^{-5} Ω-cm^2 at 400 ^{0}C. Therefore, a suitable Au overlayer improves the electrical characteristics of the Pd/Sn Ohmic contacts and lowers the ρ_c values by approximately one order of magnitude. A Au overlayer also changes the annealing cycles of the Pd/Sn contacts at the lowest ρ_c points. The five-layer Au(14 nm)/Ge(14 nm)/Au(14 nm)/Ni(11 nm)/Au(200 nm) contacts show a ρ_c of 6.49×10^{-6} Ω-cm^2 after alloying at 430 ^{0}C for 6 min. Herbert et al. [41] reported a ρ_c in the range of low 10^{-6} Ω-cm^2 with this five-layer contact after alloying at 425 ^{0}C for 140 seconds. The results reported in this thesis are in consistent with those observations.

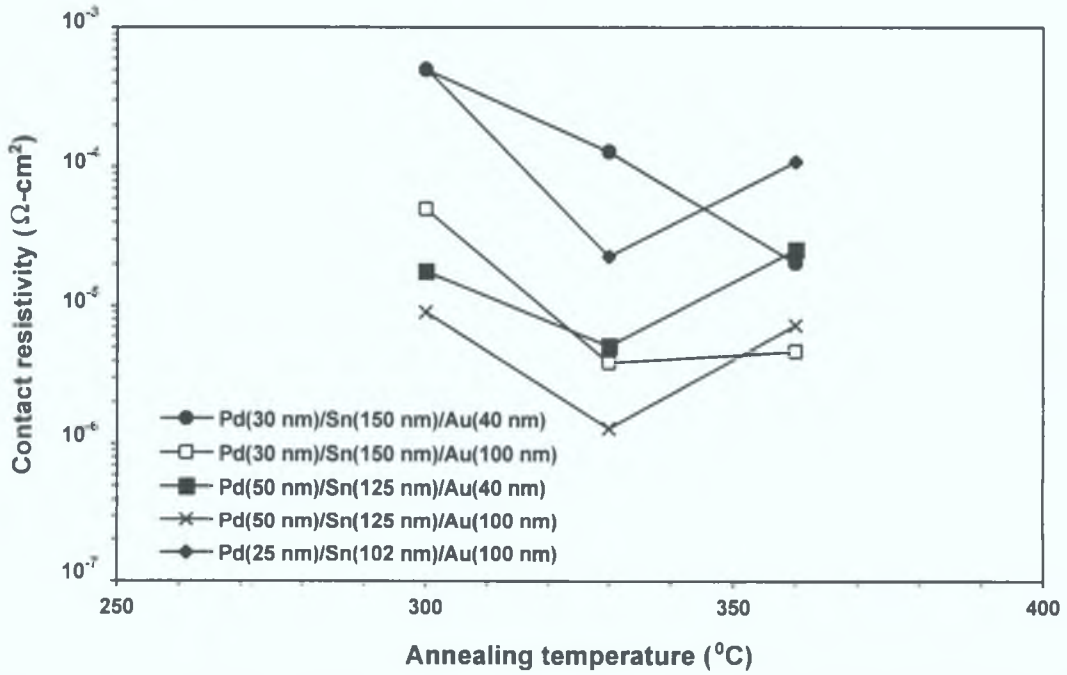


Fig.5.1. Contact resistivity vs. annealing temperature curves of the Pd/Sn/Au Ohmic contacts to n-GaAs. All contacts are annealed for 30 min.

The reduction in ρ_c values can be correlated with the production of Ga out-diffusion by Au in an open system where arsenic (As) is allowed to escape through the metallization into the surrounding atmosphere during annealing. In such a system, Au will dissolve GaAs to form Au-Ga compounds. The large positive entropy of

sublimation of As will help to drive the Au-Ga reactions [158]. The technological importance of this reaction is that out-diffusion of Ga encourages the incorporation of Sn impurities on Ga sites in the GaAs near the metal/GaAs interface, thereby resulting in the formation of a thin layer of n^+-GaAs which lowers the ρ_c values.

TABLE XIII summarizes the lowest ρ_c and measurement error, $\Delta\rho_c$, of the Pd/Sn/Au Ohmic contacts. The Pd(50 nm)/Sn(125 nm)/Au(100 nm) contacts appear to have excellent reproducibility with a $\Delta\rho_c$ of $\pm 1.0 \times 10^{-6}$ Ω-cm^2 among all of the Pd/Sn/Au metallizations investigated. The five-layer Au/Ge/Au/Ni/Au contacts show a $\Delta\rho_c$ of $\pm 3.25 \times 10^{-6}$ Ω-cm^2 after having been alloyed at 430 ^{0}C for 6 min.

TABLE XIII. Summary of calculated average ρ_c and measurement error, $\Delta\rho_c$, values of the Pd/Sn/Au and Au/Ge/Au/Ni/Au Ohmic contacts to n-GaAs.

Contact structure	Annealing condition	ρ_c (Ω-cm^2)	$\Delta\rho_c$ (Ω-cm^2)
*Pd(30 nm)/Sn(150 nm)	360 ^{0}C, 30 min	3.26×10^{-5}	$\pm 2.50 \times 10^{-5}$
Pd(30 nm)/Sn(150 nm)/Au(40 nm)	360 ^{0}C, 30 min	2.05×10^{-5}	$\pm 0.31 \times 10^{-5}$
Pd(30 nm)/Sn(150 nm)/Au(100 nm)	330 ^{0}C, 30 min	3.89×10^{-6}	$\pm 1.50 \times 10^{-6}$
*Pd(50 nm)/Sn(125 nm)	400 ^{0}C, 30 min	2.07×10^{-5}	$\pm 0.92 \times 10^{-5}$
Pd(50 nm)/Sn(125 nm)/Au(40 nm)	330 ^{0}C, 30 min	5.10×10^{-6}	$\pm 3.80 \times 10^{-6}$
Pd(50 nm)/Sn(125 nm)/Au(100 nm)	330 ^{0}C, 30 min	1.29×10^{-6}	$\pm 1.00 \times 10^{-6}$
Pd(25 nm)/Sn(102 nm)/Au(100 nm)	330 ^{0}C, 30 min	2.27×10^{-5}	$\pm 1.26 \times 10^{-5}$
Au(14 nm)/Ge(14 nm)/Au(14 nm)/ Ni((11 nm)/Au(200 nm)	430 ^{0}C, 6 min	6.49×10^{-6}	$\pm 3.25 \times 10^{-6}$

* From TABLE VII (Section 4.4.1)

5.3.2 Surface profilometry measurements

Details of surface profile measurements of the non-alloyed Pd/Sn/Au and alloyed Au/Ge/Au/Ni/Au contacts are summarized in TABLE XIV. In the as-deposited state, the Pd(50 nm)/Sn(125 nm)/Au(100 nm) contacts show a TIR of 4.5 nm and Ra of 0.5 nm, whereas for the Au(14 nm)/Ge(14 nm)/Au(14 nm)/Ni(11 nm)/Au(200 nm) contacts these values are 3.5 nm and 1.0 nm, respectively. The Pd(25 nm)/Sn(102 nm)/Au(100 nm) contacts produce a TIR of 35 nm and a Ra of 5 nm in the as-deposited condition.

At the lowest ρ_c point, the Pd(30 nm)/Sn(150 nm)/Au(40 nm) contacts display a TIR of 85 nm and a Ra of 5 nm, whereas for the Pd(30 nm)/Sn(150 nm)/Au(100 nm) contacts these values are 6 nm and 1 nm, respectively The Pd(50 nm)/Sn(125 nm)/Au(40 nm) contacts exhibit a TIR of 810 nm and a Ra of 165 nm, whereas for the Pd(50 nm)/Sn(125 nm)/Au(100 nm) contacts these values are 12 5 nm and 2 0 nm, respectively At the lowest ρ_c point, the Pd(25 nm)/Sn(102 nm)/Au(100 nm) contacts show a TIR of 20 nm and a Ra of 0 nm From the previous chapter (Section 4 4 2, TABLE IX), it is seen that the Pd(30 nm)/Sn(150 nm) contacts exhibit a TIR of 90 nm and a Ra of 15 nm at the lowest ρ_c point, whereas for the Pd(50 nm)/Sn(125 nm) contacts these values are 33 nm and 5 nm, respectively Thus, a judicious choice for a Au overlayer improves the surface profiles of the Pd/Sn contacts significantly However, the Au/Ge/Au/Ni/Au contacts show significantly rougher surface profiles with a TIR of 625 nm and a Ra of 119 nm under the alloyed condition

TABLE XIV Summary of surface profiles of the Pd/Sn/Au and Au/Ge/Au/Ni/Au contacts to n-GaAs

Contact structure	Annealing condition	TIR (nm)	Ra (nm)
Pd(50 nm)/Sn(125 nm)/Au(100 nm)	as-deposited	4 5	0 5
Pd(50 nm)/Sn(125 nm)/Au(100 nm)	330 ^{0}C, 30 min	12 5	2 0
Pd(50 nm)/Sn(125 nm)/Au(40 nm)	330 ^{0}C, 30 mm	810	165
*Pd(50 nm)/Sn(125 nm)	as-deposited	24 5	3 5
*Pd(50 nm)/Sn(125 nm)	400 ^{0}C, 30 min	33 0	5 0
*Pd(30 nm)/Sn(150 nm)	as-deposited	30 0	5 0
*Pd(30 nm)/Sn(150 nm)	360 ^{0}C, 30 min	90 0	15 0
Pd(30 nm)/Sn(150 nm)/Au(40 nm)	360 ^{0}C, 30 min	85 0	5 0
Pd(30 nm)/Sn(150 nm)/Au(100 nm)	330 ^{0}C, 30 mm	6 0	1 0
Pd(25 nm)/Sn(102 nm)/Au(100 nm)	as-deposited	35 0	5 0
Pd(25 nm)/Sn(102 nm)/Au(100 nm)	330 ^{0}C, 30 min	20 0	0 0
Au(14 nm)/Ge(14 nm)/Au(14 nm)/ Ni(11 nm)/Au(200 nm)	as-deposited	3 5	1 0
Au(14 nm)/Ge(14 nm)/Au(14 nm)/ Ni(11 nm)/Au(200 nm)	430 ^{0}C, 6 min	625	119

* From TABLE IX (Section 4 4 2)

5.3.3 Surface morphology using SEM

SEM micrographs of the Pd/Sn/Au contacts under both as-deposited and lowest ρ_c conditions are shown in Fig 5 2 Micro-crystals of the order of ~0 2 μm in diameter are observed on the surface with the Pd(30 nm)/Sn(150 nm)/Au(40 nm) contacts under both as-deposited (Fig 5 2(a)) and at the lowest ρ_c (Fig 5 2(b)) conditions However, the metallizations appear to be more uniformly distributed at the lowest ρ_c point when compared to the as-deposited state The Pd(30 nm)/Sn(150 nm)/Au(100 nm) contacts display smooth surface morphology under both as-deposited (Fig 5 2(c)) and lowest ρ_c (Fig 5 2(d)) conditions The Pd(30 nm)/Sn(150 nm) contacts produce micro-crystals of the order of ~1 0 μm in diameter under both as-deposited and lowest ρ_c conditions (Fig 4 6(a) & Fig 4 6(b)) Therefore, Au overlayers improve the surface morphology of the Pd(30 nm)/Sn(150 nm) contacts significantly The Pd(25 nm)/Sn(102 nm)/Au(100 nm) contacts show micro-crystals of the order of ~0 2 μm in diameter under both as-deposited (Fig 5 2(e)) and lowest ρ_c (Fig 5 2(f)) conditions

The Pd(50 nm)/Sn(125 nm)/Au(40 nm) contacts exhibit smooth surface morphology under as-deposited condition (Fig 5 3(a)) At the lowest ρ_c point (Fig 5 3(b)), the surface morphology of these contacts deteriorates but still better than the Pd(50 nm)/Sn(125 nm) contacts (Fig 4 7(d)) The Pd(50 nm)/Sn(125 nm)/Au(100 nm) contacts display smooth surface morphology under both as-deposited (Fig 5 3(c)) and lowest ρ_c (330 ^{0}C, 30 mm) (Fig 5 3(d)) conditions Once again, a judicious choice of Au overlayers improve the surface morphology of the Pd(50 nm)/Sn(125 nm) contacts significantly

Alloyed Au(14 nm)/Ge(14 nm)/Au(14 nm)/Ni(11 nm)/Au(200 nm) contacts produce smooth surface morphology only under as-deposited condition (Fig 5 3(e)) Subsequently, surface morphology of this five-layer contact system degrades after alloying at 430 ^{0}C for 6 min (Fig 5 3(f)) Therefore, Pd/Sn/Au metallization exhibits better surface morphology than that of alloyed Au/Ge/Au/Ni/Au metallization with a comparable contact resistivity Surface profilometry measurements (TABLE XIV) also reveal these results

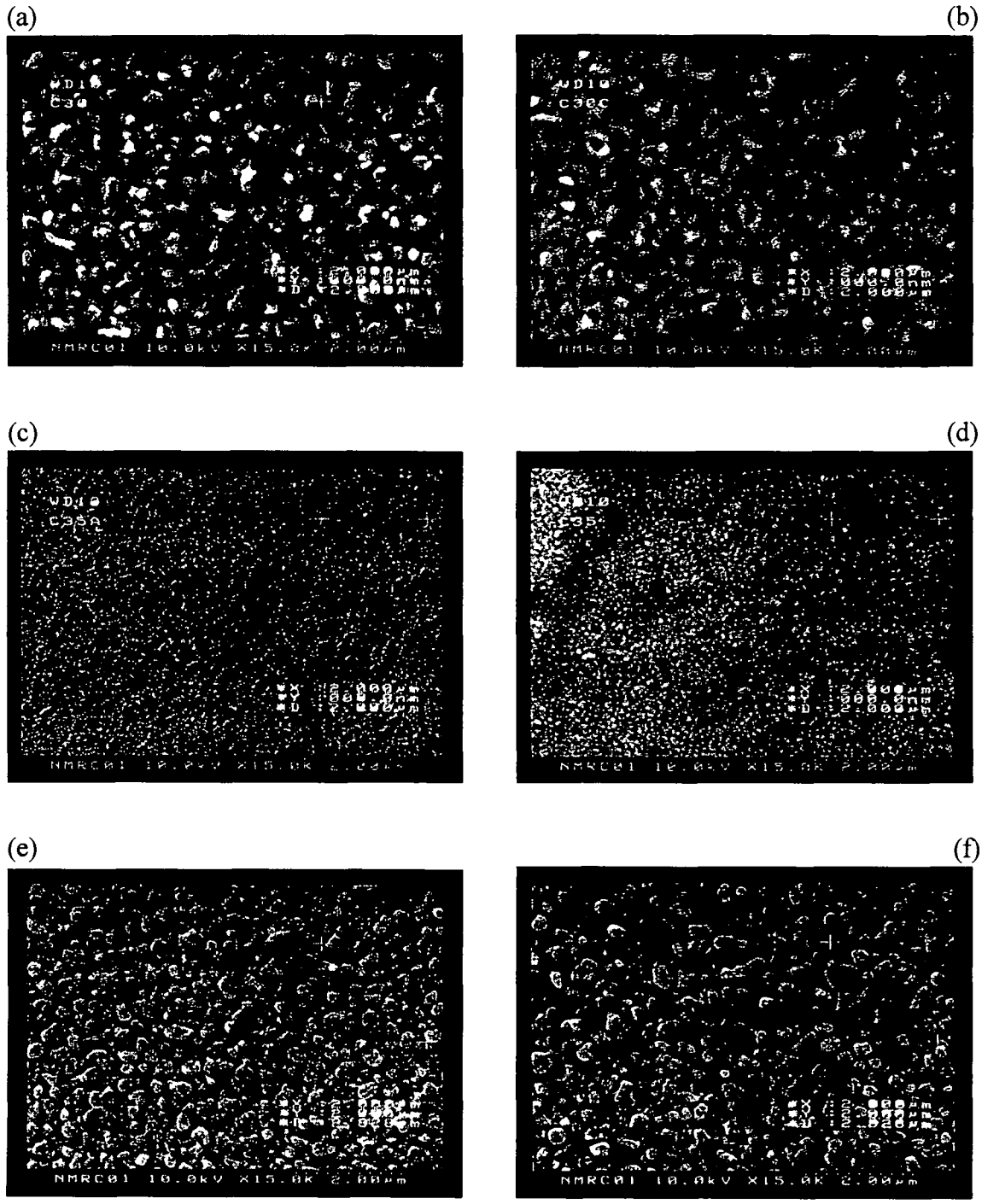


Fig 5 2 SEM micrographs of the Pd/Sn/Au contacts to n-GaAs (a) Pd(30 nm)/Sn(150 nm)/Au(40 nm), as-deposited, (b) Pd(30 nm)/Sn(150 nm)/Au(40 nm), 360 ^{0}C, 30 mm, (c) Pd(30 nm)/Sn(150 nm)/Au(100 nm), as-deposited, (d) Pd(30 nm)/Sn(150 nm)/Au(100 nm), 330 ^{0}C, 30 min, (e) Pd(25 nm)/Sn(102 nm)/Au(100 nm), as-deposited and (f) Pd(25 nm)/Sn(102 nm)/Au(100 nm), 330 ^{0}C, 30 mm

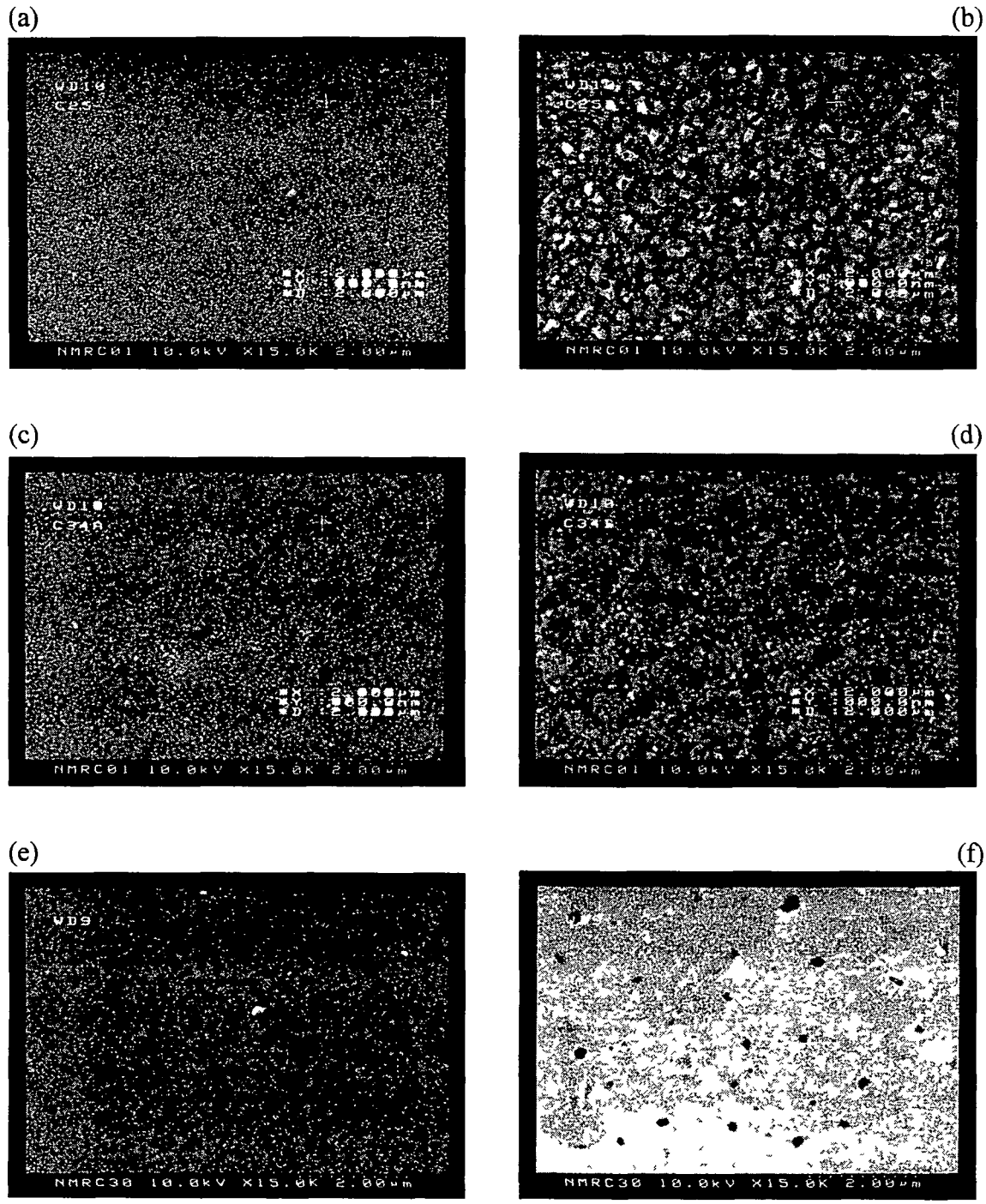
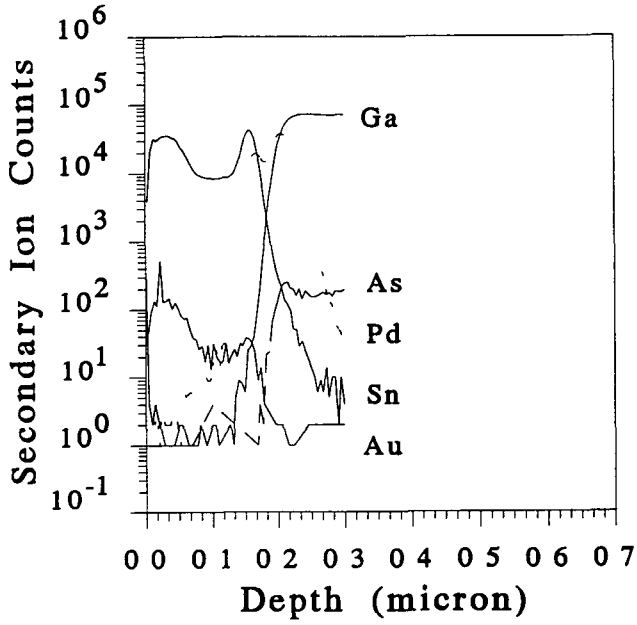
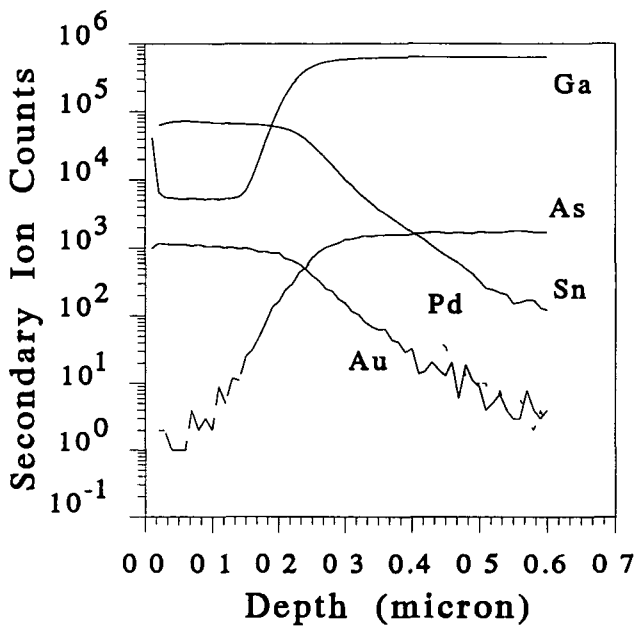


Fig 5 3 SEM micrographs of the Pd/Sn/Au and Au/Ge/Au/Ni/Au contacts to n-GaAs (a) Pd(50 nm)/Sn(125 nm)/Au(40 nm), as-deposited, (b) Pd(50 nm)/Sn(125 nm)/Au(40 nm), 330 ^{0}C, 30 min, (c) Pd(50 nm)/Sn(125 nm)/Au(100 nm), as-deposited, (d) Pd(50 nm)/Sn(125 nm)/Au(100 nm), 330 ^{0}C, 30 min, (e) Au(14 nm)/Ge(14 nm)/Au(14 nm)/Ni(11 nm)/Au(200 nm), as-deposited and Au(14 nm)/Ge(14 nm)/Au(14 nm)/Ni(11 nm)/Au(200 nm), 430 ^{0}C, 6 mm



(a)



(b)

Fig 5 4 SIMS depth profiles of the Pd(50 nm)/Sn(125 nm)/Au(100 nm) contact to n-GaAs (a) as-deposited and (b) annealed at 330 ^{0}C, 30 min

5.3.4 Contact depth profiles using SIMS

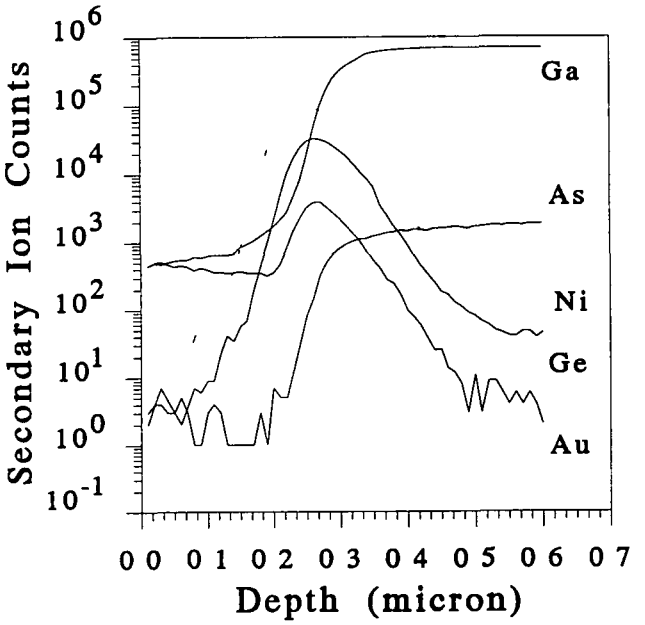
Since the reproducibility of the Pd(50 nm)/Sn(125 nm)/Au(100 nm) Ohmic contacts is superior to the other Pd/Sn/Au metallizations investigated, SIMS depth profiles of the Pd(50 nm)/Sn(125 nm)/Au(100 nm) metallization will be presented and compared with

those of the alloyed Au(14 nm)/Ge(14 nm)/Au(14 nm)/Ni(11 nm)/Au(200 nm) metallization

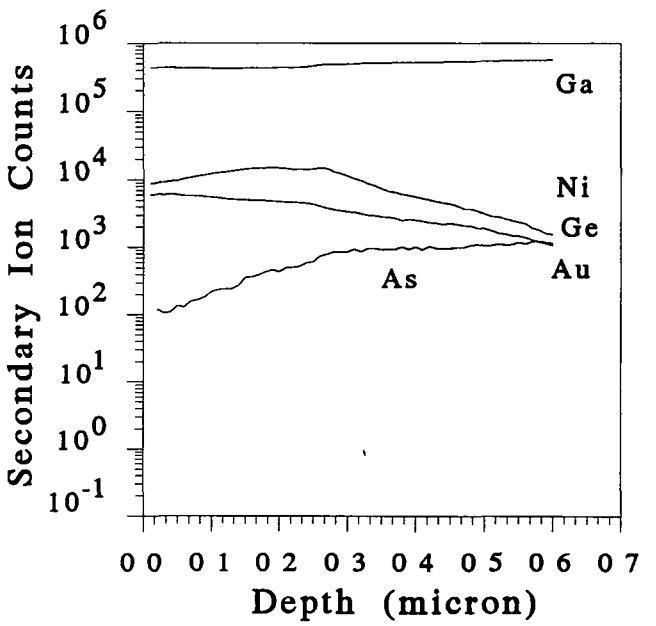
SIMS depth profiles of the Pd(50 nm)/Sn(125 nm)/Au(100 nm) contacts are shown in Fig 5 4 In the as-deposited state (Fig 5 4(a)), the metal/GaAs interface is well defined After annealing at 330 ^{0}C for 30 mm (Fig 5 4(b)), it is found that Pd, Sn and Au atoms penetrate into the underlying GaAs The exact penetration depths of these atoms can not be determined due to the 'knock-on' effect as described in Section 4 4 4 However, the metal/GaAs interface is still well defined after annealing at 330 ^{0}C for 30 mm At the minimum ρ_c points, the slopes of Pd and Sn profiles are even steeper and narrower for the n-GaAs/Pd/Sn/Au contacts (Fig 5 4(b)) than those of the n-GaAs/Pd/Sn contacts (Fig 4 13(b)) This variation of Pd and Sn profiles is due to the different annealing temperatures used in these contacts

The secondary ion counts of Ga are higher for the n-GaAs/Pd/Sn/Au contacts (Fig 5 4(b)) than those of the n-GaAs/Pd/Sn contacts (Fig 4 13(b)) This is due to the out-diffusion of Ga from GaAs by the in-diffusion of Au in the contact structures containing Au as a metallization [6] On the other hand, Ga atoms appear in the metal layer Therefore, the Pd/Sn/Au contacts are shallower than those of the Pd/Sn contacts

Fig 5 5 shows SIMS depth profiles of the n-GaAs/Au(14 nm)/Ge(14 nm)/Au(14 nm)/Ni(11 nm)/Au(200 nm) contacts under both as-deposited condition and after having been alloyed at 430 ^{0}C for 6 min In the as-deposited state (Fig 5 5(a)), the metal/GaAs interface is well defined After alloying at 430 ^{0}C for 6 mm (Fig 5 5(b)), the metal/GaAs interface is not well defined as seen with the n-GaAs/Pd/Sn/Au contacts (Fig 5 4(b)) In addition, the penetration depths of Ni, Ge and Au species into underlying GaAs are quite significant compared to the Pd, Sn and Au species in n-GaAs/Pd/Sn/Au contacts Thus, the n-GaAs/Pd/Sn/Au contacts are more abrupt and shallower than those of alloyed n-GaAs/Au/Ge/Au/Ni/Au contacts The n-GaAs/Pd/Sn contacts (Fig 4 13(b)) are also more abrupt and shallower than those of alloyed n-GaAs/Au/Ge/Au/Ni/Au contacts (Fig 5 5(b))



(a)



(b)

Fig 5 5 SIMS depth profiles of the Au(14 nm)/Ge(14 nm)/Au(14 nm)/Ni(11 nm)/Au(200 nm) contacts to n-GaAs (a) as-deposited and (b) alloyed at 430 ^{0}C for 6 min

5.3.5 Mass spectrometer analysis

Fig 5 6 shows the mass spectrometer analysis of positive secondary ions for the Pd(50 nm)/Sn(125 nm)/Au(100 nm) contacts at the lowest ρ_c point Positive secondary ions of

Pd^+, Sn^+, Au^+, Si^+, As^+, Ga^+, Ga_2^+, GaO^+, SnO^+, $PdGa^+$, $SnGa^+$ and Pd_2^+ are monitored in the ion microanalyzer Due to the noise generation at higher amu (>200) as described in Section 4 4 5, other ions could not be determined However, the detection of $PdGa^+$ and $SnGa^+$ ions indicates the out-diffusion of Ga into the metallization

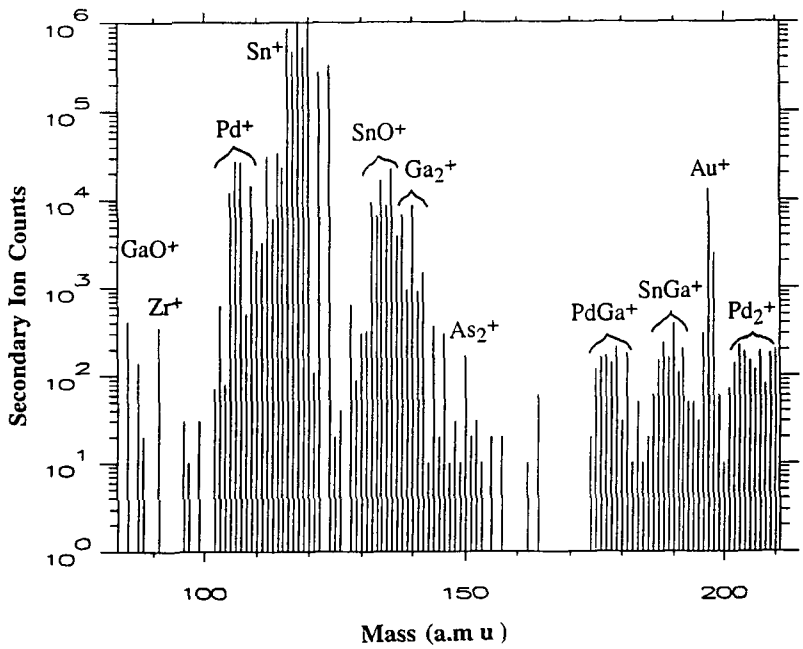
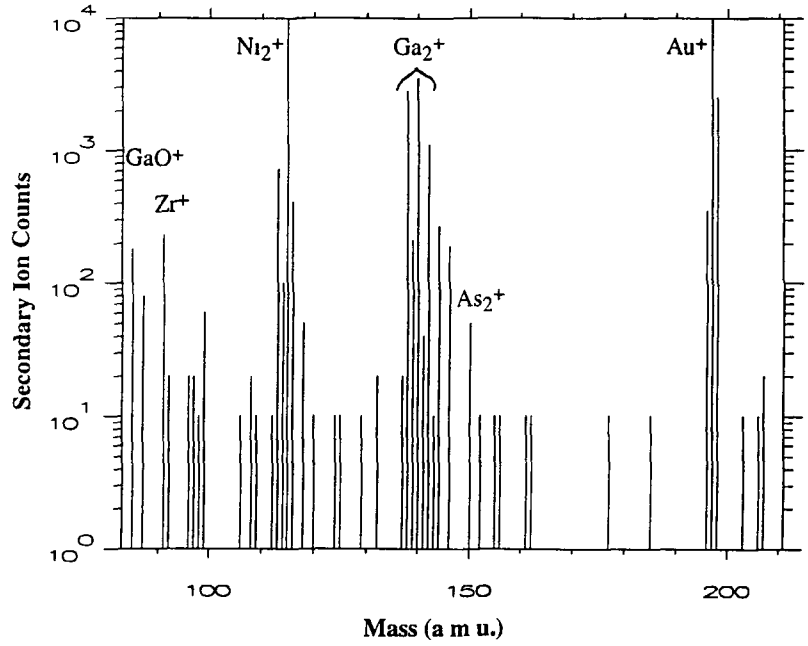
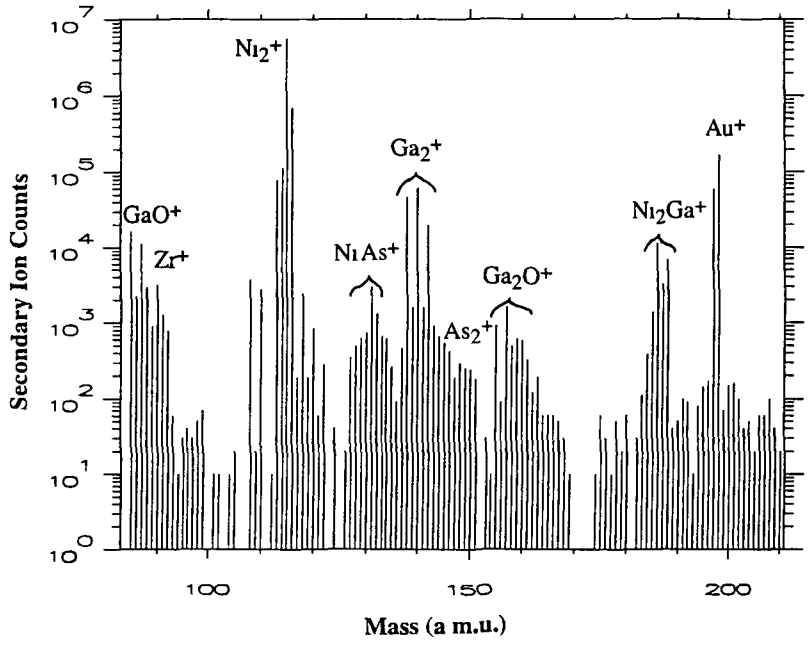


Fig 5 6 Mass spectra of positive secondary ions for the n-GaAs/Pd(50 nm)/Sn(125 nm)/Au(100 nm) contacts annealed at 330 ^{0}C, 30 mm

Fig 5 7 shows the mass spectrometer analysis of positive secondary ions for the Au(14 nm)/Ge(14 nm)/Au(14 nm)/Ni(11 nm)/Au(200 nm) contacts under both as-deposited condition and after having been alloyed at 430 ^{0}C for 6 min In the as-deposited state (Fig 5 7(a)), positive secondary ions of Ni^+, Ge^+, Au^+, Si^+, As^+, Ga^+, Ni_2^+, Ga_2^+, GaO^+, and As_2^+ are monitored in the ion microanalyzer After alloying at 430 ^{0}C for 6 min (Fig 5 7(b)), $NiAs^+$, Ga_2O^+ and Ni_2Ga^+ ions are monitored in addition to the ions detected in the as-deposited state which are in consistent with the alloyed Au-Ge/Ni contacts [71,81]



(a)



(b)

Fig 5 7 Mass spectra of positive secondary ions for the Au(14 nm)/Ge(14 nm)/Au(14 nm)/Ni(11 nm)/Au(200 nm) contacts to n-GaAs (a) as-deposited and (b) alloyed at 430 ^{0}C for 6 min

5.4 Conclusion

The effects of Au overlayers on the characteristics of Pd/Sn Ohmic contacts to n-GaAs have been investigated A comparison has also been made among non-alloyed Pd/Sn and Pd/Sn/Au and alloyed five-layer Au/Ge/Au/Ni/Au contacts A judicious choice of Au overlayers improves the characteristics of Pd/Sn contacts A Au overlayer also changes the annealing cycles at the lowest ρ_c points A lowest ρ_c of 3 89x10^{-6} Ω-cm^2 is obtained for a substrate doping of 2x10^{18} cm^{-3} with a Pd(30 nm)/Sn(150 nm)/Au(100 nm) contact after annealing at 330 ^{0}C for 30 min, whereas the Pd(50 nm)/Sn(125 nm)/Au(100 nm) contact had a minimum ρ_c of 1 29x10^{-6} Ω-cm^2 at the same annealing condition The reproducibility of the Pd(50 nm)/Sn(125 nm)/Au(100 nm) Ohmic contact is also excellent with a $\Delta\rho_c$ of ±1 0x10^{-6} Ω-cm^2 at the lowest ρ_c point The Au(14 nm)/Ge(14 nm)/Au(14 nm)/Ni(11 nm)/Au(200 nm) contacts produce a ρ_c of 6 49x10^{-6} Ω-cm^2 after alloying at 430 ^{0}C for 6 min

Proper choice of Au overlayers also improves the morphological characteristics of Pd/Sn contacts The Pd(50 nm)/Sn(125 nm)/Au(100 nm) Ohmic contacts appear to have better surface morphology and a lower metal penetration into the underlying GaAs than those of alloyed five-layer Au/Ge/Au/Ni/Au contacts as evidenced by Surface Profilometry measurements, SEM and SIMS The Pd(50 nm)/Sn(125 nm) contacts are also shallower than those of alloyed Au/Ge/Au/Ni/Au contacts Surface morphology of the Pd(30 nm)/Sn(150 nm)/Au(100 nm) and Pd(50 nm)/Sn(125 nm)/Au(100 nm) Ohmic contacts is even better than that of alloyed Au-Ge/Ni and non-alloyed Au-Ge Ohmic contacts to n-GaAs with a comparable contact resistivity [73,121]

Mass spectrometer analysis indicates the formation of PdGa and SnGa at the lowest ρ_c condition with the Pd/Sn/Au contacts However, the formation of other compounds with higher amu (>200) could not be identified due to the noise generation as described in Section 4 4 5 For the Au/Ge/Au/Ni/Au contacts, formation of NiAs and Ni_2Ga compounds are confirmed after alloying at 430 ^{0}C for 6 min

CHAPTER 6

Comparison of Pd/Sn, Pd/Ge, Pd/Sn/Au and alloyed Au-Ge/Ni Ohmic contacts to n-GaAs

6.1 Introduction

The electrical and morphological characteristics of Pd/Sn and Pd/Sn/Au Ohmic contacts are described in the previous chapters (chapter 4 & chapter 5) Non-alloyed Pd/Ge and alloyed Au-Ge/Ni are the most common Ohmic contacts for n-GaAs In this chapter, an effort has been made to fabricate these contacts on the same MESFET structure (Fig 4 3) as used for the Pd/Sn and Pd/Sn/Au Ohmic contacts Alloyed Ni/Au-Ge/Ni contacts have also been fabricated in order to investigate the effect of Ni first layer on the properties of Au-Ge/Ni Ohmic contacts The electrical and morphological characteristics of the non-alloyed Pd/Ge and alloyed Au-Ge/Ni and Ni/Au-Ge/Ni Ohmic contacts have been studied and compared with those of the Pd/Sn and Pd/Sn/Au contacts Metallizations are deposited using a resistance heating evaporator and annealing is carried out in a conventional graphite strip annealer Surface morphology of the contacts is investigated using Scanning Electron Microscopy (SEM) Conversion from Schottky to Ohmic behaviour of the contacts is confirmed by I-V measurements Contact resistivities, ρ_c, of the metallizations are measured using the cTLM method

6.2 Experiments

Contacts were fabricated on a Si-doped ($2x10^{18}$ cm^{-3}) n-GaAs epitaxial layer grown by metal-organic vapor phase epitaxy (MOVPE) in a metal-semiconductor field-effect transistor (MESFET) structure shown previously in Fig 4 3 The GaAs substrates were sequentially cleaned and degreased in the same manner as used for the preparation of Pd/Sn and Pd/Sn/Au contacts (Section 4 3 and Section 5 2) Ohmic test, morphology and TLM patterns were defined by standard photolithography and lift-off processes A solution of H_2O_2 NH_4OH DI H_2O (1 3 15 by volume) was used as an etchant for mesa definition

Prior to loading into an evaporator, the wafers were soaked in a solution of DI H_2O HCl (15 1 by volume) for at least 2 min and then blow dried using dry N_2 to remove native oxides Samples consisting of n-GaAs/Pd(50 nm)/Ge(126 nm), n-GaAs/Au-12wt % Ge(150 nm)/Ni(16 nm) and n-GaAs/Ni(5 nm)/Au-12wt %Ge(150 nm)/Ni(16 nm) structures were prepared by sequential deposition of metallizations in a resistance heating evaporator without breaking vacuum The base pressure was ~$1x10^{-6}$ Torr and pressure during evaporation was between 1 $5x10^{-6}$ Torr and 4 $5x10^{-6}$ Torr

The n-GaAs/Pd(50 nm)/Ge(126 nm) contacts were then annealed in the temperature range of 300-360 ^{0}C for 30 mm by a conventional graphite strip annealer in a flowing forming gas (5% H_2 + 95% N_2) ambient The eutectic n-GaAs/Au-Ge(150 nm)/Ni(16 nm) and n-GaAs/Ni(5 nm)/Au-Ge(150 nm)/Ni(16 nm) contacts were alloyed for 150 s in the temperature range of 400-440 ^{0}C under the same forming gas ambient in a graphite strip annealer The alloying time was measured from the moment at which the wafer temperature reached 98% of its preset value

Surface morphology of the contacts was investigated using a Cambridge S360 SEM Conversion from Schottky to Ohmic behaviour of the contacts was examined by I-V measurements Contact resistivity was measured utilizing the cTLM method

6.3 Results and Discussions

6.3.1 Electrical characteristics

The ρ_c of the contacts are measured in a test pattern conforming to the TLM (Fig 4 1), with pad spacing ranging from 2 to 128 μm The width of the Ohmic pad, W, is 140 μm The transfer length method [12] is utilized to measure ρ_c values of the contacts The Pd/Ge contacts are annealed for 30 min It is assumed that the sheet resistance of the semiconductor under the contacts, R_{sh1}, is equal to the sheet resistance of the semiconductor in between the contacts, R_{sh2} Fig 6 1 shows the measured average contact resistivity vs annealing temperature curves for 2 groups of samples, each group consists of two samples A lowest ρ_c of 2 $84x10^{-6}$ Ω-cm^2 is obtained at 330 ^{0}C for the Pd(50 nm)/Ge(126 nm) contacts This ρ_c value is approximately one order of magnitude lower than that of the Pd(50 nm)/Sn(125 nm) contacts (Fig 4 4) Moreover, the Pd/Ge contacts show excellent reproducibility with a $\Delta\rho_c$ of ±0 $12x10^{-6}$ Ω-cm^2.

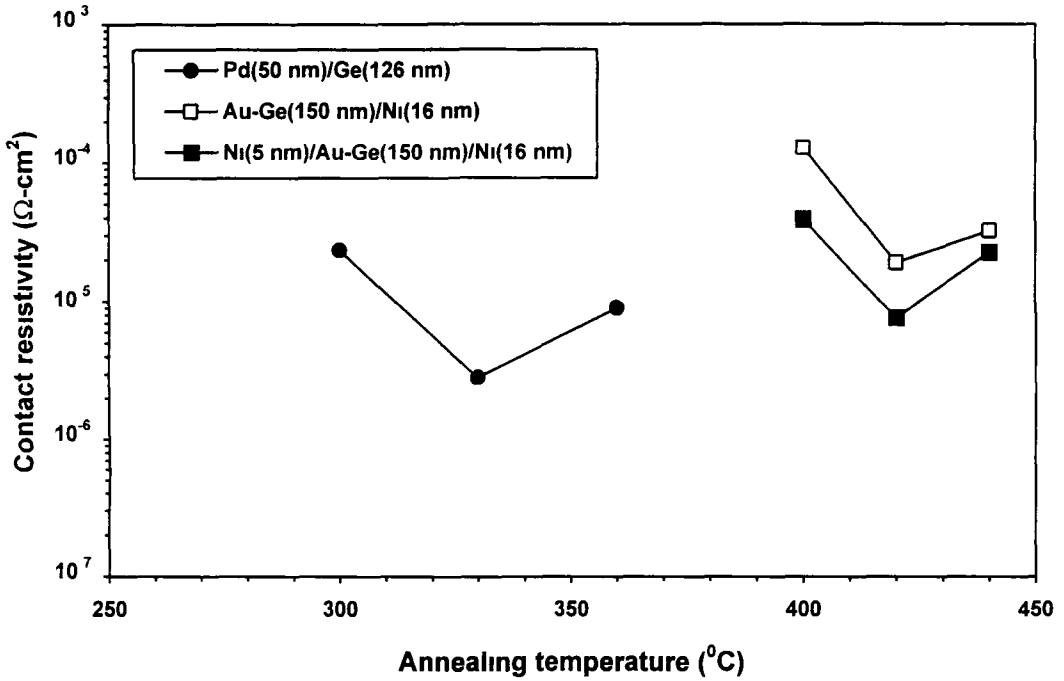


Fig 6 1 Contact resistivity vs annealing temperature curves of the non-alloyed Pd/Ge and alloyed Au-Ge/Ni and Ni/Au-Ge/Ni Ohmic contacts to n-GaAs The Pd/Ge contacts are annealed for 30 mm, whereas the Au-Ge/Ni and Ni/Au-Ge/Ni contacts are alloyed for 150 s

The alloyed eutectic Au-Ge(150 nm)/Ni(16 nm) contacts produce a minimum ρ_c of 1 90x10^{-5} Ω-cm^2 after having been alloyed at 420 ^{0}C for 150 s, whereas the Ni(5 nm)/Au-Ge(150 nm)/Ni(16 nm) contacts display a lowest ρ_c of 7 60x10^{-6} Ω-cm^2 at the same annealing condition The measurement error, $\Delta\rho_c$, of the Au-Ge/Ni contacts at the minimum ρ_c point is ±1 04x10^{-5} Ω-cm^2, whereas for the Ni/Au-Ge/Ni contacts this value is ±3 40x10^{-6} Ω-cm^2 Therefore, the Ni first layer reduces the spread of ρ_c significantly which is consistent with the observations of Shih et al [81] Moreover, a 5 nm Ni first layer in the alloyed Au-Ge/Ni Ohmic contacts lowers the ρ_c value significantly The minimum ρ_c value of the alloyed Ni/Au-Ge/Ni Ohmic contacts is slightly higher than that of the Pd(50 nm)/Sn(125 nm)/Au(100 nm) contacts annealed at 330 ^{0}C for 30 mm (Fig 5 1) However, the Au-Ge/Ni contacts produce a lowest ρ_c which is approximately one order of magnitude higher than that of the Pd(50 nm)/Sn(125 nm)/Au(100 nm) contacts The Pd(50 nm)/Sn(125 nm)/Au(100 nm) contacts show superior reproducibility with a $\Delta\rho_c$ of ±1 00x10^{-6} Ω-cm^2 (Section 5 3 1) than those of alloyed Au-Ge/Ni and Ni/Au-Ge/Ni Ohmic contacts

6.3.2 Surface morphology using SEM

SEM micrographs of the non-alloyed Pd/Ge and alloyed Au-Ge/Ni and Ni/Au-Ge/Ni contacts under both as-deposited and lowest ρ_c conditions are shown in Fig 6 2 The

Pd/Ge contacts show smooth surface morphology under the as-deposited state (Fig 6 2(a)) After annealing at 330 ^{0}C for 30 min (Fig 6 2(b)), surface morphology of this contact system deteriorates very slightly, but remains superior to that of Pd(50 nm)/Sn(125 nm) (Fig 4 7(d)) and Pd(50 nm)/Sn(125 nm)/Au(100 nm) (Fig 5 3(d)) contacts

(a) (b)

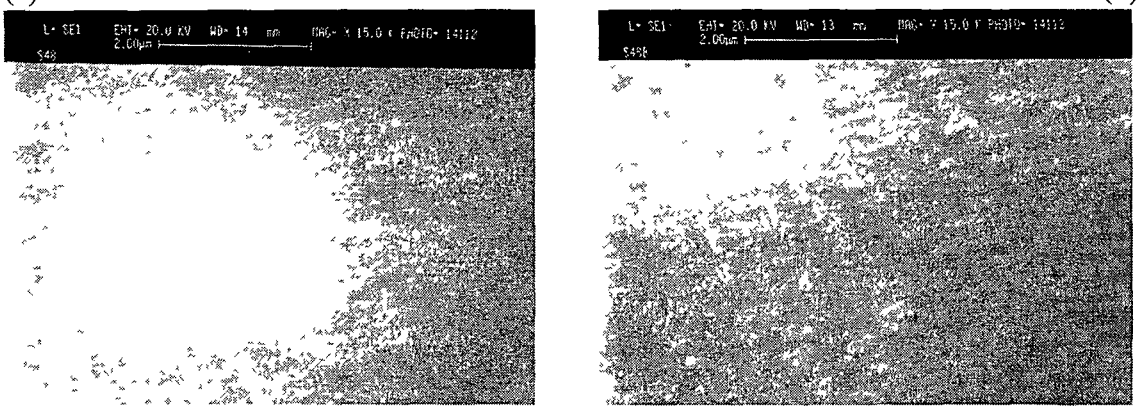


Fig 6 2 SEM micrographs of the non-alloyed Pd(50 nm)/Ge(126 nm) contacts to n-GaAs (a) as-deposited and (b) annealed at 330 ^{0}C for 30 mm

Fig 6 3 shows the SEM micrographs of the alloyed Au-Ge(150 nm)/Ni(16 nm) and Ni(5 nm)/Au-Ge(150 nm)/Ni(16 nm) contacts In the as-deposited state (Fig 6 3(a)), the Au-Ge/Ni contacts display almost smooth surface morphology After having been alloyed at 420 ^{0}C for 150 s (Fig 6 3(b)), surface morphology of the Au-Ge/Ni contacts deteriorates significantly and *balling-up* of the metallization is observed The Ni/Au-Ge/Ni contacts exhibit smooth surface morphology in the as-deposited state (Fig 6 3(c)) At the minimum ρ_c point (Fig 6 3(d)), the Ni/Au-Ge/Ni contacts show rough surface morphology *Balling-up* of the metallization is also observed in this case However, at the minimum ρ_c point, the Ni/Au-Ge/Ni contacts produce better surface morphology than that of the Au-Ge/Ni contacts (Fig 6 3(b) & Fig 6 3(d)) Therefore, a 5 nm Ni first layer improves the morphological characteristics of the alloyed Au-Ge/Ni Ohmic contacts At the lowest ρ_c point, both Pd(50 nm)/Sn(125 nm) and Pd(50 nm)/Sn(125 nm)/Au(100 nm) contacts (Fig 4 7(d) & Fig 5 3(d)) show better surface morphology than that of the alloyed Au-Ge(150 nm)/Ni(16 nm) and Ni(5 nm)/Au-Ge(150 nm)/Ni(16 nm) contacts (Fig 6 3(b) & Fig 6 3(d))

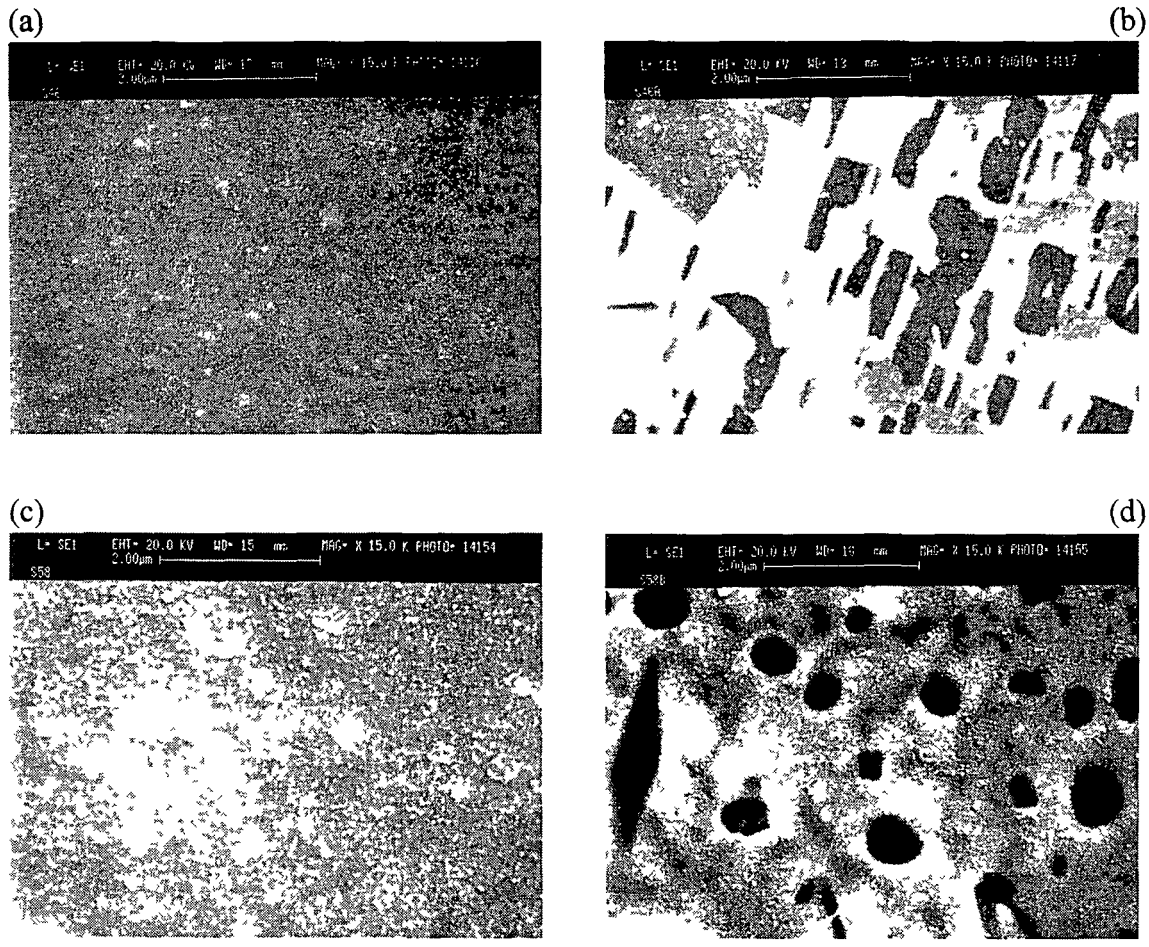


Fig 6 3 SEM micrographs of the Au-Ge/Ni and Ni/Au-Ge/Ni contacts to n-GaAs (a) Au-Ge(150 nm)/Ni(16 nm), as-deposited, (b) Au-Ge(150 nm)/Ni(16 nm), 420 ^{0}C, 150 s, (c) Ni(5 nm)/Au-Ge(150 nm)/Ni(16 nm), as-deposited and (d) Ni(5 nm)/Au-Ge(150 nm)/Ni(16 nm), 420 ^{0}C, 150 s

6.4 Conclusion

The electrical and morphological characteristics of the non-alloyed Pd/Ge and alloyed eutectic Au-Ge/Ni and Ni/Au-Ge/Ni Ohmic contacts to n-GaAs are presented and compared with those of Pd/Sn and Pd/Sn/Au contacts The Pd(50 nm)/Ge(126 nm) contacts show excellent reproducibility and produce a minimum ρ_c of 2 84x10^{-6} Ω-cm^2 after annealing at 330 ^{0}C for 30 min which is approximately one order of magnitude lower than that of the Pd(50 nm)/Sn(125 nm) contacts However, minimum ρ_c values are almost identical for both Pd(50 nm)/Ge(126 nm) and Pd(50 nm)/Sn(125 nm)/Au(100 nm) contacts A lowest ρ_c of 1 90x10^{-5} Ω-cm^2 is obtained for the Au-Ge(150 nm)/Ni(16 nm) contacts after having been alloyed at 420 ^{0}C for 150 s, whereas the Ni(5 nm)/Au-Ge(150 nm)/Ni(16 nm) contacts show a minimum ρ_c of

7 60x10^{-6} Ω-cm^2 under the same annealing condition Therefore, a 5 nm Ni first layer improves the electrical characteristics of the alloyed Au-Ge/Ni contacts The Pd(50 nm)/Sn(125 nm)/Au(100 nm) Ohmic contacts display superior reproducibility and improved electrical characteristics with a minimum ρ_c of 1 29x10^{-6} Ω-cm^2 (Fig 5 1) when compared with the alloyed Au-Ge/Ni and Ni/Au-Ge/Ni contacts

The non-alloyed Pd/Ge Ohmic contacts appear to have better surface morphology than those of Pd/Sn and Pd/Sn/Au and alloyed Au-Ge/Ni and Ni/Au-Ge/Ni Ohmic contacts A Ni first layer improves the morphological properties of the alloyed Au-Ge/Ni contacts However, surface morphology of the Pd/Sn and Pd/Sn/Au Ohmic contacts is better than those of alloyed Au-Ge/Ni and Ni/Au-Ge/Ni contacts

CHAPTER 7

Thermal and long-term stability of the Pd/Sn and Pd/Sn/Au Ohmic contacts to n-GaAs

7.1 Introduction

One of the most important criteria for an Ohmic contact is its thermal stability 410 ^{0}C and 300 ^{0}C are typical temperatures for testing the degradation of Ohmic contacts on GaAs [31,38,44,56] In this chapter, thermal and long-term stability analysis of the Pd/Sn and Pd/Sn/Au Ohmic contacts will be presented A comparison will be made between the thermal stability of the Pd/Sn and Pd/Ge contacts Thermal stability of the Pd/Sn/Au contacts will be compared with those of alloyed Au/Ge/Au/Ni/Au, Au-Ge/Ni and Ni/Au-Ge/Ni contacts SEM will be employed to investigate the surface morphology of the Ohmic contacts Contact resistivities, ρ_c, of the proposed metallizations are measured using the cTLM method

7.2 Experiments

Once again, the contacts were fabricated on a Si-doped ($2x10^{18}$ cm^{-3}) n-GaAs epitaxial layer grown by metal-organic vapor phase epitaxy (MOVPE) in a metal-semiconductor field-effect transistor (MESFET) structure shown previously in Fig 4 3 Samples consisting of n-GaAs/Pd(50 nm)/Sn(125 nm), n-GaAs/Pd(50 nm)/Ge(126 nm), n-GaAs/Pd(50 nm)/Sn(125 nm)/Au(100 nm), n-GaAs/Au(14 nm)/Ge(14 nm)/Au(14 nm)/Ni(11 nm)/Au(200 nm), n-GaAs/Au-12wt % Ge(150 nm)/Ni(16 nm) and n-GaAs/Ni(5 nm)/Au-12wt %Ge(150 nm)/Ni(16 nm) structures were prepared as described in the previous sections (Section 4 3, Section 5 3 & Section 6 2)

After Ohmic contact formation at the lowest ρ_c points, thermal stability measurements of the contacts were then carried out in a furnace at 410 ^{0}C for 10 h in a flowing forming gas (5% H_2 + 95% N_2) ambient The long-term stability of the contacts were performed at 300 ^{0}C for 400 h under the same ambient condition

Surface morphology of the contacts was investigated using a Hitachi S-4000 FESEM (FEM) and a Cambridge S360 SEM Contact resistivity was measured utilizing the cTLM method

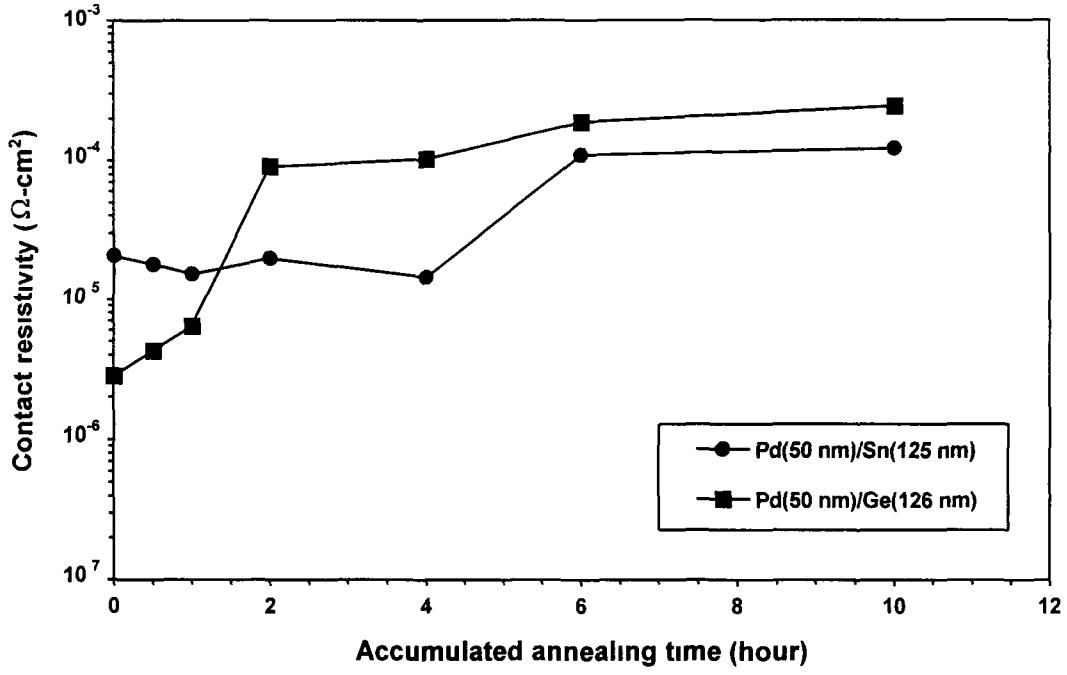


Fig 7 1 Contact resistivity vs accumulated annealing time curves for the Pd/Sn and non-alloyed Pd/Ge Ohmic contacts to n-GaAs at 410 ^{0}C

7.3 Results and Discussions

7.3.1 Thermal stability at 410 ^{0}C

The transfer length method [12] is utilized to measure ρ_c values of the contacts It is assumed that the sheet resistance of the semiconductor under the contacts, R_{sh1}, is equal to the sheet resistance of the semiconductor in between the contacts, R_{sh2} Fig 7 1 shows the thermal stability at 410 ^{0}C for the n-GaAs/Pd(50 nm)/Sn(125 nm) and non-alloyed n-GaAs/Pd(50 nm)/Ge(126 nm) contacts The average ρ_c values of 4 TLM patterns are presented in Fig 7 1 The zero accumulated annealing time value of ρ_c indicates the minimum value of ρ_c for both types of contacts before starting thermal stability at 410 ^{0}C After annealing at 410 ^{0}C for 4 h, the Pd/Sn contacts show ρ_c value in the range of low 10^{-5} Ω-cm^2 and no significant change in contact resistivity is observed After 10 h of annealing, the ρ_c value reaches to ~$1x10^{-4}$ Ω-cm^2 The ρ_c of the Pd/Ge contacts increases by approximately two orders of magnitude from its initial value after 2 h of annealing at 410 ^{0}C. After that the Pd/Ge contacts maintain a ρ_c in the range of low $1x10^{-4}$ Ω-cm^2 but still higher than those of the Pd/Sn contacts Therefore, the Pd(50

nm)/Sn(125 nm) contacts display superior thermal stability at 410 ^{0}C when compared to the Pd(50 nm)/Ge(126 nm) contacts Han et al [56] observed that the non-alloyed RTA Pd/Ge/Ti/Pt contact is thermally stable at 400 ^{0}C for 35 s Therefore, thermal stability of the Pd/Sn contact is superior to that of the Pd/Ge/Ti/Pt contact

Fig 7 2 shows SEM micrographs of the Pd/Sn and Pd/Ge contacts after having been annealed at 410 ^{0}C for 10 h For the Pd(50 nm)/Sn(125 nm) contacts (Fig 7 2(a)), surface morphology remains identical to that of observed at the minimum ρ_c condition (Fig 4 7(d)) No change in surface morphology is observed for the Pd/Ge contacts (Fig 7 2(b)) when compared to the lowest ρ_c condition (Fig 6 2(b)) However, Pd/Ge contacts display superior surface morphology to that of Pd/Sn contacts after having been annealed at 410 ^{0}C for 10 h (Fig 7 2)

(a) (b)

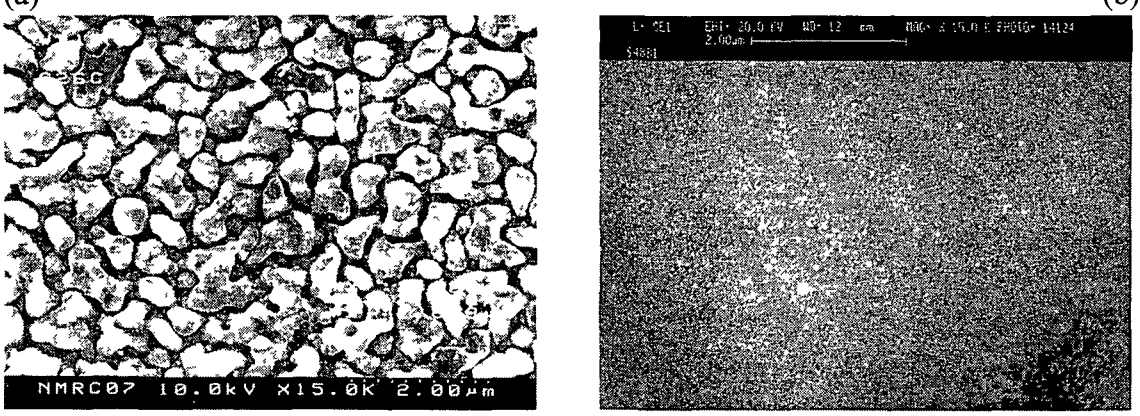


Fig 7 2 SEM micrographs of the (a) Pd(50 nm)/Sn(125 nm) and (b) non-alloyed Pd(50 nm)/Ge(126 nm) contacts to n-GaAs after having been annealed at 410 ^{0}C for 10 h

Thermal stability of the Pd(50 nm)/Sn(125 nm)/Au(100 nm) and alloyed Au(14 nm)/Ge(14 nm)/Au(14 nm)/Ni(11 nm)/Au(200 nm), Au-Ge(150 nm)/Ni(16 nm) and Ni(5 nm)/Au-Ge(150 nm)/Ni(16 nm) Ohmic contacts at 410 ^{0}C is shown in Fig 7 3 After 30 min of annealing at 410 ^{0}C, the ρ_c of the Pd/Sn/Au contacts increases by approximately one order of magnitude The ρ_c remains in the low 10^{-5} Ω-cm^2 range for up to 10 h of annealing at 410 ^{0}C The alloyed five-layer Au/Ge/Au/Ni/Au Ohmic contacts show almost identical thermal stability to the Pd/Sn/Au contacts The thermal stability of both Pd/Sn/Au and Au/Ge/Au/Ni/Au contacts is better than that of alloyed Au-Ge/Ni and Ni/Au-Ge/Ni contacts The Au-Ge/Ni contacts also show superior thermal stability when compared with Ni/Au-Ge/Ni contacts This is in consistent with observations of Shih et al [81]

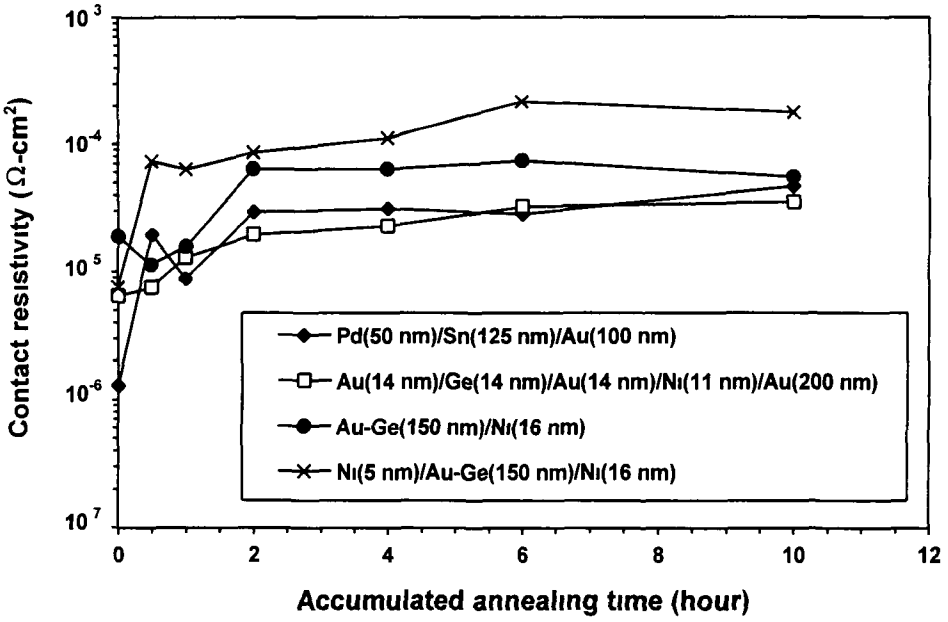


Fig 7 3 Contact resistivity vs accumulated annealing time curves for the Pd/Sn/Au, Au/Ge/Au/Ni/Au, Au-Ge/Ni and Ni/Au-Ge/Ni Ohmic contacts to n-GaAs at 410 ^{0}C

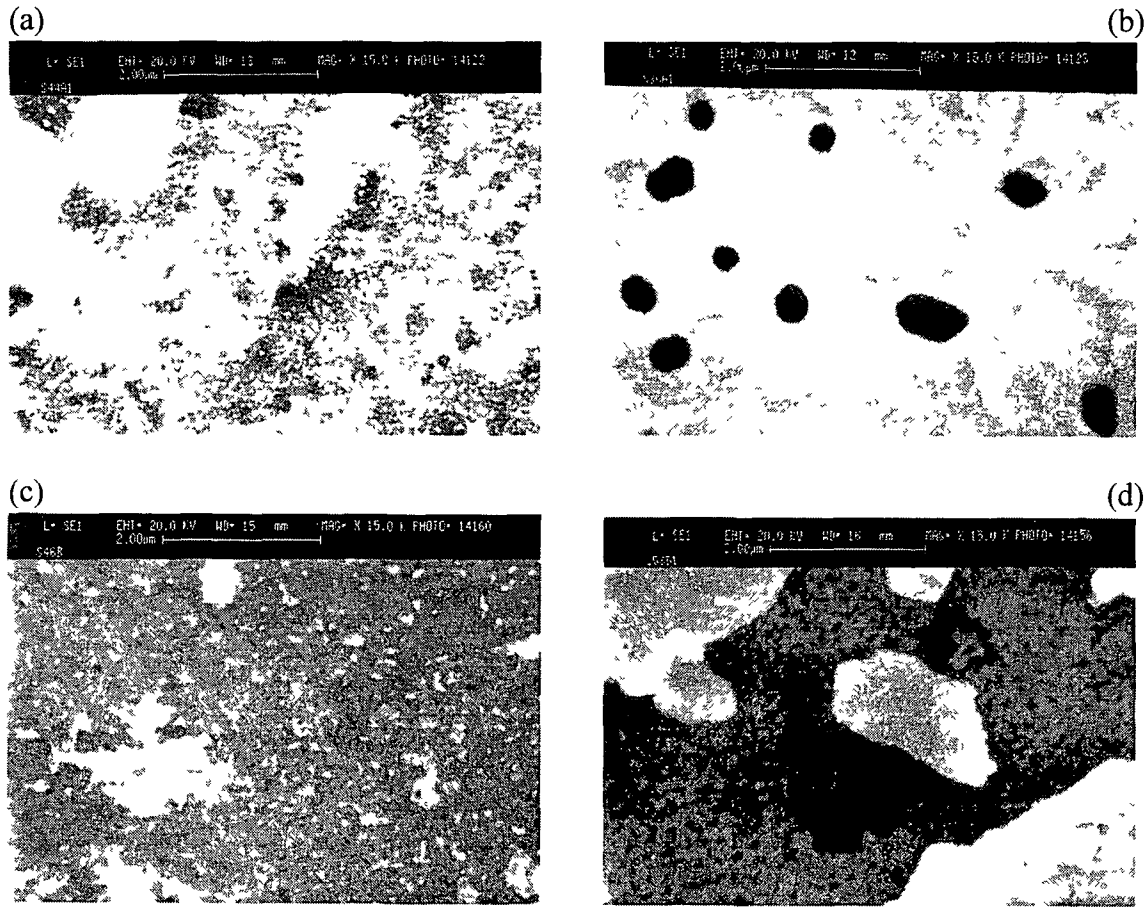


Fig 7 4 SEM micrographs of the (a) Pd(50 nm)/Sn(125 nm)/Au(100 nm) and alloyed (b) Au(14 nm)/Ge(14 nm)/Au(14 nm)/Ni(11 nm)/Au(200 nm), (c) Au-Ge(150 nm)/Ni(16 nm) and (d) Ni(5 nm)/Au-Ge(150 nm)/Ni(16 nm) contacts to n-GaAs after thermal stability at 410 ^{0}C for 10 h

SEM micrographs of the Pd/Sn/Au and alloyed Au/Ge/Au/Ni/Au, Au-Ge/Ni and Ni/Au-Ge/Ni contacts after thermal stability at 410 ^{0}C for 10 h are shown in Fig 7 4 Significant changes in surface morphology are observed for all of the contacts Segregation of metallization is observed on the surface with the Au-Ge/Ni and Ni/Au-Ge/Ni contacts (Fig 7 4(c) & Fig 7 4(d)) The surface morphology of both Pd/Sn/Au (Fig 7 4(a)) and Au/Ge/Au/Ni/Au (Fig 7 4(b)) contacts is better than that of the Au-Ge/Ni and Ni/Au-Ge/Ni contacts

7.3.2 Long-term stability at 300 ^{0}C

Long-term stability of the Pd(50 nm)/Sn(125 nm) and Pd(50 nm)/Ge(126 nm) contacts is carried out at 300 ^{0}C for 400 h and is shown in Fig 7 5 After 8 h of annealing, the ρ_c of both Pd/Sn and Pd/Ge contacts increases by approximately one order of magnitude The ρ_c of the Pd/Sn contacts remain in the low 10^{-4} Ω-cm^2 range up to 300 h Finally, it reaches the high 10^{-4} Ω-cm^2 range at 400 h The Pd/Ge contacts maintain ρ_c in the range of low 10^{-5} Ω-cm^2 up to 83 h After that ρ_c remains in the range of mid 10^{-5} Ω-cm^2 Therefore, the long-term stability of the Pd/Ge contacts appears to be better than that of the Pd/Sn contacts

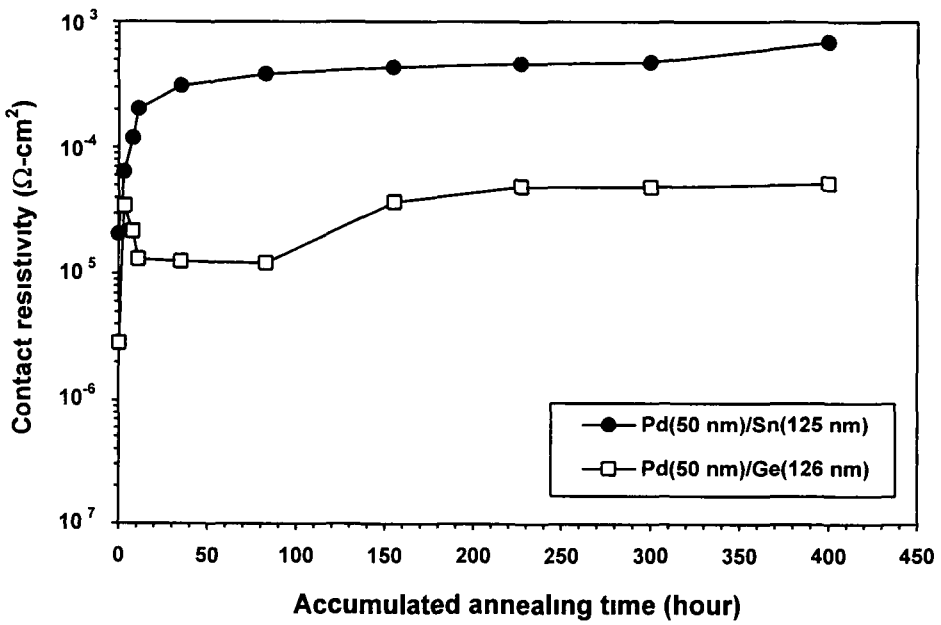


Fig 7 5 Contact resistivity vs accumulated annealing time curves for the Pd/Sn and Pd/Ge Ohmic contacts to n-GaAs at 300 ^{0}C

After annealing at 300 ^{0}C for 400 h, SEM micrographs of the Pd/Sn and Pd/Ge Ohmic contacts are shown in Fig 7 6 For the Pd/Sn contacts, no change in surface morphology is observed after 400 h of annealing at 300 ^{0}C (Fig 7 6(a)) when compared

to that of the minimum ρ_c condition (Fig.4.7(d)). No change in surface morphology is also observed after annealing the Pd/Ge contacts for 400 h at 300 ^{0}C (Fig.7.6(b)) when compared to the lowest ρ_c point (Fig.6.2(b)). However, Pd/Ge contacts show better surface morphology than that of Pd/Sn contacts after long-term stability tests (Fig.7.6).

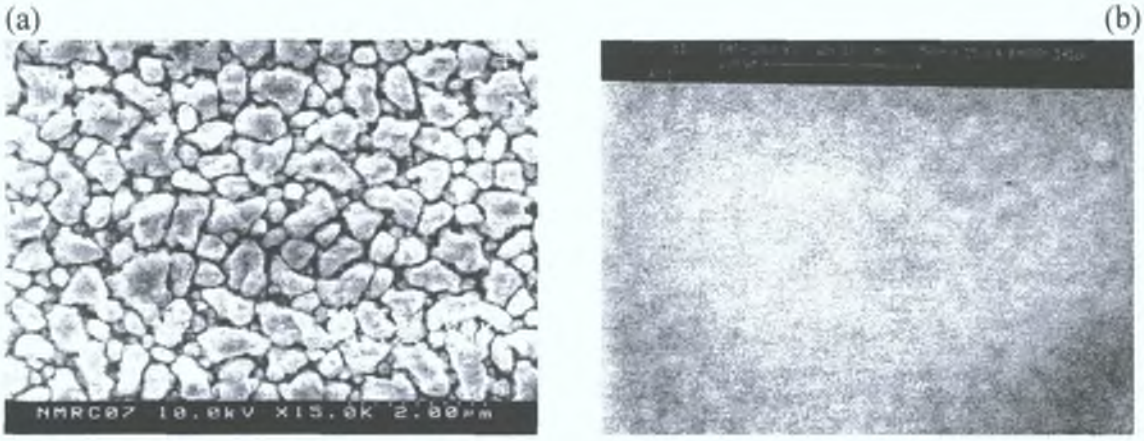


Fig.7.6. SEM micrographs of the (a) Pd(50 nm)/Sn(125 nm) and (b) Pd(50 nm)/Ge(126 nm) contacts to n-GaAs after having been annealed for 400 h at 300 ^{0}C.

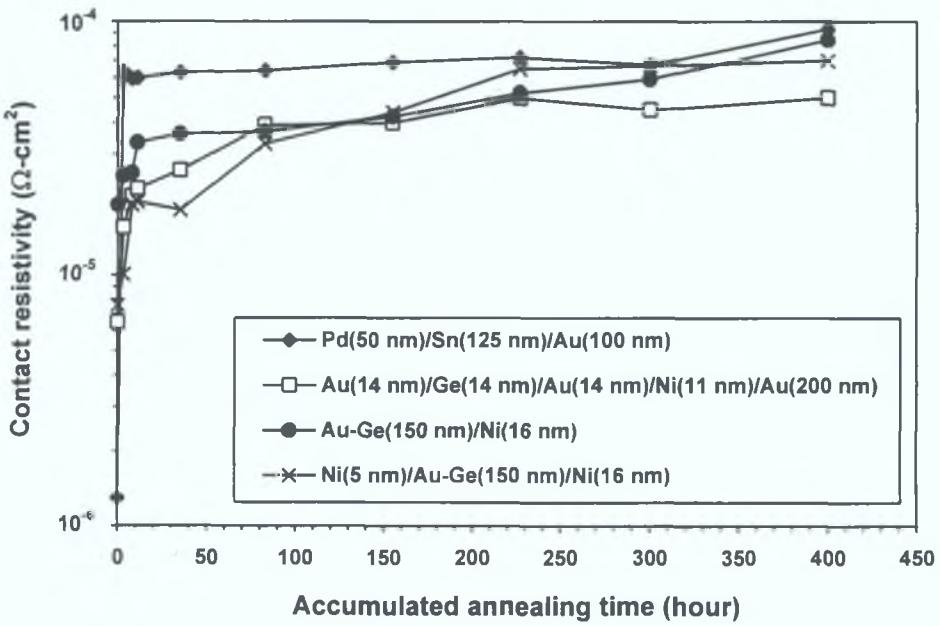


Fig.7.7. Contact resistivity vs. accumulated annealing time curves for the Pd/Sn/Au, Au/Ge/Au/Ni/Au, Au-Ge/Ni and Ni/Au-Ge/Ni Ohmic contacts to n-GaAs at 300 ^{0}C.

Fig.7.7 shows the long-term stability of the Pd/Sn/Au and alloyed Au/Ge/Au/Ni/Au, Au-Ge/Ni and Ni/Au-Ge/Ni Ohmic contacts at 300 ^{0}C. After 3 h of annealing at 300 ^{0}C, the ρ_c of Pd/Sn/Au contacts reaches the mid 10^{-5} Ω-cm^2 range and remains in this region up to 300 h. The ρ_c approaches the high 10^{-5} Ω-cm^2 range at 400 h. For the alloyed five-layer Au/Ge/Au/Ni/Au contacts, the ρ_c remains in the range

of low 10^{-5} Ω-cm^2 up to 155 h and it increases to mid 10^{-5} Ω-cm^2 at 400 h The increase in ρ_c for the alloyed Au-Ge/Ni contacts is insignificant up to 83 h of annealing at 300 ^{0}C and ρ_c remains in the range of low 10^{-5} Ω-cm^2 At 400 h, it increases to the high 10^{-5} Ω-cm^2 range The Ni/Au-Ge/Ni contacts show the best long-term stability up to 83 h of annealing at 300 ^{0}C among all of the contacts investigated, with a ρ_c in the range of low 10^{-5} Ω-cm^2 The five-layer alloyed Au/Ge/Au/Ni/Au contacts exhibit the best stability at 300 ^{0}C for 400 h among all of the Au-based contacts (Fig 7 7)

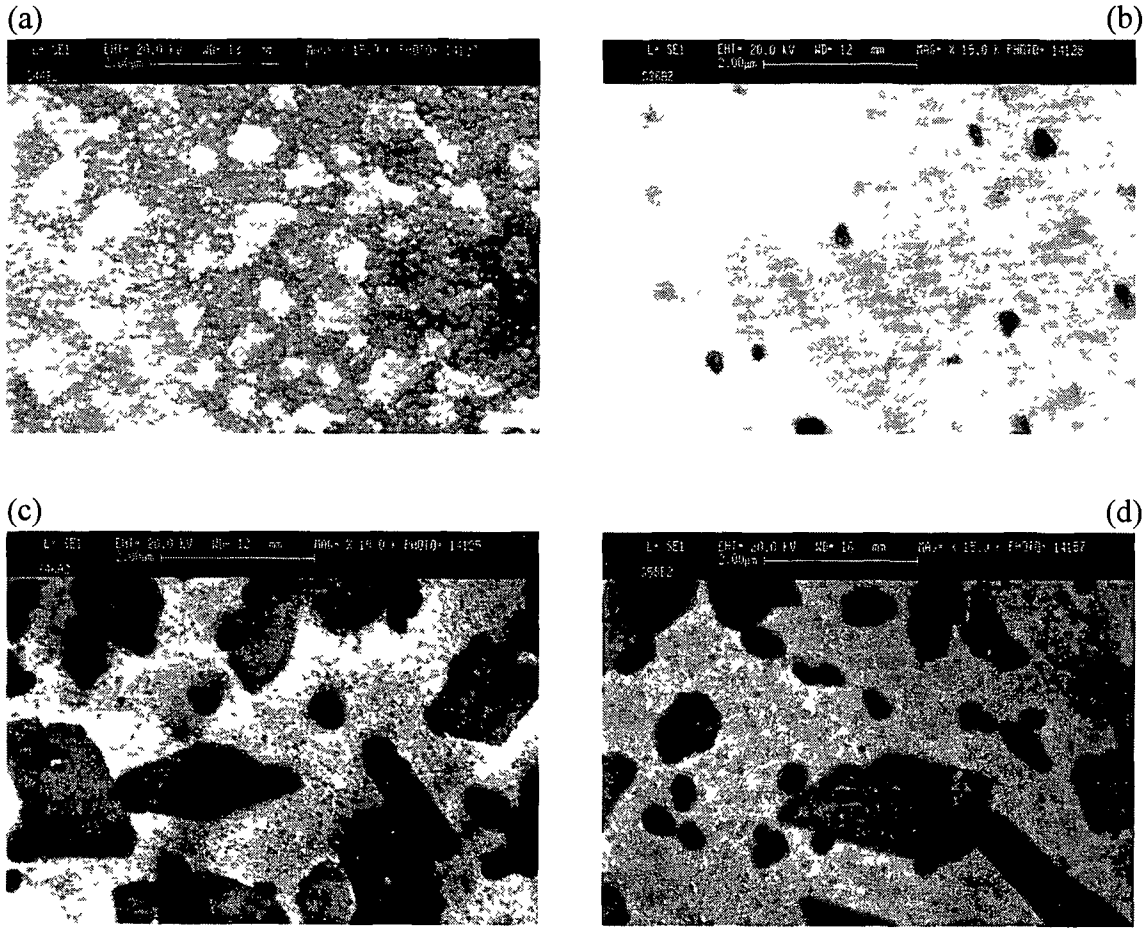


Fig 7 8 SEM micrographs of the (a) Pd(50 nm)/Sn(125 nm)/Au(100 nm) and alloyed (b) Au(14 nm)/Ge(14 nm)/Au(14 nm)/Ni(11 nm)/Au(200 nm), (c) Au-Ge(150 nm)/Ni(16 nm) and (d) Ni(5 nm)/Au-Ge(150 nm)/Ni(16 nm) contacts to n-GaAs after long-term stability at 300 ^{0}C for 400 h

After long-term stability tests at 300 ^{0}C for 400 h, SEM micrographs of the Pd/Sn/Au and alloyed Au/Ge/Au/Ni/Au, Au-Ge/Ni and Ni/Au-Ge/Ni contacts are shown in Fig 7 8 No significant change in surface morphology is observed after 400 h of annealing at 300 ^{0}C for the Pd/Sn/Au (Fig 7 8(a)) and Au/Ge/Au/Ni/Au (Fig 7 8(b)) contacts when compared to the lowest ρ_c conditions (Fig 5 3(d) & Fig 5 3(f)) However, the Au-Ge/Ni and Ni/Au-Ge/Ni contacts display almost identical morphological

characteristics after having been annealed at 300 ^{0}C for 400 h (Fig7 8(c) & Fig 7 8(d))

7.4 Conclusion

Thermal stability and long-term stability of the Pd/Sn and Pd/Sn/Au Ohmic contacts are presented and compared to the non-alloyed Pd/Ge and alloyed Au/Ge/Au/Ni/Au, Au-Ge/Ni and Ni/Au-Ge/Ni Ohmic contacts The Pd/Sn contacts show superior thermal stability at 410 ^{0}C to that of the Pd/Ge contacts After annealing at 410 ^{0}C for 4 h, ρ_c of the Pd/Sn contacts reduces to 1 44x10^{-5} Ω-cm^2 from the initial value of 2 07x10^{-5} Ω-cm^2 The ρ_c of the Pd/Ge contacts increases by approximately two orders of magnitude after 2 h of annealing at 410 ^{0}C from the initial value of 2 84x10^{-6} Ω-cm^2 No significant change in surface morphology of both Pd/Sn and Pd/Ge contacts is observed However, the Pd/Ge contacts exhibit better surface morphology than that of the Pd/Sn contacts after annealing for 10 h at 410 ^{0}C

The Pd/Sn/Au contacts show almost identical thermal stability at 410 ^{0}C to that of the alloyed five-layer Au/Ge/Au/Ni/Au contacts After annealing at 410 ^{0}C for 10 h, the ρ_c of the Pd/Sn/Au contacts increases by approximately one order of magnitude and remains in the range of low 10^{-5} Ω-cm^2 The Pd/Sn/Au contacts also display better thermal stability than that of non-alloyed Pd/Ge and alloyed Au-Ge/Ni and Ni/Au-Ge/Ni Ohmic contacts at 410 ^{0}C Although the electrical and morphological characteristics of Ni/Au-Ge/Ni Ohmic contacts are better than that of Au-Ge/Ni contacts (Section 6 3), thermal stability of the former contacts is worse Surface morphology of the above Au-Ge based contacts deteriorates significantly after annealing at 410 ^{0}C for 10 h

Long-term stability at 300 ^{0}C of the non-alloyed Pd/Ge contacts is better than that of the Pd/Sn contacts After 8 h of annealing at 300 ^{0}C, the ρ_c of the Pd/Sn contacts increases by approximately one order of magnitude from an initial value of 2 07x10^{-5} Ω-cm^2 At this condition, the Pd/Ge contacts maintain ρ_c in the range of low 10^{-5} Ω-cm^2 After annealing for 400 h at 300 ^{0}C, ρ_c of the Pd/Ge contacts remains in the range of mid 10^{-5} Ω-cm^2, which is one order of magnitude lower than that of the Pd/Sn contacts Once again, no change in surface morphology of the Pd/Sn and Pd/Ge contacts is observed The Pd/Ge contacts maintain surerior surface morphology to that of the Pd/Sn contacts after annealing at 300 ^{0}C for 400 h

The alloyed Ni/Au-Ge/Ni contacts show improved long-term stability at 300 ^{0}C only up to 83 h After that, the five-layer Au/Ge/Au/Ni/Au contacts maintain ρ_c in the range of mid 10^{-5} Ω-cm^2 which is better than those of the Pd/Sn/Au and alloyed Au-Ge/Ni and Ni/Au-Ge/Ni contacts For the Pd/Sn/Au contacts, ρ_c remains in the range of mid 10^{-5} Ω-cm^2 up to 300 h and it approaches the high 10^{-5} Ω-cm^2 range at 400 h At 300 ^{0}C, the Pd/Sn/Au Ohmic contacts display ρ_c's which are slightly higher than those of alloyed Au/Ge/Au/Ni/Au, Au-Ge/Ni and Ni/Au-Ge/Ni contacts However, the Pd/Sn/Au contacts maintain better surface morphology than that of the alloyed contacts and no significant morphological change is observed after annealing at 300 ^{0}C for 400 h Therefore, thermally stable Pd/Sn and Pd/Sn/Au Ohmic contacts appear to be promising candidates for GaAs devices

CHAPTER 8

Fabrication of GaAs MESFETs using Pd/Sn and Pd/Sn/Au Ohmic contacts

8.1 Introduction

GaAs Metal Semiconductor Field-Effect Transistors (GaAs MESFETs) have been fabricated using Pd/Sn and Pd/Sn/Au Ohmic contacts as source/drain metallizations and Schottky Al gate contacts. The characteristics of the GaAs MESFETs fabricated with non-alloyed Pd/Ge Ohmic contacts are also investigated and compared with those of the Pd/Sn and Pd/Sn/Au contacts. Metallizations are deposited using a resistance heating evaporator and annealing is carried out in a conventional graphite strip annealer. Surface morphology of the contacts is investigated using Scanning Electron Microscopy (SEM). Conversion from Schottky to Ohmic behaviour of the contacts is confirmed by I-V measurements. The I-V characteristics of the GaAs MESFETs are determined using a TEKTRONIX 576 curve tracer. Contact resistivities, ρ_c, of the metallizations are measured using the cTLM method.

8.2 Experimental Procedures

8.2.1 Level 1 - Mesa isolation

The substrate shown previously in Fig.4.3 is used for the MESFET fabrication. The first process in the fabrication cycle is the production of mesas on the surface by chemical etching. An appropriate mask and Shipley Microposit S1818 positive photoresist are used for this purpose. Mesas for the MESFETs, morphology and TLM structures were fabricated in the same chip. It is important to etch deep enough such that the bulk SI GaAs is reached. This provides mesas which are electrically isolated from each other. The sequential steps for the mesa isolation were as follows:

- The GaAs substrates were sequentially cleaned and degreased in trichloroethylene, acetone, methanol and de-ionized water (DI H_2O), each for 10 min.

- The substrates were blow-dried immediately using dry N_2
- Spin on Microposit S1818 photoresist diluted with Microposit EC solvent in the ratio of 1 4 by volume Spinner speed and acceleration were optimised using test samples Spinner speed=4500 rpm and acceleration =maximum
- Soft bake at 115 ^{0}C for 5 min and cool to room temperature
- Using a UV light mask aligner and mesa mask, expose the substrates for 25 s Expose time was optimised using test samples
- Develop in 3 1 (by volume) DI H_2O Microposit M351 developer for ~60 s and then clean in DI H_2O Dry off using N_2
- Hard bake at 115 ^{0}C for 5 min and cool to room temperature
- Etch in a solution of H_2O_2 NH_4OH DI H_2O (1 3 15 by volume)
- The etch rate for the above etchant was typically 0 8 μm/min at a room temperature of 20 ^{0}C and was determined from test samples The etch time was 4 mm 15 s so that the total etch depth became at least 3 2 μm
- Rinse in DI H_2O and dry off only using N_2
- Leave the chips in acetone for 10 min and strip off photoresist Rinse in DI H_2O and dry off using N_2

8.2.2 Level 2 - Ohmic contacts

The second level is the Ohmic level The sequential process steps of this level were as follows

- Spin on Microposit S1818 photoresist diluted with EC solvent in the ratio of 1 1 by volume on the mesa defined chip This ratio was optimised using test samples
- Soft bake at 115 ^{0}C for 5 min and cool to room temperature
- Soak in chlorobenzene for 3-4 min and dry off only This gives the resist an undercut profile which will assist the metal lift off
- Using a UV light mask aligner and Ohmic mask, expose the substrates for 12 s Expose time was optimised using test samples
- Develop in 3 1 (by volume) DI H_2O Microposit M351 developer for ~45 s and then clean in DI H_2O Dry off using N_2
- The source/drain metallizations were sequentially cleaned in trichloroethylene, acetone, methanol and de-ionized water (DI H_2O), each for 10 min and dry off using N_2
- Prior to loading into an evaporator, the wafers were soaked in a solution of DI H_2O.HCl (15.1 by volume) for at least 2 min and then blow dried using dry N_2 to remove native oxides.

- The n-GaAs/Pd(50 nm)/Sn(125 nm), n-GaAs/Pd(50 nm)/Ge(126 nm) and n-GaAs/Pd(50 nm)/Sn(125 nm)/Au(100 nm) contacts were prepared by sequential deposition of metallizations in a resistance heating evaporator (Appendix A) without breaking vacuum W boats were used as evaporation sources The base pressure was ~$1x10^{-6}$ Torr and pressure during evaporation was between $1.5x10^{-6}$ Torr and $4.5x10^{-6}$ Torr
- Leave the chips in Microposit 1165 remover for at least 3 h and strip off photoresist Rinse in DI H_2O and dry off using N_2 An ultrasonic bath was used (with care) to aid lift-off
- All contacts were annealed for 30 mm by a conventional graphite strip annealer (Appendix B) in a flowing forming gas (5% H_2 + 95% N_2) ambient The Pd(50 nm)/Sn(125 nm) and Pd(50 nm)/Ge(126 nm) contacts were annealed at 330 ^{0}C, whereas the Pd(50 nm)/Sn(125 nm)/Au(100 nm) contacts were annealed at 300 ^{0}C

8.2.3 Level 3 - Schottky (Gate) contacts

Level 3, the most critical step for device performance, involves the deposition of gate metallization between the source and drain contact pads The Schottky contact is composed of Al The gate length, L_G, used for the fabrication of MESFETs are 2, 5 and 50 μm The gate-to-source distance, L_{GS}, is equal to the gate-to-drain distance, L_{GD}, and for all MESFETs L_{GS}=L_{GD}=2 μm The sequential process steps for this level were as follows

- Spin on Microposit S1818 photoresist diluted with EC solvent in the ratio of 1 1 (by volume) on the Ohmic contact defined chip This ratio was optimised using test samples
- Soft bake at 115 ^{0}C for 5 min and cool to room temperature
- Soak in chlorobenzene for 3-4 mm and dry off only
- Using a UV light mask aligner and gate mask, expose the substrates for 20 s Expose time was optimised using test samples
- Develop in 3 1 (by volume) DI H_2O Microposit M351 developer for ~45 s and then clean in DI H_2O Dry off using N_2
- A recess gate etch was performed in order to obtain a target pinch off voltage of 5V (Appendix D) The following steps were carried out in order to achieve a channel depth, d, of 0 12 μm (120 nm)
    - A solution of H_2O_2 NH_4OH DI H_2O in the ratio of 1 3 15 (by volume) was prepared and diluted with DI H_2O in the ratio 1 10 Etch rate was checked using test pieces and the Tencor Profilometer Etch rate was ~24Å/s

- A stop etch solution of NH_4OH DI H_2O in1 5 ratio was prepared
- The substrates were placed in the etchant for 75 s in order to achieve d=0 12 μm
- Place m stop etch for 30 s
- Rinse in DI H_2O for 30 s and dry off using N_2

- The gate metallization, Al, was sequentially cleaned in trichloroethylene, acetone, methanol and de-ionized water (DI H_2O), each for 10 mm and dried off using N_2
- Prior to loading into an evaporator, the wafers were soaked in a solution of DI H_2O HCl (15 1 by volume) for at least 2 min and then blow dried using dry N_2 to remove native oxides
- A 250 nm Al gate metallization was evaporated using a W coil in a resistance heating evaporator (Appendix A) The base pressure was ~$2x10^{-6}$ Torr and pressure during evaporation was between 3 $0x10^{-6}$ Torr and 4 $0x10^{-6}$ Torr
- Leave the chips in Microposit 1165 remover for at least 3 h and strip off photoresist Rinse in DI H_2O and dry off using N_2 Lift-off was aided by careful use of an ultrasonic bath

Surface morphology of the contacts was investigated using a Cambridge S360 SEM Conversion from Schottky to Ohmic behaviour of the contacts was examined by I-V measurements The I-V characteristics of the MESFETs were determined using a TEKTRONIX 576 curve tracer Contact resistivity was measured utilizing the cTLM method

8.3 Results and Discussions

8.3.1 Ohmic contacts

The ρ_c of the Ohmic contacts are measured in a test pattern conforming to the TLM (Fig 4 1), with pad spacing ranging from 2 to 128 μm The width of the Ohmic pad, W, is 140 μm The transfer length method [12] is utilized to measure ρ_c values of the contacts All Ohmic contacts are annealed for 30 mm It is assumed that the sheet resistance of the semiconductor under the contacts, R_{sh1}, is equal to the sheet resistance of the semiconductor in between the contacts, R_{sh2} The average ρ_c for 2 groups of samples, with two samples in each group, were measured The Pd(50 nm)/Sn(125 nm) contacts show a ρ_c of $2.28x10^{-5}$ Ω-cm^2 at 330 ^{0}C, whereas for the Pd(50 nm)/Ge(126 nm) contacts this value is $2\ 84x10^{-6}$ Ω-cm^2 under the same annealing condition A ρ_c of $8\ 13x10^{-6}$ Ω-cm^2 is obtained at 300 ^{0}C for the Pd(50 nm)/Sn(125 nm)/Au(100 nm)

contacts Under these conditions, contact resistances, R_c, of the Pd/Sn, Pd/Ge and Pd/Sn/Au Ohmic contacts are 3 88Ω, 1 41Ω and 2 31Ω , respectively

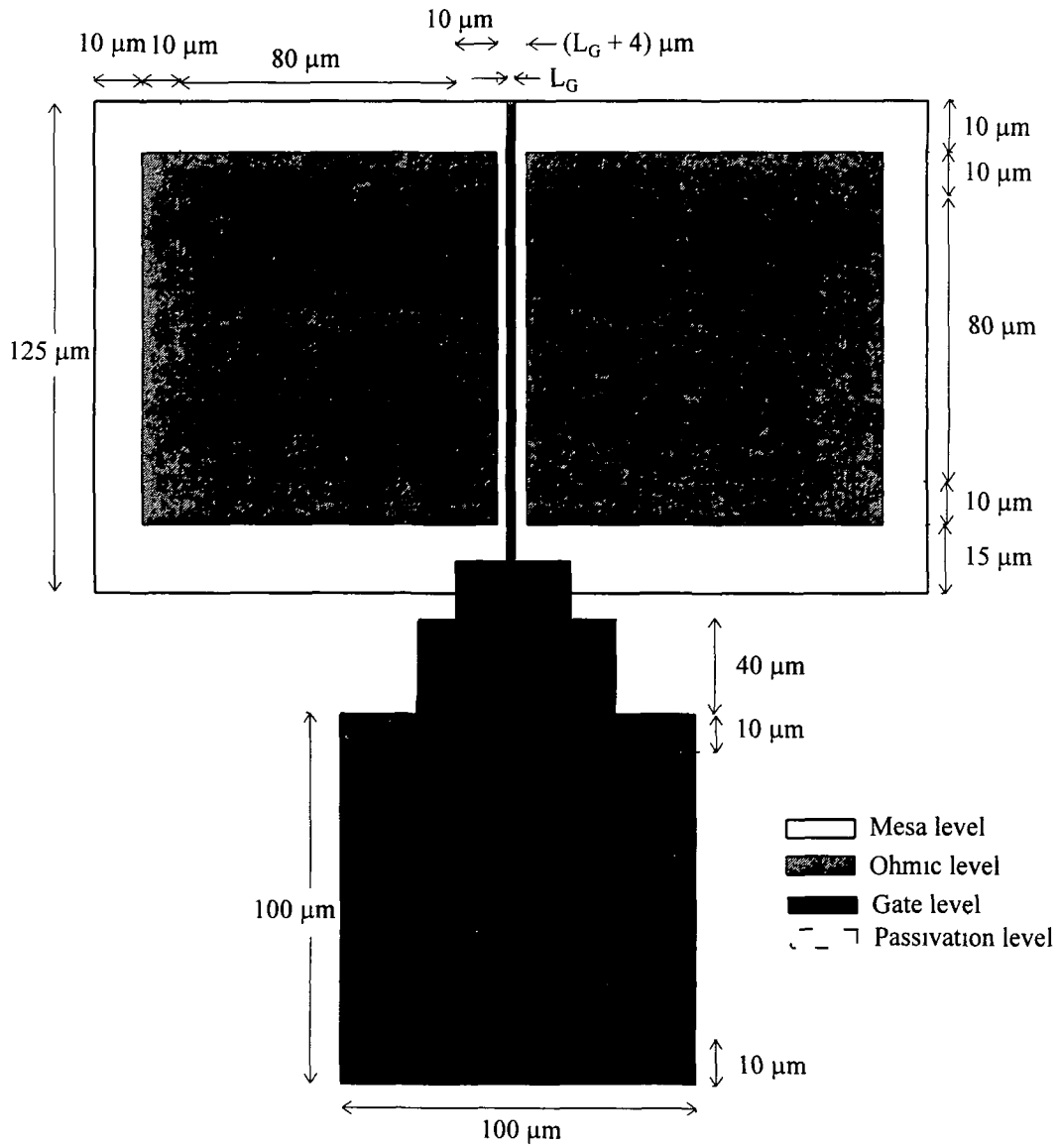


Fig 8 1 Layout of GaAs MESFET Alignment marks are not included

8.3.2 MESFET characterization

The layout of the GaAs MESFET is shown in Fig 8 1 Level 4 (passivation level) was not used for this characterization MESFETs with gate lengths, L_G, of 2 μm, 5 μm and 50 μm were investigated in this study The dimensions of the source and drain Ohmic pads is 100 μm x 100 μm MESFET characteristics were investigated under the gate metal as-deposited condition All MESFETs operated in depletion mode. MESFET transconductance, g_m, and series resistance, R_S, were extracted from the I-V characteristics The R_S was measured in the linear region and was defined by

$$R_S = \left.\frac{\partial V_{DS}}{\partial I_{DS}}\right|_{V_{GS}=0V}, \tag{8.1}$$

whereas g_m was measured in the saturation region and was defined by

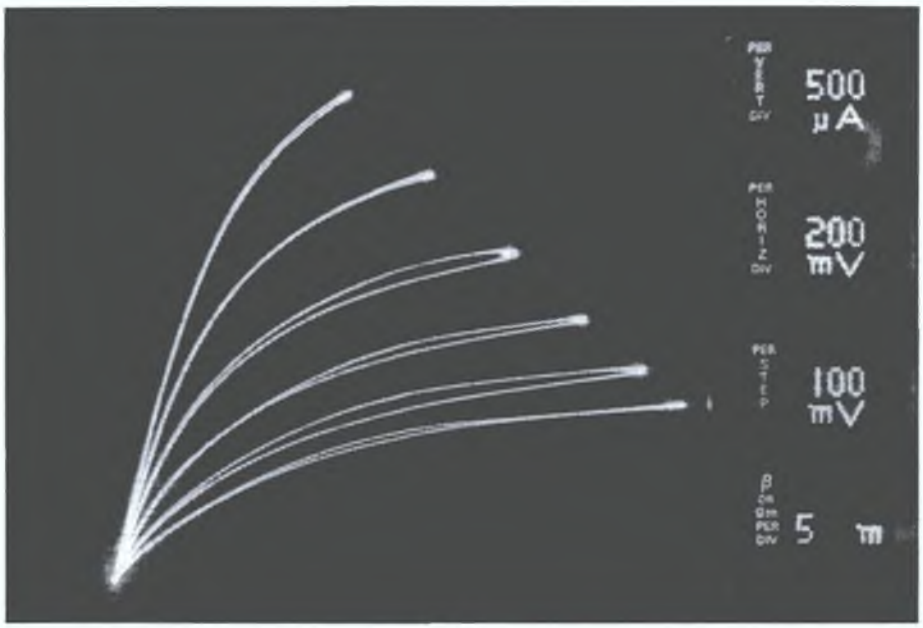
$$g_m = \left.\frac{\partial I_{DSS}}{\partial V_{GS}}\right|_{V_{DS}=const.}, \tag{8.2}$$

where I_{DS} = drain current and I_{DSS} = drain saturation current. Both R_S and g_m have a significant effect on the performance of GaAs MESFETs. Higher R_S produces greater heat dissipation and larger voltage drop in the extrinsic parts of the device, which in turn reduces the value of I_{DS}. The relationship between R_S and g_m is defined by

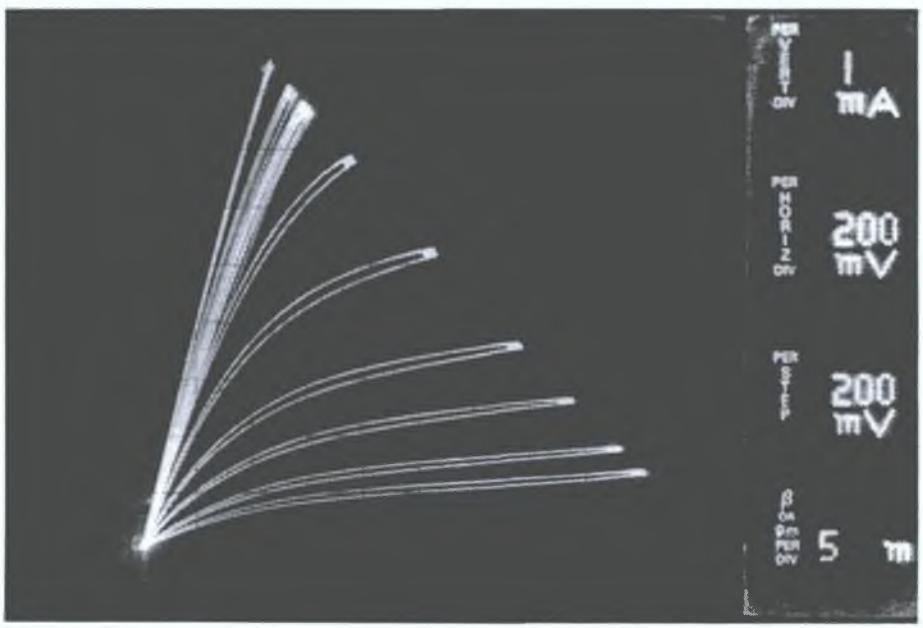
$$g_m = \frac{g_m(\text{int})}{1 + R_S g_m(\text{int})}, \tag{8.3}$$

where g_m(int) is the intrinsic transconductance of the device. As R_S increases, g_m decreases as seen from eqn.(8.3). Any degradation in I_{DS} and g_m will have a corresponding effect on the speed of the GaAs ICs [159]. In analog circuits, the small-signal voltage gain is directly proportional to g_m [160].

Fig.8.2 compares the I-V characteristics of the MESFETs fabricated with Pd/Sn and Pd/Sn/Au metallizations for L_G = 2 μm. It is seen that these characteristics exhibit looping behaviour (i.e., hysteresis of drain current). It is believed that the looping phenomenon is attributed to slow transient behaviour of deep traps present in semi-insulating substrates [161]. This type of looping phenomenon in GaAs MESFETs is also observed by other researchers [162-164]. In the case of Pd/Sn Ohmic metallizations (Fig.8.2(a)), R_S=107Ω (linear, V_{GS}=0V) and g_m=107.1 mS/mm (V_{GS}=-0.1V and V_{DS}=0.94V) . For the Pd/Sn/Au metallizations (Fig.8.2(b)), R_S=52.63Ω (V_{GS}=0V). Due to the difficulty of viewing I-V characteristics at V_{GS}=0V in the saturation region (Fig.8.2(b)), g_m is calculated at V_{GS} = -0.8V and V_{DS} = 0.76V. This value is 100 mS/mm. Generally, maximum g_m (g_{max}) occurs around V_{GS} = 0V. Therefore, g_{max} for this MESFET would, in all liklihood, be greater than 100 mS/mm. The calculated g_m values under different gate bias conditions for the above MESFETs are shown in TABLE XV and TABLE XVI. From these tables, it is clear that the MESFET with Pd/Sn/Au metallization displays an improved g_m when compared to the Pd/Sn contact.



(a)



(b)

Fig.8.2. I-V characteristics of the MESFETs for L_G=2 μm with (a) Pd/Sn and (b) Pd/Sn/Au as source/drain contacts.

TABLE XV. Calculated g_m values under different gate bias conditions for a MESFET with L_G =2 μm and Pd/Sn source/drain contacts (V_{DS}=0.94V).

V_{GS}(V)	-0.1	-0.2	-0.3	-0.4	-0.5
g_m (mS/mm)	107.1	98.2	88.1	78.6	69.3

TABLE XVI Calculated g_m values under different gate bias conditions for a MESFET with L_G =2 μm and Pd/Sn/Au source/drain contacts (V_{DS}=0 76V)

V_{GS}(V)	-0 8	-1 0	-1 2	-1 4	-1 6
g_m (mS/mm)	100	92 5	77 1	67 2	57 5

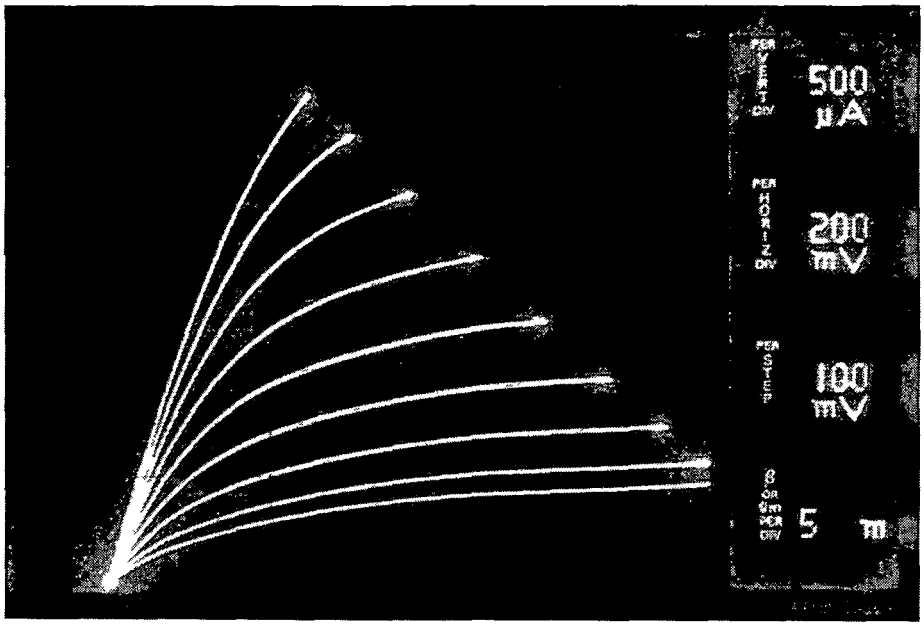


Fig 8 3 I-V characteristics of the MESFET for L_G=5 μm with Pd/Sn as source/dram contacts

Fig 8 3 shows the I-V characteristics of the MESFET for L_G=5 μm with Pd/Sn as source/drain metallization At V_{GS}=0V, R_S=110Ω For this MESFET, g_m values are calculated at V_{DS}=0 78V and are shown in TABLE XVII The g_{max} occurs at V_{GS}=-0 1V which is 71 4 mS/mm

TABLE XVII Calculated g_m values under different gate bias conditions for a MESFET with L_G =5 μm and Pd/Sn as source/drain contacts (V_{DS}=0 78V)

V_{GS} (V)	-0 1	-0 2	-0 3	-0 4	-0 5	-0 6	-0 7	-0 8
g_m (mS/mm)	71 4	69 6	69 0	67 0	64 3	60 7	56 1	51 5

A MESFET with Pd/Sn/Au as source/drain contacts yields R_S=109 22Ω (V_{GS}=0V) for L_G =5 μm (Fig 8 4) The g_m values are calculated for V_{DS}=0 78V and are shown in TABLE XVIII The g_{max} occurs at V_{GS}=-0 1V and is 64 3 mS/mm Therefore, MESFETs with both Pd/Sn and Pd/Sn/Au source/drain contacts show almost identical R_S values at L_G =5 μm However, the Pd/Sn contact shows improved g_m values when

compared with the Pd/Sn/Au metallization This result is somewhat surprising and this may be due to the production variations

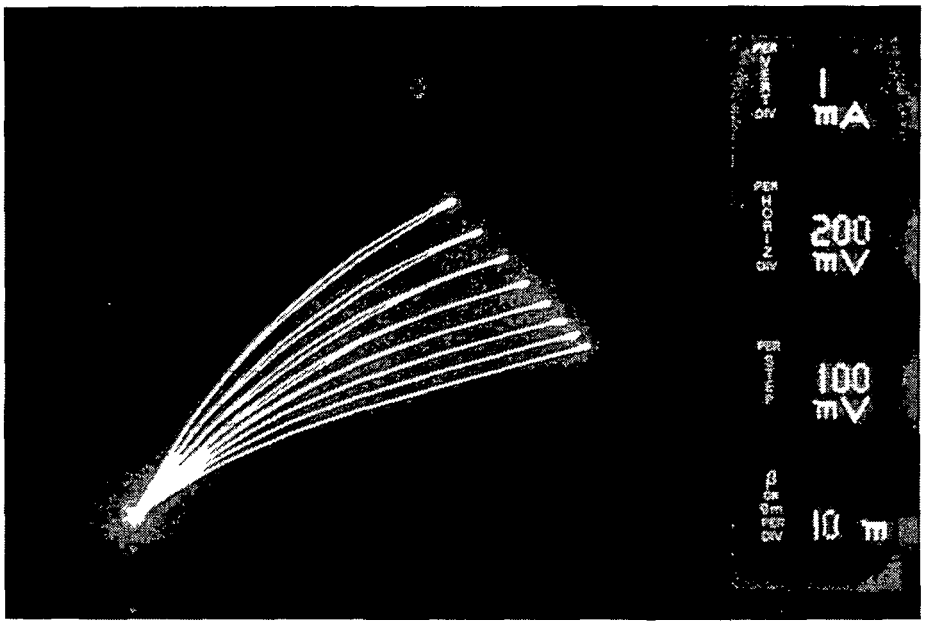


Fig 8 4 I-V characteristics of the MESFET for L_G =5 μm with Pd/Sn/Au as source/drain contacts

TABLE XVIII Calculated g_m values under different gate bias conditions for a MESFET with L_G =5 μm and Pd/Sn/Au as source/drain contacts (V_{DS}=0 78V)

V_{GS} (V)	-0 1	-0 2	-0 3	-0 4	-0 5	-0 6	-0 7
g_m (mS/mm)	64 3	60 0	54 3	50 0	45 7	42 9	40 8

A MESFET with L_G =50 μm and Pd/Sn as source/drain contacts yields a R_S=505Ω at V_{GS}=0V The I-V characteristics for this MESFET is shown in Fig 8 5 TABLE XIX summarizes g_m values at different gate bias points for V_{DS}=1 89V The g_{max} is 20 8 mS/mm (V_{GS}=-0 1V, V_{DS}=1 89V) For Pd/Sn/Au metallization (Fig 8 6), the calculated R_S is 485Ω at V_{GS}=0V The g_m data are calculated at V_{DS}=2V and are shown in TABLE XX The g_{max} is 22 2 mS/mm (V_{GS}=-0 1V, V_{DS}=2V) which is slightly higher than that of the Pd/Sn contacts (TABLE XIX)

TABLE XIX Calculated g_m values under different gate bias conditions for a MESFET with L_G =50 μm and Pd/Sn as source/drain contacts (V_{DS}=1 89V)

V_{GS} (V)	-0.1	-0 2	-0 3	-0 4	-0 5	-0 6	-0 7	-0 8
g_m (mS/mm)	20 8	19 4	19 4	19 1	18 3	18 1	17 9	16 9

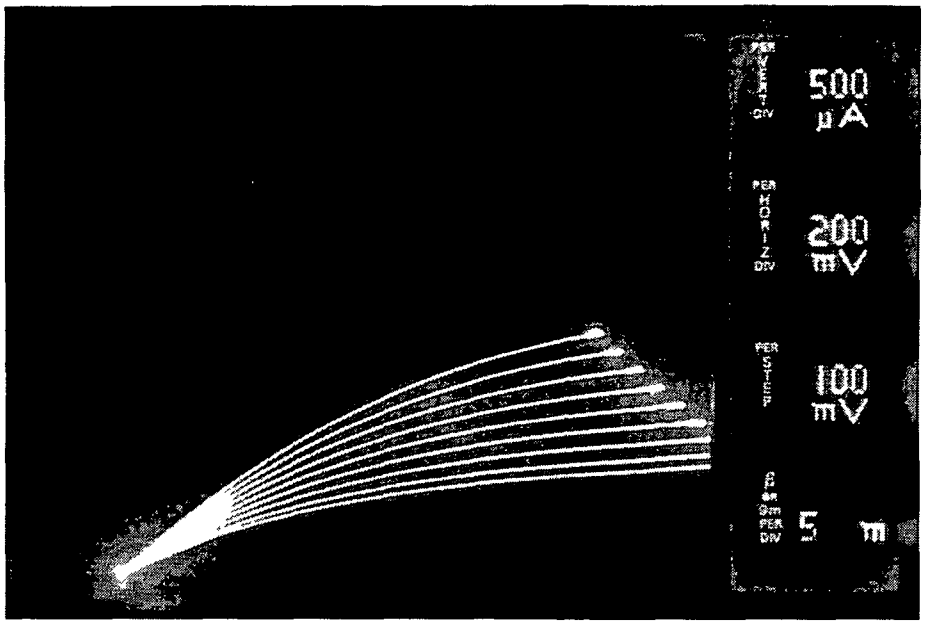


Fig 8 5 I-V characteristics of the MESFET for L_G =50 μm with Pd/Sn as source/drain contacts

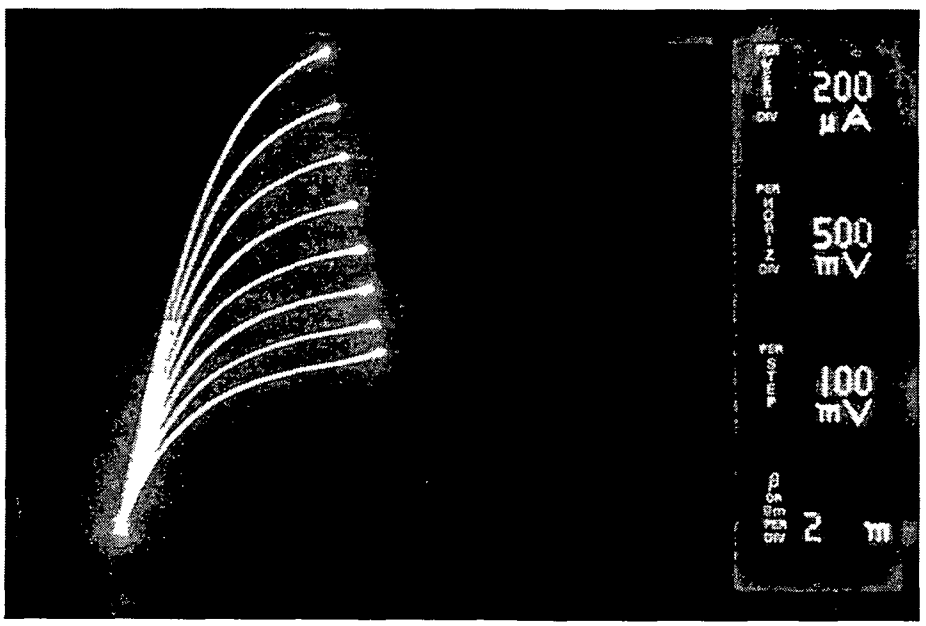


Fig 8 6 I-V characteristics of the MESFET for L_G=50 μm with Pd/Sn/Au as source/drain contacts

TABLE XX Calculated g_m values under different gate bias conditions for a MESFET with L_G =50 μm and Pd/Sn/Au as source/drain contacts (V_{DS}=2V)

V_{GS} (V)	-0 1	-0 2	-0 3	-0 4	-0 5	-0 6	-0 7
g_m (mS/mm)	22 2	20 8	20.4	19 4	18 9	18 1	17 3

Although MESFETs were fabricated with Pd/Ge metallization for L_G =2 μm, the I-V characteristics were very poor and hence omitted from this study For L_G=5 μm, the I-V characteristics for the MESFET fabricated with Pd/Ge as source/drain contacts is shown in Fig 8 7 At V_{GS}=0V, R_S=49 71Ω The g_m values are calculated at V_{DS}=1 89V and are shown in TABLE XXI The measured g_{max} has a broad peak and is 92 9 mS/mm At V_{DS}=1 89V, the I-V curve is not in the saturation region for V_{GS}=0V For this reason, g_{max} occured at different V_{GS} The calculated R_S is better than that of the Pd/Sn and Pd/Sn/Au contacts It is believed that this improved R_S is due to the lower R_c with the Pd/Ge contacts (Section 8 3 1) This may also be due to production variations However, the Pd/Ge metallization also produces a better g_{max} than that of the Pd/Sn and Pd/Sn/Au contacts

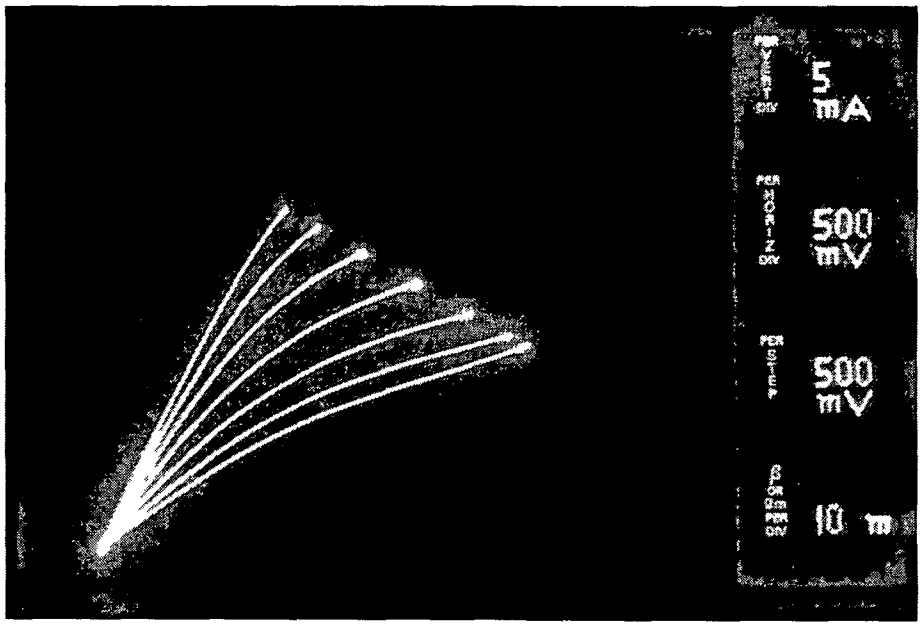


Fig 8 7 I-V characteristics of the MESFET for L_G =5 μm fabricated with Pd/Ge as source/drain contacts

TABLE XXI Calculated g_m values under different gate bias conditions for a MESFET with L_G =5 μm and Pd/Ge as source/drain contacts (V_{DS}=1 89V)

V_{GS} (V)	-0 5	-1 0	-1 5	-2 0	-2 5	-3 0
g_m (mS/mm)	92 9	92 9	90 5	85 7	80 0	73 3

For the MESFET with L_G =50 μm and Pd/Ge as source/drain contacts, R_S=316Ω at V_{GS}=0V The g_m parameters are calculated from the I-V curve of Fig 8 8 at V_{DS}=1 34V and are summarized in TABLE XXII. The g_{max} is 15 3 mS/mm at V_{GS}=-0 5V which is comparable to that of the MESFETs fabricated with Pd/Sn and Pd/Sn/Au contacts at the same V_{GS} (TABLE XIX & TABLE XX)

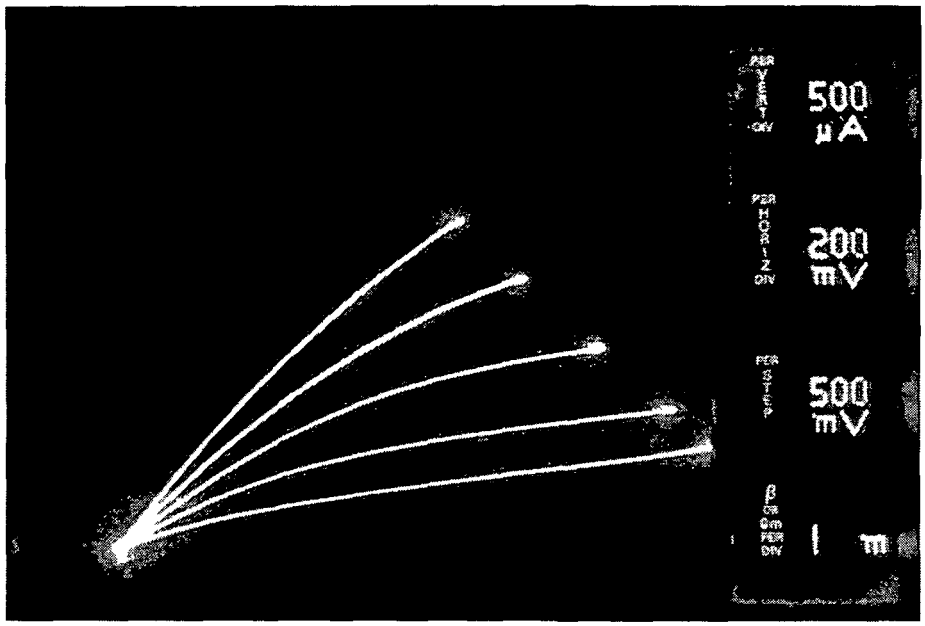


Fig 8 8 I-V characteristics of the MESFET for L_G =50 μm with Pd/Ge as source/drain contacts

TABLE XXII Calculated g_m values under different gate bias conditions for a MESFET with L_G =50 μm and Pd/Ge as source/drain contacts (V_{DS}=1 34V)

V_{GS} (V)	-0 5	-1 0	-1 5	-2 0
g_m (mS/mm)	15 3	14 6	13 7	12 3

The gate I-V characteristics (i e I_{GS} vs V_{GS}) are almost identical for all metallizations Fig 8 9 shows this characteristic for the Pd/Sn source/dram contacts with L_G =2 μm Diode behaviour is expected and it is observed The V_F at which diode current starts to increase from its zero value is ~0 5V

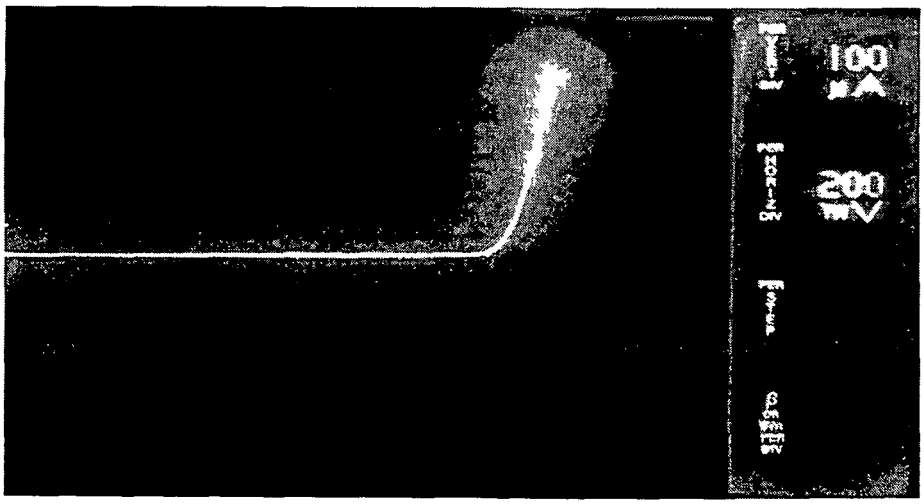


Fig 8 9 Gate leakage I-V characteristics, i e I_{GS} vs. V_{GS}

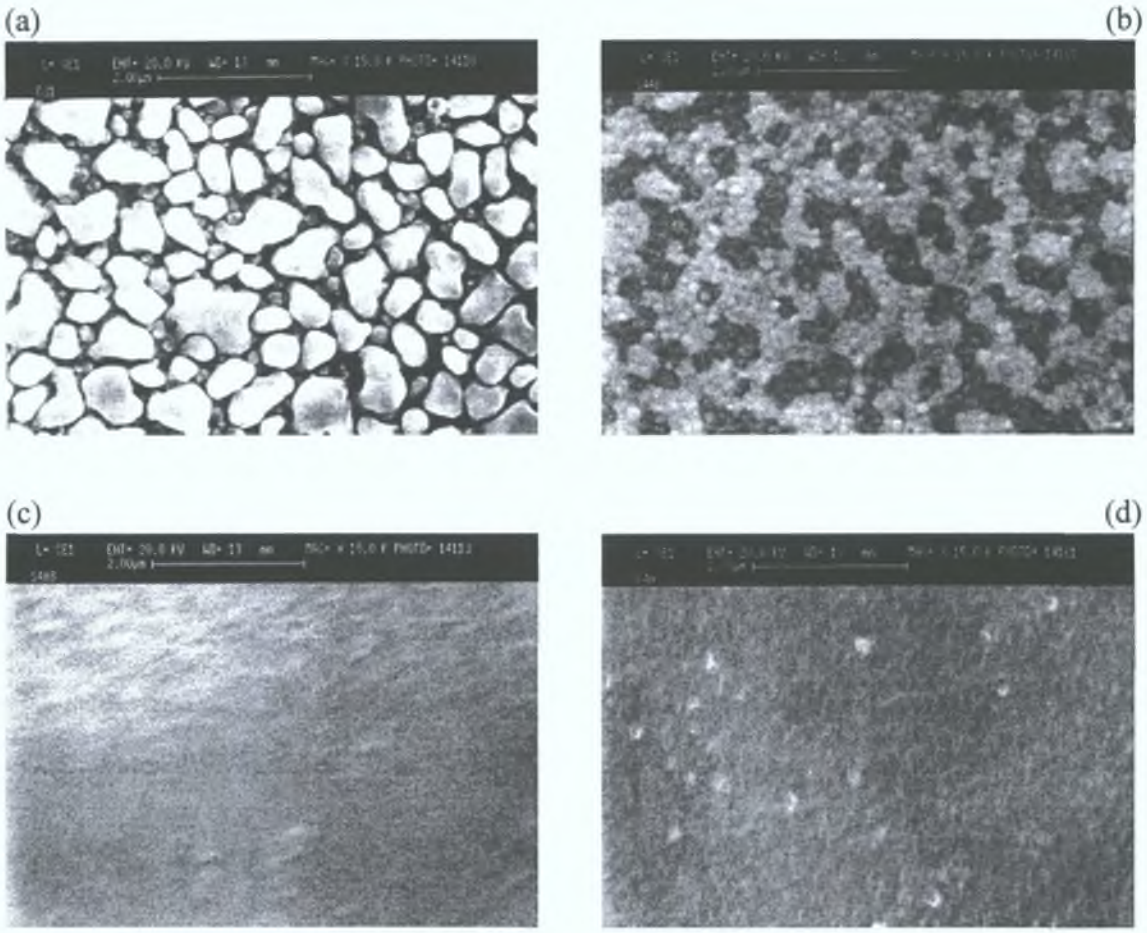


Fig.8.10. SEM micrographs of the source/drain and gate metallizations: (a) Pd/Sn, (b) Pd/Sn/Au, (c) Pd/Ge and (d) Al.

SEM micrographs of the source/drain and gate metallizations are shown in Fig.8.10. The Pd/Ge metallization (Fig.8.10(c)) exhibits smooth surface morphology compared to the Pd/Sn contact (Fig.8.10(a)) and is slightly better than the Pd/Sn/Au metallization (Fig.8.10(b)). The as-deposited Al gate metallization also displays smooth surface morphology (Fig.8.10(d)). A typical MESFET with a L_G =5 μm and Pd/Sn as source/drain contacts is shown in Fig.8.11. The contact edges and alignment accuracy for 2 μm MESFETs with different source/drain metallizations are shown Fig.8.12, Fig.8.13 and Fig.8.14. Morphological characteristics display a significant effect on contact edge uniformity. For all MESFETs, gate metallization shows smooth and uniform contact edges. The contact edges are poor for the Pd/Sn metallization (Fig.8.12) and are due to the rough surface morphology. The maximum amplitude of this undulation is ~0.65 μm. Improved surface morphology produces better edge uniformity for the contacts. It is obviously better for the Pd/Sn/Au metallization (Fig.8.13) and is ~0.10 μm. Although the edge uniformity for the Pd/Ge contact is very good and the undulation is virtually impossible to measure, this metallization system exhibits a slight lift-off problem as seen in Fig.8.14.

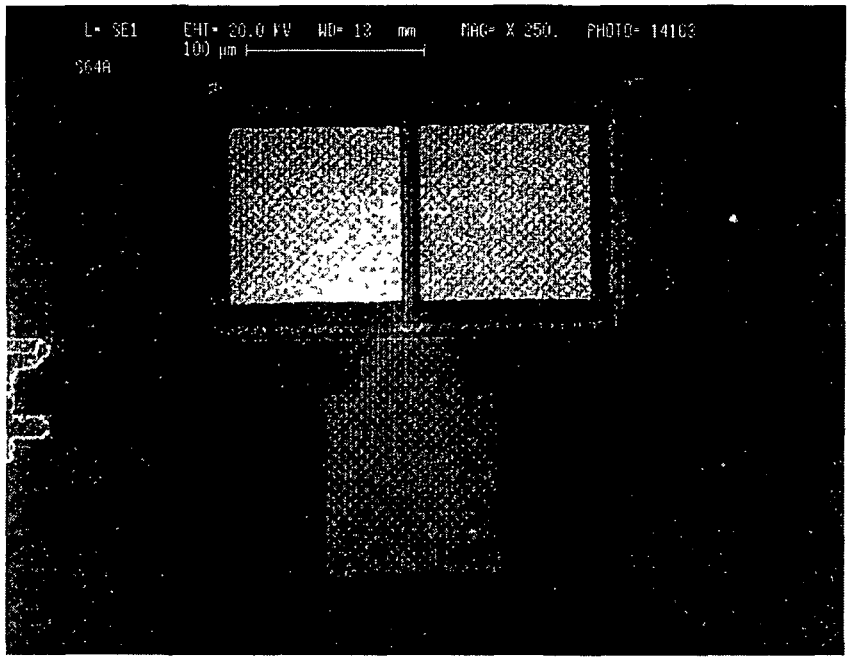


Fig 8 11 SEM micrograph of a typical MESFET device showing Gate, Source and Drain regions and also some alignment marks

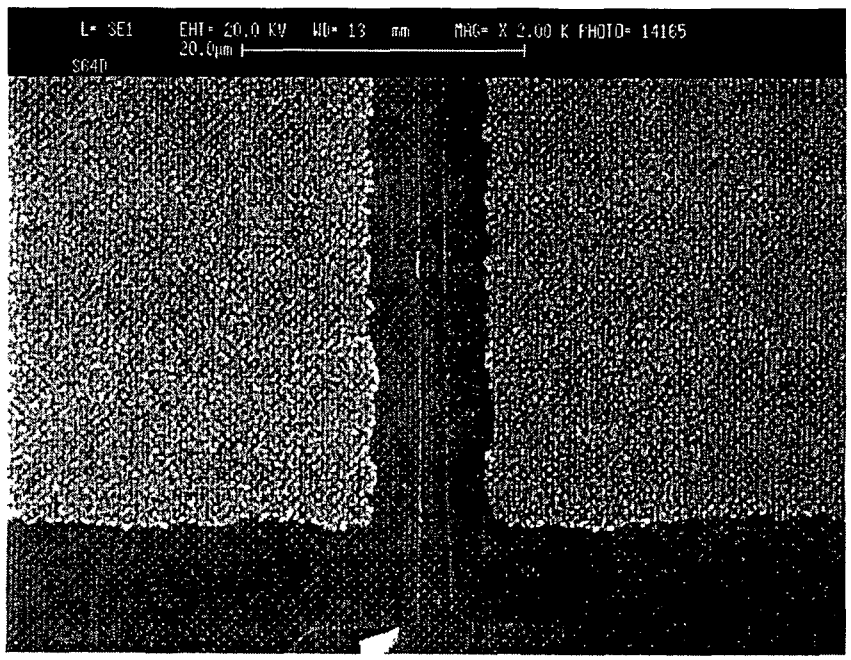


Fig 8 12 SEM micrograph showing alignment accuracy and edge uniformity of a MESFET fabricated with Pd/Sn Ohmic contacts for L_G = 2 µm

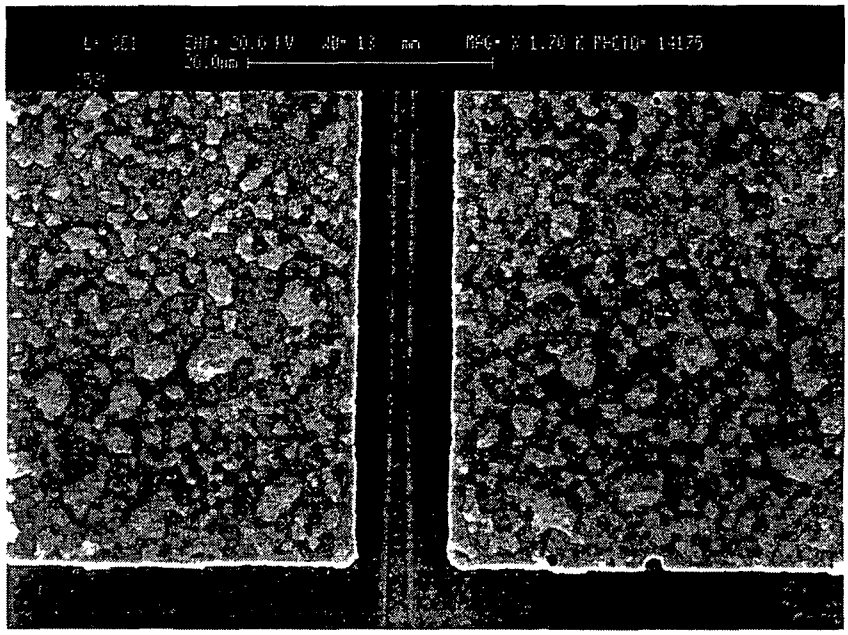


Fig 8 13 SEM micrograph showing alignment accuracy and edge uniformity of a MESFET fabricated with Pd/Sn/Au Ohmic contacts for L_G = 2 μm

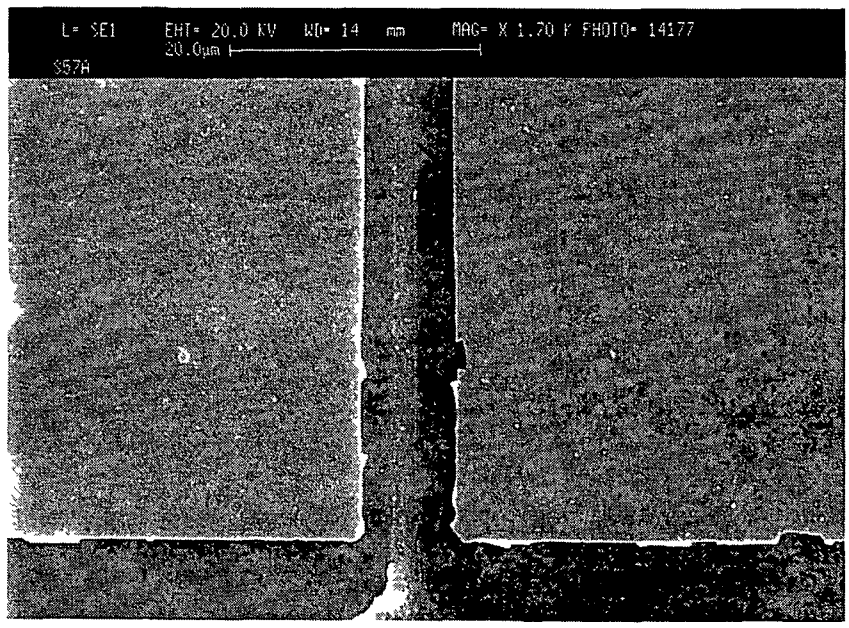


Fig 8 14 SEM micrograph showing alignment accuracy and edge uniformity of a MESFET fabricated with Pd/Ge Ohmic contacts for L_G = 2 μm

8.4 Conclusion

GaAs MESFETs have been fabricated with Pd/Sn, Pd/Sn/Au and Pd/Ge metallizations as source/drain Ohmic contacts MESFETs with gate length of 2 μm, 5 μm and 50 μm are investigated MESFETs with Pd/Sn/Au metallizations show improved characteristics compared to Pd/Sn contacts Although MESFETs with Pd/Ge metallizations were fabricated for L_G=2 μm, the I-V characteristics were very poor and thus omitted from this study

The gate length, L_G, appears to have significant impact on R_S This is due to the increase in channel resistance with an increase in L_G [165] g_m decrease with increasing L_G (eqn 8 3), as expected The Pd/Ge metallization displays slightly better R_S and g_m values compared to the Pd/Sn/Au metallization at L_G=5 μm

Morphological characteristics have a significant impact on the edge uniformity of the contacts Sharp edge definition/uniformity of the source/drain metallizations is necessary for VLSI GaAs devices Improved morphology implies better edge definition The edge definition of source/drain contacts fabricated with Pd/Sn/Au metallization is better than that of the Pd/Sn metallization The Pd/Ge contacts show slightly improved surface morphology when compared to Pd/Sn/Au metallization However, the edge definition of the Pd/Sn/Au metallization is comparable to that of the Pd/Ge contacts

CHAPTER 9

Conclusions and suggestions for future research

9.1 Conclusions

The main objective of this study was to develop and characterize a novel Pd/Sn Ohmic contact system to n-GaAs for use in microwave, optoelectronic and low-dimensional devices The proposed Ohmic contact system has been developed and systematically and extensively characterized using Scanning Tunneling Microscopy (STM), Tencor Surface Profilometry, Scanning Electron Microscopy (SEM), Energy Dispersive Analysis of X-rays (EDAX), Secondary Ion Mass Spectrometry (SIMS) and Current-Voltage (I-V) measurements Contact resistivities, ρ_c, of the proposed metallizations were measured utilizing a conventional Transmission Line Model (cTLM) method

Initially, Pd and Sn evaporation rates were optimized for better surface morphology of the contacts usmg STM The effects of Sn to Pd thickness ratio (m) on the properties of Pd/Sn metallizations were also presented Annealing cycles were optimized for minimum values of ρ_c Proper choice of two-step annealing cycles marginally improves morphological and electrical characteristics of the contacts But it does not change contact abruptness Although it is postulated that the Ohmic contact formation mechanisms of the Pd/Sn metallizations undergo solid-phase reaction (Fig 4 8), the non-alloying behaviour could not be confirmed due to SIMS insensitivity as described in Section 4 4 5

The effects of Au overlayers on the properties of Pd/Sn Ohmic contacts, i e the properties of Pd/Sn/Au metallizations were also analysed It is seen that a judicious choice of Au overlayers improves the characteristics of the Pd/Sn contacts An overlayer of Au also changes the annealing cycles at the minimum ρ_c points Both Pd/Sn and Pd/Sn/Au Ohmic contacts are very adhesive to the substrates The Pd/Sn and Pd/Sn/Au metallizations are more abrupt than the alloyed five-layer Au/Ge/Au/Ni/Au contacts

A comparison has also been made between the electrical and morphological characteristics of the Pd/Sn, Pd/Sn/Au, non-alloyed Pd/Ge and alloyed eutectic

Au-Ge/Ni and Ni/Au-Ge/Ni contacts. The Pd/Sn Ohmic contacts show almost identical ρ_c values when compared with alloyed Au-Ge/Ni contacts. However, morphological characteristics of the Pd/Sn metallizations are even better than those of alloyed Au-Ge/Ni and Ni/Au-Ge/Ni contacts at the lowest ρ_c conditions. The Pd/Sn/Au Ohmic contacts display comparable ρ_c values to the non-alloyed Pd/Ge metallizations with only a slightly deteriorated surface. The electrical and morphological properties of the Pd/Sn/Au metallizations are much better than those of alloyed Au-Ge/Ni and Ni/Au-Ge/Ni contacts.

One of the most important criteria for an Ohmic contact is its thermal stability. No significant change in surface morphology is observed for the Pd/Sn and Pd/Ge metallizations after annealing at 410 ^{0}C for 10 h. The Pd/Sn metallizations exhibit excellent thermal stability at 410 ^{0}C when compared to the non-alloyed Pd/Ge metallizations. Even the Pd/Sn/Au metallizations show better thermal stability at this temperature than that of non-alloyed Pd/Ge contacts with a slightly deteriorated surface morphology. Thermal stability of the five-layer alloyed Au/Ge/Au/Ni/Au Ohmic contacts is almost identical to that of the Pd/Sn/Au metallizations. However, the Pd/Sn/Au Ohmic contacts display improved thermal stability when compared to the alloyed Au-Ge/Ni and Ni/Au-Ge/Ni metallizations with a better surface morphology.

An analysis of the long-term stability of the Ohmic contacts was carried out at 300 ^{0}C. The non-alloyed Pd/Ge metallizations show better long-term stability than the Pd/Sn contacts. No change in surface morphology is observed for the Pd/Sn and Pd/Ge metallizations after annealing at 300 ^{0}C for 400 h. Although Pd/Sn/Au metallizations maintain ρ_c values which are slightly higher than those of alloyed Au-Ge/Ni, Ni/Au-Ge/Ni and Au/Ge/Au/Ni/Au metallizations, no singificant morphological change is observed with Pd/Sn/Au conatcts after having been annealed at 300 ^{0}C for 400 h. At this temperature, the ρ_c values of the Pd/Sn/Au metallizations are only slightly higher than those of non-alloyed Pd/Ge contacts.

Finally, GaAs MESFETs have been fabricated using Pd/Sn and Pd/Sn/Au metallizations as source/drain contacts. Non-alloyed Pd/Ge Ohmic contacts have also been utilized to fabricate GaAs MESFETs. MESFETs with gate lengths of 2 μm, 5 μm and 50 μm were investigated.

The morphological characteristics of the source/drain and gate metallizations impose an ultimate limit on gate-to-source and gate-to-drain separations (L_{GS} & L_{GD}). Improved morphology implies sharper edge definition for the contacts. Surface

morphology of the non-alloyed Pd/Ge metallizations is better than that of Pd/Sn metallizations The Pd/Ge metallizations also display slightly improved surface morphology when compared to the Pd/Sn/Au contacts Although, edge definition for the Pd/Sn/Au source/drain contacts is comparable to that of non-alloyed Pd/Ge metallizations, Pd/Ge contacts tend to exhibit imperfect metal lift-off

Thermal stability of the Ohmic contacts at a device processing temperature (400 ^{0}C) is of serious concern One of the most important reasons for developing non-alloyed Pd/Ge Ohmic contacts was to overcome the thermal instability of the conventional alloyed Au-Ge/Ni metallizations Although, non-alloyed Pd/Ge metallization offers somewhat better electrical and morphological properties, thermal stability of this contact system still require further studies The newly developed Pd/Sn Ohmic contacts display better thermal stability at 410 ^{0}C when compared to the non-alloyed Pd/Ge metallizations At this temperature, thermal stability of Pd/Sn/Au metallizations is also better than that of non-alloyed Pd/Ge contacts with a slightly deteriorated surface morphology Thermal stability of Pd/Sn/Au Ohmic contacts is much better than that of alloyed Au/Ge/Au/Ni/Au, Au-Ge/Ni and Ni/Au-Ge/Ni metallizations The analysis of long-term stability at 300 ^{0}C shows that both Pd/Sn/Au and Pd/Ge metallizations have almost identical stability at this temperature The long-term stability of Pd/Sn/Au metallizations is much better than that of alloyed Au/Ge/Au/Ni/Au, Au-Ge/Ni and Ni/Au-Ge/Ni contacts with a improved surface morphology Therefore, thermally stable Pd/Sn and Pd/Sn/Au metallizations provide promising candidates for future GaAs devices

9.2 Suggestions for Future Research

For future research with Pd/Sn and Pd/Sn/Au Ohmic contacts, the following suggestions are made

- X-Ray Diffraction (XRD) method could be employed in order to investigate the non-alloying behaviour of the contacts This measurement will also determine the phase formation of the metallizations

- Transmission Electron Microscopy (TEM) will show the metal/GaAs interface which will indicate the spiking or non-spiking nature of the contacts

- A Rapid Thermal Annealer (RTA) could be employed for contact formation This should improve the overall characteristics of the contacts

- Auger Electron Spectroscopy (AES) could determine the actual depth profiles of the contacts as SIMS cannot indicate real profiles (Section 4 4 4)

- For fabrication of GaAs MESFETs in the sub-μm range utilizing these metallizations, electron beam evaporation of metals is recommended

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Appendix A

Resistance heating (Thermal) evaporator

An Edwards Coating System E306A (Fig A1) was used as a resistance heating (thermal) evaporator for the deposition of metallizations on the GaAs substrates Initially, the whole system was disassembled and chemically cleaned using trichloroethylene, acetone, methanol and de-ionized water (DI H_2O) An ultrasonic bath was used for the cleaning of small parts All parts were then dried in the fume hood The system was then reassembled

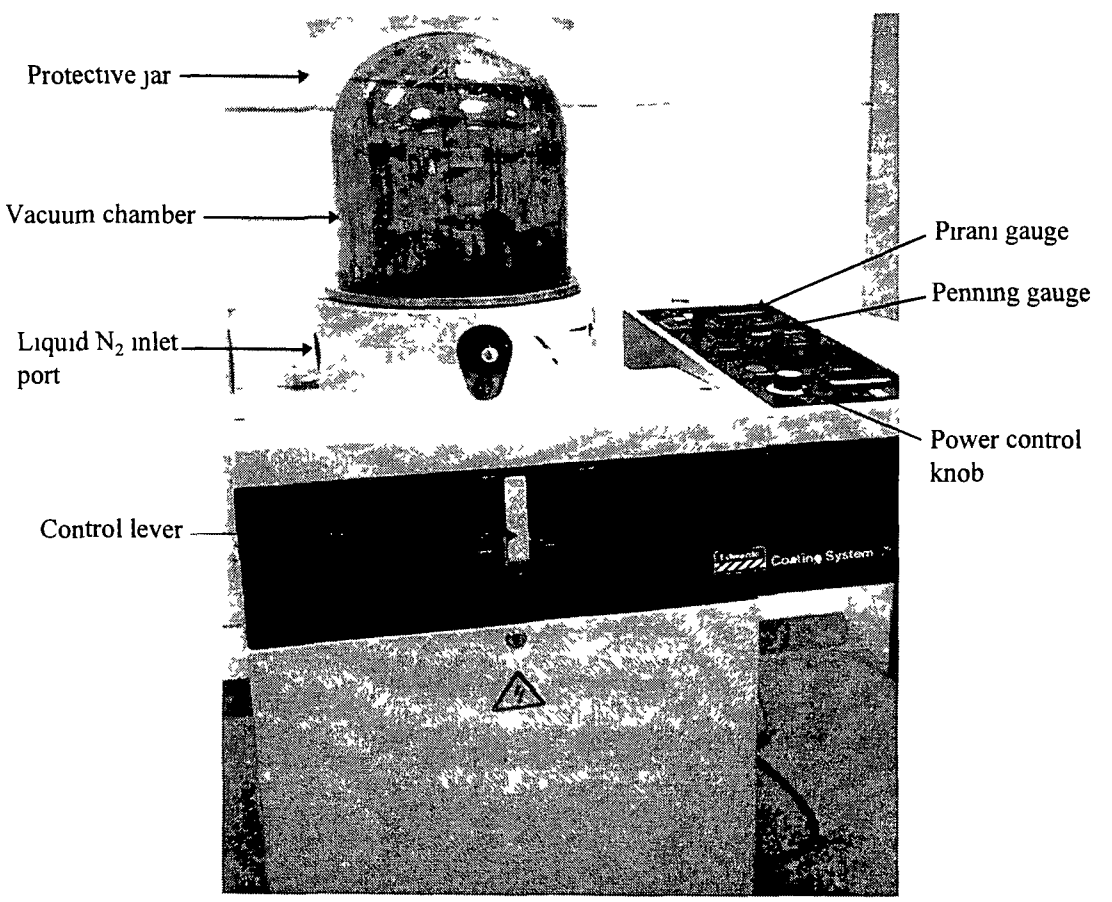


Fig A1 Photograph of Edwards Coating System E306A indicating some of the components

Initially, the system had only one evaporation source This source was a low tension (LT) source and was not sufficient for the evaporation of Pd After some modification of the system, a second evaporation source (high tension, HT) was connected Fig A2 shows the HT transformer, LT transformer, rotary pump and diffusion pump After reassembling, the minimum base pressure was $2x10^{-7}$ Torr

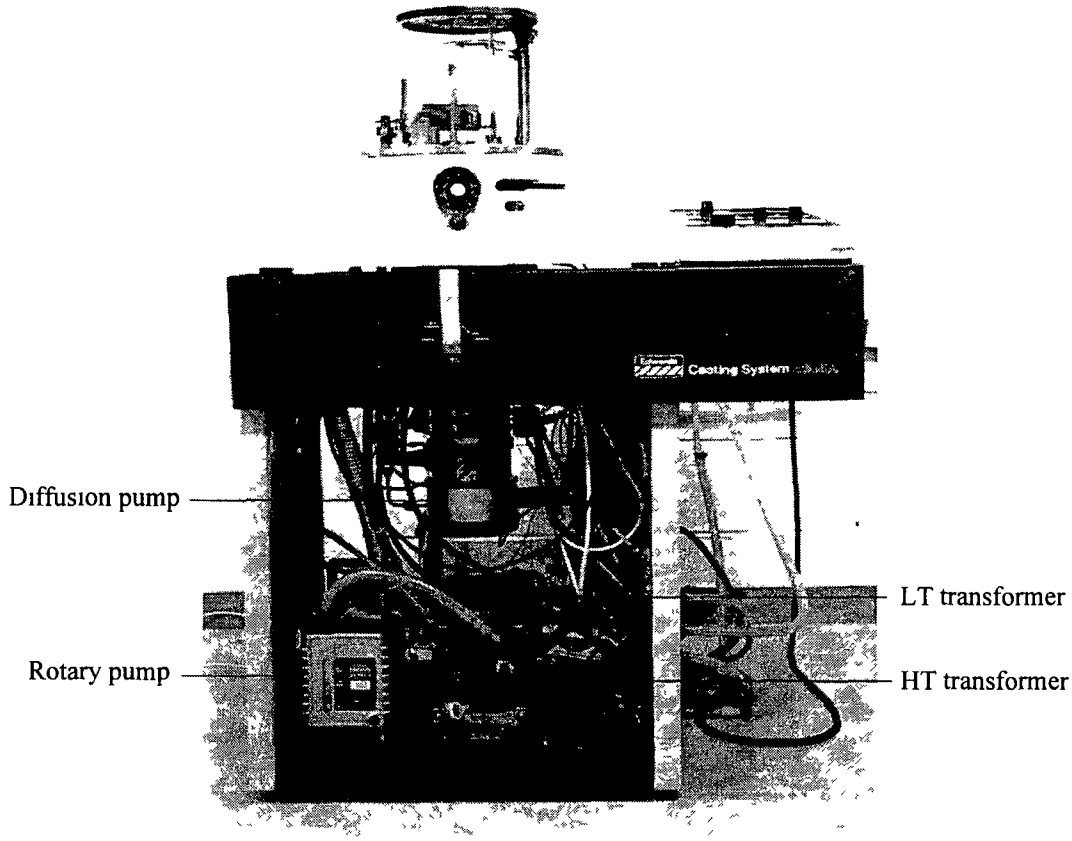


Fig A2 Photographs of resistance heating evaporator indicating HT transformer, LT transformer, rotary pump and diffusion pump

A close-up of the base plate of the system is shown in Fig A3 W boats were used for the evaporation of all metals, except Al For Al evaporation, a W coil was used The system has three shutters The substrate shutter was used to isolate the substrates from the source when outgassing of the system occurs The second shutter, known as the crystal shutter, was used with the crystal thickness monitor The third shutter, known as the source shutter, was used to isolate the HT and LT boats so that metal inter-mixing does not occur

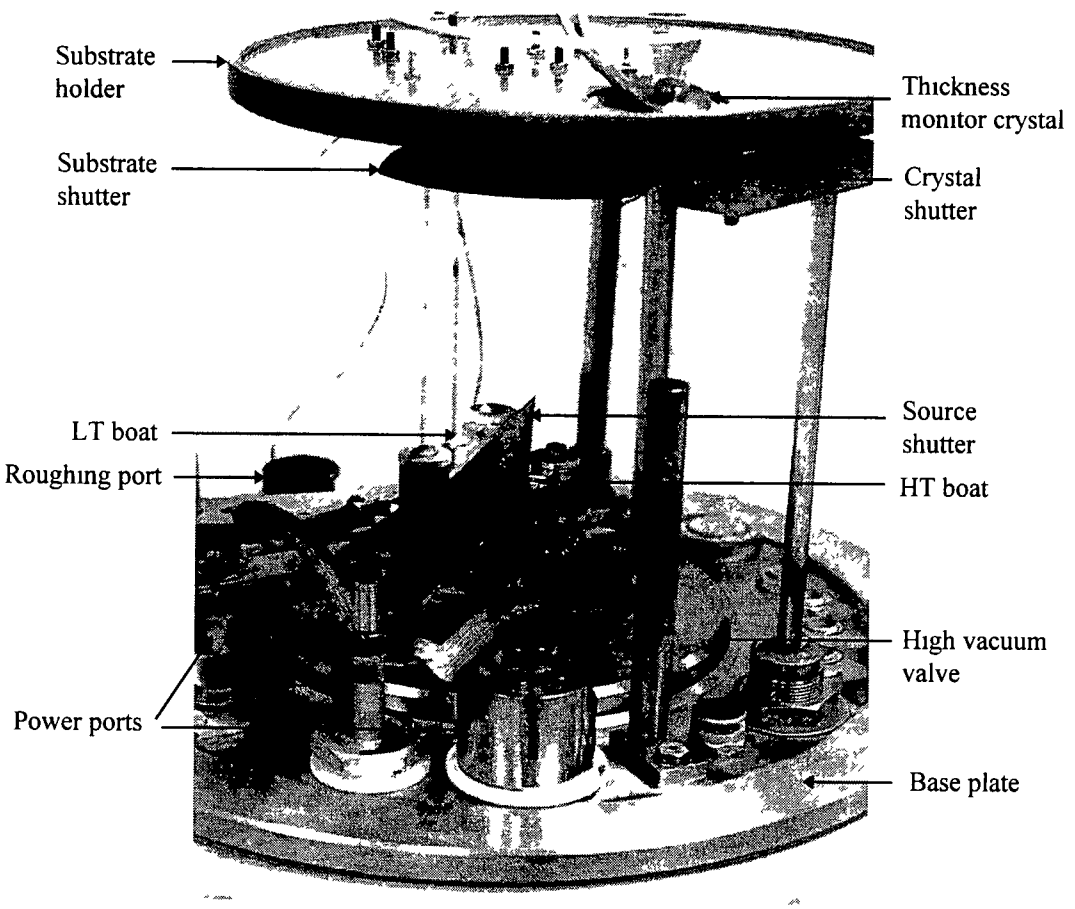


Fig A3 Detailed photograph of base plate of the evaporator Shutters and other components are indicated

Appendix B

Graphite strip annealer

The graphite strip annealer is shown in Fig B1 The main components of the annealer are a rotary pump, transformer, thermocouple with monitor, annealing chamber, cooling water system and annealing ambient The system is newly designed and built Forming gas (5% H_2 + 95% N_2) is used for the annealing ambient A valve (Fig B1) is used to isolate the pump from the annealing chamber during annealing

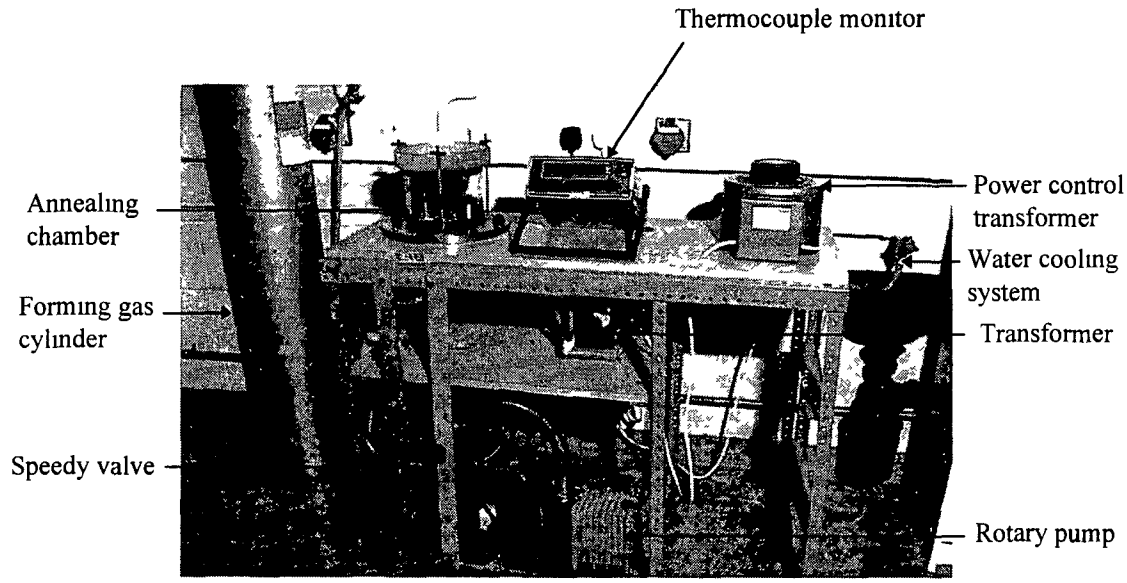


Fig B1 Photograph of the graphite strip annealer indicating main components

A close-up of the base plate is shown in Fig B2 The graphite strip is held by the water cooled power ports The middle of the graphite strip is thinned and its surface area is reduced to achieve higher temperature A small hole is drilled in this thinned region for the thermocouple Samples are placed next to this hole so that accurate sample temperature is monitored The rate of temperature rise is ~10 ^{0}C/s up to 400 ^{0}C and above 400 ^{0}C this rate falls slightly The temperature fall rate is higher than the rise rate and is ~12 ^{0}C/s up to 200 ^{0}C Below 200 ^{0}C, this fall rate reduces The maximum attainable temperature of this annealer is 550 ^{0}C

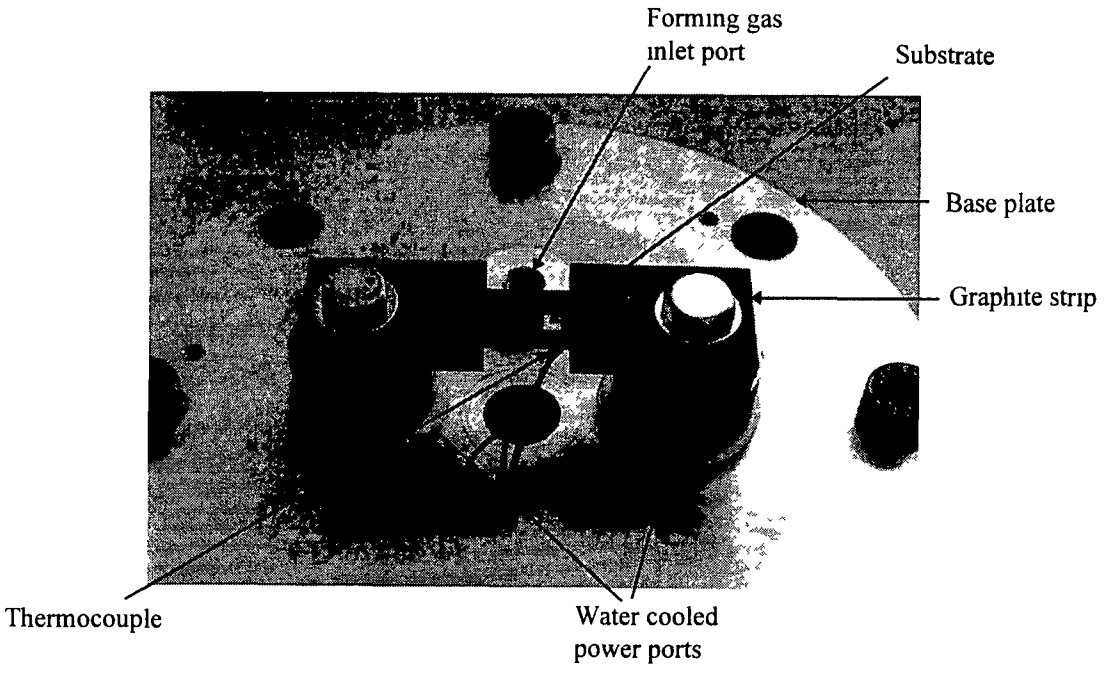
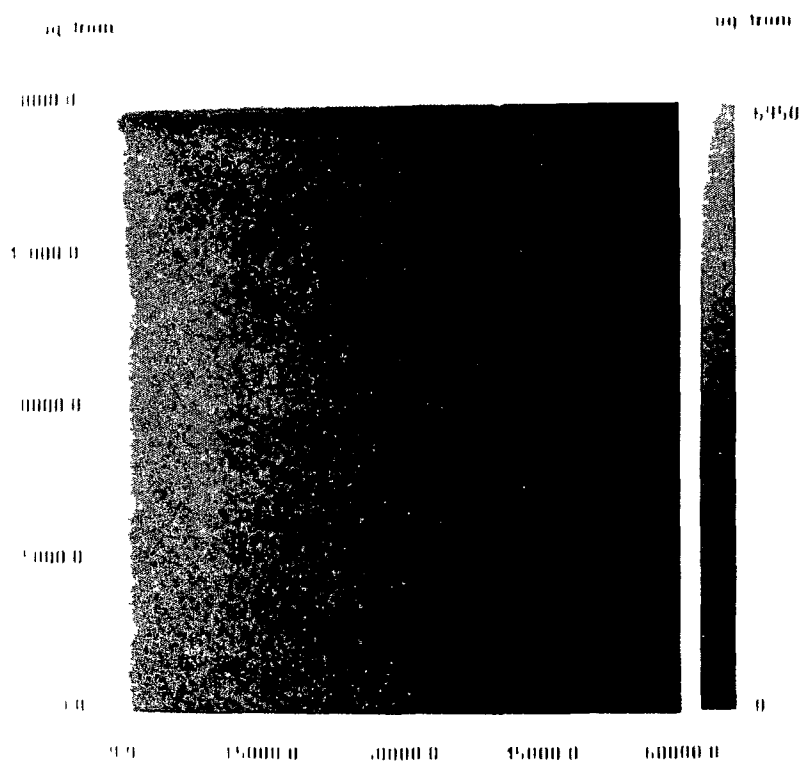


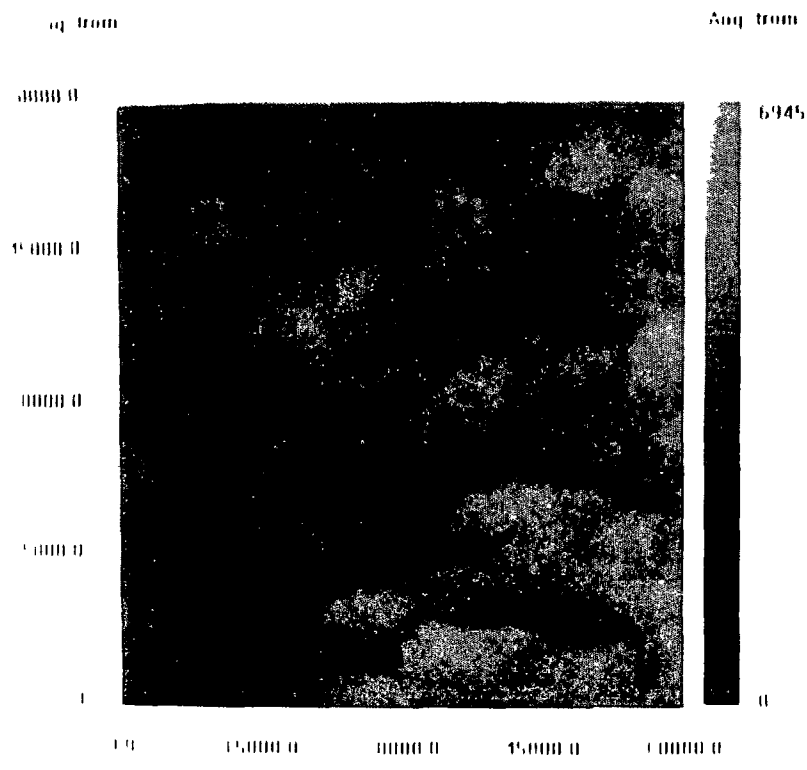
Fig B2 Photograph of base plate of the graphite strip annealer indicating various components

Appendix C

Original STM photographs of the Pd/Sn contacts to GaAs(SI)

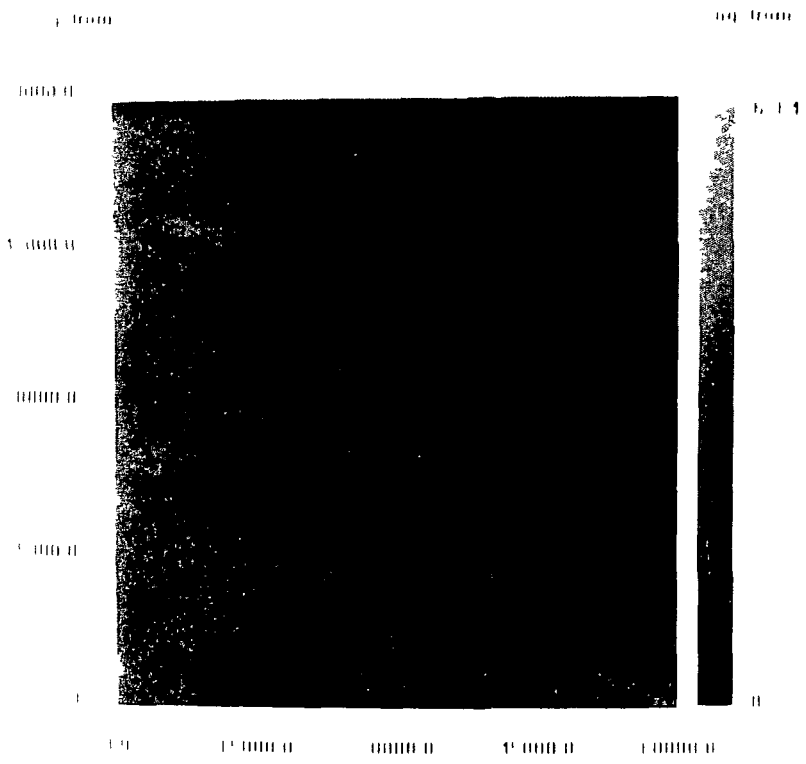


Sample A (as-deposited)

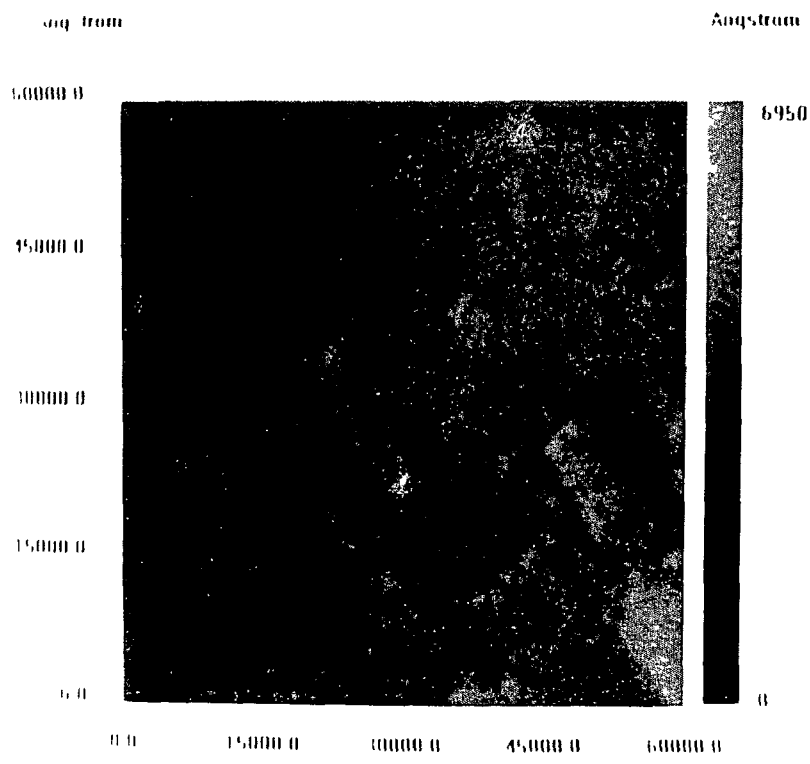


Sample A (200 ^{0}C 10 mm)

Fig 3 2 Original STM photographs of sample A

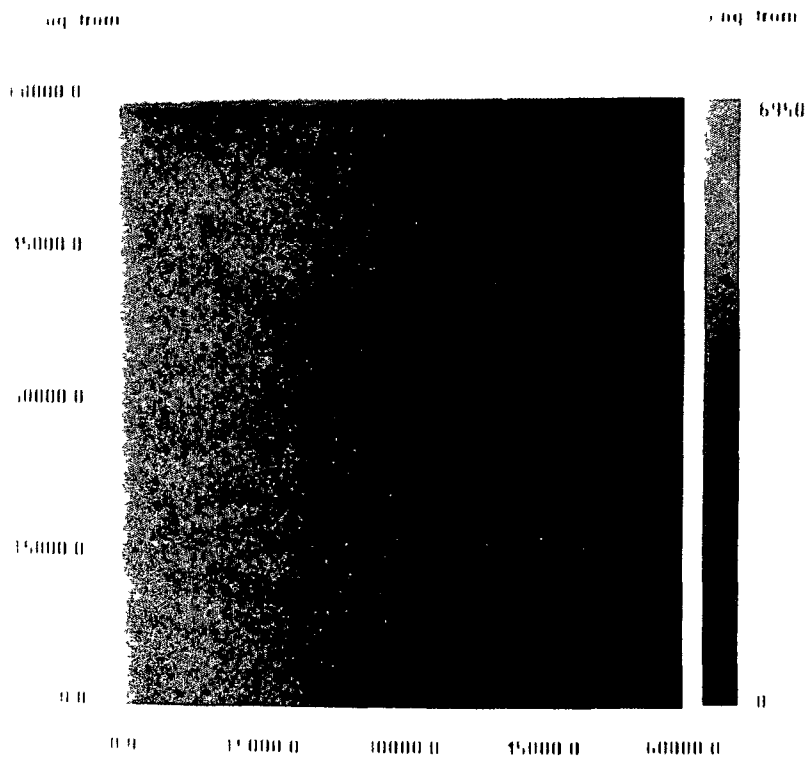


Sample E (as-deposited)

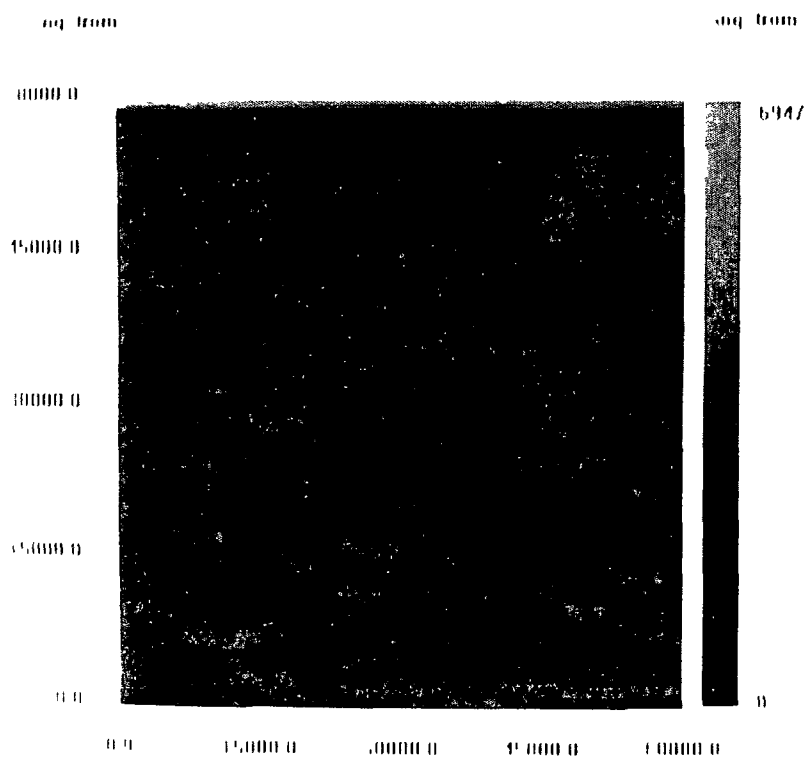


Sample E (200 ^{0}C 10 min)

Fig 3 2 Original STM photographs of sample E

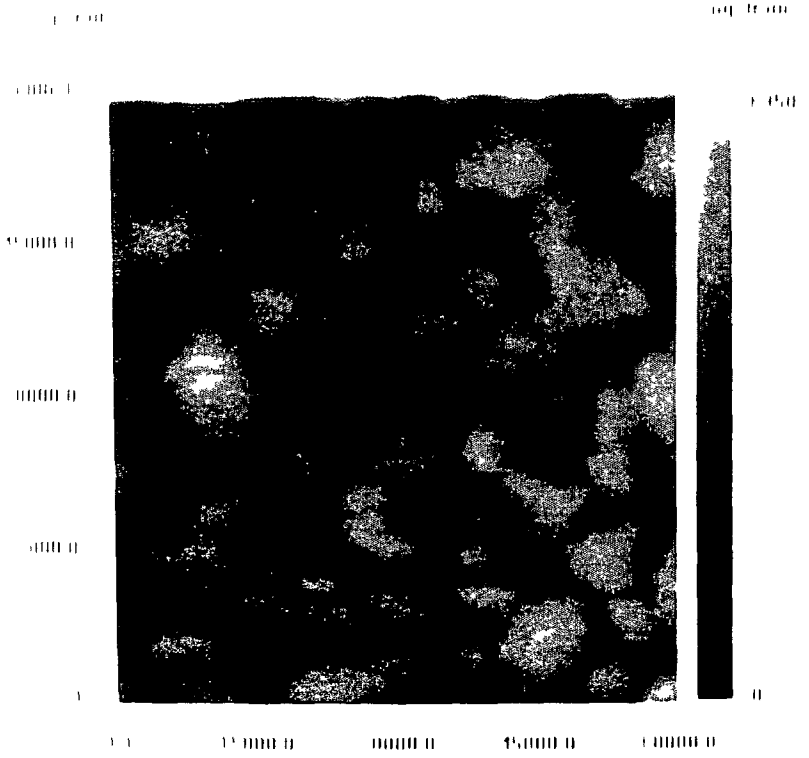


Sample G (as-deposited)

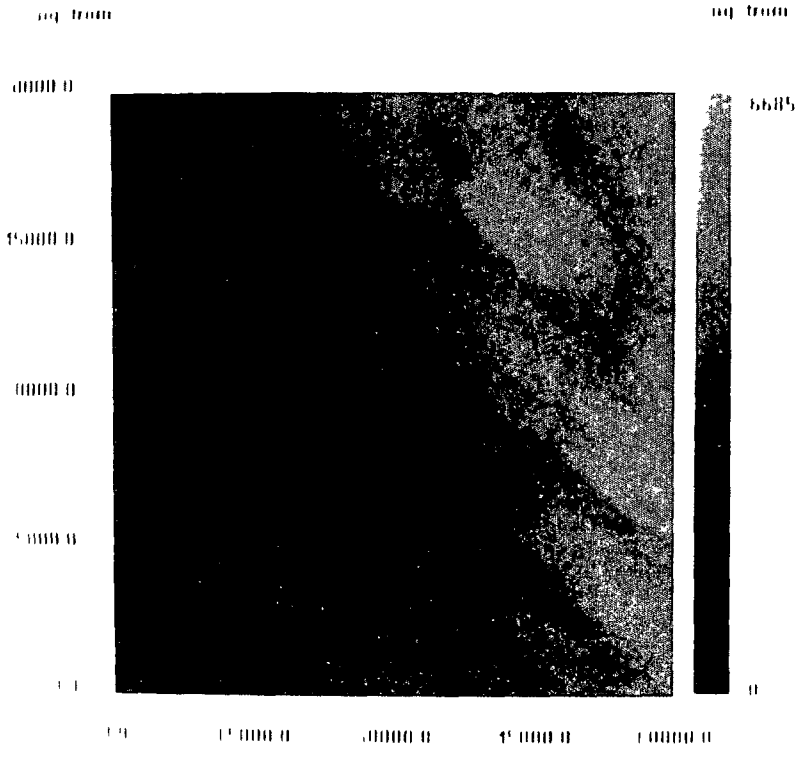


Sample G (200 ^{0}C, 10 min)

Fig 3 3 Original STM photographs of sample G

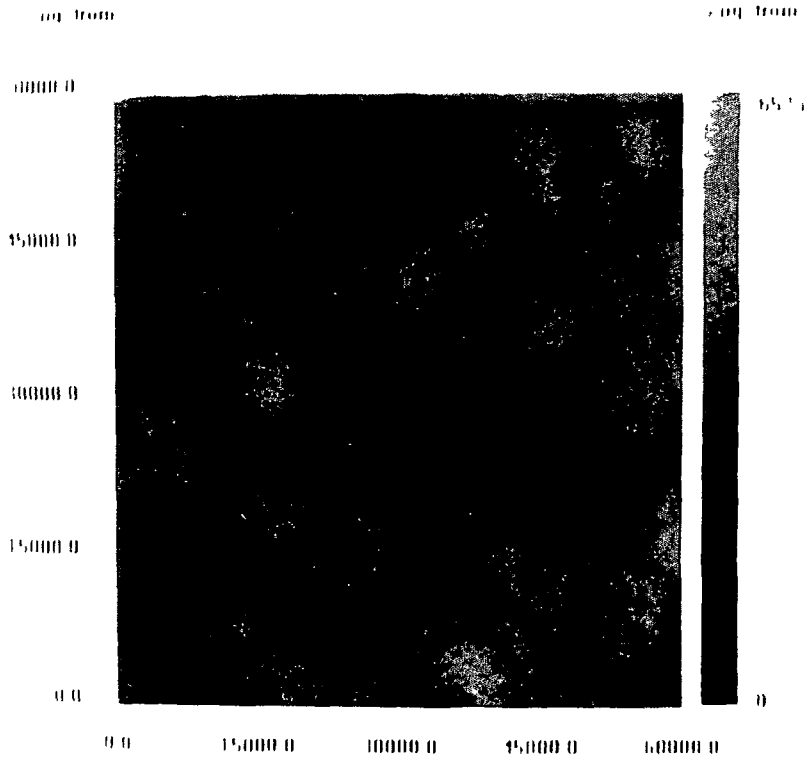


Sample H (as-deposited)

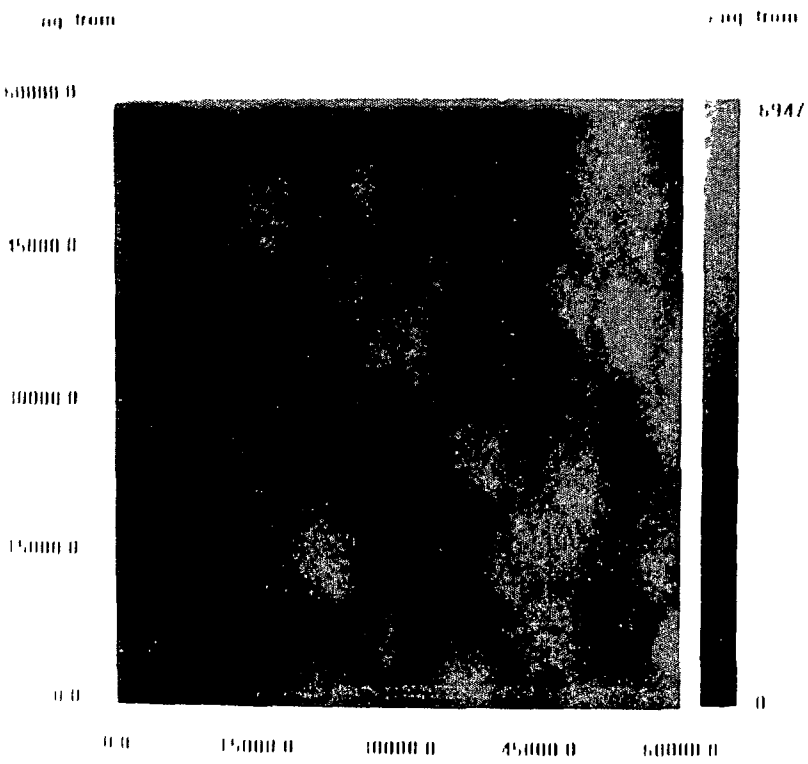


Sample H (200 ^{0}C 10 min)

Fig 3 3 Original STM photographs of sample H

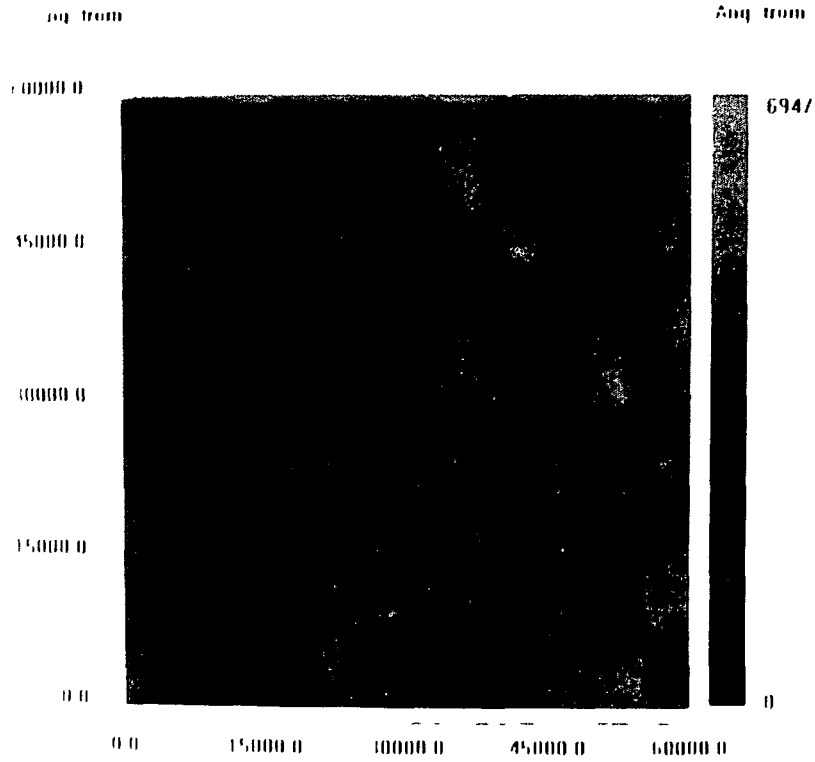


Sample E (350 ^{0}C 10 min)

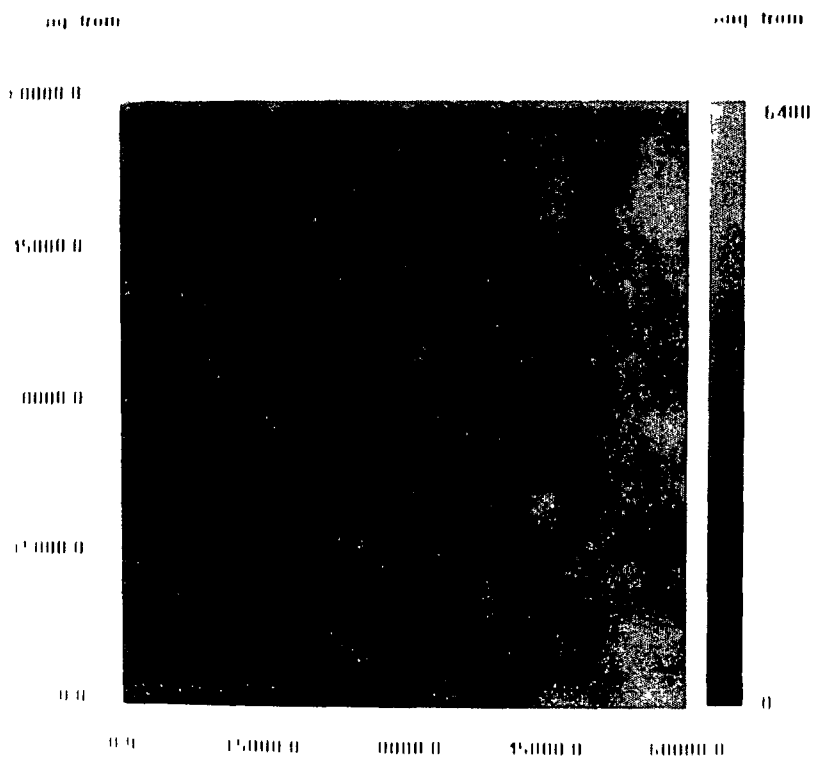


Sample E (400 ^{0}C 10 min)

Fig 3 5 Original STM photographs of sample E

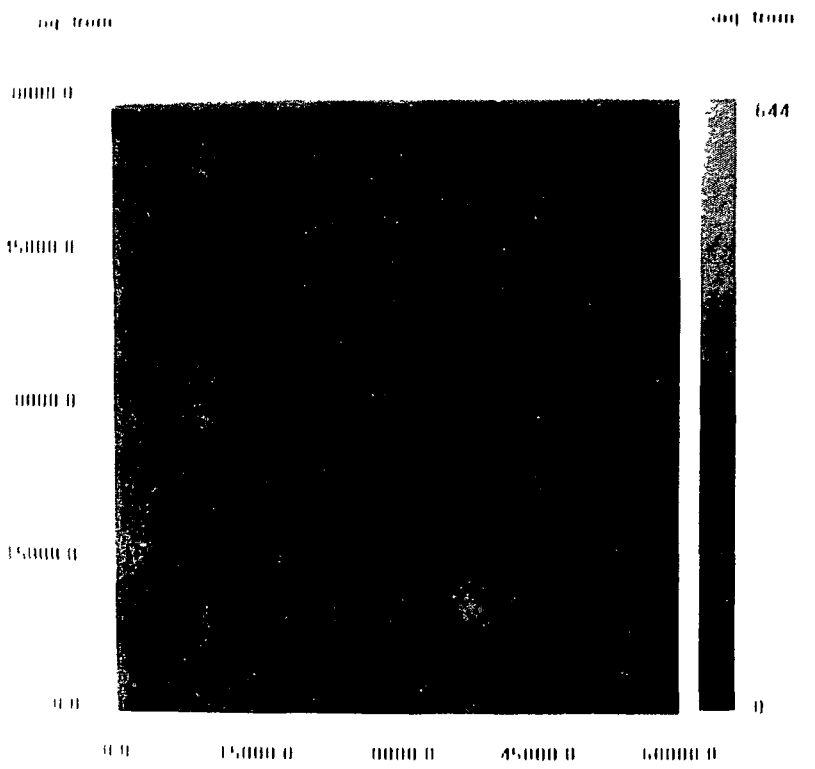


Sample H (350 ^{0}C, 10 min)

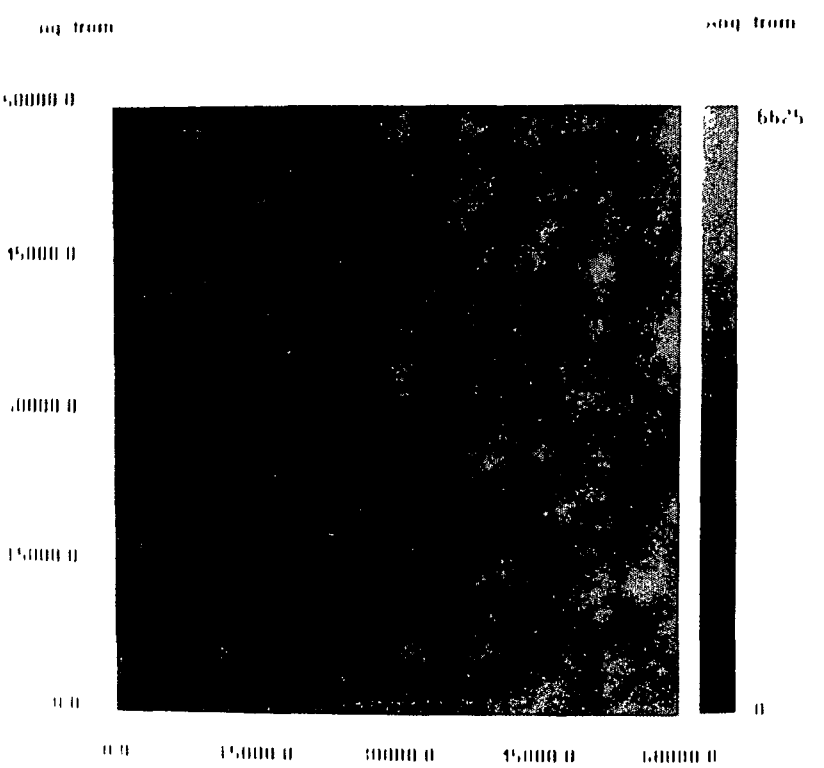


Sample H (400 ^{0}C 10 min)

Fig 3 5 Original STM photographs of sample H



Sample A (350 ^{0}C, 10 mm)



Sample A (400 ^{0}C, 10 mm)

Fig 3 6 Original STM photographs of sample A

Appendix D

Calculation of pinch off voltage

The relationship between the pinch off voltage, V_P, and the channel depth, d, is given by

$$d = \sqrt{\frac{2\varepsilon_s (V_P + V_B)}{qN_D}}$$

where ε_s = intrinsic permittivity = 13 1 x 8 85 x 10^{12} F/m

V_B = Built in potential = 0 8V

q = electronic charge = 1 9 x 10^{-19}C

N_D = donor concentration = 5 0 x 10^{23} m^{-3}

Thus when d = 0 12 μm, V_P = 5V

Appendix E

Publications based on this work

1 M S Islam, P J McNally, D C Cameron and P A F Herbert, "The Importance of the Pd to Sn Ratio and Annealing Cycles on the Performance of Pd/Sn Ohmic Contacts to n-GaAs," *Thin Solid Films*, 1996 (in press)

2 M S Islam, P J McNally, D C Cameron and P A F Herbert, "Effects of Au Overlayers on the Electrical and Morphological Characteristics of Pd/Sn Ohmic Contacts to n-GaAs," *Thin Solid Film*, 1996 (in press) (presented at the Int Conf on Metallurgical Coatings and Thin Films (ICMCTF'96), San Diego, CA, USA, 22-26 April 1996)

3 M S Islam, P J McNally, D C Cameron and P A F Herbert, "Comparison of Pd/Sn and Pd/Sn/Au Thin-Film Systems for Device Metallization," *Mater Res Soc Symp Proc*, Vol 427, 1996 (Mater Res Soc (MRS) 1996 Spring Meeting, San Francisco, USA, 8-12 April 1996) (in press)

4 M S Islam, P J McNally, D C Cameron and P A F Herbert, "Ohmic Contacts to n-type GaAs made with Pd/Sn and Pd/Sn/Au Metallizations," *Proc of the 8th Mediterranean Electrotechnical Conf (melecon '96)*, Bari, Italy, 13-16 May 1996, pp 385-388

5 M S Islam, P J McNally, D C Cameron and P A F Herbert, "Effects of Annealing Cycles on the Electrical and Morphological Characteristics of Pd/Sn Ohmic Contacts to n-GaAs," *Proc of the 8th Mediterranean Electrotechnical Conf (melecon '96)*, Bari, Italy, 13-16 May 1996, pp 1294-1297

6 M S Islam, P J McNally, D C Cameron and P A F Herbert, "Characterization of Pd/Sn Ohmic Contacts on n-GaAs using Electrical Measurements, EDAX and SIMS," *Proc of the 3rd IEEE Int Workshop on High Performance Electron Devices for Microwave and Optoelectronic Applications (EDMO'95)*, King's College London, UK, 27 November 1995, pp 26-31

7 M S Islam, P J McNally, D C Cameron and P A F Herbert, "A Novel Pd-Based Ohmic Contact System for n-type GaAs A Structural, Morphological and Electrical Investigation," *Proc of the 6th European Conf on Applications of Surface and Interface Analysis '95 (ECASIA'95)*, Montreux, Switzerland, 9-13 October 1995, published by Wiley & Sons, pp 299-302

8 M S Islam, P J McNally, D C Cameron and P A F Herbert, "Properties of Pd/Sn Ohmic Contacts to n-GaAs," *Proc of the Int Conf on Advances in Materials and*

Processing Technologies '95 (AMPT'95), Vol I, Dublin City University, Ireland, 8-12 August 1995, pp 40-49

9 M S Islam, P J McNally and D C Cameron, "Palladium-Based Ohmic Contacts to n-type GaAs- A Review of Recent Advances," *Proc of the Int Conf on Advances in Materials and Processing Technologies '95 (AMPT'95)*, Vol I, Dublin City University, Ireland, 8-12 August 1995, pp 18-29

10 M S Islam, P J McNally and D C Cameron, "Thermal Stability of the Pd/Sn and Pd/Ge Ohmic Contacts to n-GaAs," *Int Conf on Metallurgical Coatings and Thin Films (ICMCTF'97)*, San Diego, CA, USA, 21-25 April 1997 (submitted)