

# Preparation and Temperature Cycling Reliability of Electroless Ni(P) Under Bump Metallization

Weimin Chen, Paul McCloskey, James F. Rohan, Patrick Byrne, and Patrick J. McNally, *Senior Member, IEEE*

**Abstract**—The reliability of electroless Ni(P) under-bump metallization (UBM) was evaluated via temperature cycling and solder bump shear strength tests. Commercial diodes and dummy dies fabricated in-house were used as substrates for the electroless Ni(P) UBM deposition. Solder bumps were formed after reflowing eutectic 63Sn37Pb solder foils over the Ni(P) UBM. The solder bump shear strength was measured before and after different temperature cycling. The results from this study showed that the UBM thickness and dimension had important effects on the solder bump shear strength and reliability. Both the larger UBM dimension and larger UBM thickness tended to induce higher stress in the UBM, which resulted in the lower solder bump shear strength and lower temperature cycling reliability. A better UBM structure solution for high current electronic packaging application is indicated in this paper.

**Index Terms**—Electroless Ni(P) deposition, electronic packaging, reliability, shear strength test, solder bump, thermal cycling, under-bump metallization (UBM).

## I. INTRODUCTION

WITH the trend towards higher power and lower voltage, the current levels passing through interconnections is expected to rise [1] and thermal dissipation of the device is expected to increase dramatically as a result of the high resistance of wire-bonding interconnection. This will lower the power efficiency of embedded devices, and increase the device operation temperature, leading to a decrease in device reliability. Thus, more efficient and expensive thermal management solutions will be required. This will result in higher cost and lower packaging density.

Unlike wire-bonding, solder bump interconnection has shorter connections and much lower resistance and inductance, and consequently the switching frequency of devices can be improved. It is suitable for 3-D packaging, thus high-density packaging is easily obtained, which opens up the possibility of smaller and lighter devices. Some manufacturers have already adopted this technique for power packaging at lower

power levels ( $<10$  W) [2]. Recently, Tyndall has succeeded in introducing solder bump interconnections for a 4.2-kW dc-dc converter for automotive applications with a much better thermal performance than the corresponding wire-bonding packaging [3].

As indicated above, the current carrying requirements for solder interconnects in the future are projected to significantly increase, consequently electromigration may become a serious reliability issue for the solder bump interconnections [4], [5]. Electromigration failure has been extensively studied for Al and Cu based interconnections in integrated circuits, though it is only in the last few years that electromigration failure in solder bump interconnection attracted the attention of researchers [4]. In the 2000 International Technology Roadmap for Semiconductors (ITRS) the current density limitation for electromigration failure is set to about  $2.6 \times 10^3$  A/cm<sup>2</sup> at 100 °C for 100 000 MTTF (mean time to failure) for eutectic SnPb solder. The operational current density is close to  $2.6 \times 10^3$  A/cm<sup>2</sup> or higher for an ambient temperature of 25 °C or a case temperature of 70 °C for some power devices [6].

Current density will decrease if one increases the overall solder bump cross-sectional size, thus electromigration failure in solder bump interconnection can be mitigated. As the solder bump provides an effective route for thermal dissipation, increasing the solder bump cross-section size is also useful for reducing the junction temperature. The overall solder bump cross-section size increase can be achieved through using either single larger or multiple smaller solder bumps. The first solution is simpler in structure and easier to achieve.

A UBM is usually necessary for achieving reliable solder bump interconnection. There are quite a few metals and metal sandwich combinations which can be used as the UBM [7]. Among them, the electroless nickel phosphorous [Ni(P)] UBM is becoming popular. Its effective and selective deposition features render it an attractive UBM preparation process [8]–[11]. Electroless Ni(P) plating plus solder paste printing and reflowing is the most economical solution for UBM and solder bumping. This process and the corresponding reliability issues have been the focus of recent research [7], [12]–[14].

In addition to the intrinsic stress introduced in the electroless plating process [15], the thermal expansion coefficient (TEC) mismatch between Ni(P) UBM and the underlying materials introduces thermomechanical stress in the Ni(P) UBM. Excessive stress will induce premature solder bump failure or long-term interconnection reliability issues. The bond pad dimension of power chips such as the commercial IXYS diodes utilized in this study can be as large as 1.45 mm  $\times$  1.45 mm or even larger [16]. Information about the feasibility of such UBM structures on large bond pads is useful for the development of solder bump interconnection for power packaging.

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W.-M. Chen is with Intel, Shanghai 200135, China (e-mail: chen-weimin@hotmail.com).

P. McCloskey, J. F. Rohan, and P. Byrne are with the Tyndall National Institute, Cork, Ireland.

P. J. McNally is with the Microelectronics Group, Research Institute for Networks and Communications Engineering (RINCE), Dublin City University, Dublin 9, Ireland.

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TABLE I  
SAMPLE PREPARATION CONDITIONS AND RELATED INFORMATION

Samples	A	B	C	D
Die	Commercial	Dummy	Dummy	Dummy
Al thickness ( $\mu\text{m}$ )	4	1	1	1
Pad dimension ( $\text{mm}^2$ )	1.45 $\times$ 1.45	1.45 $\times$ 1.45	1.45 $\times$ 1.45	0.8 $\times$ 0.8
Ni(P) UBM deposition process	Zincate	Zincate	Zincate-free	Zincate

TABLE II  
MEASURED UBM THICKNESS AND SURFACE  
ROUGHNESS FOR THE DIFFERENT SAMPLES

Samples	A	B	C	D
Ni(P) UBM thickness ( $\mu\text{m}$ )	1.8 $\pm$ 0.9	4.8 $\pm$ 0.4	5.7 $\pm$ 0.8	5.3 $\pm$ 0.5
Surface roughness ( $\mu\text{m}$ )	0.8 $\pm$ 0.38	0.3 $\pm$ 0.17	0.4 $\pm$ 0.3	0.2 $\pm$ 0.07
P% in Ni(P) UBM (wt%)	17.1	10.8	9.5	10.2

Sample size: more than 20

In this study, the reliability of the Ni(P) UBM with two different pad dimensions were assessed with air to air thermal cycling and solder bump shear strength. Valuable information was obtained for further solder bump structure optimization.

## II. EXPERIMENTS

The aluminium bond pads used in this study were 1.45 mm  $\times$  1.45 mm (for *A*, *B*, and *C*) or 0.8 mm  $\times$  0.8 mm (for *D*) in size. In-house dummy dies (*B*, *C*, and *D*) and commercial diode dies (IXYS Corporation, Santa Clara, USA) (*A*) were used for the electroless nickel UBM deposition. The Ni(P) UBM of samples *A*, *B*, and *D* were deposited with the conventional zincate process [7], [14], while the Ni(P) UBM of sample *C* was deposited with a simpler in-house developed zincate-free process [17]. In this process, the wafer was etched in a 10% peroxide/ammonia solution prior to an isopropyl alcohol rinse and then the substrate was immersed directly in electroless nickel bath. The nickel bath used was a commercial solution Nimax SB provided by Canning U.K. (now McDermid). The sample preparation conditions and related information are summarized in Table I. The UBM deposition time for samples *A*, *B*, and *C* was 30 min, and for sample *D* was 26 min.

The UBM surface morphology was analyzed using a Hitachi S-4000 scanning electron microscope (SEM), an attached Princeton Gamma-Tech Energy dispersive x-ray (EDX) spectroscopy analysis system was used for the phosphorous content analysis in Ni(P) UBM.

The Ni(P) UBM thickness and surface roughness was measured with a Tencor Alphastep 200 surface profilometer. The thickness and roughness of each sample listed in Table II is the average value for more than 20 measurements across the wafer.

The interface structures between different layers in the studied samples were analysed through cross-section preparation in epoxy molds or via the focused ion beam (FIB) etching method. Cross-sectioning involved mounting the samples in cold setting clear epoxy; the cured assemblies were then ground in a Metaserv 2000 grinder with sequentially more finely graded SiC papers, and finally polished with 1- $\mu\text{m}$  and 0.5- $\mu\text{m}$  alumina suspensions, respectively.

A fei 200DE FIB apparatus was used for the focused ion beam (FIB) etching of the Ni(P) UBM of sample *A* and *B* in a small

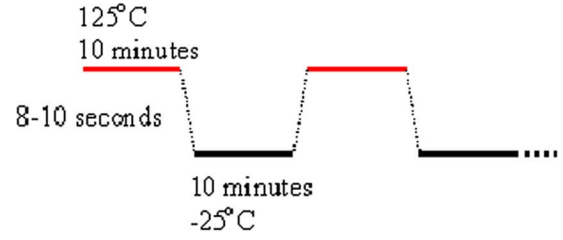


Fig. 1. Temperature profile for thermal cycling.

rectangular area for the observation of the Ni(P) UBM and the Al metallization interface structure.

Solder bumps were prepared by reflowing eutectic Sn37Pb solder foils over the Ni(P) UBM. The reflow was achieved in a programmable SRO-702 IR oven under  $\text{N}_2$  atmosphere with the peak temperature of 210  $^\circ\text{C}$ . The achieved height for the solder bumps was approximately 600  $\mu\text{m}$  (for samples *A*, *B*, and *C*) and 330  $\mu\text{m}$  (for sample *D*), respectively. No clean type Kester RMA rosin flux was used during reflow for higher quality solder bumps.

The thermal cycling test was conducted according to the temperature profile of Fig. 1 with the high and low temperatures being 125  $^\circ\text{C}$  and  $-25^\circ\text{C}$ , respectively. The transition time between the two temperatures is around 8–10 s.

The shear strength of solder bumps as-prepared and after various temperature cycling was measured and analysed. The measurement was performed using a Royce System 552 Universal bond tester at room temperature with a shear rate of 500  $\mu\text{m/s}$ . The gap between silicon and the tip of the shear tool was about 50  $\mu\text{m}$ . For all the samples, 15 bumps were sheared for each test condition, and an average solder bump shear strength was obtained.

## III. RESULTS AND DISCUSSION

### A. Electroless Ni(P) UBM Preparation

The average UBM thickness and the phosphorous content of the various samples are listed in Table II. It shows that the phosphorous content for each of the samples is different. The phosphorous content for substrates plated from the same bath and at the same pH and temperature differs as a result of the plating rate experienced by each of the samples. Sample *A* deposits at the lowest rate and has the highest P content. This is to be expected based on the information provided by the solution supplier (Nimax SB, Technical Data Sheet 2543, Wm Canning, Ltd., Birmingham, UK). The plating rate is influenced by the substrate processing during aluminium deposition, subsequent dielectric deposition, bond pad chemical treatment for cleans, etchants, zincate treatment, and finally nickel deposition, etc. The much thinner UBM of sample *A* may be due to the Al pad surface contamination. A thin layer of organic contamination often exists on the aluminium pad surface for the as-received commercial devices [18]. Such contamination was confirmed by Fourier Transform Infrared Spectroscopy (FTIR) analysis for sample *A*. This organic contamination hinders the zinc seed deposition and growth, and consequently affects (reduces) the nickel nucleation and deposition rate [19].

Fig. 2 shows examples of typical cross-sectional optical images for as-plated large pad samples. The roughness for sample

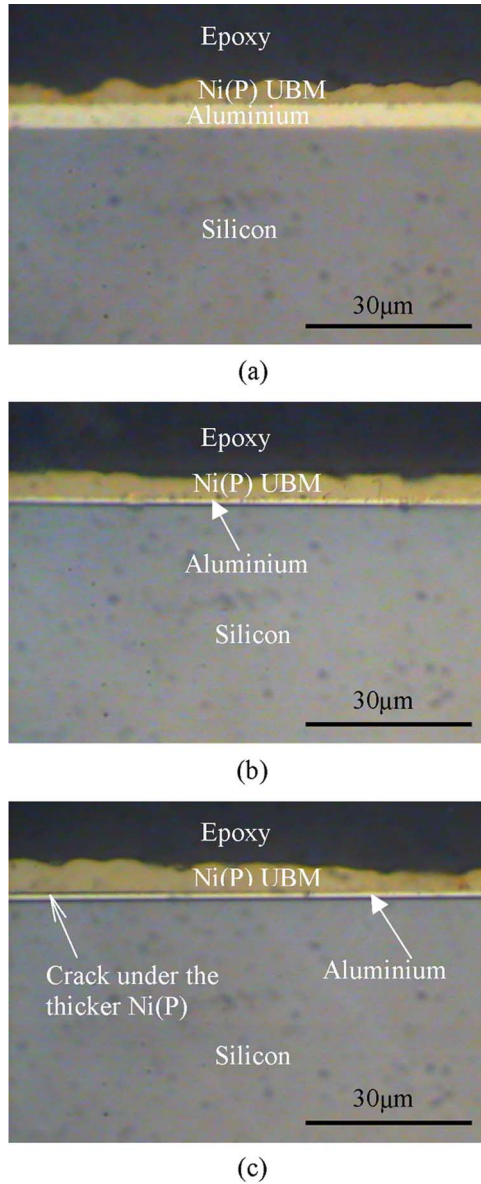


Fig. 2. Typical cross-sectional optical images for different samples: (a) sample A; (b) sample B; and (c) sample C.

A is approximately  $0.8 \mu\text{m}$  while that of sample B and C is much lower,  $0.3 \mu\text{m}$  and  $0.4 \mu\text{m}$ , respectively. Results in [20] indicated that the surface roughness of the Ni(P) UBM increased with decreased phosphorous content. The Ni(P) had a hyper-eutectic composition and the surface image was unclear with a high phosphorous content ( $>11 \text{ wt.\% P}$ ). The UBM surface image became clearer and the Ni(P) particle size increased with a decrease of the phosphorous content. Such UBM surface morphology is confirmed by samples A, B, C (Fig. 3) and our recent study [11]. However, the surface roughness measurement results in this study do not show this trend. This is due to the different surface conditions (commercial diode and dummy die) and different deposition methods (zincate and zincate-free) involved in this study.

For sample C, it can be observed that the UBM thickness differs from one region to another as shown in Fig. 2(c), the UBM being thicker in the left hand side. The Tencor thickness

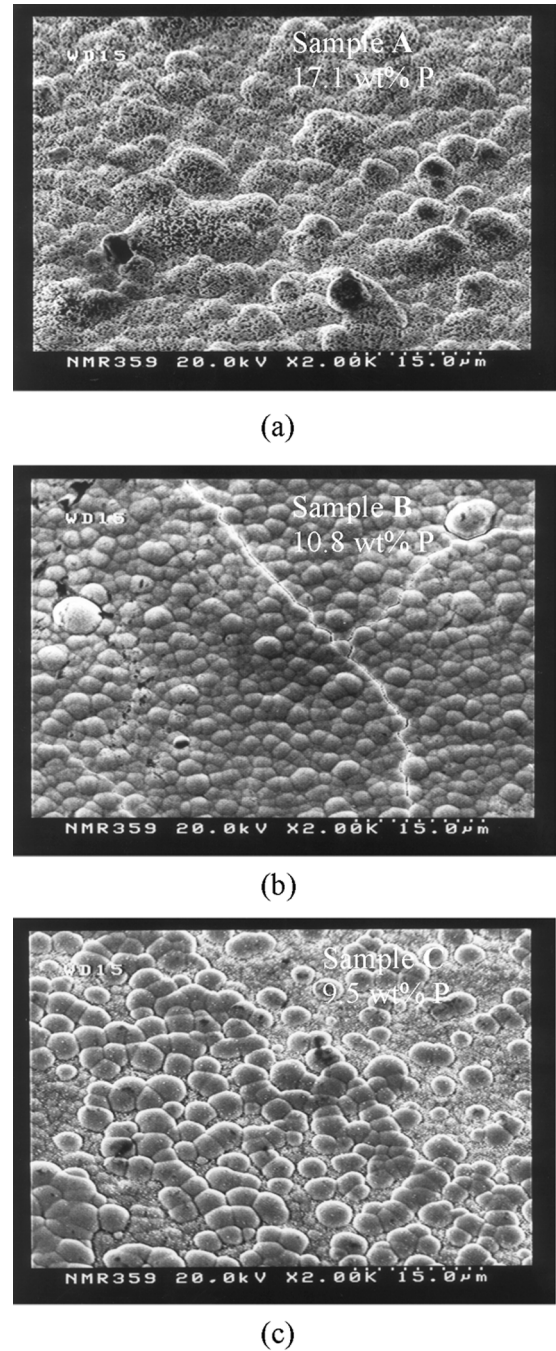


Fig. 3. Surface morphology of the Ni(P) UBM for (a) sample A, (b) sample B, and (c) sample C. The surface image of sample A is unclear, and the Ni(P) particle size of samples B and C increases with decreasing of the phosphorous content.

profile (Fig. 4) indicates an island UBM growth feature for this sample. This suggests that the Ni(P) UBM has different deposition rates on different parts of the pad. The high UBM surface roughness ( $\sim 0.4 \mu\text{m}$ ) is partially due to this nonuniform Ni(P) thickness. Unlike the other samples, C, was deposited with the zincate-free process. This process can deposit uniform and well adhered Ni(P) UBMs on small Al pads ( $40 \mu\text{m} \times 40 \mu\text{m}$ ) [17]. The nonuniform UBM deposition over the large pads,  $1.45 \text{ mm} \times 1.45 \text{ mm}$ , of this process may be due to incomplete protection of the aluminium pad after the peroxide etch and



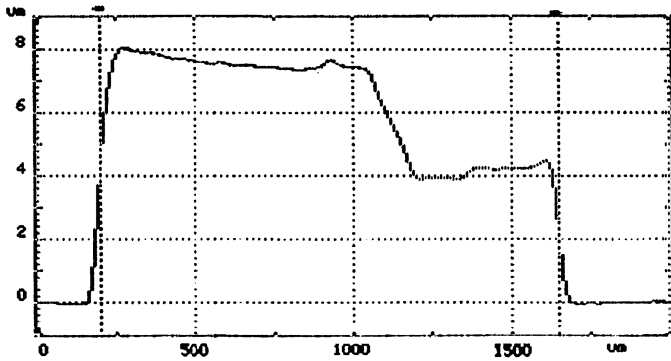


Fig. 4. Typical Ni(P) UBM height profile for sample *C* showing nonuniform UBM thickness.

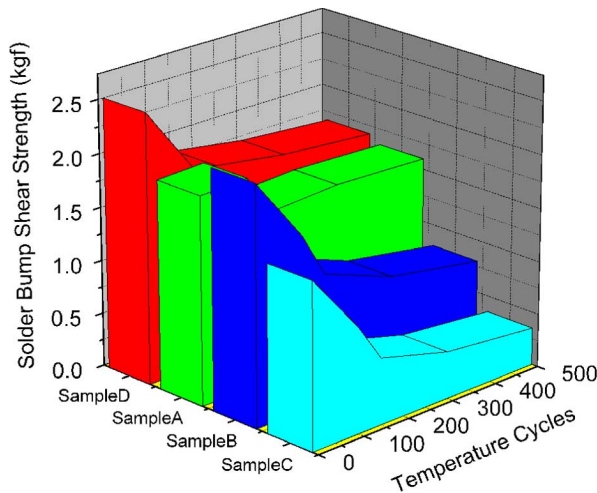


Fig. 5. Shear strength for solder bumps as-prepared and after various thermal cycles.

before the nickel deposition. The initiation of electroless nickel deposition will be impeded on certain areas of these large bond pads where a reoxidation of the aluminium takes place given that the aluminium is not protected with zinc as in the zincate process. This result suggests that zincate-free process which works well on small bond pads achieves less uniform electroless nickel deposits on larger pads and less uniform deposits than the alternative zincate process.

#### *B. Larger Bond Pad Solder Bumps Thermal Cycling Reliability and Failure Mechanisms*

Solder bump shear strength of samples *A*, *B*, and *C* after various thermal cycles (0, 100, 150, 300, and 500 cycles) is shown in Fig. 5. The highest average solder bump shear strength before temperature cycling of these samples was 2.24 kgf for sample *B*.

After thermal cycling, the shear strength for all samples initially decreased dramatically then gradually. There were three solder bump failure modes for these samples, i.e., solder failure, cratering in the silicon and interface delamination between Ni(P) UBM and the underlying aluminium metallization. Table III lists the prevalence of the solder bump failure modes.

During shear tests, if the shear force is higher than the solder strength while the interface adhesion is higher than the net

interface strength, solder bumps will fail inside the solder; however if the net interface stress is higher than the interface adhesion, interface delamination will become a failure mode. The net interface stress is the sum of the internal interface stress and shear tool induced force during tests. The internal interface stress includes the intrinsic and extrinsic stress [14], [21]. Intrinsic stress is due to plating defects, such as, hydrogen, vacancies and micro-voids, etc. The defect reduction induced in Ni(P) UBM densification introduces the intrinsic tensile stress [15], [21], [22]. Extrinsic stress is caused by thermo-mechanical stress due to temperature changes and the TEC mismatch between the different layers [21], [23]. A two dimensional ABACUS finite element analysis indicated that the extrinsic stress in the studied samples was tensile under room temperature.

Fig. 2(c) shows a typical cross-sectional optical image of sample *C*, the Ni(P) UBM delamination occurred in the thicker part, but it was absent in the thinner region. The as-plated Ni(P) UBM delamination occurred as the result of higher interface stress than the interface adhesion force. The above phenomenon indicates that the interface stress increases with the UBM thickness. Many factors may affect the stress in the film, such as the surface cleaning, substrate surface roughness, additives in the plating solution and the film thickness, etc. [22], [24], [25]. It is shown in the literature that the relation between stress and thickness of the deposited thin film is complicated. The stress reported may either decrease or increase with the thin film thickness, or the trend may change after reaching a certain deposit thickness [22], [24], [26].

A Ni(P) UBM thickness  $>5.8 \mu\text{m}$  resulted in delamination from the underlying Al metallization for sample *C*. This implies that the UBM thickness plays an important role in the solder bump reliability and must be tightly controlled. For sample *C*, 30% of the as-prepared solder bump samples failed via the interface delamination mode, and it became a main failure mode after 100 thermal cycles and finally became the only mode after 500 thermal cycles. In the reflowing process for solder bump formation and the subsequent thermal aging during thermal cycling, intermetallic compounds (IMCs) are formed between the solder and Ni(P) UBM [7], which will introduce tensile stress in the Ni(P) UBM [20]. In addition, the repeated TEC mismatch induced thermomechanical stress during thermal cycling also promotes the interface delamination, thus it gradually becomes a main failure mode for this sample after thermal cycling.

Sample *B* failed inside the solder before thermal cycling. However cratering in the underlying silicon became a main failure mode after thermal cycling tests (see Table III). The aluminium metallization of this sample was severely etched by the aggressive plating solution during the zincate process Fig. 6(a). This rough interface promoted good adhesion between the Ni(P) UBM and the underlying aluminium through mechanical interlocking. There were numerous cracks in the as-plated Ni(P) UBM of this sample, Fig. 3(b) shows such cracks in this sample. No cracks were observed in the other samples. These cracks were formed as the result of two factors, namely high internal stress in the Ni(P) UBM and the excellent adhesion between the Ni(P) UBM and Al metallization. The Ni(P)/Al interface adhesion, i.e., higher adhesion strength resulting

TABLE III  
STATISTICS FOR THE SOLDER BUMPS FAILURE MODES AND THEIR PERCENTILE PREVALENCE AFTER VARIOUS THERMAL CYCLES FOR THE FOUR TYPES SAMPLES

Temperature Cycles	As-prepared	100	150	300	500
<b>A</b>	100% solder fail	100% solder fail	5% interface fail; 95% solder fail	15% interface fail; 85% solder fail	20% interface fail; 80% solder fail
<b>B</b>	100% solder fail	70% cratering in Si; 30% solder fail	80% cratering in Si; 20% solder fail	95% cratering in Si; 5% solder fail	95% cratering in Si; 5% solder fail
<b>C</b>	30% interface fail; 70% solder fail	60% interface fail; 40% solder fail	60% interface fail; 40% solder fail	90% interface fail; 10% solder fail	100% interface fail
<b>D</b>	100% solder failed.	Mainly failed in solder; but 70% bumps failed partially at interface.	Mainly failed in solder; but 83% bumps failed partially at interface.	Mainly failed in solder; but 91% bumps failed partially at interface.	Mainly failed in solder; but 91% bumps failed partially at interface; 4% bumps failed partially with silicon cratering.

from the severely etching of the aluminium surface during the zincate process prevented the interface delamination of sample *B*. Consequently solder bumps of sample *B* did not fail via the delamination mode. During thermal cycling, the high TEC mismatch induced stress was repeatedly imposed on silicon under the UBM and micro-cracks develop in the silicon as shown in Fig. 7.

This image shows a cross-section of sample *B* after different thermal cycles. After 100 thermal cycles, cracks had developed in the Si under the Ni(P) UBM around their edges. While after 500 thermal cycles, cracks even became continuous in some regions of the underlying Si, such as shown in Fig. 7(b). Therefore most of the bumps failed via a Si cratering mode under the shear force during test (Table III).

Among the larger bond pad samples, i.e., samples *A*, *B*, and *C*, sample *A* displayed the highest shear strength after thermal cycling and it changed least after different numbers of thermal cycles. Solder bumps of this sample failed only in the solder before and at the early stage of thermal cycling. But after 150 thermal cycles, interface delamination similar to sample *C* started to become a failure mode, and its occurrence ratio increased with increasing of the thermal cycles. This interface delamination was again caused by the repeated TEC mismatch induced thermal stress during thermal cycling. The phase transformation induced stress due to the Ni(P) UBM/solder IMCs formation [7], [20] would also increase the interface delamination. These stresses promoted the expansion and merger of micro-cracks along the interface, and reduced the interface adhesion strength, which increased the tendency of interface delamination during shear tests. As a result, some samples failed through the interface delamination mode.

Due to the larger aluminium crystal size ( $\sim 400$  nm) for the commercial diode wafer pads of sample *A* than that of sample *B* ( $\sim 80$  nm) [27], the aluminium surface of sample *A* was not etched as severely as that of sample *B* during the zincate Ni(P) UBM deposition process [as shown in Fig. 6(b)].

The mechanical interlocking effect, which provided the high interface adhesion, in the UBM/Al interface of sample *A* was not as strong as that of sample *B*. For sample *C*, where the zincate-free process was less severe by comparison with the zincate process, the Ni(P) UBM/Al interface of this samples was also relatively smooth. Therefore the Ni(P) UBM/Al interface adhesion for these two samples were lower than that of sample *B*. Consequently cracks would not develop in the Ni(P) UBM even if there was high internal stress in it (for example, in sample *C*) and cratering in silicon similar to sample *B* was not a failure mode for these two samples. Interface delamination instead became a failure mode.

The relative higher solder bump shear strength and better thermal cycling reliability for sample *A* are most likely due to its thinner UBM and thicker aluminium pad. As mentioned previously, a thinner UBM introduces lower interface stress. The thicker aluminium pads of the commercial wafer substrates used in this study relieves part of the stress built in the Ni(P) UBM. Consequently higher solder bump shear strength and temperature cycling reliability were achieved for this sample. However, the thin UBM ( $\sim 1.8$   $\mu\text{m}$ ) would induce other reliability problems. Experimental results have indicated that the Ni(P) UBM would be consumed by solder during reflow and high temperature operation [7]. After thermal aging at 150 °C for 1500 h, a Ni(P) UBM with a thickness of about 4.5  $\mu\text{m}$  as-plated thinned to about 3.2  $\mu\text{m}$  in the eutectic Pb-free Sn3.5Ag solder bump, and the remaining Ni(P) UBM turned into a cracked P-rich Ni(P)-compound layer. This P-rich layer would continue to be consumed by the solder under high temperature operation [7]. In other words, the Ni(P) UBM will thin and finally be consumed completely, leading to the solder and aluminium having direct contact, at which point the solder bumps will lose adhesion to the underlying aluminium and cause open circuit failure for the device. Thus a thin Ni(P) UBM, like that of sample *A*, may induce reliability problems for devices used at high operation temperature. This

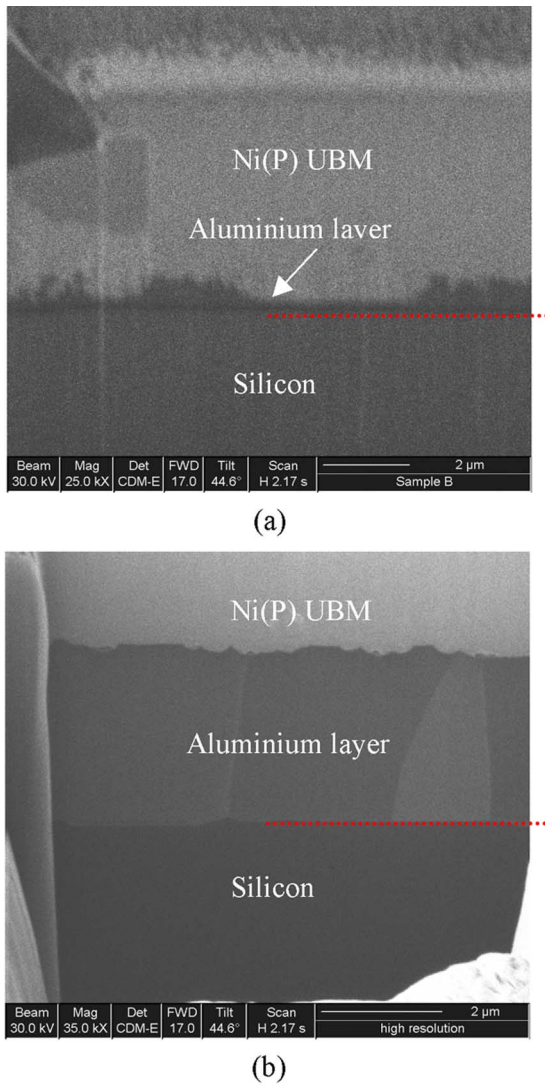


Fig. 6. Ni(P) UBM and the underlying Al metallization interface structure shown with the FIB images: (a) sample *B* and (b) sample *A*.

is especially true for power devices. An appropriate Ni(P) UBM thickness should be maintained.

### C. Smaller Bond Pad Solder Bumps Thermal Cycling Reliability

The cross-sectional optical image of the smaller pad sample, *D*, showed that its Ni(P) UBM adhered well to the underlying aluminium, i.e., no Ni(P)/Al interface delamination. Actually cross-sectional optical images showed that, even when the Ni(P) UBM thickness was about  $9\ \mu\text{m}$ , it still adhered well to the underlying aluminium for a pad size of  $0.8\ \text{mm} \times 0.8\ \text{mm}$ . A thicker Ni(P) UBM ( $13\ \mu\text{m}$  or thicker) lifted off from the underlying aluminium. These results confirm the earlier contention that the interface stress between the Ni(P) UBM/Al interface increases with UBM thickness.

As indicated earlier, the Ni(P) UBM for larger bond pads ( $1.45\ \text{mm} \times 1.45\ \text{mm}$ ) either lifted off from the underlying aluminium when its thickness was around  $5.8\ \mu\text{m}$  (sample *C*, with low adhesion strength), or cracked when its thickness is around  $4.8\ \mu\text{m}$  (sample *B*, with high adhesion strength). Each situation resulted in a lower thermal cycling reliability for solder bumps.

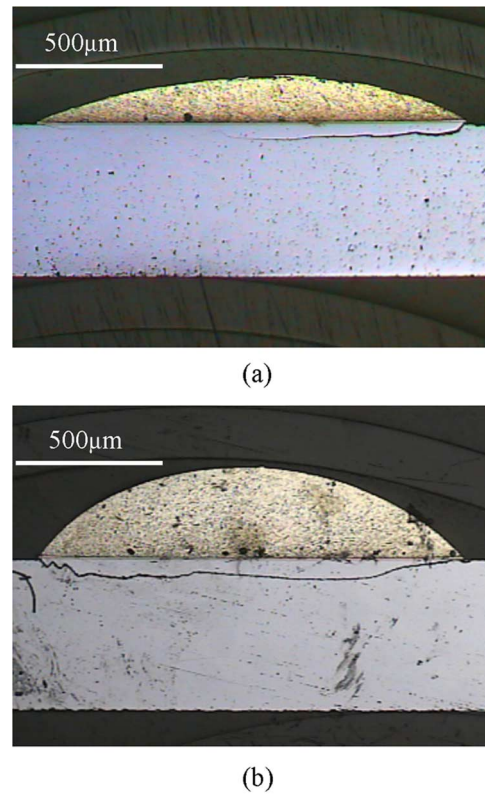


Fig. 7. Cross-sectional optical image of sample *B* after various thermal cycles: (a) After 100 cycles—close to the edge of solder bump and (b) After 500 cycles—closer to the centre of solder bump as compared to (a). Sections not carried out at the same location relative to the centre of the bump. Hence height of bump on sections appears different.

But for smaller bond pads ( $0.8\ \text{mm} \times 0.8\ \text{mm}$ ), a thicker Ni(P) UBM (before reaching  $9\ \mu\text{m}$ ) did not lift off from the underlying aluminium, nor were cracks observed in such UBM. Therefore smaller pad appeared to induce lower stress in the Ni(P) UBM.

The solder bump shear strength of sample *D* after various thermal cycles is also shown in Fig. 5. The corresponding solder bump failure modes are listed in Table III. Similar to samples *A* and *B*, the as-prepared solder bumps failed only inside the solder, and the shear strength was  $2.53\ \text{kgf}$ , which was higher than any of the corresponding values for the larger pad samples *A*, *B*, or *C*. Examples of more strongly adhered deposits on smaller bond pads have been given in the literature. In [8], Hutt *et al.* achieved  $5.8\ \text{kgf/mm}^2$  for  $580\text{-}\mu\text{m}$  octagonal bond pads. In [23] a value of  $13\ \text{kgf/mm}^2$  was achieved for  $100\text{-}\mu\text{m}$  square pads.

After thermal cycling tests, the failure location of sample *D* was still mainly inside the solder. For some bumps partial Ni(P) UBM/Al interface delamination was observed during shear tests, i.e., part of the UBM broke and delaminated from the underlying aluminium. These occurred mainly around bump edges. As shown in Table III, the prevalence of this failure mode increased with thermal cycling. This partial Ni(P) UBM/Al interfacial delamination was again due to the interface stress related to the solder bump structure, solder bump fabrication process and IMCs formation induced phase change, as well as the high strain caused by the shear tool during shear test [14]. Furthermore, the repeated high thermo-mechanical stress

during thermal cycling would introduce some micro-cracks (micro-delamination) in the Ni(P) UBM/Al interface of this sample. Such micro-cracks increased with the thermal cycling. Consequently, this partial Ni(P) UBM/Al interface delamination occurred more easily during shear strength measurement after high numbers of thermal cycles.

As shown in Table I, sample *D* and *B* were prepared with the same conditions. Like sample *B*, the Ni(P) UBM/Al interface adhesion strength for sample *D* is high. The partial silicon cratering after 500 cycles was also the result of micro-crack formation in silicon during cycling because of the high thermo-mechanical stress and good interface adhesion.

Although partial interface delamination, or partial silicon cratering, occurred for sample *D* during shear tests, no complete interface delamination or cratering was observed. Fig. 5 indicates that the solder bump shear strength of this sample is higher than that of other samples after different thermal cycles. Therefore sample *D*, with smaller bond pads, is more reliable than larger bond pad samples. Additionally, the UBM of sample *D* was as thick as  $5.3\ \mu\text{m}$ , which could survive more than 1500-h thermal aging at  $150\ ^\circ\text{C}$  for both the eutectic Sn37Pb solder and Pb-free eutectic Sn3.5Ag solder [7]. Given the increased adhesion strength with decreasing pad area listed above it may be expected that smaller bond pads with a constant Ni(P) UBM thickness (for example,  $5\text{-}\mu\text{m}$ ) will result in higher solder bump reliability.

The results presented above indicate that multiple smaller pads, rather than one larger pad, will be a more reliable solution for solder bump interconnections used for power electronic packaging under high current applications. A detailed finite element modelling analysis for the interface stress with varying UBM dimension and thickness may give useful information for further solder bump structure optimization.

#### IV. CONCLUSION

Electroless nickel deposition on aluminium bond pads depends not only on the zincate and electroless nickel plating conditions but also on the aluminium substrate type and pretreatment. The deposition rate is sensitive to many parameters in the overall process. This work has confirmed that decreased deposition rate from a nickel bath operated at the constant pH and temperature will result in higher phosphorus content in the UBM deposit.

The Al pad dimension and Ni(P) UBM thickness affect the interface stress in the Ni(P) UBM, which consequently affects the solder bump shear strength and reliability, as well as the solder bump failure modes during shear test. The UBM thickness plays an important role in the solder bump reliability and must be tightly controlled.

Stress in the electroless Ni(P) UBM increases with its thickness and dimension. A thicker UBM increases the likelihood of interface delamination or silicon cratering, and reduces the solder bump shear strength. Upon reaching a certain UBM thickness value, Ni(P) UBM/Al delamination or silicon cratering will become the main failure mode after thermal cycling.

A smaller ( $0.8\ \text{mm} \times 0.8\ \text{mm}$ ) bond pad results in better solder bump shear strengths and higher thermal cycling reliability. Multiple smaller bond pads are a better solution for reliable solder bump interconnection in electronic packaging

for high current applications. UBM structure optimization is necessary to satisfy reliable solder bump interconnection.

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#### REFERENCES

- [1] *International Technology Roadmap for Semiconductors*, ITRS, 2007 [Online]. Available: <http://public.itrs.net/>
- [2] S. C. O'Mathuna, P. Byrne, G. Duffy, W. Chen, M. Ludwig, T. O'Donnell, and P. McCloskey, "Packaging and integration technologies for future high-frequency power supplies," *IEEE Trans. Ind. Electron.*, vol. 51, no. 6, pp. 1305–1312, Dec. 2004.
- [3] M. Tuttle, P. Byrne, N. Cordero, W. Chen, S. C. O'mathuna, P. McCloskey, P. Cheasty, and D. O'Sullivan, "Demonstration of increased power densities through advanced 3d power packaging," in *Proc. Eur. Microelectron. Packag. Symp.*, Prague, Czech Republic, Jun. 16–18, 2004, pp. 201–206.
- [4] K. N. Tu, "Recent advances on electromigration in very-large-scale-integration of interconnects," *J. Appl. Phys.*, vol. 94, pp. 5451–5473, Nov. 2003.
- [5] P. Elenius, H. Yang, and R. Benson, "Solder bars—a novel flip chip application for high power devices," in *Proc. 50th Electron. Comp. Technol. Conf.*, Piscataway, NJ, 2000, pp. 697–701.
- [6] S. C. O'Mathuna, "Packaging and thermal issues," in *Proc. Power Technol. Roadmap Workshop*, Feb. 8, 2003, [CD ROM].
- [7] W.-M. Chen, P. McCloskey, P. Byrne, P. Cheasty, G. Duffy, J. F. Rohan, J. Boardman, A. Mulcahy, and S. C. O'Mathuna, "Degradation of electroless Ni(P) under-bump metallization in Sn3.5Ag and Sn37Pb solders during high-temperature storage," *J. Electron. Mater.*, vol. 33, pp. 900–907, Aug. 2004.
- [8] D. A. Hutt, C. Q. Liu, P. P. Conway, D. C. Whalley, and S. H. Mannan, "Electroless nickel bumping of aluminum bondpads—Part I: Surface pretreatment and activation," *IEEE Trans. Comp. Packag. Technol.*, vol. 25, no. 1, pp. 87–97, Mar. 2002.
- [9] D. A. Hutt, C. Liu, P. P. Conway, D. C. Whalley, and S. H. Mannan, "Electroless nickel bumping of aluminum bondpads. II. Electroless nickel plating," *IEEE Trans. Comp. Packag. Technol.*, vol. 25, no. 1, pp. 98–105, Mar. 2002.
- [10] E. J. O'Sullivan, A. G. Schrott, M. Paunovic, C. J. Sambucetti, J. R. Marino, P. J. Bailey, S. Kaja, and K. W. Semkow, "Electrolessly deposited diffusion barriers for microelectronics," *IBM J. Res. Develop.*, vol. 42, pp. 607–620, Sep. 1998.
- [11] J. F. Rohan and G. O'Riordan, "Characterization of the electroless nickel deposit as a barrier layer/under bump metallurgy on IC metallization," *Microelectron. Eng.*, vol. 65, pp. 77–85, Jan. 2003.
- [12] J. W. Jang, P. G. Kim, K. N. Tu, D. R. Frear, and P. Thompson, "Solder reaction-assisted crystallization of electroless Ni-P under bump metallization in low cost flip chip technology," *J. Appl. Phys.*, vol. 85, pp. 8456–8463, Jun. 1999.
- [13] M. O. Alam, Y. C. Chan, and K. C. Hung, "Interfacial reaction of Pb-Sn solder and Sn-Ag solder with electroless Ni deposit during reflow," *J. Electron. Mater.*, vol. 31, pp. 1117–1121, Oct. 2002.
- [14] W. M. Chen, P. McCloskey, and S. C. O'Mathuna, "Isothermal aging effects on the microstructure and solder bump shear strength of eutectic Sn37Pb and Sn3.5Ag solders," *Microelectron. Rel.*, vol. 46, pp. 896–904, May/Jun. 2006.
- [15] Z. Chen, X. D. Xu, C. C. Wong, and S. Mhaisalkar, "Effect of plating parameters on the intrinsic stress in electroless nickel plating," *Surf. Coat. Technol.*, vol. 167, pp. 170–176, Apr. 2003.
- [16] *Efficiency Through Technology*, IXYS, 2007 [Online]. Available: <http://www.ixys.com/#>
- [17] J. F. Rohan, P. A. Murphy, and J. Barrett, "Zincate-free, electroless nickel deposition on aluminium bond pads," *J. Electrochem. Soc.*, vol. 152, no. 1, pp. C32–C35, 2005.
- [18] S. Haque and G.-Q. Lu, "Effects of device passivation materials on solderable metallization of IGBTs," *Microelectron. Rel.*, vol. 41, pp. 639–647, May 2001.
- [19] E. W. C. Yau, J. F. Gong, and P. Chan, "Al surface morphology effect on flip-chip solder bump shear strength," *Microelectron. Rel.*, vol. 44, pp. 323–331, Feb. 2004.

- [20] J. Y. Song and J. Yu, "Residual stress measurements in electroless plated Ni-P films," *Thin Solid Films*, vol. 415, pp. 167–172, Aug. 2002.
- [21] R. Weil and K. Parker, *Electroless Plating: Fundamentals and Applications, The Properties of Electroless Nickel*, G. O. Mallory and J. B. Hajdu, Eds. Orlando, FL: Amer. Electroplaters & Surf. Finish. Soc., 1990, ch. 4.
- [22] J. B. Kushner, "Factors affecting residual stress in electrodeposited metals," *Met. Finish.*, pp. 46–52, Apr. 1958.
- [23] Y.-D. Jeon and K.-W. Paik, "Stresses in electroless Ni-P films for electronic packaging applications," *IEEE Trans. Comp. Packag. Technol.*, vol. 25, no. 1, pp. 169–173, Mar. 2002.
- [24] R. Weil, "Origins of stress in electrodeposits- 1," *Plating*, vol. 57, pp. 1231–1237, Dec. 1970.
- [25] S. A. Watson, "The effect of some addition agents on stress in nickel deposits," *Trans. Inst. Met. Finish.*, vol. 40, pp. 41–47, 1963.
- [26] D. Mitchell, Y. Guo, and V. Sarihan, "Methodology for studying the impact of intrinsic stress on the reliability of the electroless Ni UBM structure," *IEEE Trans. Comp. Packag. Technol.*, vol. 24, no. 4, pp. 667–672, Dec. 2001.
- [27] W.-M. Chen, J. F. Rohan, P. J. McNally, L. Nagle, P. Byrne, P. McCloskey, and S. C. O'Mathuna, "Effects of under bump metallization on the solder bump reliability," in *Proc. IMAPS'04*, Nov. 14–18, 2004, [CD ROM].



**James F. Rohan** received the B.Sc. and M.Sc. degrees in chemistry from University College Cork, Cork, Ireland, in 1988 and 1992 respectively, and the Ph.D. degree in electrochemistry from Southampton University, Southampton, U.K., in 1994.

After two years with EIC Laboratories, Norwood, MA, he joined the National Microelectronics Research Centre (now Tyndall National Institute), Cork, working in the Interconnection and Packaging Group. Since 1999, he has led the Plating Technologies Team investigating interconnect and packaging, microfabrication and electrochemical research and development for novel metallization and micropower source integration.



**Patrick Byrne** received the B.Sc. degree in materials science and the Ph.D. degree from the University of Limerick, Limerick, Ireland, in 1993 and 1998, respectively. In his doctoral work, he studied high temperature liquid metal interactions with silicon nitride based ceramics and characterized the long-term reliability implications of the environmental exposure to the ceramic matrix.

He joined the NMRC (now the Tyndall National Institute), Cork, Ireland, in 1996 as a Research Scientist as part of the Power Electronics Group. His responsibilities included research in the areas of power packaging interconnect, reliability and product development research programs for indigenous Irish industry. Currently, he is working in the field of advanced high-density power packaging solutions within the EPI Group, Tyndall National Institute.



**Weimin Chen** received the Ph.D. degree in materials and microelectronics.

He was employed by the Assembly Technology Development Department (ATD-S), Intel, Shanghai, China. His work in Intel was for flash product packaging development. Before joining Intel, he did research with the Tyndall National Institute (Formerly as National Microelectronics Research Centre), University College, Cork, and a few other research institutes. His main research interests are electronic packaging and reliability physics of

electronic components and devices.

Dr. Chen received the Best Poster Award at the 4th International Conference on Materials for Microelectronics and Nanoengineering, Helsinki, Finland, June 2002.



**Paul McCloskey** received the B.Sc. degree in chemical engineering from Queens University, Belfast, U.K., in 1981, and the M.Sc. degree in energy studies and the M.Sc. degree in microelectronics from the University of Ulster, Ulster, U.K., in 1984 and 1991, respectively.

He has worked for 14 years in electronics manufacturing and is currently the Team Leader of the Energy Processing for ICT (EPICT) Team, Tyndall National Institute, Cork, Ireland (the EPICT team carries out research that addresses the provision of energy for future

ICT with a particular focus on the development of miniaturized integrated devices such as generators, inductors, transformers and sensors).



**Patrick J. McNally** (M'94–SM'06) received the B.E. degree (with first class honors) from University College Galway, Galway, Ireland, and the Sc.M. and Ph.D. degrees from Brown University, Providence, RI, in 1988 and 1992, respectively.

He is an Associate Professor in the School of Electronic Engineering, Dublin City University (DCU), Dublin, Ireland, and was Director of the Research Institute for Networks and Communications Engineering, DCU (2002–2004). He now directs RINCE's Nanomaterials Processing Laboratories.

He is a contributor to the Design Group for the PETRA III x-ray synchrotron, HASYLAB, Hamburg, Germany and was a member of the X-Ray Topography Workgroup for construction of the ANKA Synchrotron Beamline, Karlsruhe, Germany. He is a Member of the Editorial Board for the *Journal of Materials Science: Materials in Electronics*. He is and was Principal Researcher for numerous Forbairt and Enterprise Ireland and Science Foundation Ireland research programmes. He led the development of Ireland's first Postgraduate Taught Masters course in Nanotechnology, i.e./GCert/GDip/MEng Major in Nanoelectronics and Photonics, which was launched in September 2005 as a Major within the School of EE's Electronic Systems postgraduate taught degree programme. His main research interests include nanomaterials and electronic device process characterization (micro-Raman and photoacoustic spectroscopy), synchrotron x-ray topography, and novel materials for Si-based photonics (principally copper halides).

Dr. McNally is a Fellow of the Institute of Physics, and a member of the Materials Research Society and the Institute of Engineers of Ireland. He was Chairman of the Programme Committee for the 6th International Conference on Materials for Microelectronics and Nanoengineering, Cranfield, UK (2006), Chaired the 5th version of this conference series (MFMN2004, Southampton, UK—sponsored by the Institute of Materials), and has served on previous Programme and International Advisory Committees for this series of conferences.