Synchrotron X-Ray Topographic Analysis of the Impact of Processing Steps on the Fabrication of AlGaAs/InGaAs p-HEMT's

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***Abstract*—Synchrotron X-Ray Topography (SXRT) has been uniquely applied to nondestructively reveal and evaluate the damage throughout the depth of the wafer, caused by the deposition of source/gate/drain metallization and of so-called "passivation" dielectric layers on power $Al_{0.22}Ga_{0.78}As/In_{0.21}Ga_{0.79}As$ pseudomorphic HEMT's. Device metallization is visible due to the stress imposed on the underlying substrate and is detected as a strain field by SXRT. Experimental results are in good agreement with simulation. The quality and detail of the initial control topographs disappear when the Si_3N_4 dielectric layer is deposited. This is believed due to the passivating layer introducing such strain into the crystal that it overwhelms the metallization strain, in addition to producing a significant amount of stress-induced defect and dislocation generation.**

I. Introduction

THE impact of device processing and the need for powerful and sophisticated process characterization techniques is becoming ever more critical with the increasing complexities of electronic device structures. Furthermore, modern epitaxial methods have provided ready access to nano-engineered substrate materials which demand increasingly effective wafer qualification techniques. These demands are particularly acute in the area of III-V compound semiconductor devices, where the improved electrical properties of e.g., GaAs-based devices, are employed for microwave components working at GHz frequencies.

An example of such a need is considered here, namely the characterization of the fabrication of power pseudomorphic-HEMT's (p-HEMT's) on epitaxial structures grown by low pressure Metal-Organic Vapor Phase Epitaxy (MOVPE) technology incorporating a Si planar doped (δ-doped) $Al_{0.22}Ga_{0.78}As$ supply layer [1].

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Conventional analysis techniques, such as Scanning Electron Microscopy (SEM), Transmission Electron Microscopy (TEM), Auger Electron Spectroscopy (AES), or Rutherford Backscattering (RBS), all provide useful information, but are either *intrusive and destructive,* or are limited in the extent to which they can map through process layers and 3-D through the full depth of the semiconductor wafer, and thus, in the information provided.

Synchrotron X-Ray Topography (SXRT) is a technique which overcomes many of these drawbacks in that it is a *noncontact, nondestructive* characterization tool capable of tracking an individual wafer through all processing steps from virgin wafer to completed circuits, providing a comprehensive 3-D record of the induced stresses and defect generation attributable to each fabrication level on individual devices and full circuits.

This work charts the unique application of SXRT in order to elucidate the impact of critical process steps on the development of internal mechanical stresses and defect generation in the aforementioned p-HEMT structures. Specific attention is paid to:

1) source/gate/drain metallization and consequent stress generation in the underlying substrate;
2) and the impact on the substrate of the deposition of "passivating" dielectric overlayers.

These steps are of crucial importance, especially in III-V semiconductor devices. The mechanical stresses imposed on the substrate by such metal or dielectric overlayers lead to large regions of uncontrollable piezoelectric charge in the active regions of a device [2]–[5] and have a serious impact on the electrical performance of these devices, e.g., stress-induced threshold voltage shifts of the order of 500 mV in some situations [6]. Furthermore, in the event of these overlayers being responsible for defect generation within the substrate, it is well known that the proximity of these crystalline defects or dislocations is correlated with changes in the electrical characteristics of III-V device structures [2], [4], [7].

II. Device Structure

The test samples were grown on GaAs substrates oriented 2° off (100) toward [110] in a horizontal LP-MOVPE reactor. Further details are reported elsewhere [1]. The reactant gases used were AsH_3, TMGa, TMAl and SiH_4 (1% in H_2). The

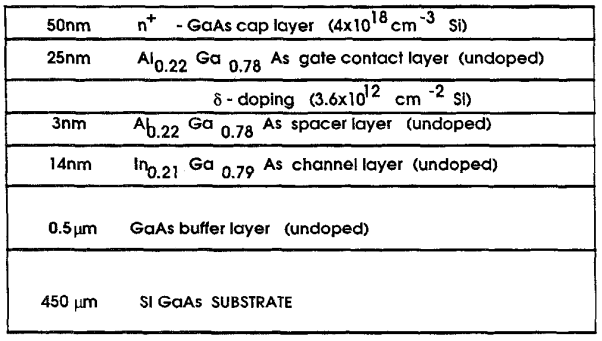


Fig. 1. Vertical structure of the p-HEMT devices used in this study. (Not drawn to scale.)

growth conditions for all the device materials were a temperature of 650°C, a V/III ratio of 175 and a pressure of 20 mBar. An AsH_3 partial pressure of 2.2×10^{-2} mBar was maintained during growth interruption. The p-HEMT vertical structure is shown in Fig. 1. The vertical structure design and optimization was carried out on a 1-D simulator solving autoconsistently the Poisson and Schroedinger equations.

Mesa etching was used to isolate the active areas of the transistors, and the Ohmic contacts of the source and drain electrodes were realized by electron beam evaporation and lift-off of a Au-Ge-Ni alloy followed by a rapid thermal anneal process. The gate recess was obtained by wet selective etching and the gate metals (Ti/Pt/Au) were deposited by electron beam evaporation and lifted off using a triple resist level technique. Devices with source/gate/drain metallization will be referred to as HEMT-1. A further set of devices (referred to as HEMT-2) underwent deposition of a 1800 Å thick layer of Si_3N_4 passivation. This layer was deposited by plasma-enhanced chemical vapor deposition at 250°C. These passivated devices were also examined by SXRT and the results of a comparison to the HEMT-1 devices follows in Section IV. The gate and drain electrodes are arranged in a standard interdigitated configuration as shown in Fig. 2.

III. Synchrotron X-Ray Topography (SXRT)

X-Ray Topography (XRT) is a nondestructive technique which can provide a map of the defect distribution in crystals [8]–[11]. This technique is based on the difference in reflecting power between perfect and distorted parts of a crystal. It is sensitive to strain fields extending over more than several micrometers and therefore XRT is mainly used for the study of dislocations, planar defects, stacking faults, domain walls in ferroelectric and magnetic materials, growth defects or large precipitates.

Localized imperfections may act as independent scattering centres e.g., small angle scattering by small precipitates or thermal diffuse scattering, but it is the *strains* they induce which modify the diffraction of X-rays by the good crystal. The image of a dislocation line, for instance, on an X-ray topograph is not an enlargement of the "core" of the dislocation. By core is meant that inner region surrounding the defect where continuous elasticity is no longer valid and which has a diameter of a few Angstroms [12]. Rather, the strains due to the dislocation perturb the crystal for several microns from the defect from the X-ray aspect, and it is these regions far from the core, which give rise to the defect image, through a deviation from the ideal Bragg reflection observed in the more perfect crystalline regions.

Geometrical resolution is governed by the incident beam local divergence on the sample and usually lies in the micron range. In fact, wavelength and angular spread of the incident beam, together with its lateral extension, are crucial parameters in X-ray topography. Synchrotron radiation X-ray beams provide low divergence beams, which, given their very high intensity, provide for excellent X-ray topographs.

Two main experimental set-ups were used as described below.

1) *White Beam Topography (Large-Area Topography)*
   This is one of the most commonly used techniques, described in [8], [9], and provides for an improvement over Lang topography [10] in that the traversal stage can be eliminated. When a single crystal is immersed in a white X-ray beam a number of lattice planes (hkl) select out of the continuous spectrum the proper wavelengths to be reflected according to Bragg's Law

$$2d_{hkl} \cdot \sin\theta_B = n\lambda \tag{1}$$

   where d_{hkl} is the interplanar spacing of (hkl) lattice planes, θ_B is the Bragg angle, and n is an integer. A beam diffracted in a certain direction $2\theta_B$ with respect to the incident beam has a spectrum of wavelengths $\lambda, \lambda/2, \lambda/3$, etc. corresponding to diffraction lattice planes $(hkl), (2h\ 2k\ 2l), (3h\ 3k\ 3l)$ etc. The fundamental reflection hkl or its harmonics may, however, be structure factor forbidden. This is the well-known Laue method. However, due to the low divergence of the synchrotron radiation beam, each spot of this particular Laue pattern is itself a high-resolution topograph [9].
2) *Section Topography*
   An arrangement similar to that for Large-Area Topography is used, only in this case the incoming beam is collimated into a narrow ribbon by a slit typically 10–15 μm in width. A set of Laue case section topograph images of sample cross sections are produced as previously described and, provided that the Bragg angle is not too small, the image gives detailed information about energy flow within the crystal and direct depth information on defects present in a particular crystal slice [13].

The measurements were performed at HASYLAB-DESY, Hamburg, Germany (Hamburger Synchrotronstrahlungslabor am Deutschen Elektronen-Synchrotron), utilising the continuous spectrum of synchrotron radiation from the DORIS storage ring bending magnet. The ring operated at a positron energy of 4.45 GeV and at typical currents of 50–100 mA. The aforementioned Laue pattern of topographs was recorded either on a Kodak type R or on a Kodak High-Resolution Professional X-ray film having an emulsion grain size of about 0.05 μm. Both the section and large-area modes were used in producing topographs. In

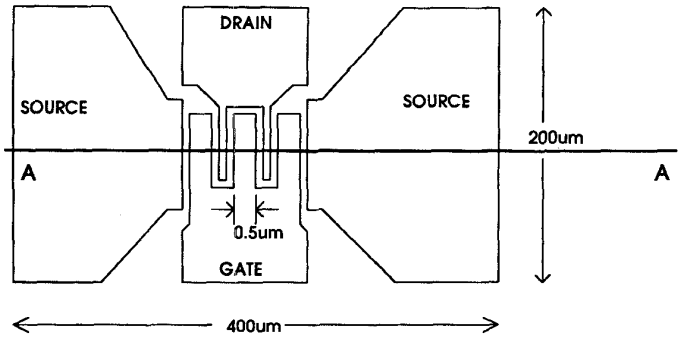


Fig. 2. Schematic electrode configuration for and s of p-HEMT devices. Not drawn to scale. The individual devices can be fabricated with up to four gate fingers. A central source finger, which is air bridge connected, is not shown on the diagram.

section topography, the beam was limited by a horizontal slit having a width of 15 μm. The surface of the wafer made an angle of 63.5° with the beam. In large-area topography, the beam was limited by a rectangular slit of 3 mm × 7 mm and the wafer surface was set perpendicular to the beam. As noted, both methods used transmission geometry, i.e., the diffracted beam passed through the wafer.

Previous experimental studies relied on either mechanical stressing of devices [6] which could only approximate the actual stresses due to device process overlayers, or on interferometric techniques (e.g., Fourier transform infra-red spectroscopy) which enabled a characterization of dielectric film chemistry and stress [14], or on scanning Auger microscopy techniques [14] which are destructive. The experiments performed in [14] measured wafer bow as a means of deducing the stress state of blanket layers of deposited dielectric overlayers. However, none of the above experiments could observe regions where the imposed dielectric film (or metallization) stresses become locally concentrated (e.g., at a dielectric/metal discontinuity) and they could not observe the generation of strain fields or dislocations throughout the entire depth of the wafer. The ability of SXRT to do so nondestructively is almost unique. This is true even in the presence of significant wafer bow, due to the fact that all parts of the crystal (distorted or not) will still give homogenous images, each area extracting the proper wavelength from the incident white beam [8].

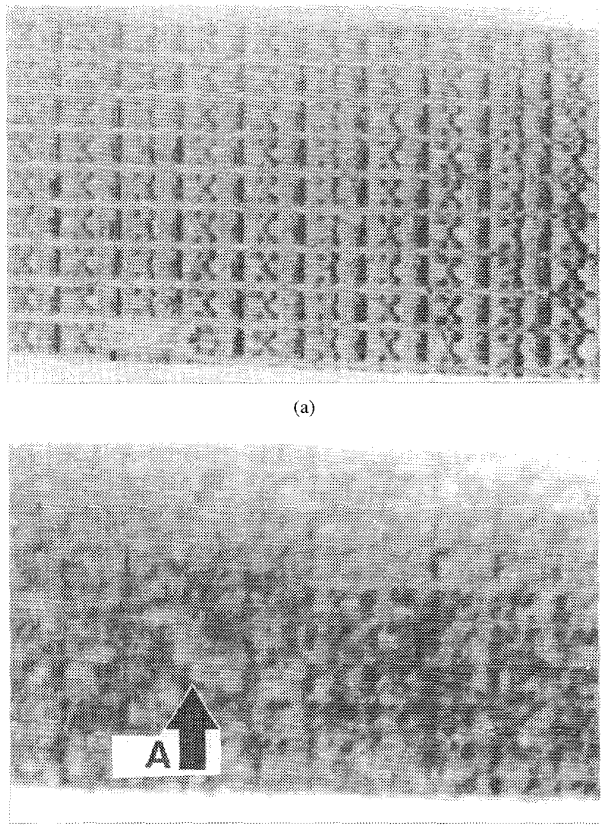
It is sometimes important to know the harmonic content of the outgoing diffracted beam rather than that of the incoming beam hitting the sample. For example, in the case of a 111 section topograph the fundamental wavelength is 0.0993 nm and that of the 333 harmonic is 0.0331 nm. The relative brightness values are roughly 2 and 1, respectively. In order to find out the relative intensities of the diffracted beam one has to find the mass absorption coefficients of GaAs at those wavelengths, to take into account the structure factor and finally to estimate the spectral sensitivity of the film. However, if one considers orientational contrast only, which is the dominant factor in this study, the effect of the harmonics on image contrast should be negligible. The width of a dislocation image depends, according to the kinematical theory of X-ray diffraction, on the wavelength [9], [12]. The harmonics widen the image lines and one may observe blurred images. This is not of great significance in the situation described here, since dislocations in GaAs will not be individually resolved, as discussed further in Section IV.

IV. Results and Discussion

Fig. 3(a) is a large-area topograph of a $\bar{1}\,\bar{3}\,\bar{5}$ reflection of an array (10 × 9) of devices which have undergone processing up to and including the source/gate/drain metallization (HEMT-1). The definition of this metallization is very clear, with an exceptional contrast visible at the edges of these overlayers. These regions become visible because they induce strain in the underlying semiconductor crystal lattice structure, thus inducing localized lattice curvature. There is a local deviation from Bragg's Law in these regions and hence a contrast with respect to more perfect crystal is observed on the film. Note also that the definition of these regions is not entirely homogenous across the devices, a clear indicator of nonuniform metallization stresses even for individual devices. Relatively few crystal defects/dislocations are observed which implies that the substrate is of reasonably high quality and, most importantly, that *neither* the LP-MOVPE growth or the metallization processing is responsible for large-scale defect/dislocation generation.

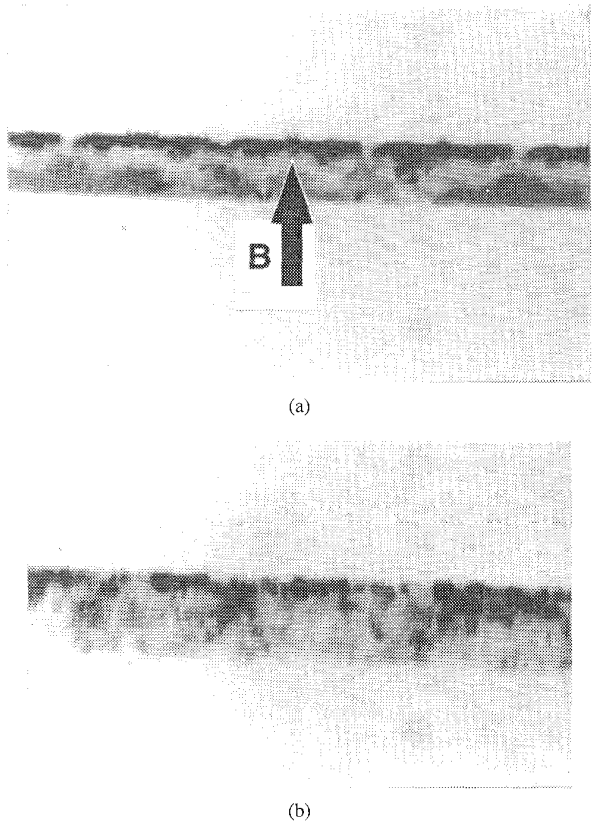
Fig. 3(b) is a large-area topograph of a $\bar{1}\,\bar{3}\,\bar{5}$ reflection of a similar array (10 × 9 also) of devices which have been metallized, but also upon which the Si_3N_4 "passivating" layer has been deposited (HEMT-2). The quality and detail observed in Fig. 3(a) for HEMT-1 has disappeared. The dielectric layer has now introduced so much strain into the crystal that it completely overwhelms the metallization strain, and the individual FET's are barely made out. This is clear visual evidence that the dielectric layer is the major factor in the production of unwanted stresses and strains throughout the depth of the underlying processed wafer substrate. Such information was previously only attainable through intrusive and destructive experimentation [6], [14]. The magnitude of the biaxial stress introduced by such a dielectric overlayer is typically of the order of 10^8 Nm^{-2}, generally at least an order of magnitude greater than that due to the metallization process.

Furthermore, there is also clear evidence of defect generation, indicating that the deposition of highly stressed Si_3N_4



(a) (b)

Fig. 3. (a) Large-area $\bar{1}\bar{3}\bar{5}$ topograph for the HEMT-1 device array—metallization only. (b) Large-area $\bar{1}\bar{3}\bar{5}$ topograph for the HEMT-2 device array—dielectric overlayer is also deposited in this case.



(a) (b)

Fig. 4. (a) A $\bar{1}\bar{1}\bar{1}$ section topograph of an array of HEMT-1 devices—metallization only. The top surface of the crystal is uppermost in the topograph. (b) A $\bar{1}\bar{1}\bar{1}$ section topograph of an array of HEMT-2 devices—dielectric overlayer is also deposited in this case; orientation as per (a).

layers can lead to widespread and detrimental defect generation in the underlying crystal. This can be observed in particular as "black streaky regions" especially on the left hand side of the topograph (marked with arrow A in the figure). In order to image slices through the devices, section topographs through the substrate (ST) were produced for the above two structures along a line marked "A-A" in Fig. 2. Fig. 4(a) is a $\bar{1}\bar{1}\bar{1}$ section topograph (ST) of the device structure HEMT-1. An array of 3 HEMT's is clearly seen. The strains imposed on the crystal due to the source/gate/drain metallization appear as black regions of contrast (indicating increased X-ray intensity) at the top of the topograph. The strain field is at its most intense in the gate/drain interdigitated region and is seen as a small "black bump" at the centre of the image of each HEMT (marked with arrow B in this figure). The gate/drain fingers appear lifted out of the rest of the topograph and are easily resolved, showing the enhanced stress concentration at the edges of the metal fingers in this region. These topographs map diffraction in the crystal material. The enhanced stress in the gate/drain fingers induce such intense local lattice curvature in the crystalline material directly beneath them, that their corresponding Bragg angle is shifted with respect to the rest of the wafer; the images of these regions are therefore also slightly shifted on the topographs, as seen in Fig. 4(a). The metallization induced strains penetrate up to one-half of the wafer thickness and this profile is qualitatively in agreement with previous simulations [3], [5] and the following model.

The substrates were qualified as having etch pit densities of $\leq 1\times10^4$ cm^{-2}. It can be seen from Figs. 3(a) and 4(a) that one cannot distinguish individual dislocations, but rather, one can observe the strain fields due to macroscopic distributions of defects/dislocations under the device metallization. As discussed in [13], the detectability limit for individual dislocations is of the order of 10^4 cm^{-2}, which is confirmed by the observations in this study. It is also clear from Figs. 3(b) and 4(b) that the number of dislocations (though not individually resolvable) increases by at least on order of magnitude beyond this figure, upon deposition of the dielectric overlayer.

Using the model described in [5], a simplified metal strip test structure, assuming a biaxial metallization stress for all contacts of 10^7 Nm^{-2}, was simulated by means of a finite element method stress analysis. The results are shown in Fig. 6 and are seen to be in good qualitative agreement with the observed profiles. The device coordinate system is chosen such that the x axis is in the $[0\,\bar{1}\,1]$ direction, the y axis in the $[0\,\bar{1}\,\bar{1}]$ direction and the z axis in the [100] direction. The diffraction planes are defined by the normal vector $[\bar{1}\,\bar{1}\,\bar{1}]$. If the X-ray beam is approximated by a narrow beam advancing from the X-ray source toward the GaAs wafer in the direction of the vector $\boldsymbol{b}$ (see Fig. 5) then the beam is in the y-z plane.

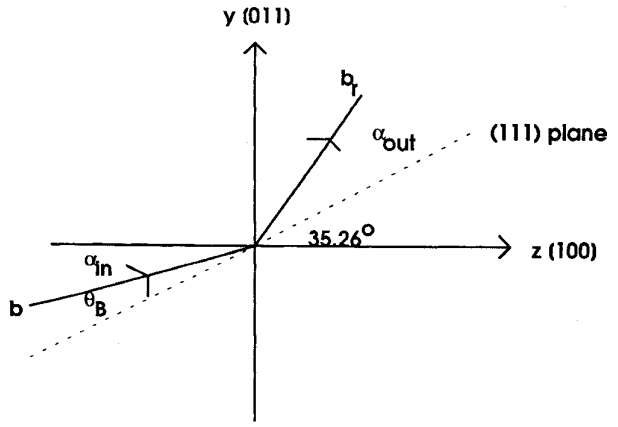


Fig. 5. Definition of the geometry used for the simulation of contrast features for section topography.

Furthermore if the beam is reflected from the $(\bar{1}\,\bar{1}\,\bar{1})$ planes, the reflected beam ($\boldsymbol{b_r}$ in Fig. 5) is in the y-z plane too, for the case of an undistorted crystal. The X-ray beam arrives at an angle of $\alpha_{\rm in} = 26.5°$ toward the z axis and is reflected at an angle of $\alpha_{\rm out} = 44.02°$ still in the y-z plane in the case of undistorted crystal. The resulting Bragg angle is $\theta_B = 8.76°$.

If the metal strips are assumed to be deposited on the (100) GaAs surface lengthways along the y axis, and if the source-to-drain direction is along the x axis, the stress-strain field exerted by the metal on the substrate varies only in the x-z plane. The crystal displacements u and w in the x and z directions, respectively, are obtained by the 2-D finite element method [5]. The stress exerted on the GaAs is modeled by assuming that the forces at the metal edges parallel to the x axis point toward the metal strip [15], causing the GaAs regions below the metal to be under compression. The magnitude of the forces per unit length is $|S| = T_m\sigma_m$ where $T_m = 0.25$ μm is the metal thickness and σ_m is an average metal stress approximated by a stress value an order of magnitude lower than the stress generally found in dielectric films deposited on GaAs, i.e., $\sigma_m = 10^7$ N/m^{-2} [2]–[6].

Neglecting dynamical scattering effects and taking into account the fact that the incident beam has a continuous spectrum of wavelengths, an X-ray beam diffracted from a point in the strained region will travel through the remaining crystal at an angle slightly different from the Bragg angle θ_B by the amount $\Delta\theta$. This difference is due to the change in spacing between the diffraction planes and in their tilt, due to the strain induced by the metal.

Quite generally, the angle of the reflected beam can be modified by $\Delta\theta_H$ so that the reflected beam is still in the y-z plane, or the beam can be reflected at an angle of $\Delta\theta_V$ with respect to the y-z plane. This results in an orientation contrast. If the diffraction planes are parallel to the x axis, as is the case here, the in-plane shift of the reflection angle is given by $2\Delta\theta_H$ with

$$\Delta\theta_H = -|\cos\gamma|\tan\theta_B\frac{\partial w}{\partial z} \tag{2}$$

where the minus sign indicates that an increase of the distance between diffraction planes, i.e., $\partial w/\partial z > 0$, results in a decrease of the reflection angle, γ is the angle between the normal of the diffraction plane and the z axis ($\gamma = 125.26°$), and $|\cos\gamma|$ indicates that $\Delta\theta_H$ is invariant to the rotation of the diffraction planes through 180° (as a consequence of neglecting dynamical scattering effects). The out-of-plane shift of the reflection angle is given by $2\Delta\theta_V$ where

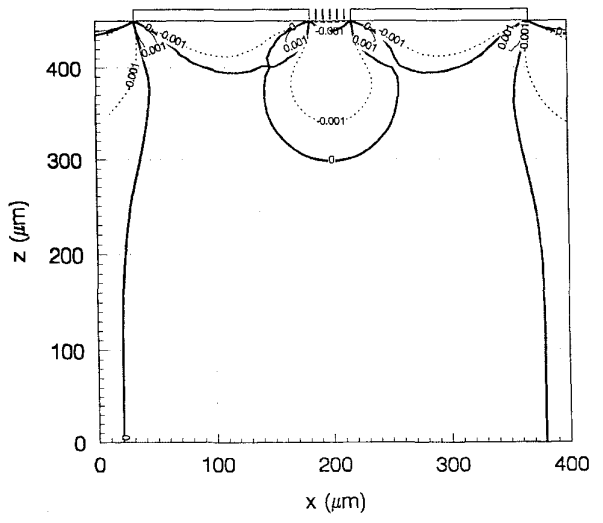
$$\Delta\theta_V = \frac{1}{2}\left(\frac{\partial u}{\partial z} + \frac{\partial w}{\partial x}\right). \tag{3}$$

The contour plots of $\Delta\theta_H$ and $\Delta\theta_V$ are shown in Fig. 6(a) and (b), respectively. The $\Delta\theta_H$ shifts are approximately an order of magnitude lower than the $\Delta\theta_V$ shifts. Although the $\Delta\theta_H$ and $\Delta\theta_V$ shifts do not directly correspond to the topographic image, the regions with higher $\Delta\theta_H$ and $\Delta\theta_V$ will scatter the incoming beam more than the less strained regions of the crystal. Consequently, a change in sign in $\Delta\theta_V$, in particular, will correspond to a reversal in orientation contrast in a section topograph. Good qualitative agreement is found with the section topographs and particularly for a region at least 150 μm away from the device midpoint, where simulation agrees very well with contrast reversal as seen in Fig. 4(a).

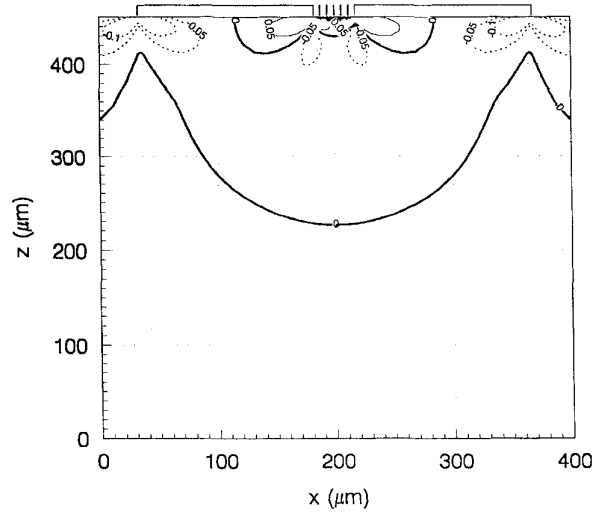
Fig. 4(a) and (b), in particular, shows topograph detail corresponding to multiple crystal defects and dislocations rendered visible by the surrounding strain fields. Such fields appear to interact with the stress fields set up by the metallization. This phenomenon, combined with the inhomogeneity of the stresses imposed by the overlayers, results in *no two devices* sharing an identical stress profile. This situation is exacerbated by deposition of the dielectric overlayer, as seen in Fig. 4(b). Virtually all details of the metallization-induced stresses have now gone, and the topograph provides clear evidence that the so-called "passivation" layer is, in fact, a damaging layer in terms of its introduction of severe, overwhelming and unwanted stresses into the device. It is also now possible to observe many defects generated by the severe stressing of the underlying crystal. The largest concentration of defect distribution is seen for regions under the metal/dielectric interfaces, where the imposed stresses are severely enhanced.

The introduction of severe stresses and defect/dislocation generation has serious implications for III-V device electrical performance. Firstly, these materials are piezoelectric, and stresses in the device produce unwanted regions of piezoelectric charge in or near active device regions, with a consequent impact on device performance [2]–[6], [14]. Secondly, stress fields can produce stress enhanced lateral diffusion of dopant species with significant deterioration in the ability to control device parameters, e.g., threshold voltage [16]. Finally, the distribution of defects and dislocations in a wafer is known to correlate with variations in device operating characteristics [7], [17].

This is confirmed by an analysis of electrical data for these devices before and after dielectric passivation. Table I outlines details of these parameters where I_F = source-drain current with $V_S = 0$ V, $V_D = 3$ V, and $V_G = 0.5$ V; I_{DSS} = source-drain current with $V_S = 0$ V, $V_D = 3$ V and $V_G = 0$ V; G_m = maximum extrinsic transconductance measured at



(a)



(b)

Fig. 6. The (a) in-plane $\Delta\theta_H$, and (b) out-of-plane $\Delta\theta_V$ shifts in arc seconds for a $\overline{1}\,\overline{1}\,\overline{1}$ section topograph of the simulation test structure. The contours of $\Delta\theta_H = 0$ and $\Delta\theta_V = 0$ are shown as thick full lines. The contours of positive (thin full lines) and negative (dotted lines) angle shifts are also shown. The metallization stripes are shown at the top of each graph: two 150-μm long metal contacts and five 1 mm long metal fingers spaced 5 μm from each other and from the long contacts. The strips are deposited on the y-z surface and it is assumed that the width (i.e., the in the y direction) is much longer than the size of the structure in the x direction. A change in the sign of $\Delta\theta_V$ will correspond to a reversal in contrast as observed on a section topograph.

$V_D = 3$ V; V_P = pinch-off voltage measured at $V_D = 3$ V with a source-drain current equal to 1% of I_{DSS}; and V_{BKD} = drain breakdown voltage obtained by imposing $V_G = V_P$ and measuring the drain voltage required to reach a drain-source current equal to 5% of I_{DSS}.

The data from Table I confirm that the passivating layer plays a major role in the deterioration of device performance. All of the mechanisms referred to in the previous paragraph will most likely contribute to these effects. The changes in device performance are quite large, but this is consistent with the topographic evidence which confirms that the dielectric overlayer plays a significant role in the generation of large unwanted strain fields within the substrate, as well as being responsible for a large dislocation build-up throughout the wafer, especially near active device regions at the wafer surface.

TABLE I
ROOM TEMPERATURE ELECTRICAL PARAMETERS FOR p-HEMT'S BEFORE AND AFTER DIELECTRIC PASSIVATION

	I_F (mA)	I_{DSS} (mA)	G_m (mS)	V_P (V)	V_{BKD} (V)
AFTER GATE DEPOSITION (HEMT-1)	35	24	24	-1.12	-8.5
AFTER DIELECTRIC DEPOSITION (HEMT-2)	34	17	34	-0.86	-5.4
% CHANGE	-2.9	-29.2	+41.7	+23.2	+36.5

V. CONCLUSION

Synchrotron X-Ray Topography has been used for the first time to examine the impact of critical device processing steps on pseudomorphic AlGaAs/InGaAs HEMT's. This technique, which relies on crystalline diffraction properties, can be used to locate regions of high stress and/or defect or dislocation generation within the devices. What are believed to be the clearest images to date of the stresses imposed on a compound semiconductor wafer due to source/gate/drain metallization have been generated and subsequently simulated. It can be seen that the stress profile of no two devices is identical. This situation deteriorates upon the deposition of a Si_3N_4 dielectric overlayer. Severe stresses are observed in the substrate and a large number of defects and dislocations are also produced. The fact that this "passivating" layer is seen to be a "damaging" layer has serious implications for III-V device processing.

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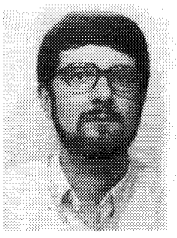

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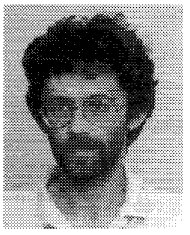

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