Non-Destructive Laboratory-Based X-Ray Diffraction Mapping of Warpage in Si Die Embedded in IC Packages

C. S. WONG[1], N. S. BENNETT[1], D. MANESSIS[2], A. DANILEWSKY[3] and P. J. McNALLY[1]

[1]*Nanomaterials Processing Laboratory, School of Electronic Engineering, Dublin City University, Dublin 9, Ireland.*

[2]*Fraunhofer IZM Berlin, Microperipheric Research Center, Berlin Center of Advanced Packaging, Gustav-Meyer-Allee 25, Berlin, Germany.*

[3]*Kristallographie, Institut für Geowissenschaften, Albert-Ludwigs-Universität, Freiburg, Germany.*

Email: chiu.wong2@gmail.com Tel no: +353-1-7005872

Abstract

Reliability issues as a consequence of thermal/mechanical stresses created during packaging processes have been the main obstacle towards the realisation of high volume 3D Integrated Circuit (IC) integration technology for future microelectronics. However, there is no compelling laboratory-based metrology that can non-destructively measure or image stress/strain or warpage inside packaged chips, System-on-Chip (SoC) or System-in-Package (SiP), which is identified as a requirement by the International Technology Roadmap for Semiconductors (ITRS). In the work presented here, a triple-axis Jordan Valley Bede D1 X-ray diffractometer is used to develop a novel lab-based technique called X-ray diffraction 3-dimensional surface modeling (XRD/3DSM) for non-destructive analysis of manufacturing process-induced stress/warpage inside completely encapsulated packaged chips. The technique is demonstrated at room temperature and at elevated temperatures up to 115^{o}C by *in situ* XRD annealing experiments. The feasibility of this technique is confirmed through the charactersation of die stress inside

encapsulated commercially available ultra-thin Quad Flat Non-lead (QFN) packages, as well as die stress in embedded QFN packages at various stages of the chip manufacturing process.
Keywords: Non-destructive, X-ray diffraction, stress, integrated circuit, embedded QFN package, Warpage.

1. Introduction

Traditional Si CMOS scaling following Moore's Law is becoming increasingly difficult as physical limits are approached at sub-20 nm nodes and beyond. Future advances in modern nanoelectronics may well depend on "More-than-Moore" approaches. System in Package (SiP) and other advanced package technologies provide such a route for the continued improvement in chip performance, with reduced power, cost and size at the system level, in a complementary approach to the new materials and architectures that can support Moore's Law scaling [1].

The existing advanced packages are however plagued by reliability problems, meaning they are not as reliable as traditionally packaged Integrated Circuit (IC) systems. Issues such as thermal and mechanical stress generation are primary concerns affecting the future integration requirements of advanced SoC/SiP systems. The fabrication process of a complete packaged IC is a tricky one, as it involves the use of different materials of distinct coefficients of thermal expansion (CTEs), *e.g.* die bond pad, die attach adhesive/epoxy glue, moulding compounds and Cu-filled through-silicon-vias (TSVs) [2-6]. Thermal stress and warpage are frequently generated in the packaged chip during the thermal processing steps as a consequence of the CTE mismatch of these materials [7-11]. Other factors such as the bonding of wires to the die itself [3], thinning of the wafer/die below 100 µm and embedding/lamination processes can also lead to stress and induced warpage/material deformation [12-13]. The process-induced stresses can even be large enough to induce cracking or interfacial delamination in the package, which by

potentially degrading the performance and reliability of the packaged chip, could ultimately lead to device failure.

Scanning acoustic microscopy (SAM) [14, 15], scanning electron microscopy (SEM) [15] and X-ray radiography [12, 13] are the most commonly used techniques for characterising packaged chip integrity, such as die cracking and delamination inside packaged chips, but none of these techniques is capable of quantitatively measuring the magnitudes of stresses or lattice misorientations inside packaged chips [16]. A recently developed synchrotron X-ray technique based on 3-dimensional X-ray diffraction imaging combined with 3-dimensional surface modelling (3DSM) has, for the first time, enabled the non-destructive imaging and measurement of strain and internal damage in packaged Si chips [17]. This technique has been used to reveal defect images with x-y spatial resolutions of < 5 μm throughout the entire probed Si wafer volume and was used to produce 3D strain/warpage maps of the nature and extent of the strain fields in completely packaged Quad Flat Non-lead packaged chips.

Nonetheless, an obvious drawback to widespread implementation of this technique is the fact that until now the techniques have required a synchrotron X-ray source. In this paper we describe a variant of this technique using monochromatic X-ray radiation generated by a conventional lab-based X-ray tube. This technique, which we label as "laboratory-based XRD/3DSM" can be used to non-destructively image, map and measure Si strain/warpage inside a fully encapsulated QFN packaged chip at various stages of the chip manufacturing process.

2. Experiment Details

2.1 Sample Structures

i) UQFN packages

In this study, a commercially available 28-pin UQFN flash microcontroller (Manufacturer Part No. PIC16LF1827-I/MV) from Microchip was examined. The cross-sectional schematic diagram of the UQFN package is illustrated in Fig. 1. The package consists of a Si die attached onto a copper/copper alloy lead frame by die adhesive film/epoxy glue, and finally encapsulated by a moulding compound. The contact pads of the UQFN package are connected to the Si die using wire-bonding technology, creating thin wires. The physical dimensions and the material properties of the UQFN package under test are estimated from X-ray radiographic images (not shown here) of the UQFN package, and references [18-21], as summarised in Table I.

ii) Embedded QFN packages

The second type of package investigated in this study is an embedded QFN package [12]. These consist of a 5 mm x 5 mm active die bonded Si chip (50 µm thick), embedded face-up on a substrate, with a peripheral bond pad pitch of 100 µm (see Fig. 1b)). The overall dimension of the package is measured to be 10 mm (W) x 10 mm (L) x 160 µm (H). The five major embedding/processing steps (see Fig. 2) of these QFN packages are listed below [12]:

i) The Si die is bonded onto the core substrate.

ii) Embedding by a ~ 100 µm thick resin coated copper (RCC) dielectric layer from the top side of the chip.

iii) Microvias were drilled through to the chip pads using a pulsed 355 nm UV laser.

iv) Via electroplating of copper.

v) Finally, the packaging process is complemented by the Cu structuring on the bottom side of the package. These packages were processed in a large panel format and they were separated using a laser or a standard (wafer) saw. More details regarding the QFN chip embedding, assembly and processing steps can be found in references [12]. For the embedded QFN packages, we investigated these packaged chips after two of the most potentially decisive processing steps marked by black square boxes in Fig. 2.

2.2 Investigation of die stress in packaged chips.

i) Development of a novel lab-based XRD/3DSM technique

XRD/3DSM is a novel technique for non-destructive analysis of strain/warpage inside completely encapsulated packaged chips. It was developed using standard XRD techniques [23, 26, 30], utilising a lab-based triple-axis Jordan Valley Bede D1 X-ray diffractometer with a copper (λ = 1.5405Å) radiation source operated at 45 kV and 40 mA. We have produced maps of the entire silicon die, which reveal the lattice misorientation/warpage of the (110) crystallographic plane in Si die via mapping of 004 symmetric rocking curve (RC) full-widths-at-half-maximum (FWHMs) as a function of position across fully encapsulated packages. The incident X-ray beam was reduced down to a 250 µm x 250 µm square by using horizontal and vertical slits. The small beam size is to ensure a high spatial resolution, as each of the RCs contains information on the lattice deformation averaged across this 250 µm x 250 µm area.

Each RC was recorded by rotating the specimen (ω axis) through a suitable angular range about the Bragg angle of the Si 004 reflection, with detector (2θ axis) fixed at twice the Bragg angle. By using this experimental geometry, the FWHM of the RC is directly related to the lattice misorientation/warpage of the (110) plane in the Si die. Figs. 3a)-b) illustrate the RCs of a warped Si die inside the packaged chip compared to a perfect (100) Si specimen without warpage. In the case where the Si die is curved or warped, the FWHM of the RC is broadened (see Fig. 3a)). This warpage creates a curvature of the Si crystal planes. Therefore there will be a range of angular positions on the distorted Si die in which the Bragg diffraction conditions are satisfied.

A spatially resolved RC map can be produced by integrating a series of RCs collected at different positions across the Si die of the package (in the x-direction) [22]. This is demonstrated in Fig. 3c), showing a RC map composed from 12 individual RCs, recorded as a function of x-position across the bottom edge of the Si die - with a step resolution of 200 µm indicated by the red arrow in Fig. 3a). The RC map of the Si specimen is also shown in Fig. 3d) for comparison. Concerning Fig. 3c), the variation of RC peak position (ω-ω_0) across the Si die is a signature of warpage-induced tilt [22]. From the RC map, one can observe that the diffraction angle of the RC recorded from the left part of the Si die (x<1.2) occurs at larger diffraction angles than the centre part of the Si die (ω_o), while it decreases below ω_o for the reflections from the right-hand side of the Si die. This phenomenon explicitly shows that the Si die is warped in a convex shape. In other words, the RC map for a convex die is shown by the image in Fig. 3c) [22].

Although the RC map is useful in revealing the type of warpage or direction of tilt developed during the packaging processes, it is not precise enough for a deep insight into the deformation, for instance, in identifying the highly distorted region of the Si die. Therefore, our

approach is to convert the RC map into a FWHM line scan by extracting the FWHM of each individual RC of the RC map, fitted using the "Asymmetric Double Gaussian" peak function by *Quick Graph* [23], the peak analysis software provided with the JV Bede D1 tool. From the FWHM line scan shown in Fig. 3e), the highly distorted region (largest FWHM) can be unambiguously identified to be the centre part of the Si die. In contrast, the FWHM extracted from the perfect Si specimen (Fig. 3f) is rather constant across the whole sample.

A series of FWHM line scans were repeated at 200 or 400 μm steps (for relatively high or low spatial resolutions, respectively) from the bottom edge of the Si die stepping continuously towards the top edge of the Si die (in the y-direction), controlled using an automatic motorised x-y sample stage on the JV Bede D1 diffractometer system. A full map of RC FWHMs, which reveals the warpage across the whole Si die of the packaged chip, was reconstructed by modifying the 3-dimensional surface modelling technique outlined in reference [17]. The FWHM line scans were imported into Solidworks^{TM} [24]. These formed a series of 3D curves (see Fig. 4a), in which the x and y coordinates correspond to the on-chip location where each RC was recorded, and z represents the FWHM extracted from each RC recorded at each x-y position. These 3D curves were then connected using the boundary surface feature in Solidworks^{TM} [17] to create a surface mesh, as shown in Fig. 4b). These 3D curves were formed into a solid surface XRD/3DSM model (see Fig. 4c). The sample was then rotated successively by 90^{o} around the [001] axis and the processes were repeated, in order to evaluate the lattice misorientations of the two orthogonal (110) crystallographic planes in the Si die.

ii) Synchrotron X-ray Topography (SXRT)

In order to verify the lab-XRD results, the packages were also studied using SXRT. Synchrotron X-ray topography (SXRT) is a powerful technique for investigating defects, stresses and lattice misorientation in semiconductor and other electronic materials. For SXRT, a white beam is used for the measurements, i.e. a continuous radiation spectrum consisting of a continuum of wavelengths (λ) each of which can be diffracted subject to the Bragg criterion being satisfied. Due to use of a white beam, all parts of the irradiated crystal (these include, structural defects, lattice tilts/misorientations and strain fields distributed within the crystals) are simultaneously visible on topographs regardless of the sample orientation. Considering the packages under test, the type of warpage/lattice misorientation in Si die can be unambiguously revealed using SXRT, and therefore it can be used to validate the lab-based XRD result.

X-ray topographs were taken at HASYLAB-DESY, Hamburg, using the continuous radiation spectrum emitted by a bending magnet source in the DORIS III storage ring. The positron ring at DORIS III had particle energy of 4.45 GeV and a beam current of 100-150 mA. Topographs were recorded on a high resolution Slavich VRP-M holographic film (grain size <0.04 μm) set 80 mm from the sample in back-reflection geometry [3]. LauePT software [25] was used to index the Laue spots in the individual topographs. The topographs were magnified using an optical microscope allowing details of the package/process induced warpage/strain and defects to be observed and analysed.

iii) *In Situ* XRD Annealing Experiments

Additionally, the JV Bede D1 system was equipped with an Anton Paar DHS 1100 heating stage. This allowed us to perform *in situ* XRD annealing experiments without the need to

remove the specimen from the sample stage or further XRD set-up alignment, prior to the heating experiments. This process is a good way of replicating the thermal response of the packaged chip at temperatures it may encounter during manufacture and operation. The *in situ* stage ensured the position of the specimen mounted on the heating stage remained constant, both prior to and after each heating experiment was carried out, ensuring very high repeatability and reliability of results. During the heating experiments, the sample was completely covered by a graphite dome, and the annealing temperature was monitored by a thermocouple controlled temperature unit.

iv) Finite Element Analysis (FEA)

For the purpose of developing a deeper understanding of the experimental results, we have also adopted Finite Element Analysis (FEA) in this study. Solidworks^{TM} was used to create a three dimensional model of the UQFN package and advanced features of the program were used for performing two types of FEA studies; i) Static analysis – to predict stresses and displacement caused by static/mechanical loading, and ii) Thermal analysis – to predict stress and displacements due to thermal expansion. The results predicted from FEA will be used for direct comparison with the experimental measurements. The properties of the materials used in the FEA were assumed to be linear-elastic and they are depicted in Table III.

3. Results and Discussion

3.1 Commercially available UQFN packages

Figs. 5a) and 5b) show the XRD/3DSMs of a UQFN package recorded at phi = 0^o and 90^o, respectively. They are, in effect, 2D maps of the warpage/lattice deformations of two orthogonal (110) planes which have developed in the Si die during the packaging process. Each

of the XRD/3DSM surfaces is built up from a total of 5 horizontal (phi = 0^o) and 5 vertical (phi = 90^o) FWHM line scans, respectively, using a 400 µm step size between two adjacent FWHM line scans. For ease of comparison of the lattice misorientation in the Si die in two orthogonal (110) planes, the XRD/3DSM recorded at phi = 0^o and 90^o are combined and shown in Fig. 5c). The XRD/3DSM of the UQFN package clearly reveals that the warpage is relatively low at the corners of the Si die and increases gradually approaching the chip centre and also near the central edges of the die. This non-uniformly distributed warpage is thought to be due to process-induced thermal stress as a result of the CTE mismatch between different materials, most probably from the die attach process [7-11]. Smaller stresses are typically generated during later processing stages, for instance, during the molding compound encapsulation process and thermal cycling reliability testing. In general, the die attach process comprises of the attachment of the die onto the lead frame and the curing of the bonding adhesive at an elevated temperature (> 100^oC) [18, 21]. Assuming a similar die attach process was used for the UQFN package under test, wherein an epoxy glue was applied to the Si die, and that the thermosetting adhesive crosslinks and hardens during the adhesive curing process, this most likely generates thermal stress upon cooling down to room temperature [7-11], as illustrated in Figs. 5e)-f). This stress occurs because the copper lead frame possesses a much larger CTE and is likely to undergo greater expansion at the time at which the Si die was bonded onto the copper lead frame and cured at an elevated temperature (> 100^oC). The thermal stress is formed upon cooling down the materials to room temperature as a result of the much faster shrink rate of the underlying copper lead frame, and the contraction force/compressive stress causes the central region of the Si die to warp. In contrast, the warpage is relatively low in the corners due to the fact that they were tightly bonded

to the copper lead frame by the glue, leading to the lattice deformation as observed by XRD/3DSM in Figs. 5a)-c).

The UQFN package was also investigated by SXRT in order to validate data obtained from XRD/3DSM. The $\bar{2}28$ large area back reflection (LABR) topograph of the UQFN package is shown Fig. 5d). The projection of the diffraction vector, $\vec{g}$ of the X-ray beam onto the plane of the recording film is represented by the arrow. The darker hemispherical features shows in the topograph are the diffracted intensity from the edges of warped Si die. These features are formed by orientation contrast phenomena due most likely to the deviation of the Bragg angle as a consequence of the strain-induced tilt of the diffraction planes [17]. Similar to the results from XRD/3DSM, the most highly distorted region is identified to be the centre of the Si die for which the diffracted intensity is "defocused" and recorded at different locations on the film. In addition, tilts in the Si towards the central regions of the edges of the die also lead to the apparent bowing of the recorded die edges as seen in the topograph (e.g. see Arrow A). The similar nature of the distortion observed from LABR topography confirms the XRD/3DSM results obtained from lab-based XRD measurements.

This warpage as a result of CTE mismatch of different materials would be expected to relax back if a thermal load is applied to the UQFN package. In order to verify and observe how the warpage of the Si die evolves as a function of temperature, we have performed *in situ* XRD annealing experiments using the Anton Paar heating stage at temperatures ranging from 25^{o}C to 115^{o}C in 30^{o}C steps, recorded at phi = 0^{o}. For each case, the RC FWHM maximum was extracted from the highly distorted centre and central edge regions of the UQFN package, as shown in Fig. 6a). The warpage (FWHM) was greatly reduced as the UQFN package was heated up from 25^{o}C (FWHM = ~0.19^{o}) to 115^{o}C (FWHM = ~0.09^{o}). These observations from *in situ*

XRD annealing experiments imply that thermal process-induced strain relief has occurred at elevated temperatures. The greater expansion rate of the underlying copper lead frame most plausibly relaxes the Si warpage. This same experiment was repeated on a second UQFN package, and the extracted FWHM of the highly distorted region is also shown in Fig. 6a). Repeat experiments consistently show a similar trend of tilt reduction as a function of temperature, and thus demonstrate a high reproducibility of results. The slight variation of warpage measured from both chips can be interpreted as due most probably to slight physical differences from chip-to-chip.

Importantly, the lab-based XRD technique can be used to quantitatively estimate the stress associated with warpage induced in each chip during the packaging process. This 'warpage stress' is biaxial stress ($\sigma_{xx} + \sigma_{yy}$) – the sum of stress from two in-plane directions due to the contraction forces, as previously discussed. The warpage stress can be calculated using the angular offset between the peak positions of RCs measured at two adjacent regions, using the following equation [26]

$$(\sigma_{xx} + \sigma_{yy}) = E[(t*\Delta\omega_{Bragg})/2\Delta d]$$

where E is the modulus of Si, t is the thickness of the chip, $\Delta\omega_{Bragg}$ and Δd are the peak position difference and the distance between two adjacent RCs which are recorded in the direction parallel to the incident X-ray beam, respectively. The warpage stresses across the whole Si die can also be reproduced using the same XRD/3DSM technique. These are demonstrated in Figs. 6b) showing maps of warpage-induced stresses across the entire Si die in the UQFN package measured at phi = 0^o and 90^o, in which the warpage stress is comparatively low around the corners of the Si die due to lower warpage or lattice misorientation, as previously discussed.

In order to verify the stress values of the *in situ* XRD annealing experiments, we have carried out FEA using Solidworks™. The 3D model used in the Solidworks™ simulations was sketched according to the physical dimensions of the UQFN package as summarised in Table I. The finite element model of the full UQFN package was created based on 65034 3D brick elements nodes and 41590 mesh elements to produce tetrahedral meshing, as depicted in Fig. 7.

The preliminary FEA simulations were performed using the following procedure:

Step 1- Sketching the 3D FEA model:

3D FEA model of the UQFN package (see Figs. 7) was sketched using the physical attributes summarised in Table I.

Step 2- Creating the deformed 3D FEA model:

Mechanical loading was applied to the die adhesive layer (in both x and y directions) in order to form a 3D FEA model with warpage (Fig. 8a) which is similar to that of experimentally measured results (see Fig. 8c) i.e. a stress of ~ 70 MPa at the central edge of the die (around the region indicated by red arrows in Figs. 8a & c). This deformed 3D FEA model was used as a model for a simulation study of temperature effects.

Step 3- Effect of thermal load:

Thermal load was applied to the deformed 3D FEA model in order to observe the transition of warpage inside the packaged chip. As an example, the simulation result at 115^{o}C is illustrated in Fig. 8b).

For comparison, the stress ($\sigma_{xx} + \sigma_{yy}$) extracted from simulations is compared to that of experimental results recorded at phi = 0^{o} (around the region indicated by the red arrow in Figs. 8a)-d), as shown in Fig. 8e). The excellent agreement between the simulation and experimental results confirms the aforementioned assumption where the underlying copper lead frame expands

more rapidly than that of Si die at elevated temperature, and compensates and relaxes the warpage generated initially during the die attach process. Therefore, it is believed that most of the stress appears to develop during curing of the die-attach adhesive, due to the difference in expansion of the Si die and lead frame, as reported by several authors [7-11].

3.2 Embedded QFN packages

Previous sections have demonstrated the concept of XRD/3DSM through the implementation of this technique for characterising die stress inside fully encapsulated UQFN packages. In order to demonstrate the feasibility of XRD/3DSM in characterising a packaged chip with a more complex structure, we have also applied this technique to investigate embedded QFN packages. In particular we have focussed on characterisation at two stages of embedded QFN manufacture, as shown in Fig. 2. During the first of these, copper metallisation, the Si die is laminated by a ~ 100 µm thick RCC dielectric layer and covered entirely by a copper layer.

i) Copper metallisation

Figs. 9a) show the XRD/3DSMs of a chip following copper metallisation recorded at phi = 0^o and 90^o, demonstrating lattice misorientation/deformation of (110) planes in the Si chip. For the embedded QFN package, the FWHM lines were recorded across the Si die using a step size of 200 µm, and therefore the resolution is higher relative to the XRD/3DSM of the UQFN packages, in order to reveal finer detail in the Si die for this more complex embedded package. From Figs. 9a)-b), it is obvious that a distinctive 'rippled' profile with a peak-to-peak pitch of 550 – 600 µm has developed up to or during this processing step. Lattice misorientations are higher around the edges of the Si die, corresponding to an estimated stress in the range ~ 90 MPa

- ~ 140 MPa. The development of these features is thought to be due either to the microvia laser drilling process or the vacuum lamination process.

In order to confirm this, an X-ray radiographic image of the chip after copper metallisation is shown in Fig. 9c). The X-ray radiographic image clearly demonstrates the cross-hatch pattern across the entire QFN package. This is almost certainly a result of the fibreglass weave pattern of the core substrate. The dimension of this cross-hatch pattern is measured to be ~ 550 - 600 μm, which correlates well to the peak-to-peak pitch of the 'rippled' profile observed from XRD/3DSM. Note, that while X-ray radiography reveals this ripple pattern, it is unable to quantitatively reveal stress, as XRD/3DSM can. The lattice deformation developed after copper metallisation is thought to be due to vacuum lamination process-induced stress, as these features are not consistent with the patterning of the microvias, which are located around the periphery of the Si die (see Fig. 9c). During the lamination process, the die bonded Si chip on the core substrate is covered from the top side with an RCC layer in a pressurised chamber. A pressure > 12 bar is required to ensure sufficient flow of the RCC dielectric in order to prevent the formation of voids around the chips [4]. It is likely that stress is generated during this process as a consequence of the use of high pressure. The Si chip will be pressed against the substrate due to the clamping force, leading to the development of a distinctive 'rippled' profile on the Si chip, following the fibreglass weave surface morphology of the core substrate.

ii) Structuring of conductor lines

The final processing step (see Fig. 2) of the embedded QFN package is the Cu structuring on the bottom side of the package. The XRD/3DSMs recorded at phi = 0^o, 90^o and the combination of both phi scans are shown in Figs. 10a)-c), respectively, clearly illustrating different types of lattice deformation/warpage have developed after this processing step. The stresses at the highly distorted regions are estimated to have increased slightly to ~120 MPa - 170 MPa, corresponding to the region marked by a red ellipse in the warpage map.

The large warpage developed after structuring of conductor lines is thought to be linked to manufacturing induced-stresses, which may result from two major factors. Firstly, the placement accuracy during the die bonding or die placement process has been reported to be one of the most crucial processes for chip embedding. This is because a small misalignment of chip position can potentially result in insufficient support from either the top or bottom surface of the chip [4, 17], and subsequently leads to warpage. In additional, the CTE mismatch between silicon and copper-filled TSVs can also induce thermo-mechanical stress, leading to material deformation, delamination and cracking in the packaged chip [5-6].

These findings have an important implication for the manufacturing induced stress development in Si die. Considering the UQFN or the embedded QFN packages under investigation, it is likely that manufacturing induced stress will impact on the reliability and functionality of the integrated devices that are fabricated on deformed Si [27-29]. Therefore, reduction of process-induced stress will be a fundamental issue that needs to be addressed for the realisation of high volume 3D IC integration technologies for future microelectronics. Diagnosing such stresses will also be key and laboratory-based XRD using 3DSM can serve as a straightforward, non-destructive and *in situ* characterisation methodology for providing detailed

information on the lattice warpage/strain developed in packaged chips including during crucial elevated thermal processing steps. Furthermore, unlike radiographic imaging, XRD/3DSM can quantitatively estimate stress values generated during the packaging process.

4. Conclusion

We demonstrate a novel laboratory-based X-ray diffraction analysis technique (XRD/3DSM) which can map major warpage features non-destructively in fully encapsulated packaged chips. Tilt direction and stress can also be evaluated separately, by using the rocking curve maps and peak deviations between rocking curves measured at two adjacent regions.

In the commercially available UQFN packages tested in this study, XRD/3DSM reveals that warpage is considerably lower at the corners of the Si die, but significantly larger at the central regions of the die. *In situ* XRD annealing experiments and FEA simulations confirmed that most of the stress is developed during the die attach process. In a second avenue of the study, changing lattice misorientation/warpage was revealed during different manufacturing process steps for embedded QFN packages.

XRD/3DSM is a promising methodology that can be used to gain a better understanding of the sources and distribution of strain inside packaged chips, and thereby help to improve the manufacturing efficiency, performance and reliability of advanced packaging products.

This transfer of our technique from a synchrotron X-ray source environment to a laboratory tool makes such lab-based non-destructive imaging and evaluation of warpage/strain characterisation of Si wafer die inside packaged SoC/SiP using XRD/3DSM a realistic possibility within a fab environment.

Acknowledgments

This work was supported by the EU FP7 MNT ERA-Net 'ENGAGE' project with local support from Enterprise Ireland. PMN also acknowledges the support of the 'INSPIRE' programme, funded by the Irish Government's Programme for Research in Third Level Institutions and Science Foundation Ireland's 'Precision' Strategic Research Cluster (08/SRC/I1411).

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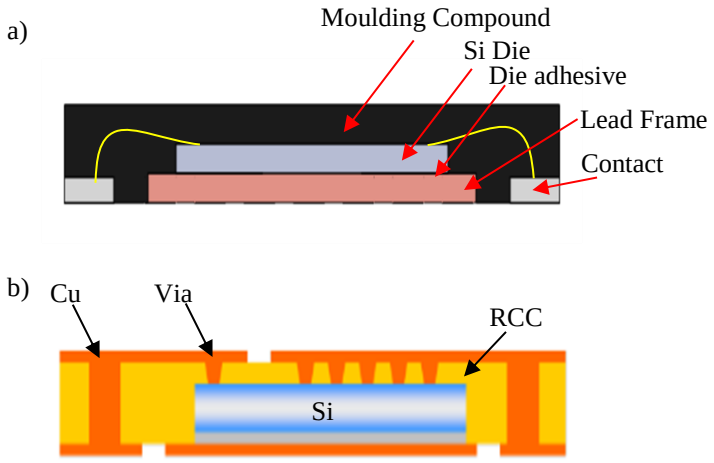


Fig. 1. Cross-sectional schematic diagram for the a) UQFN package, and b) embedded QFN package. Dimensions are described in the text and in Table I.

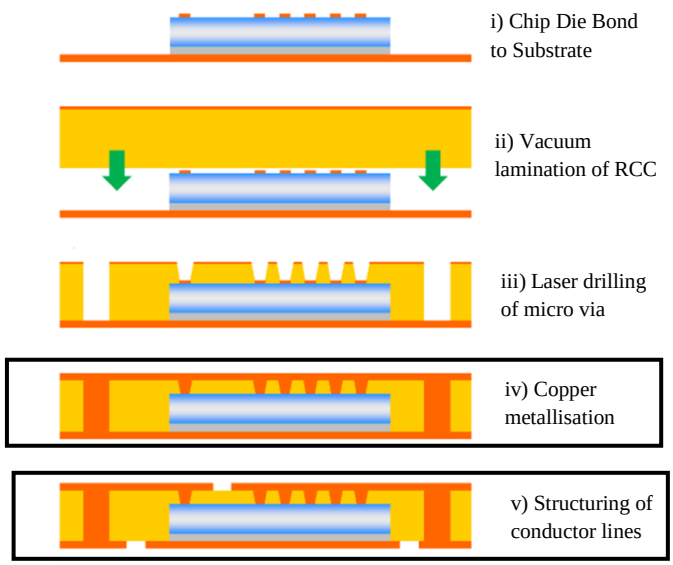


Fig. 2 Schematic diagram showing the process sequence of embedded QFN package [12].

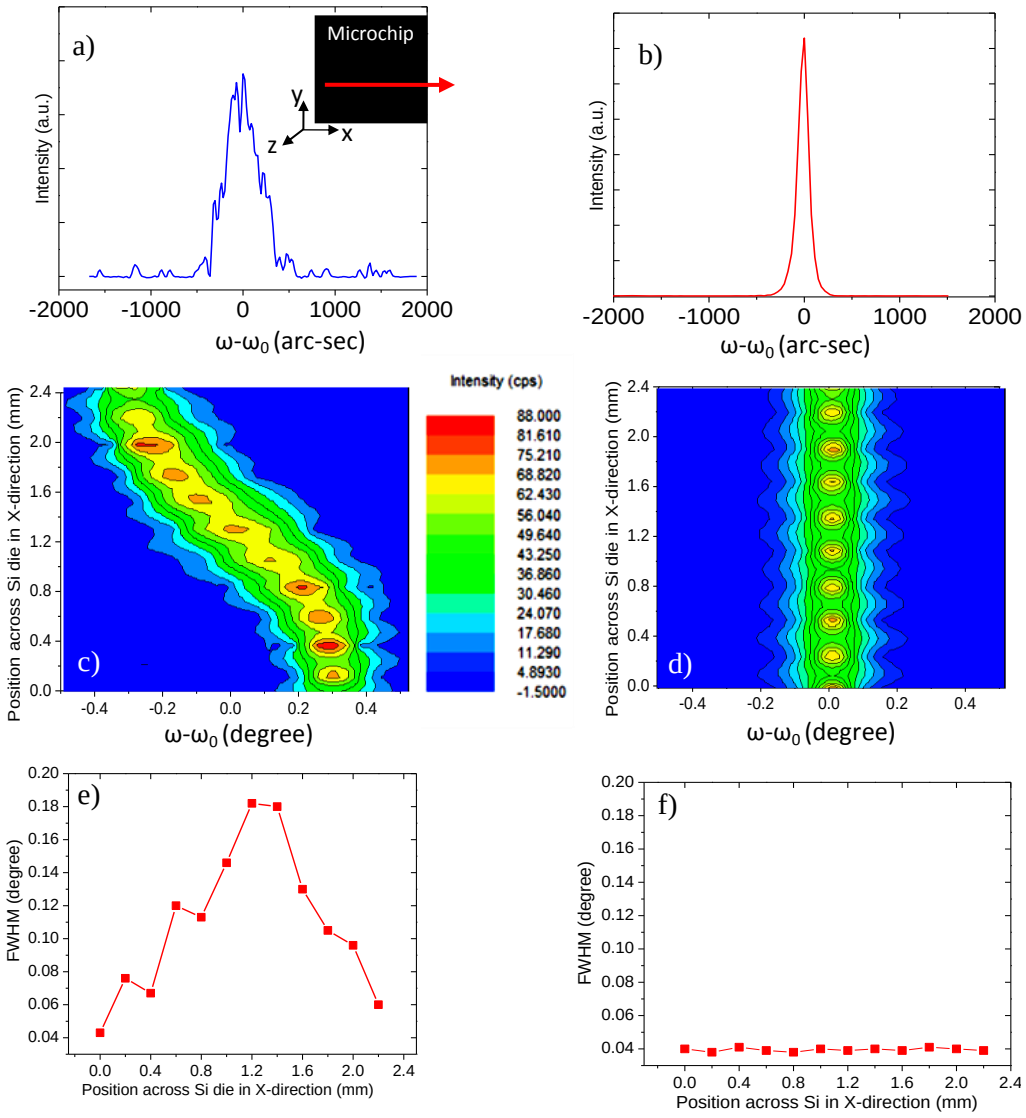


Fig. 3 004 Rocking curves of a) a warped Si die and b) a 'perfect' Si specimen without warpage. Figs. 3c)-d) are the RC maps across the Si die in a packaged chip and the Si specimen in the x-direction, respectively. The FWHM line scans from the RC maps are shown in Figs. 3e)-f).

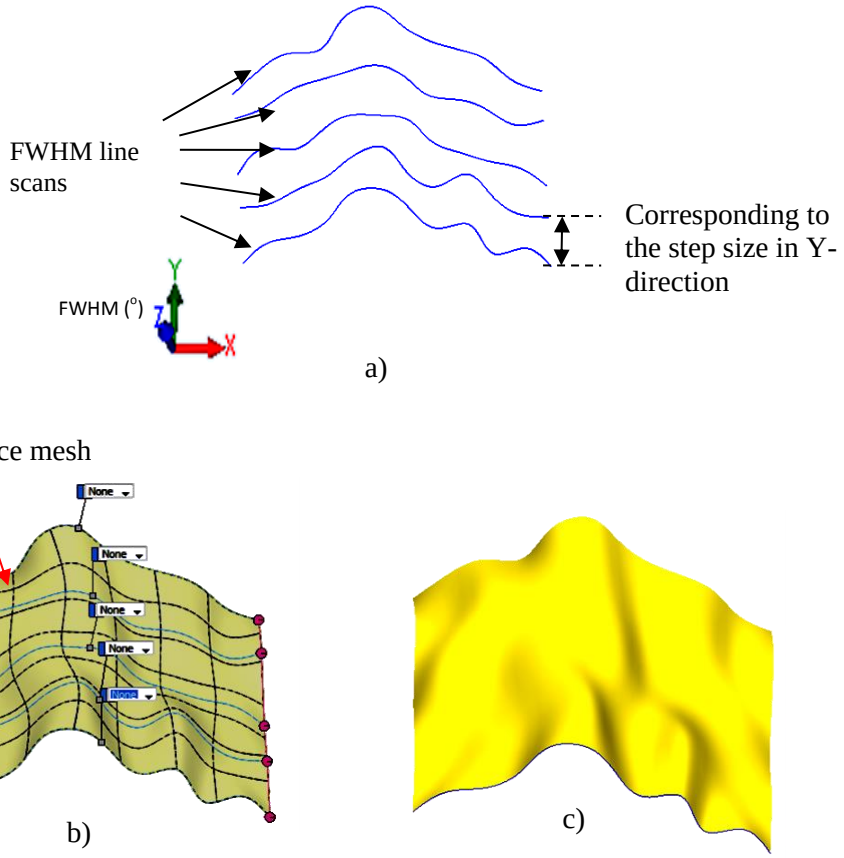


Fig. 4 a) A series of FWHM line scans recorded at phi = 0^{o} are imported into Solidwords^{TM}, b) Boundary surface feature used to connect FWHM line scans, and c) A solid surface model of XRD/3DSM, demonstrating the lattice misorientations of the (110) plane in an example Si die inside a fully encapsulated packaged chip.

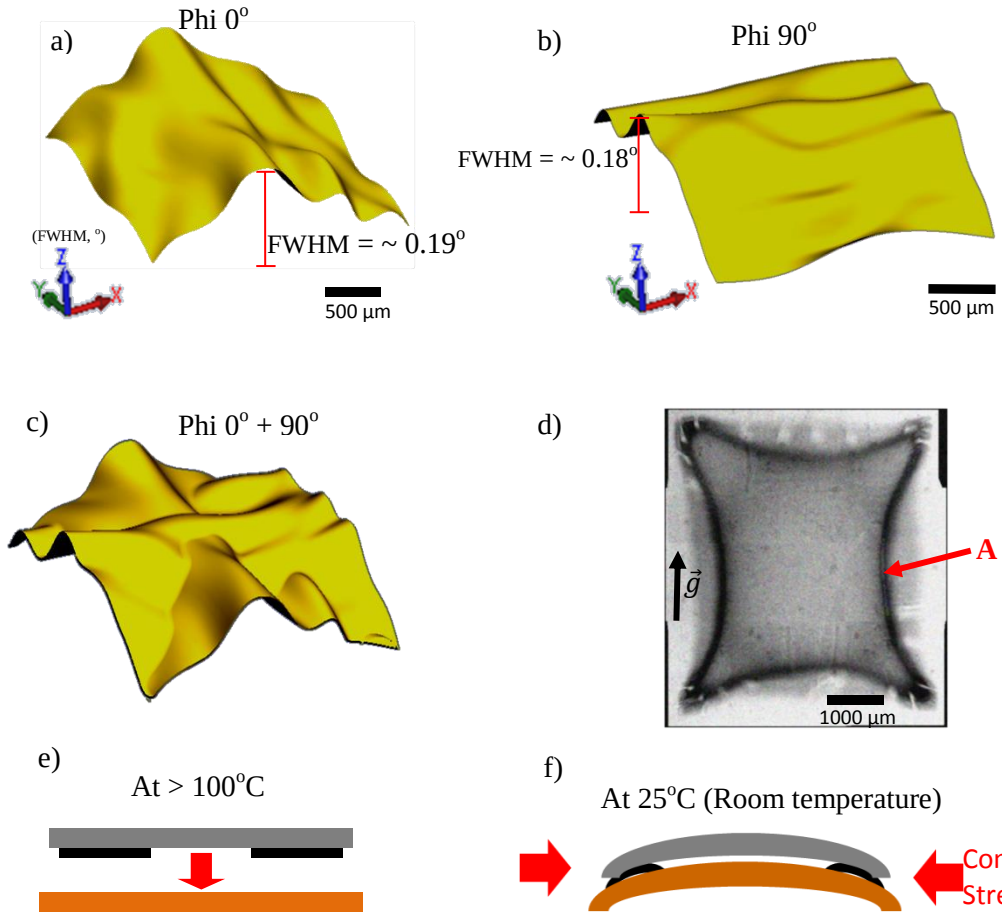
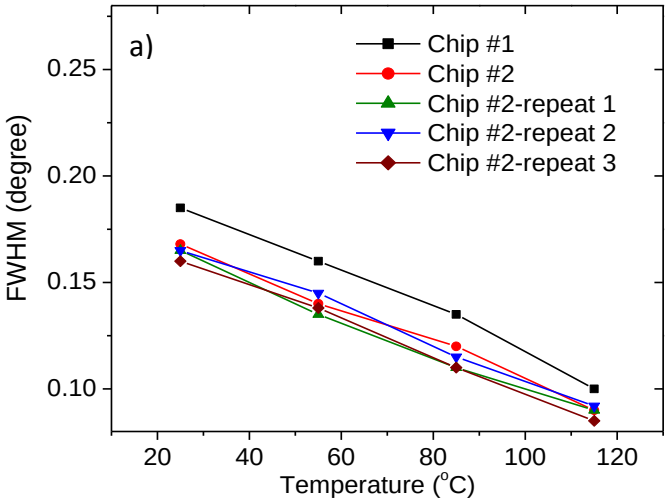


Fig. 5a)-c) are the XRD/3DSMs of the UQFN package recorded at phi = 0°, 90° and combination of phi = 0° and 90°, respectively, and d) is the $\bar{2}28$ large area back reflection topography of the UQFN package. Figs. 5e)-f) demonstrate schematically the formation of warpage by thermal stress due to CTE mismatch between different materials.



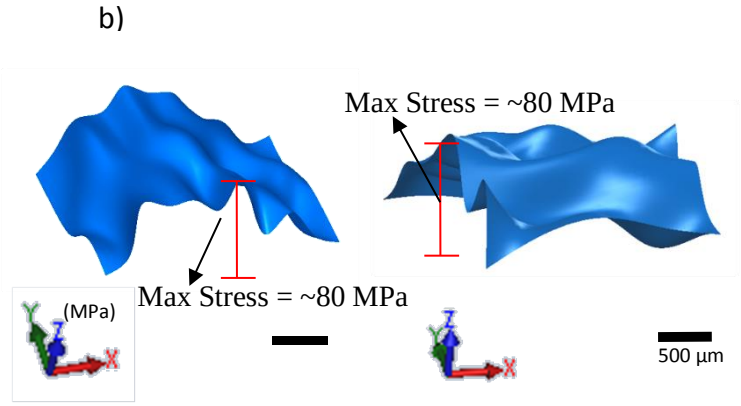


Fig. 6a) The extracted RC FWHM as a function of temperature recorded at phi = 0^{o}, illustrating the reduction of warpage in packaged chips as temperature increases. b) XRD/3DSMs showing the distribution of warpage induced stresses across the whole Si die recorded at phi = 0^{o} and 90^{o} (left/right).

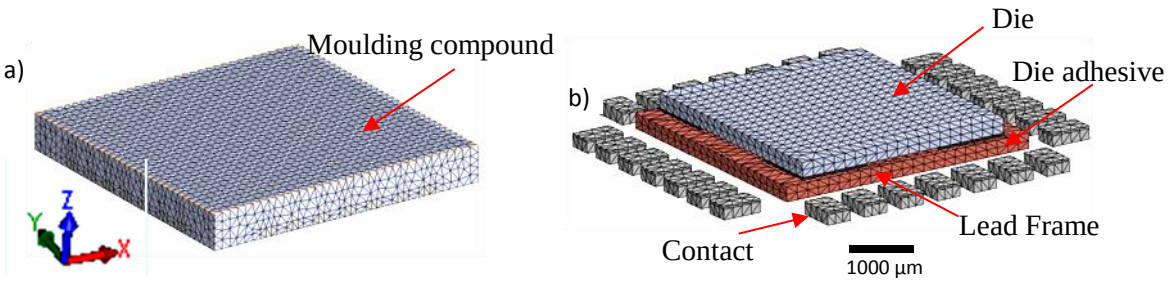
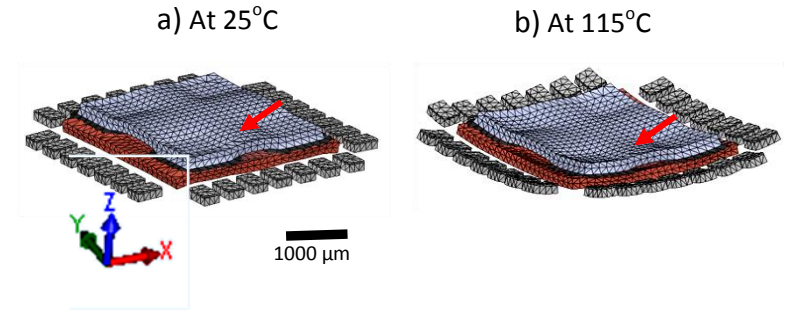


Fig. 7 The 3-dimensional FEA model of the UQFN package used in this study a) Fully encapsulated UQFN package, and b) The cap is hidden for ease of comparison.

Simulation Results –

Deformed 3D FEA models of the fully encapsulated UQFN package. Note that, the cap is hidden for ease of comparison.



Experimental Results –

XRD/3DSMs of UQFN package at phi = 0°

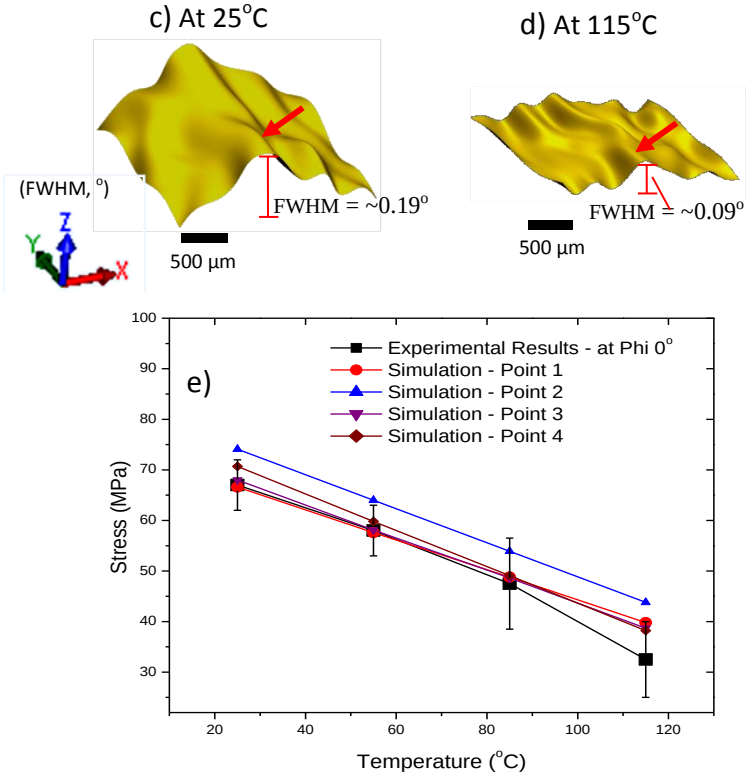


Fig. 8 Transition of warpage in the packaged chip as a function of temperature. a) Deformed 3D FEA model at 25°C, b) Deformed 3D FEA model at 115°C, c)-d) are the XRD/3DSMs at phi 0° obtained from lab-based XRD measurements at 25°C and 115°C, respectively. e) Effect of temperature on the stress transition in a silicon. The stress is measured and calculated around the position marked by the red arrows in a)-d)**.**

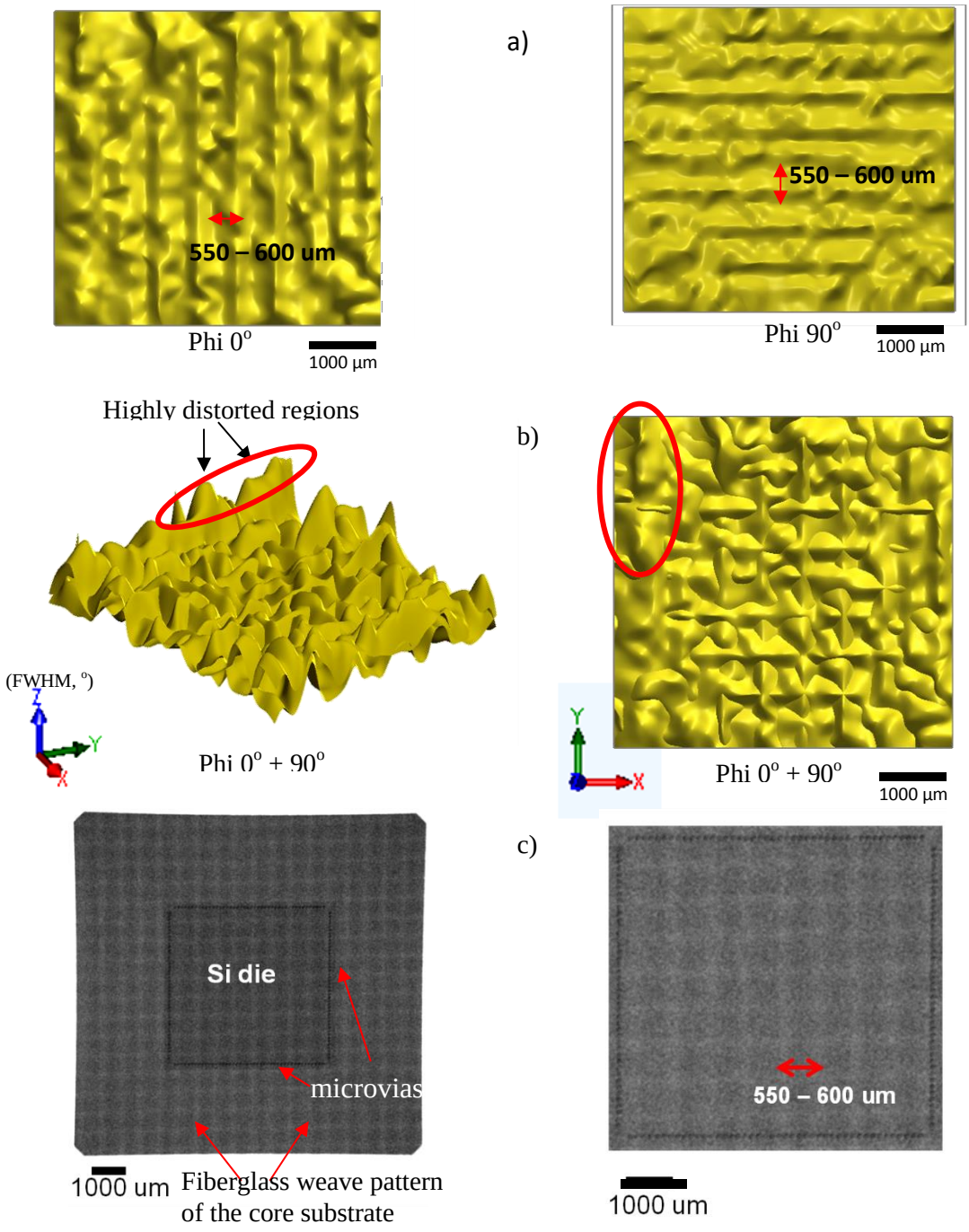


Fig. 9a) XRD/3DSM of a QFN chip recorded at phi = 0° and 90° (left/right), illustrating lattice deformation of the (110) planes in the Si chip after copper metallisation, and b) The combination of XRD/3DSM recorded at phi = 0° and 90°, from different viewpoints (left/right). c) X-ray radiographic image of package after copper metallisation showing the embedded chip and microvias located around the edges of the embedded Si die (right, shows a magnified view of the centre of the left image).

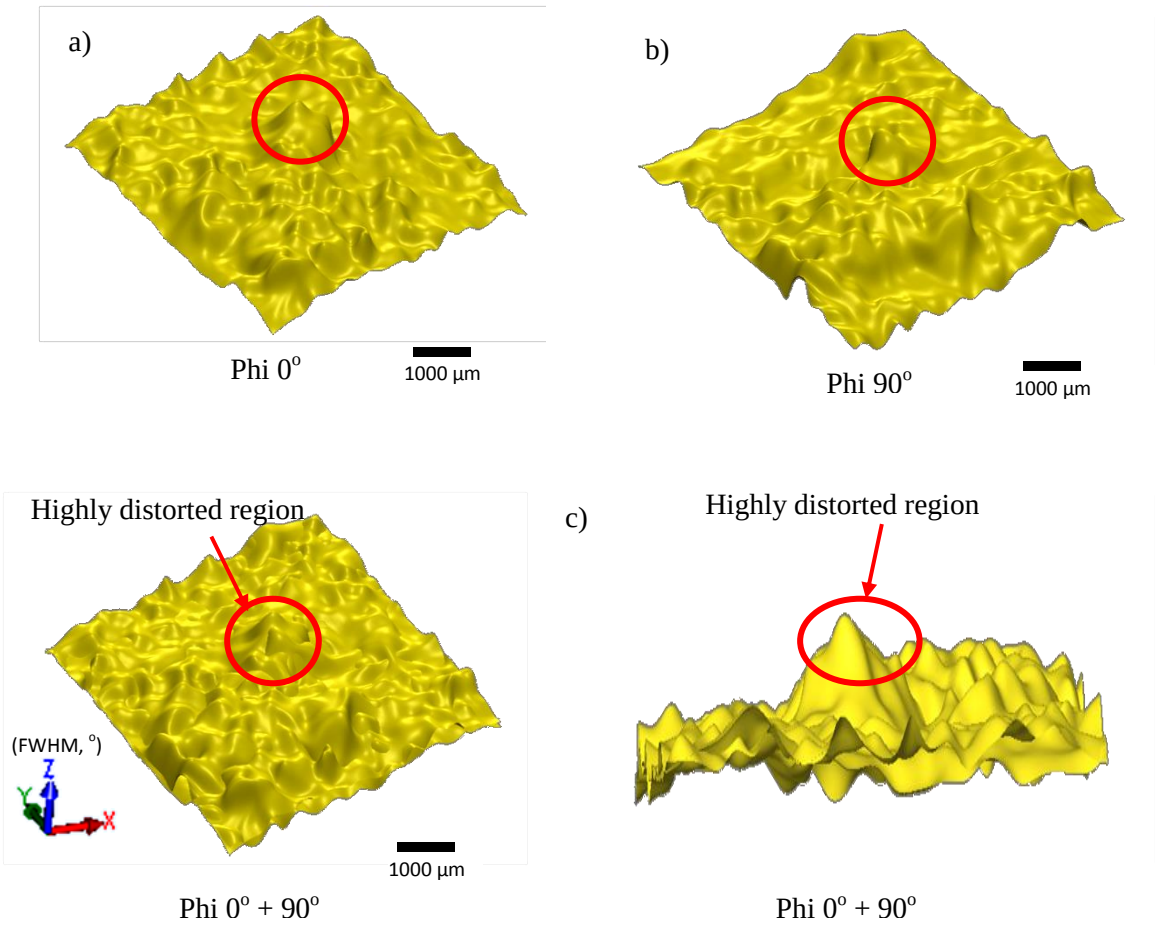


Fig. 10a) XRD/3DSMs recorded at phi = 0^{o} and 90^{o} (left/right), respectively, showing warpage/lattice deformation of the (110) planes inside the packaged chips after the structuring of conductor lines, and c) are the combination of XRD/3DSMs recorded at two different phi, from different viewpoints (left/right).

Table I. UQFN package physical attributes.

Attribute	**Materials**	**Dimension, mm**		
		Width	**Length**	**Height**
Lead frame/Exposed pad	Copper alloy	2.80	2.80	0.150
Die adhesive	Silver Epoxy	0.70	0.70	0.025
Die	Silicon	2.20	2.40	0.150
Cap	Epoxy Resin	4.00	4.00	0.175
Overall dimension		4.00	4.00	0.500

Table II. Embedded QFN package physical attributes.

Attribute	**Materials**	**Dimension, mm**		
		Width	**Length**	**Height**
Lead frame/Exposed pad	Copper	10.00	10.00	0.100
Die adhesive	Die attach film	5.00	5.00	0.020
Die	Silicon	5.00	5.00	0.050
Cap	Resin-coated-copper	10.00	10.00	0.100
Overall dimension		10.00	10.00	0.270

Table III Properties of materials used in FEA simulation.

Attribute	**Materials**	**Young's modulus (GPa)**	**CTE (10^{-6}/K)**	**Poisson's ratio**
Lead frame/Exposed pad	Copper alloy	110	24	0.370
Die adhesive	Silver Epoxy	12	65	0.394
Die	Silicon	169	2.69	0.3
Cap	Epoxy Resin	2.4	55	0.35