Dublin City University

School of Physical Sciences

Fabrication and characterisation of copper diffusion barrier layers for future interconnect applications

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Doctor of Philosophy

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Supervised by Professor Greg Hughes

Declaration

I hereby certify that this material, which I now submit for assessment on the programme of study leading to the award of doctor of philosophy is entirely my own work, that I have exercised reasonable care to ensure that the work is original, and does not to the best of my knowledge breach any law of copyright, and has not been taken from the work of others save and to the extent that such work has been cited and acknowledged within the text of my work.

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Dedications and Acknowledgements

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Publications arising from this work

Chemical and electrical characterisation of the segregation of Al from a CuAl alloy (90%:10% wt) with thermal anneal.

C. Byrne, A. Brady, L. Walsh, A.P. McCoy, J. Bogan and G. Hughes

Thin Solid Films (under review)

Cu diffusion barrier effectiveness of a CuAl alloy (90%:10% wt) for interconnect applications

C. Byrne, R. Lundy, B. Brennan, A.P. McCoy, J. Bogan and G. Hughes

(Complete, awaiting submission)

In-situ XPS chemical analysis of $MnSiO_3$ copper diffusion barrier layer formation and simultaneous MOS fabrication

C. Byrne, B. Brennan, J. Bogan, G. Hughes and A.P. McCoy

ACS Applied Materials & Interfaces (under review)

Photoemission study of the identification of Mn silicate barrier formation on carbon containing low-k dielectrics

J. Bogan, A.P. McCoy, R. O'Connor, P. Casey, C. Byrne and G. Hughes

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The impact of porosity on the formation of manganese based copper diffusion barrier layers on low-k dielectric materials

A.P. McCoy, J. Bogan, L. Walsh, C. Byrne, R. O'Connor, G. Hughes and J. Woicik

Journal of Applied Physics (D), (accepted and awaiting publication)

Conference Proceedings

Spin on porous low-k carbon doped oxides for future interconnect technologies

C. Byrne, R. Lundy, S. Daniels and G. Hughes

Intel Ireland Research Conference (IIRC) (2013), Clontarf Castle, Dublin 21st – 22nd November 2013

Aluminium based self-forming copper diffusion barriers for future interconnect technologies

C. Byrne and G. Hughes

Oral presentation, Intel Ireland Research Conference (IIRC) (2014), The Science Gallery (Trinity College Dublin), 18th November 2014.

Characterisation of a CuAl alloy for future interconnect technologies

C. Byrne, A.P. McCoy, J. Bogan, A. Brady and G. Hughes

International Interconnect Technology Conference (IITC) and Materials for Advanced Metallization Conference (MAM), Grenoble (2015)

Contents

Fabrication and characterisation of copper diffusion barrier layers for future interconnect applications.

Conor Byrne

Abstract

The focus of this thesis is the fabrication and characterisation of ultra-thin self-forming Cu diffusion barrier layers for future interconnect technologies. These barrier layers form by the chemical interaction of an expelled metal from a copper alloy with the surface of a dielectric material to form a stable chemical species suitable for integration into future interconnect fabrication strategies. Studies of both manganese and aluminium as the alloying elements were undertaken and the characterisation techniques included x-ray photoelectron spectroscopy (XPS), transmission electron microscopy (TEM), x-ray absorption spectroscopy (XAS) and secondary ion mass spectroscopy (SIMS). Electrical characterisation measurements used to establish the effectiveness of the barrier layers at preventing copper diffusion were performed on fabricated metal-oxide-semiconductor (MOS) structures. A novel approach involving interface chemistry studies and MOS device fabrication on the same dielectric substrate was successfully demonstrated. Barrier formation on a range of prototype low-k dielectric materials with different carbon concentrations and porosities were undertaken and surface chemical modifications prior to barrier layer formation were also investigated. The results show that both Mn and Al are effective at preventing copper diffusion into SiO_2, but the inherent porous structure of low-k dielectrics present significant challenges to barrier layer formation, particularly at the dimensional range required for future technology nodes.

1 Introduction

1.1 Background

In 1965 Gordon Moore, co-founder of Intel, made one of the most famous technological observations in semiconductor history [1]. Moore noted that since production of the first integrated circuit (IC) chips in 1958, every two years the number of on-chip components had doubled and predicted that this trend would continue to advance the emerging semiconductor device industry.

This prediction has led to a manufacturing template which has been used to relentlessly drive the industry towards smaller and smaller feature sizes, thereby creating faster and cheaper IC chips for device integration. This growth in technological advancement coupled with lower cost and decreased power consumption has allowed mankind to explore, communicate, discover and invent at an ever increasing rate. From the first Moon landings in 1969, to the modern communication network of satellites and high speed server farms, the impact of increasingly complex computing power has been wide ranging. With mobile technology, anyone at virtually any location on the planet using a device no bigger than the palm of a human hand can access internet technology. Thus it can be seen that Moore's law has changed the way we live our lives in the developed world making it quite possibly one of the most dramatic observations made by a human in the history of mankind.

The current world leader in IC production is the Intel Corporation which adopts Moore's law in the famous "Tick-Tock" cycle [2]. This cycle begins with a "die-shrink" (tick) of

a previous generation of IC chip, thereby reducing feature sizes of on-chip components. The second part of the cycle is the "tock" stage where the on-chip feature size remains constant, but a change in on-chip architecture is made, thereby squeezing as much performance from the previous "tick" stage as possible, before the next die-shrink (tick) stage. From the first commercial microprocessor IC chip produced, the Intel 4004, with feature sizes of 10,000 nm to the currently developed Intel Skylake Core i7 (the "tock" to the released 14 nm Broadwell die-shrink) microprocessor with feature sizes of 14 nm, Intel have dominated the market. This downward trend in feature sizes has allowed more and more devices to be fabricated on a single IC chip, from the Intel 4004 with a transistor count of 2,300 to the currently available Intel 10 core Xeon Haswell-EP with a record breaking 5.5 billion transistors, showing that the modern IC transistor count is almost 2.4 million times that of the initial IC chip produced (give or take a few million transistors). To put this in perspective, the current Intel 10 core Xeon Haswell-EP processor is roughly the size of the nail on a small finger, but within that area there is a transistor for every man, woman and child on the face of the Earth.

This dramatic increase in transistor count, with parallel reduction in feature sizes has been possible only with intensive research in the areas of materials growth, deposition, photolithography, patterning, etching and engineering [3]. Thus the semiconductor field has been one of the most intensely researched scientific disciplines in the history of applied physics. Issues encountered during die-shrinking require intense research, traditionally related to the famously small transistors. However in recent years, research has begun to be increasingly focus on the interconnects, which essentially wire-up the transistors in a well-defined way. This is because performance bottlenecks are emerging due to the increasing complexity of interconnect fabrication.

The focus of the research work carried out in this thesis is on the back end of line (BEOL) where the interconnect structures are located. The continuous reduction in dimensions demands the fabrication of smaller and smaller interconnect structures and requires an intensive research effort if the projected performance improvements are to be realised [3].

1.2 RC time delay

As stated previously one of the current challenges to improve device performance is found in the complexity of the BEOL interconnect stage of the IC chip as schematically shown in Figure 1.1. BEOL processes are concerned with the wiring of the transistors, which are fabricated in the front end of line (FEOL) process, to relay the digital signals in the IC chip. As seen in Figure 1.1, the structure of interconnects consist of a metal conduction line primarily copper, surrounded by an insulating material known as the inter-layer dielectric (ILD).

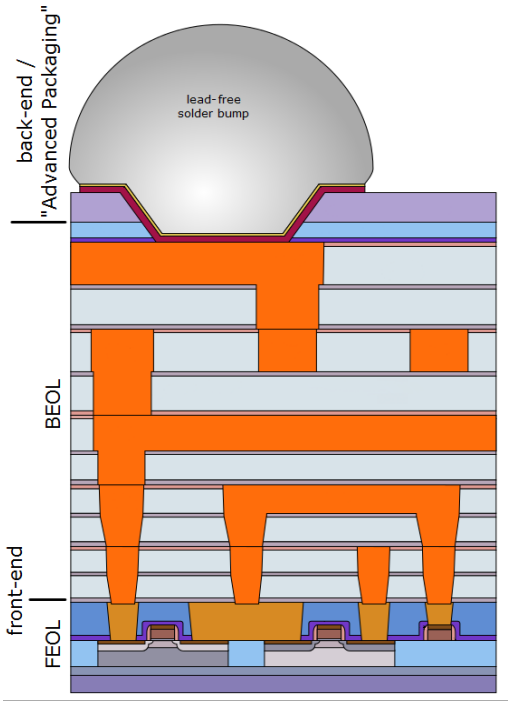

Figure 1.1: Side on schematic of a modern IC chip, displaying both FOEL and BEOL segments [4].

In order to demonstrate the issues with BEOL interconnects, an explanation of resistive-capacitive (RC) time delay must be presented. The switching frequency of an interconnect structure is determined by the RC time delay of the structure, given by:

$$\tau = R.C$$

Equation 1.1: RC time delay equation.

where R is the resistance of the metal wire and C is the parasitic capacitance between parallel metal wiring structures, separated by the ILD material. The resistance of the interconnect wire can in turn be given as:

$$R = \frac{\rho L}{A}$$

Equation 1.2: Resistance of an interconnect wire.

where R is the resistance of the interconnect wire, L is the length of the wire, A is the cross-sectional area of the interconnect wire and ρ is the intrinsic resistivity of the conducting material used. Thus it can be seen via Equation 1.2 that as the cross-sectional area (A) decreases due to die-shrinking, the overall resistance of the interconnect structure increases, in turn increasing the delay in switching speeds as given in Equation 1.1.

In addition to an increase in RC delay due to an increase in resistance, the delay time can increase due to an increase in parasitic capacitance between interconnect lines following die-shrinkage. As seen in Figure 1.2, two adjacent metal lines can be modelled as a parallel plate capacitor structure.

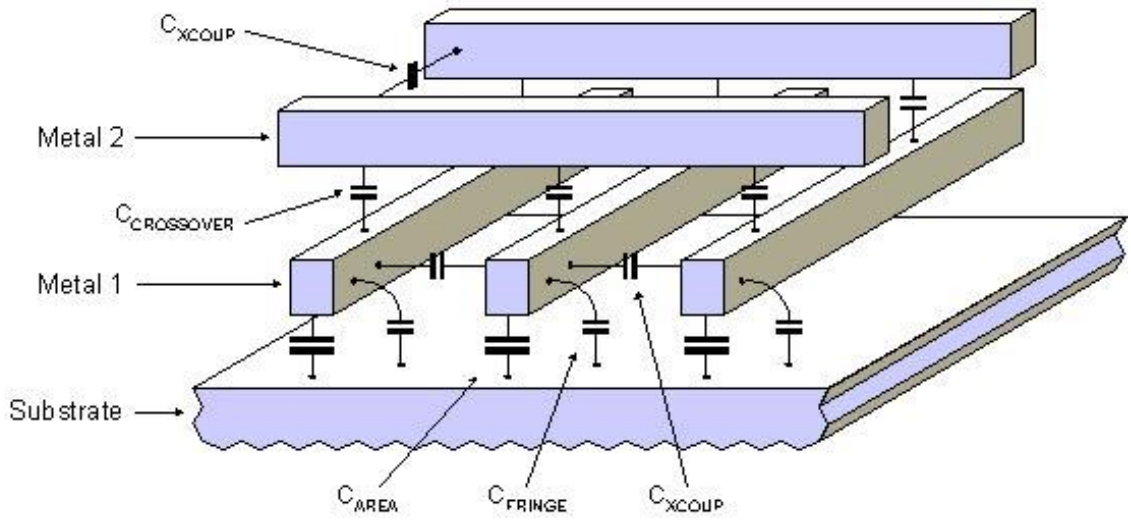

Figure 1.2: 3D representation of the parasitic capacitance between adjacent metal interconnect structures [5].

The capacitance between two interconnect lines, with an ILD material between them can be expressed via the parallel plate capacitor equation, given as:

$$C = \frac{\varepsilon A}{d}$$

Equation 1.3: Parallel plate capacitor equation.

where C is the capacitance between two metal plates of common cross sectional area A, separated by a distance d, with a material dielectric constant of ϵ. Therefore as interconnect lines are fabricated closer together due to die-shrinking, the parasitic capacitance between the lines increases, in turn increasing the RC time delay of the interconnect structure overall.

Thus it can be seen that the process of die-shrinking negatively impacts on the RC time delay of the interconnect lines, causing a decrease in switching speeds of the device

overall and potentially resulting in an increase in power consumption due to an increase in the resistance of the interconnect lines. As can be seen via Equation 1.2 and Equation 1.3, the only controllable factors available to combat the increase in RC time delay, are to lower the intrinsic resistivity of the metal in the conducting line and/or to decrease the electrical permittivity factor of the ILD material. Both of these approaches will be discussed below.

1.3 Copper as an interconnect material

Traditionally, aluminium (Al) was used as the interconnect metal of choice due to its low resistivity (28.2×10^{-9} Ω-m) and ease of deposition, etching and patterning to form interconnect lines. With the relentless shrinking of interconnect structures in accordance with Moore's law, the use of aluminium became too resistive a material to use as the interconnect metal line. Consequently, a change was needed to a lower resistivity material, however given the already low resistivity value of aluminium (28.2×10^{-9} Ω-m), few choices were available to integrate as a new metal line, namely gold (24.4×10^{-9} Ω-m), copper (16.8×10^{-9} Ω-m) or silver (15.9×10^{-9} Ω-m) [6]. Due to the expense of using either gold or silver, copper (Cu) became the interconnect metal of choice. With the change to Cu came a number of advantages most notably, a decrease in interconnect resistivity and consequently a decrease in power consumption. In addition there was increased resistance to electromigration failure, compared to aluminium. . However, along with the benefits to the change in Cu also came a number of disadvantages such as the tendency for Cu diffusion into any surrounding ILD materials, poor adhesion of Cu to ILD materials and the less pronounced but still present electromigration issues especially with increased current density as a result of die shrinking [7].

1.3.1 Ta/TaN Cu diffusion barrier

As stated previously, with the change to Cu as the metal interconnect of choice came the issue of Cu diffusing into any surrounding silicon oxide based ILD materials. This issue if left unaddressed would eventually lead to interconnect device degradation and ultimately failure of the interconnect lines due to electrical shorting of the structures. Additionally Cu has been shown to cause deep level traps in Si, indicating that if any Cu were to diffuse into electrically active devices in the FEOL such as transistors, it would cause device failure. Thus the need for a physical barrier layer between the Cu metal line and ILD material became evident. The barrier stack currently in use for containment of Cu in the conducting lines is a dual layer of Ta/TaN. The need for a dual layer is due to the fact that although TaN is a good Cu diffusion barrier, Cu does not adhere well to it, thus an interlayer of Ta is placed between the TaN and Cu materials as seen in the microscopy image in Figure 1.3.

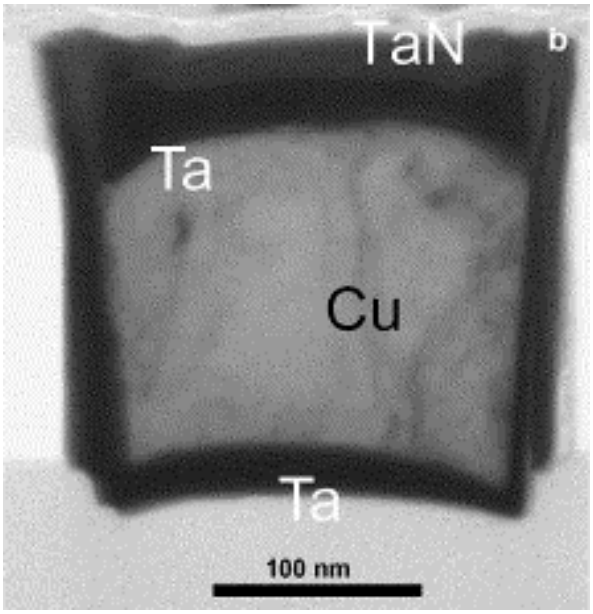

Figure 1.3: Cross sectional scanning electron microscopy (SEM) image of a Cu / Ta / TaN / ILD interconnect structure [5].

As interconnect structures continue to shrink in dimensions in accordance with Moore's law, the current Ta/TaN barrier arrangement has been difficult to correspondingly scale. Therefore, for future scaled structures, it would occupy too much of the volume available in the interconnect line, minimising the volume of Cu thereby causing an increase in interconnect resistance. In addition the physical vapour deposition (PVD) method of sequentially depositing these layers makes it difficult to obtain uniformly deposit barriers on increasingly high aspect ratio structures. Thus a new paradigm of barrier layer is needed to replace the relatively thick current Ta/TaN dual layer. The new barrier layer solution must be ultra-thin (~ 5 nm) in order to maximise volume available for Cu in the conducting line, promote adhesion between the Cu and ILD material and also prevent Cu from diffusing into the surrounding ILD material.

1.3.2 Electromigration of Cu

Electromigration is the phenomenon of conducting material moving or distorting during electrical current transport. This physical phenomenon is problematic for IC interconnect structures due to the fact that it can result in the formation of voids within metal lines. When a metal line such as an interconnect carries an electrical current, an "electron wind" is generated in the metal. This "electron wind" can collide with metal atoms in the conducting lines of the structure (especially at grain boundary sites) and cause them to move or migrate to other regions. This in turn can create voids within the conducting line as can be seen in Figure 1.4 [8]. Aluminium was particularly prone to electromigration failure due to the relative low mass of single Al atoms. With the switch to Cu (higher mass value), electromigration is reduced however it is still problematic due to die shrinking [7] as the increased current density within the conducting lines increases the probability of electromigration. Poor adhesion between the copper and the surrounding

dielectric material can also lead to significant electromigration effects. Therefore the need for a barrier material with strong adhesion between the conducting metal line and ILD becomes increasingly important as line dimensions continue to shrink.

In an effort to minimise electromigration, the Al can be alloyed with Cu in the interconnect line. This process causes the Al to segregate to the grain boundaries in the Cu metal which greatly reduces electromigration problems by minimisation of movement of Cu atoms at the grain boundaries [9].

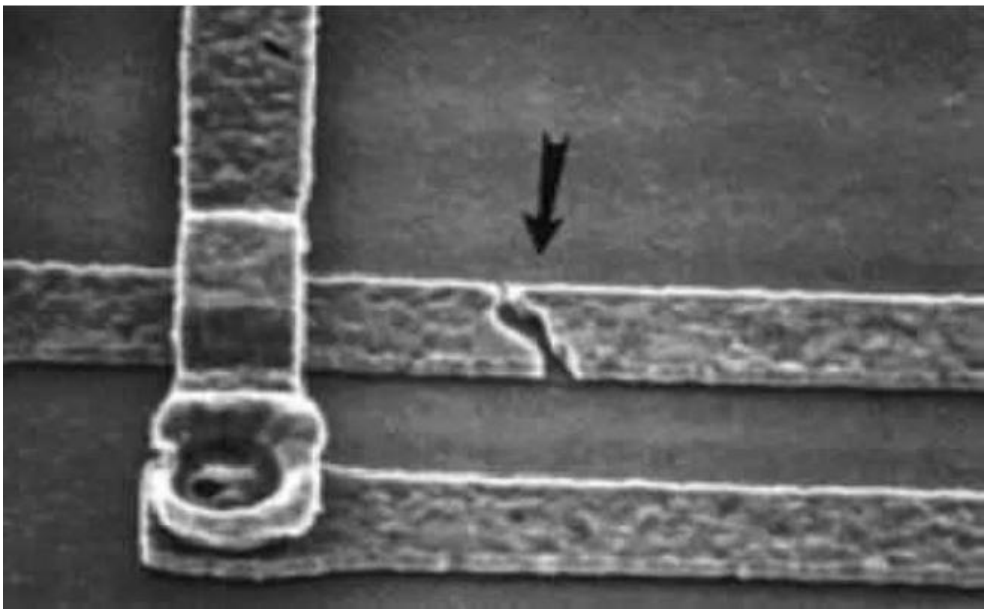

Figure 1.4: SEM imaging of a Cu interconnect line failure due to electromigration [4].

1.4 Low-k materials

Equation 1.1, the RC time delay factor can also be lowered by lowering the parasitic capacitance between the conducting metal lines within an IC chip. The capacitance between two interconnect lines can be modelled by the parallel plate capacitor as seen in Equation 1.3. Therefore, the smaller the distance between the conducting lines, the larger the capacitance. This is problematic in terms of die shrink as the metal lines are located

closer and closer to each other. The only variable that could be changed to lower the capacitance during die shrink is the dielectric constant - ε. By lowering the dielectric constant of the ILD, the capacitance overall will be lower and thus the RC time delay will also be reduced. The k-value of a material is defined as the electrical permittivity of the material divided by the electrical permittivity constant of free space, as given in Equation 1.4:

$$\kappa = \frac{\varepsilon_{material}}{\varepsilon_0}$$

Equation 1.4: k value equation for a dielectric material.

where k is the k-value of the material, $\varepsilon_{material}$ is the electrical permittivity of the material and ε_0 is the electrical permittivity of free space (8.85×10^{-12} F/m). When the values for silicon dioxide (SiO_2) are used, the k-value for SiO_2 is found to be ~ 3.9. This value is used as the bench mark for low-k materials as anything which is defined as low-k must have a lower k-value than 3.9. Dielectric materials such as SiO_2, when placed in an electric field, can be polarised as schematically illustrated in Figure 1.5. When no electric field is placed across the dielectric, the orientation of the dipoles in the molecules are in a random orientation, with the sum of the fields equating to zero. When an external electric field is applied to the dielectric, the dipoles in the material distort and orientate into a position as shown in the lower half of Figure 1.5. The degree to which these molecules distort and orientate can be equated to the k-value of the material. Thus, if a material has a high k-value, a larger shift in dipole and orientation will be seen in comparison to a material of lower k-value. Due to the fact that a large shift in dipole under an applied electric field will give rise to a large capacitance overall, it can be seen that the

k-value of the material is related to the capacitance of the material i.e. a large k-value will give rise to a larger capacitance than a lower k-value material of similar dimensions. This can be shown when Equation 1.3 and Equation 1.4 are combined to yield Equation 1.5 which shows the dependence of capacitance on k-value.

$$C = \frac{\kappa \varepsilon_0 A}{d}$$

Equation 1.5: Parallel plate capacitance equation with k-value dependence.

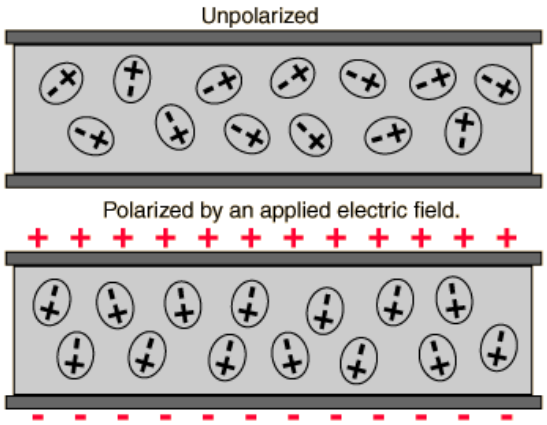

Figure 1.5: Electrical polarisation of a dielectric material under applied voltage [10].

Thus, if the capacitance of the material is dependent on the electrical polarisability, by changing the material to a lower k-value, the parasitic capacitance of interconnect lines can be reduced thereby lowering the RC time delay.

One of the methods used in developing low-k materials was to replace some of the high polarisable Si-O bonds in SiO_2 with less polarisable bonds such as silicon-carbon bonds. Thus by introducing carbon into the dielectric material, the k-value and in turn the

resulting capacitance should be lowered. These materials are usually referred to as CDO (carbon doped oxide) materials. The general schematic structure of these materials can be seen in Figure 1.6. With the addition of lower polarisable carbon bonds, it is possible to reduce the k-value to as low as ~ 2.5 [11]. While SiO_2 was the original ILD of choice, manufacturing has shifted its sights to CDO materials such as Black Diamond ™which was developed by Applied Materials (AMAT) and Aurora CDO ™ which was developed by ASM international.

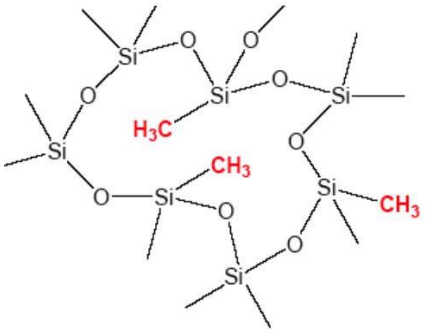

Figure 1.6: Structure of a CDO dielectric [12].

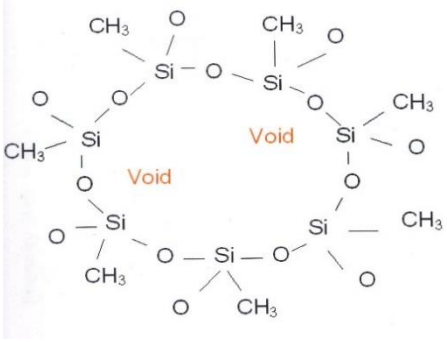

Figure 1.7: Structure of a CDO dielectric with voids [12].

By definition from Equation 1.4, the lowest k-value that can be achieved is a k-value of 1, which is that of a vacuum, although air has a similar k-value. Therefore by the introduction of voids in the dielectric material the overall k-value of the material will be lowered. This has been achieved using SiO_2 and even CDO materials to further push the k-value downward in an effort to reduce parasitic capacitance [13]. An example of a structural makeup of a CDO material with induced voids is presented in Figure 1.7. As can be seen, the chemical makeup of the dielectric is identical to that of the initial CDO layer in Figure 1.6, however the existence of voids in the material lowers the overall k-value of the dielectric.

In addition to the decrease in k-value and the RC time delay achieved with these materials, a set of challenges must be met. These challenges range from manufacturing difficulties due to the fact that these materials typically have a lower Young's modulus than traditional ILD materials meaning that they can be damaged easily during processing [14]. Further to physical damaging of the dielectric, the chemistry of these new carbon doped oxides means that any materials used in conjunction with them must not react in an undesirable way such as metal carbide formation at any metal-dielectric interface [15]. The introduction of voids to these materials also presents a fast route for any metals, especially Cu, to diffuse quickly through the porous material [16,17].

1.5 Self-forming Cu diffusion barrier

As described previously, the current method of preventing the Cu diffusion into the surrounding ILD material is by way of a TaN/Ta barrier. If this barrier could be scaled down while still retaining good Cu diffusion and adhesion properties it would allow more room in the interconnect trench for Cu leading to a decrease in line resistance and an overall decrease in RC time delay. However, the indications are that it is difficult to scale this barrier layer system to the thicknesses required for future interconnects and the fact that it is a physical vapour deposition (PVD) process makes it unsuitable for the high aspect ratio structures increasingly required in BEOL fabrication.

One solution which has been proposed is the use of a self-forming barrier (SFB) [18]. The idea behind this approach of barrier layer formation is to alloy a material such as aluminium or manganese with the Cu during deposition of the interconnect line. The structure is then annealed during which the alloyed material is expelled from the Cu and chemically reacts with the dielectric layer to form a barrier at the metal/ILD interface. Ideally, this reaction should be self-limiting to typically a few nanometers (~3nm) to

ensure the barrier formed is of the required thickness dimension. Any excess of the alloying element will diffuse to the surface of the Cu line during the thermal anneal where it can be removed by further processing steps such as chemical mechanical polishing (CMP). This process is schematically shown in Figure 1.8 where (a) is the patterned ILD material, (b) is the deposition of the Cu alloy and (c) is the subsequent anneal, chemical reaction and formation of the self-forming barrier at the surface of the ILD layer. Two candidate metals which are currently being investigated for use as an alloying element with Cu to form a SFB are manganese and aluminium. The metal manganese (Mn) shows great promise for use as an SFB alloying material due to the fact that it is expelled from Cu when annealed [19]. This means that during the anneal stage, the Mn will be expelled from the Cu before the Cu has time to migrate through the ILD material. The Mn then chemically reacts at the interface to form manganese silicate which has potential to be an excellent barrier material in terms of preventing Cu ion diffusion and has good adhesion properties [18].

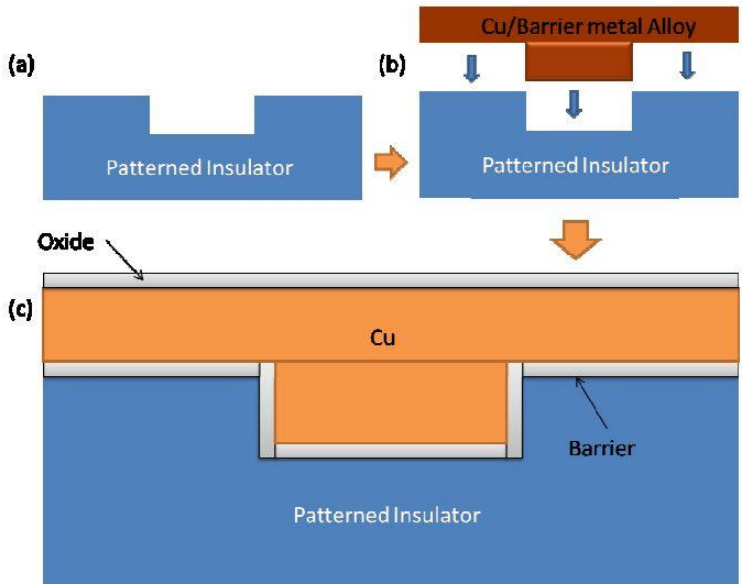

Figure 1.8: Self forming barrier process [4].

The second alloy material under investigation for use in the SFB approach is aluminium (Al). This metal has a number of advantages for use in processing, the first being it is a metal which has previously been used in the industry and thus is well understood for manufacturing purposes. The second aspect which makes Al an attractive candidate is the high heat of formation of Al_2O_3 ~ - 1677.4 kJ/mol which is significantly higher than that of the stable oxide of silicon, SiO_2 ~ - 910.4 kJ/mol [20]. These thermodynamic values indicate that Al should readily react with the ILD to form a chemically stable layer of Al_2O_3 which has the potential to act as an excellent Cu diffusion barrier layer. The third promising aspect of using Al metal is the fact that Al can migrate to the Cu grain boundaries during the anneal stage where it can act to suppress electromigration in the interconnect line [9,21].

1.6 Thesis investigation

The experimental work presented in this thesis is on the topic of chemical, structural and electrical performance of self-forming Cu diffusion barriers formed on a variety of dielectric substrates. An introduction has been outlined, describing previous generations of IC material fabrication and design. Issues with future iterations of die-shrinking in relation to materials has been outlined, in particular the need for a Cu diffusion barrier to overcome the problematic issues of (a) Cu diffusion into surrounding ILD material, (b) promotion adhesion between the Cu line and ILD material and (c) be thin enough to allow maximum volume of Cu fill within interconnect lines to minimise resistance. As stated previously, self-forming barriers could be a viable solution to the problems associated with current barrier layer stacks. The work in this thesis follows on from previous chemical and structural studies of copper diffusion barrier layer formation in the Surface and Interface Research Group (SIRG) in DCU [4,22] which paved much of the foundational work of in-situ chemical analysis of $MnSiO_3$ as a self-forming barrier candidate material on SiO_2 dielectric substrates. Studies of barrier formation on prototype low-k dielectric materials and the development of a capability to fabricate metal-oxide-semiconductor (MOS) test structures for electrical testing of the barrier integrity were undertaken. In addition an alternative self-forming barrier layer candidate metal, aluminium (Al), is explored from both interface chemistry and electrical test device perspectives. The following is a brief outline of the work presented in the experimental results chapters of this thesis:

<u>Chapter 4</u>: "In situ parallel fabrication and interface characterisation of metal oxide semiconductor barrier layer test structures"

This chapter follows directly on from the initial in-situ interface chemistry study of Mn deposited on SiO_2 dielectric layers to form $MnSiO_3$ barrier layers undertaken by the SIRG [4,22,23,15,24,25,19,26]. This chapter further expands on the analysis of the barrier formed by utilising a novel approach of in-situ fabrication of MOS structures with and without a $MnSiO_3$ barrier layer, in an ultra-high vacuum (UHV) system monitored by XPS analysis throughout fabrication process. The highly controlled environment in which the MOS devices were fabricated, allowed direct correlation of the chemistry of barrier formation with the subsequent electrical testing of the fabricated MOS devices.

<u>Chapter 5</u>: "Manganese silicate barrier formation of different porosity carbon doped oxide dielectrics"

This chapter focuses on the formation of a $MnSiO_3$ barrier on industrially relevant, high porosity (50% porous) and low porosity (0% porosity) carbon doped oxide (CDO) materials. Both 50% and 0% CDO materials were exposed to identical thin film Mn depositions and anneal treatments, thereby allowing the effect of porosity on barrier layer formation to be observed. In-situ X-ray photoelectron spectroscopy (XPS) and well as X-ray absorption spectroscopy (XAS) and transmission electron microscopy (TEM) were employed to characterise the formation of $MnSiO_3$ on these technologically relevant dielectric materials.

Chapter 6: "CuAl (90:10 %) alloy for use in BEOL IC interconnect technologies"

A copper-aluminium alloy is the focus of this chapter as an alternative candidate for self-forming barrier layer formation on SiO_2. A Cu/Al alloy was studied as opposed to a sequential deposition study (as in the Mn studies) in order to expand upon the self-forming barrier concept. A variety of methods including X-ray photoelectron spectroscopy (XPS), secondary ion mass spectroscopy (SIMS), hard energy X-ray photoelectron spectroscopy (HAXPES),Transmission electron microscopy (TEM) and a range of electrical characterisations are employed to study a CuAl (90:10 % wt) alloy deposited on 100 nm SiO_2 dielectric substrates.

Chapter 7: "CuAl alloy barrier layer properties for future interconnect applications"

This final experimental results chapter carries on from the previous chapter by using a CuAl alloy as a self-forming barrier. In depth electrical analysis is performed on both reference pure Cu MOS and CuAl alloy MOS devices in order to establish the effectiveness of the CuAl alloy at preventing Cu diffusion into the underlying oxide layer. Bias thermal stress (BTS) and pure thermal stress testing was performed in addition to electrical characterisation of capacitance voltage (CV) and leakage current (IV) measurements. Scanning electron microscopy was used to image both the Cu and CuAl alloy in addition to atomic force microscopy (AFM) and optical imaging of the sample surfaces following thermal stress treatments. Secondary ion mass spectroscopy (SIMS) was employed to track the diffusion of Cu into the oxide layer of the MOS devices following thermal stress measurements.

1.7 References

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2 Experimental Techniques

2.1 Introduction

A variety of experimental techniques are used in this study in order to characterise and test Cu diffusion barrier growth, structure, chemical composition and electrical effectiveness. The main technique used in the study was an in-situ approach of metal depositions and anneal stages in conjunction with X-ray photoelectron spectroscopy (XPS) analysis. XPS is an ideal technique to use for in-situ Cu diffusion barrier layer studies however; the technique only gives information on chemical composition and chemical interactions within approximately the top 5-7 nm of the surface of interest. Other ex-situ techniques are exploited in order to gain additional information such as transmission electron microscopy (TEM), used to image the interfaces of samples and elementally map the interfaces when used in electron energy loss spectroscopy (EELS) mode. Secondary ion mass spectroscopy (SIMS) is a chemical depth profiling technique, utilising a high energy ion beam to sputter the surface of the sample of interest. As the beam sputters through the sample, ejected fragments of the sample surface are analysed with a mass spectrometer in order to track elemental changes throughout the structure of the samples. X-ray absorption measurements (XAS) is a further technique used to identify the precise chemical species present within a sample. Electrical characterisation of fabricated barrier layers is of great interest due to the industrial relevance of electrical testing of future interconnect components. Capacitance-voltage (CV) sweeps are performed on fabricated metal oxide semiconductor (MOS) structures both with and without a Cu diffusion barrier in order to test barrier effectiveness at preventing Cu diffusion into the oxide material.

2.2 X-ray photoelectron spectroscopy

As stated previously, the main experimental technique used in this study was X-ray photoelectron spectroscopy (XPS). The use of XPS demands an ultra-high vacuum environment to ensure effective operation of the technique and to maintain the chemical composition of the sample in a stable state throughout the measurement period. An in-situ approach was typically adopted in this study, meaning that any substrates of interest were inserted into a UHV system with in-situ XPS, thin film metal deposition and annealing capabilities, thereby allowing the sample to remain in UHV during the course of experimental procedure without the need to break vacuum and expose the interface of interest to atmospheric contamination. This allowed XPS spectra to be acquired from ultra-clean interfaces, thereby minimising any contamination problems during experimentation.

2.2.1 Basic Principles

XPS is a highly surface sensitive technique used to identify the chemical species present in approximately the top ~7 nm of a surface of interest. This is achieved by irradiating the sample with mono-energetic soft X-rays [1]. Conventional XPS typically utilises a dual X-ray anode configuration of a magnesium (Mg) and aluminium (Al) anode in order to produce characteristic X-ray lines of Mg Kα (1253.6 eV) and Al Kα (1486.6 eV) energies. As the sample is irradiated by either anode radiation, electrons are emitted from the sample surface via the photoelectron effect with binding energy (E_b) given as;

$$E_b = h\upsilon - KE$$

Equation 2.1: Binding energy of an electron.

Where h is Planks constant (6.626 x 10^{-34} m^2kg/s), υ is the frequency of the electromagnetic radiation which caused the photoelectron to be ejected and KE is the kinetic energy of the electron ejected from the atom. Due to the fact that the photon energy (hυ) is well defined, a measurement of the kinetic energy of the emitted electron should give the necessary information needed to obtain the binding energy of the electron from its initial atomic state. In addition, due to the well-defined electron energy levels within an atom, elemental identification can be achieved via the measurement of the kinetic energy of electrons emitted from the sample surface during irradiation from the anode target. The fact that soft X-rays are used, in contrast to conventional photoelectric effect which typically utilises UV radiation, electrons from higher binding energy core levels of the atom can be ejected, as schematically shown in Figure 2.1.

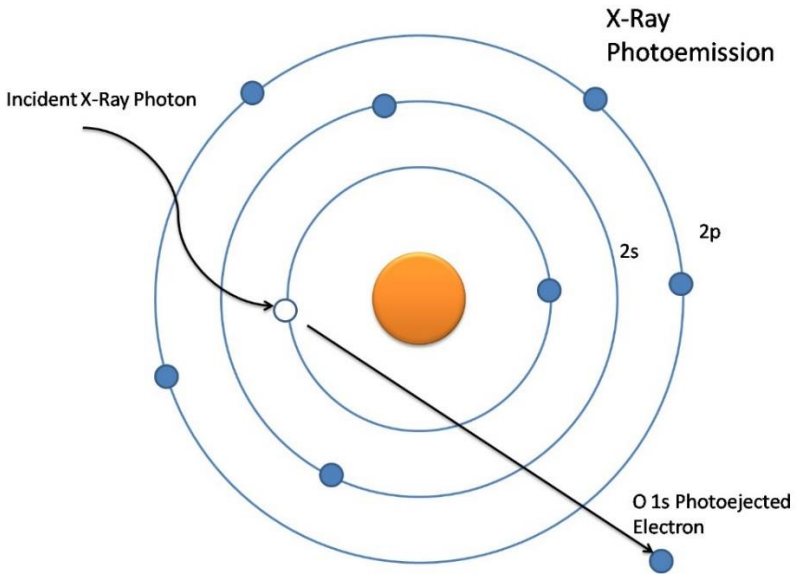

Figure 2.1: Creation of a photoelectron via the absorbance of an incident X-ray photon [2].

Thus, using a relatively more energetic radiation source, deeper core level electrons can be ejected, enabling multiple electron levels in the atom to be measured. In order to precisely measure the binding energy of emitted electrons, an accurate measurement of the kinetic energy of the photoemitted electrons must be made. This measurement is achieved via the use of an electron energy analyser as seen in Figure 2.2 which is connected to a data acquisition system.

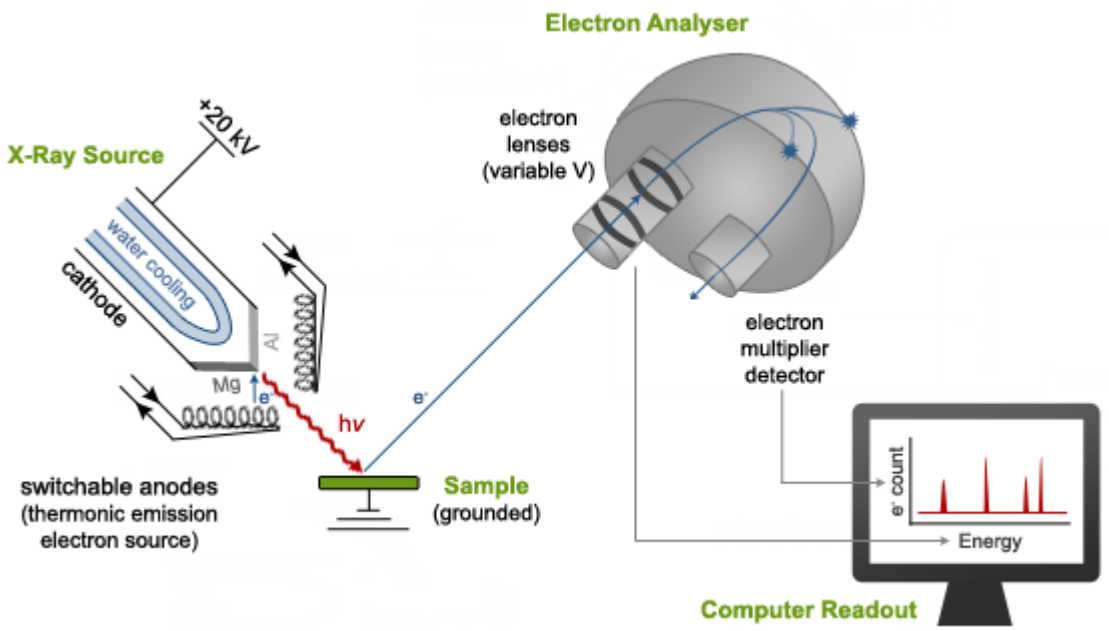

Figure 2.2: Typical XPS experimental set up [3]

As seen in Equation 2.1, the binding energy is only dependant on the kinetic energy of the electron (assuming the exact photon energy of the radiation used is known). This however is only correct for isolated atoms [4], and not true for electrons emerging from a solid surface sample, as used in XPS analysis. Consideration must be given to the workfunction of the material (ϕ_s) which is defined as the energy difference between the sample Fermi level and the vacuum level. Thus, Equation 2.1 must be modified to allow for this change, giving:

$$E_b = h\upsilon - KE - {}^{\Phi}{}_s$$

Equation 2.2: Modified binding energy equation due to the sample workfunction.

As stated previously, the sample and electron analyser must be grounded during analysis. This then causes both the Fermi level of the sample and spectrometer to be at the same energy level as schematically shown in Figure 2.3.

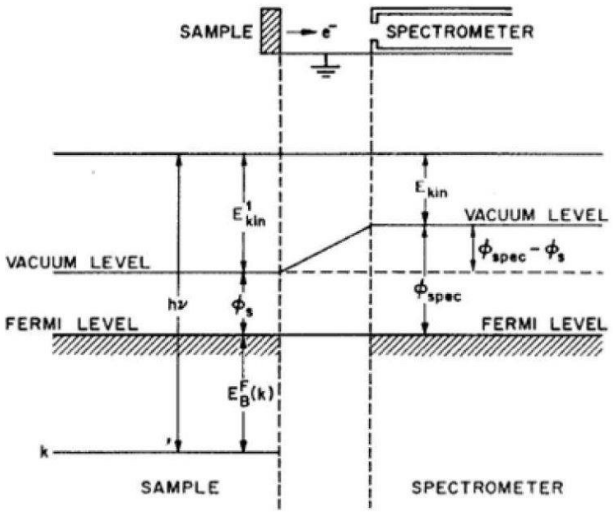

Figure 2.3: Energy band diagram of sample and electron analyser grounded [5].

As can be seen from Figure 2.3, the kinetic energy of the electron as measured by the electron analyser will not be equal to the value described via Equation 2.1 due to the effects of both the sample workfunction (ϕ_s) and the spectrometer workfunction (ϕ_{spec}) [5]. Thus the actual kinetic energy of the electron (KE) as measured by the spectrometer (KE_{spec}) will be given as:

$$KE = KE_{spec} + ({}^{\Phi}{}_{spec} - {}^{\Phi}{}_s)$$

Equation 2.3: Kinetic energy of electron measured by spectrometer due to variable workfunction differences of sample and spectrometer.

When this definition of KE is substituted into Equation 2.2, it is found that the binding energy of the electron as measured via the kinetic energy measurement in the electron energy analyser, with work function, ϕ_{spec}, can be given as:

$$E_b = h\upsilon - KE_{spec} - {}^{\Phi}{}_{spec}$$

Equation 2.4: Binding energy of the electron measured via spectrometer following photoemission process.

Thus, if the photon energy (hυ), kinetic energy of the electron as measured by the spectrometer (KE_{spec}) and workfunction of the spectrometer (ϕ_{spec}) are known, the binding energy of the electron before being emitted from the atom can be calculated. The workfunction of the spectrometer can be experimentally found by calibrating the system with a known standard such as gold (Au). A scan of the intense Au 4f peak, which has a well-established binding energy (BE) position of 83.98 eV [6] allows calibration of the binding energy axis during data acquisition.

2.2.2 Sampling Depth of XPS

As stated previously, XPS is a very surface sensitive technique, with the ability to acquire chemical information from ~ 5-7 nm into a sample surface. The XPS sampling depth for a particular surface depends on the sample parameters such as density and the angle of detection. Thus the guide thickness of ~ 7 nm sampling depth can be drastically altered via the above parameters. Figure 2.4 schematically illustrates the relative areas and depth penetrations of both the incoming X-ray photon and outgoing photoelectrons. As can be seen, the average depth penetration of a 1 keV photon into solid matter is on the order of

~ 1 μm, this is in contrast to the escape depth of the electrons from the sample surface which is on the order of < 10 nm. Photons of 1 keV do not interact with matter as much as electrons, which interact strongly within the sample via collisions.

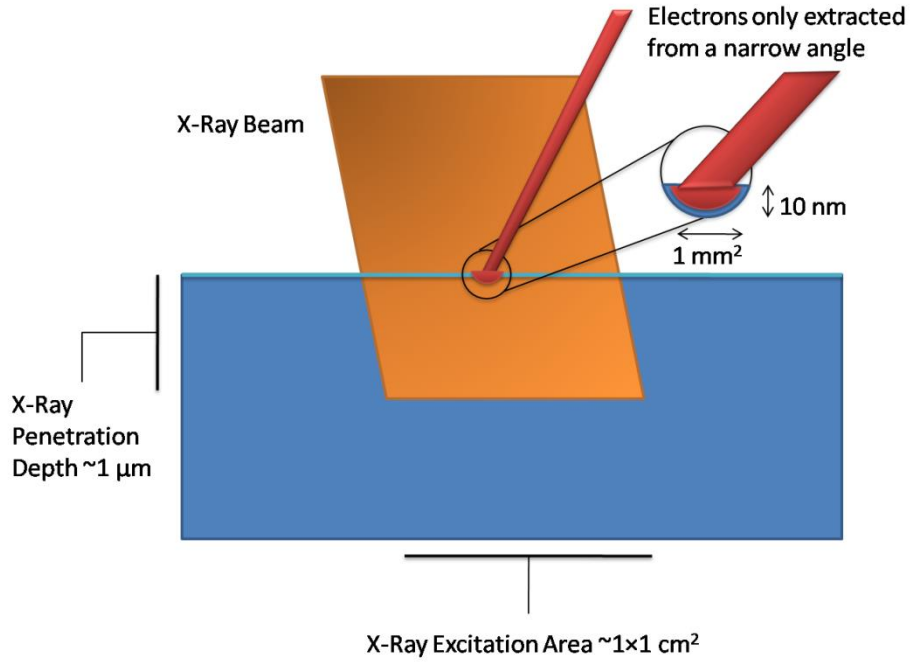

Figure 2.4: Diagram of sample surface during XPS analysis showing the typical penetration depth for the incident X-rays and the sampling depth of the photoemitted electrons [4].

If no electron collisions occurred within the sample following the photoabsorption process, the XPS sampling depth would be equal to the photon penetration depth. Thus it can be seen that the depth sensitivity of XPS is not a human engineered design, but a result of probabilistic scattering of electrons via collisions within the sample. The probability of an electron scattering within the sample following photoemission can be directly related to the sampling depth, showing that a low probability of collisions gives a greater sampling depth. Thus an understanding of the mean free path (MFP), which is defined as the average distance an electron with a given energy will travel in the sample

before a collision is of importance in order to calculate effective sampling depths during XPS analysis. Figure 2.5 shows a plot of electron MFP as a function of kinetic energy for a wide range of different materials. The inelastic mean free path (IMPF) is defined the average distance an electron of a certain kinetic energy will travel in a material before undergoing an inelastic collision (a collision which alters the original kinetic energy

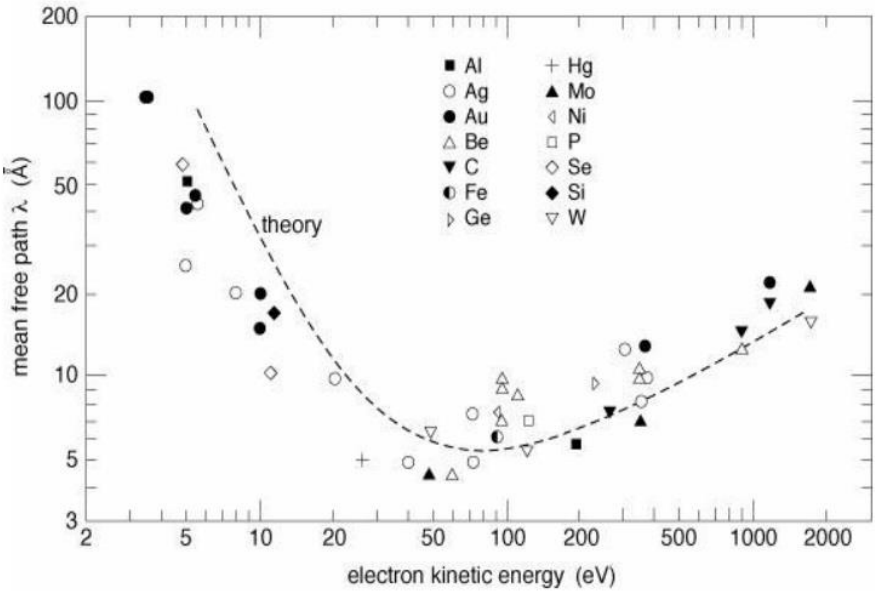

Figure 2.5: Mean free path (MFP) for electrons in a variety of materials with various kinetic energies [7].

value). The probability of an electron undergoing an inelastic collision within the sample P(d) following photoemission is given as:

$$P(d) = \exp(-\frac{d}{\lambda})$$

Equation 2.5: Probability of electron undergoing inelastic collision as a function of travelling distance.

where d is the travel distance of the electron and λ is the IMFP of the electron of a certain kinetic value within a particular material (sample and kinetic energy dependant). Using Equation 2.5, a plot can be generated showing that as the electron travels further through the solid sample (d increasing) the probability of an inelastic collision increases. This curve is shown in Figure 2.6, which indicates that the majority (~95 %) of non-scattered electrons come from the top 3λ of the sample surface, which is commonly referred to as the sampling depth. As the distance travelled increases to 4λ, it can be seen that the probability of an electron not undergoing an inelastic collision is virtually zero. It is however theoretically possible (although extremely unlikely) that an electron which was ejected from the sample at the highest photon penetration depth into the sample could traverse through the sample and into the electron analyser without undergoing a scattering

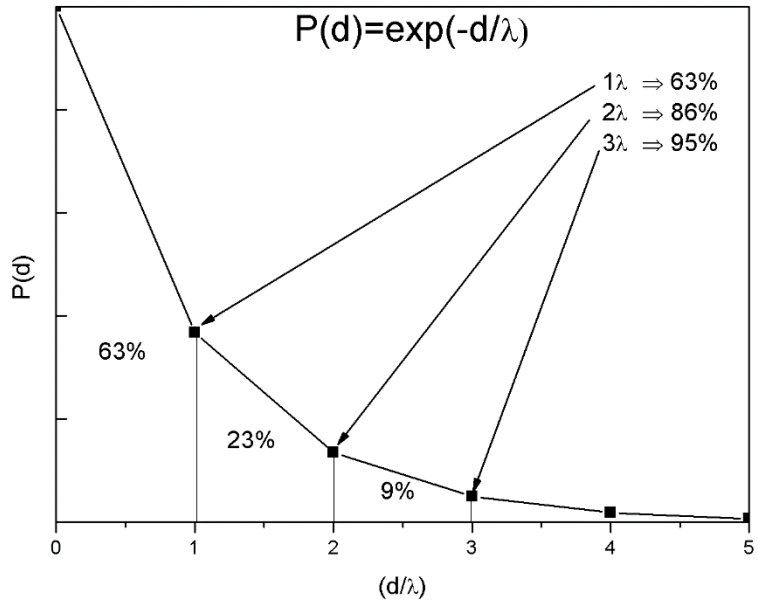

Figure 2.6: Graph of the probability of an electron undergoing an inelastic collision within a sample material [2].

event. In addition the penetration depth of a photon into a solid material is also given as a probabilistic event, as seen in the Beer-Lambert law shown in Equation 2.6.

$$I = I_o . exp^{(-\mu x)}$$

Equation 2.6: Beer-Lambert law.

where I_o is the original intensity of photon intensity before entering the sample, μ is the linear absorption coefficient (material and photon energy dependant) and x is the distance travelled into the sample. Due to the exponential decay of the original intensity (I_o) of the radiation to an intensity of I at a distance x into the sample, it is seen that the probability is small, but non-zero that a photon could travel to the bottom of the sample and cause photoemission of an electron. As stated above, this electron then has the ability to travel through the sample without undergoing any inelastic scattering and be detected by the electron analyser. This shows that theoretically the sampling depth of XPS is infinite, however given the extremely low probabilities of these events actually happening, and the fact that 95% of the electrons come from within the top 3λ of the sample surface, XPS is practically defined as having a sampling depth of ~ 7 nm / 3λ. Only electrons which escape the surface and enter the analyser without undergoing inelastic collisions can be related back to the original BE of that electron, thus providing elemental and chemical information from the sample surface. Electrons which undergo inelastic scattering contribute to the XPS spectra in various ways, mainly as an increase in background of the spectra as seen in Figure 2.7, in contrast to the non-scattered electrons which give rise to sharp well defined photoemission peaks.

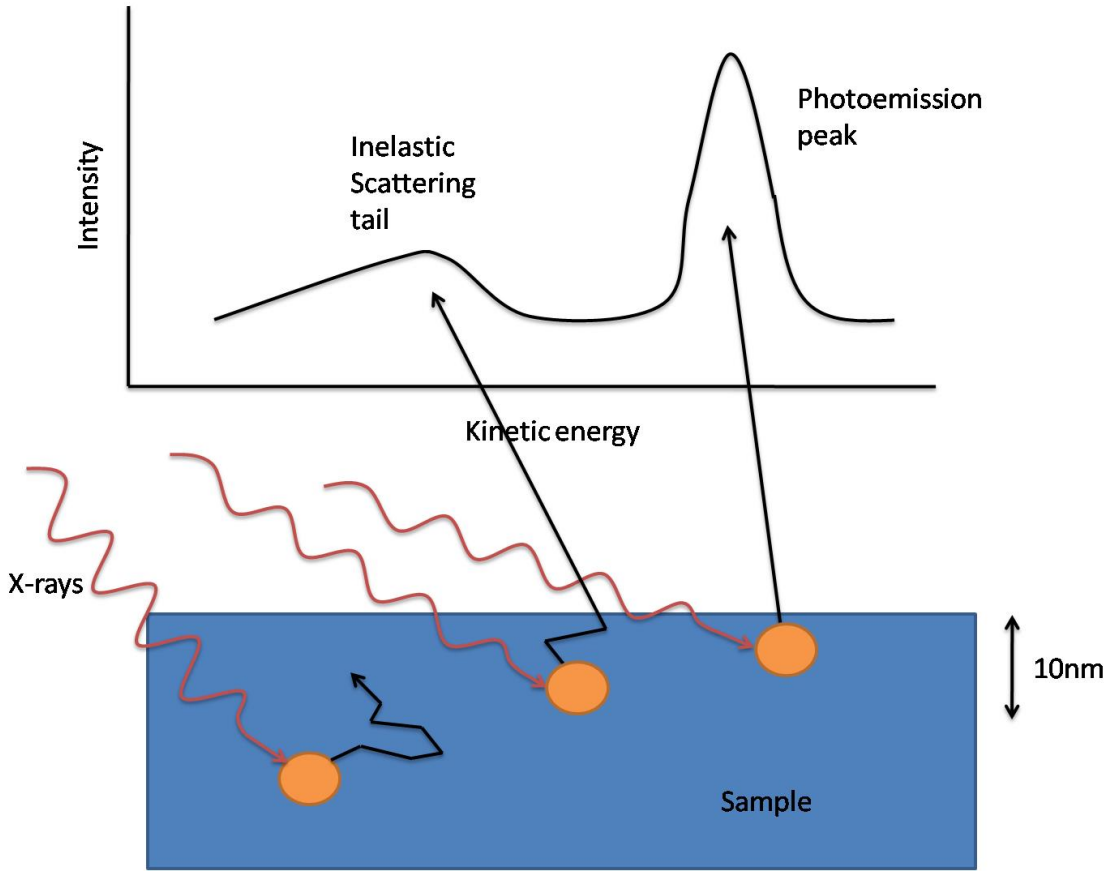

Figure 2.7: Scattered and non-scattered electrons contributing to the XPS spectra [4].

2.2.3 Spectral Features

The plot of a typical XPS survey scan (0 – 1000 eV) for a pure Cu film is shown in Figure 2.8 with the electron binding energy scale on the x-axis (eV) and with the corresponding number of electron counts for each BE position on the y-scale.

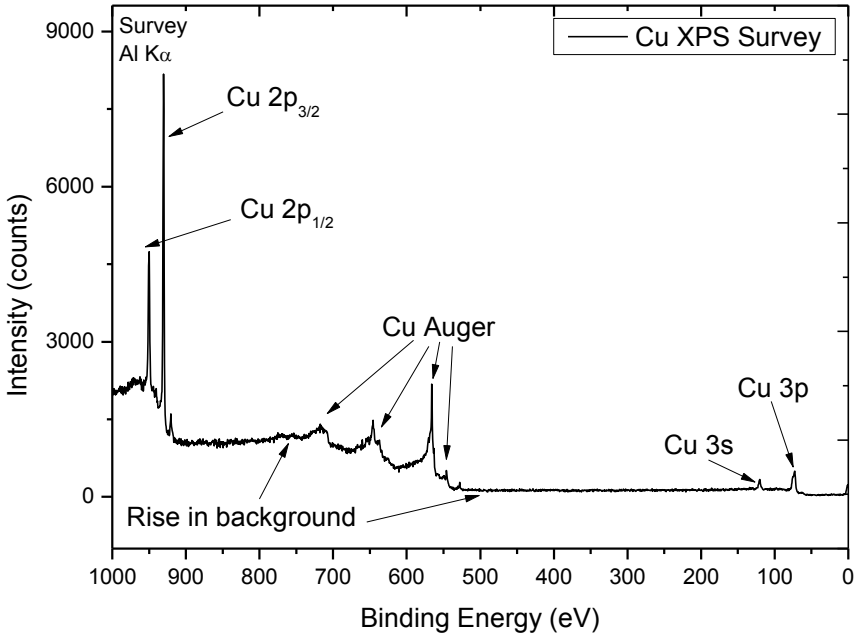

Figure 2.8: XPS survey spectra of a pure Cu film.

As can be seen from the Cu survey spectra, a number of spectral features are evident. Two photoemission peaks at ~ 75 eV and ~ 123 eV are due to non-scattered electrons photoemitted from the Cu 3p and Cu 3s orbitals, respectively. Between the BE positions of ~ 550 eV and ~ 750 eV are a number of features associated with Cu Auger processes which will be described in detail in a later section. At higher BE (~ 933 eV and ~ 953 eV) are photoemission lines originating from the Cu 2p orbital, with orbital splitting evident from the well separated Cu $2p_{3/2}$ (~933 eV) and Cu $2p_{1/2}$ (~953 eV). Thus is can also be seen that the Cu 2p orbitals are at a higher BE position relative to the outer orbital shells of the Cu 3s and Cu 3p lines. An important point to note is the fact that the Cu 2p photoemitted electrons have a kinetic energy much lower than the Cu 3p photo-emitted electrons (~ 858 eV kinetic energy difference). As stated previously, photoemitted electrons with a larger KE will have a larger IMFP, thus increasing the effective sampling depth. This indicates that although the sampling depth for the Cu film may be on the order

of ~ 7 nm, not all spectral features may come from this depth. In fact the Cu 2p lines, due to the much lower KE of the ejected electrons, are much more surface sensitive relative to the higher KE of the Cu 3p orbital. In addition to the spectral lines described above, a rise in the background of the spectrum is also noted towards higher binding energies (lower KE). This is due to scattered photoemitted electrons loosing KE, and contributing to the spectral background. Auger lines, as observed in Figure 2.8 are a spectral features caused via the Auger process which is an internal electron emission process as schematically depicted in Figure 2.9.

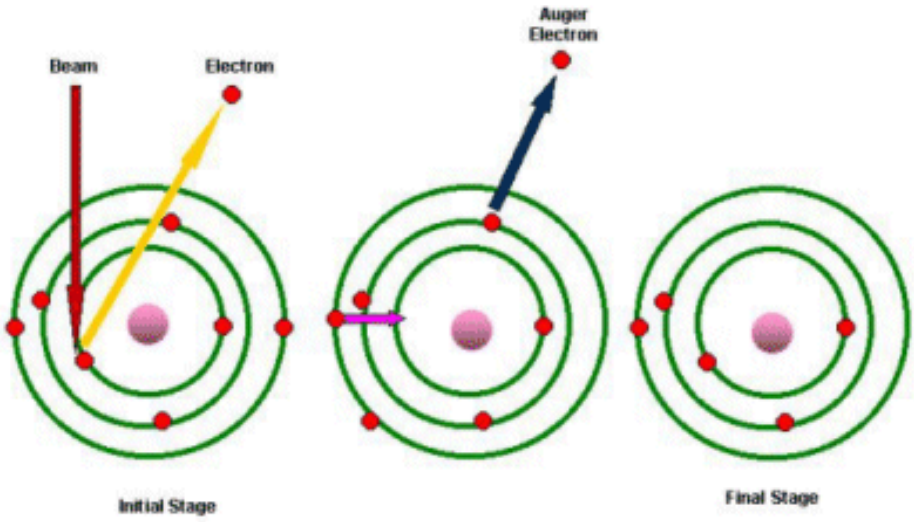

Figure 2.9: Auger process within an atom [8].

As shown within the diagram, an initial inner-core electron is removed due to absorption of a photon or energy transfer from an incident high energy electron-beam. An outer level electron then fills the vacancy left from the initial electron ejection. Quantum mechanics shows that the electron, originally in the outer orbital, has too much energy to reside in the inner orbital when it makes the transition to fill the vacancy. Thus the energy can be transferred to an electron in an outer orbit, where upon if this electron receives enough energy it can be ejected from the atom and detected in the photoemission spectrum. In

contrast to photoemission peaks, where the KE of the ejected electron is dependent upon the photon energy used, the Auger process is independent of initial photon energy due to the fact that it is an internal excitation process within the atom. Thus if photoemission spectra are acquired with both the Mg Kα and Al Kα, the photoemission peaks for the Cu sample will reside in the same positions on a binding energy scale, whereas the Auger lines will move depending on what anode is selected. If a kinetic energy x-axis is selected, the Auger lines would remain stationary upon anode switching, with the photoemission lines moving to new KE positions. This effect, as seen in Figure 2.10, where a Cu film was subjected to two XPS survey spectra scans, with the Al X-ray anode and also with the Mg X-ray anode. A shift in Auger features is evident relative to the locked positions of the photoemission peak features as a binding energy axis is used.

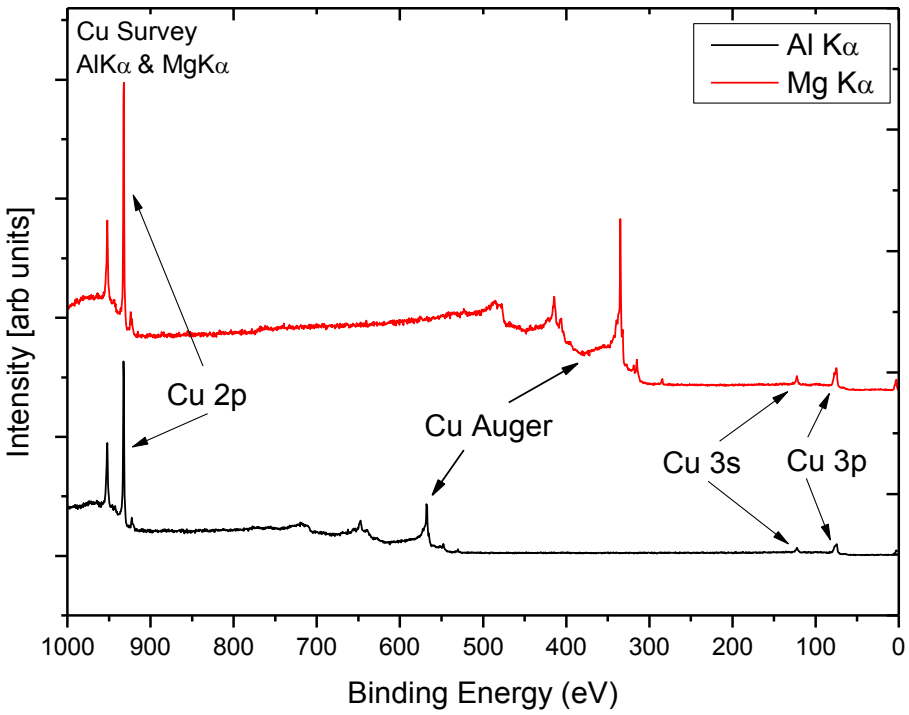

Figure 2.10: XPS Cu survey spectra using both Al and Mg anodes showing the apparent shift on the AES spectral features on a binding energy axis.

Survey spectra, typically taken from 0 eV upwards to ~ 1000 eV are primarily used to identify all elements within the sample surface. Once all elements have been identified, narrow window, high resolution spectra of the strongest photoemission lines for each element are taken. Figure 2.11 displays XPS survey and narrow window spectra for a 5 nm thermally grown SiO_2 layer on a Si substrate.

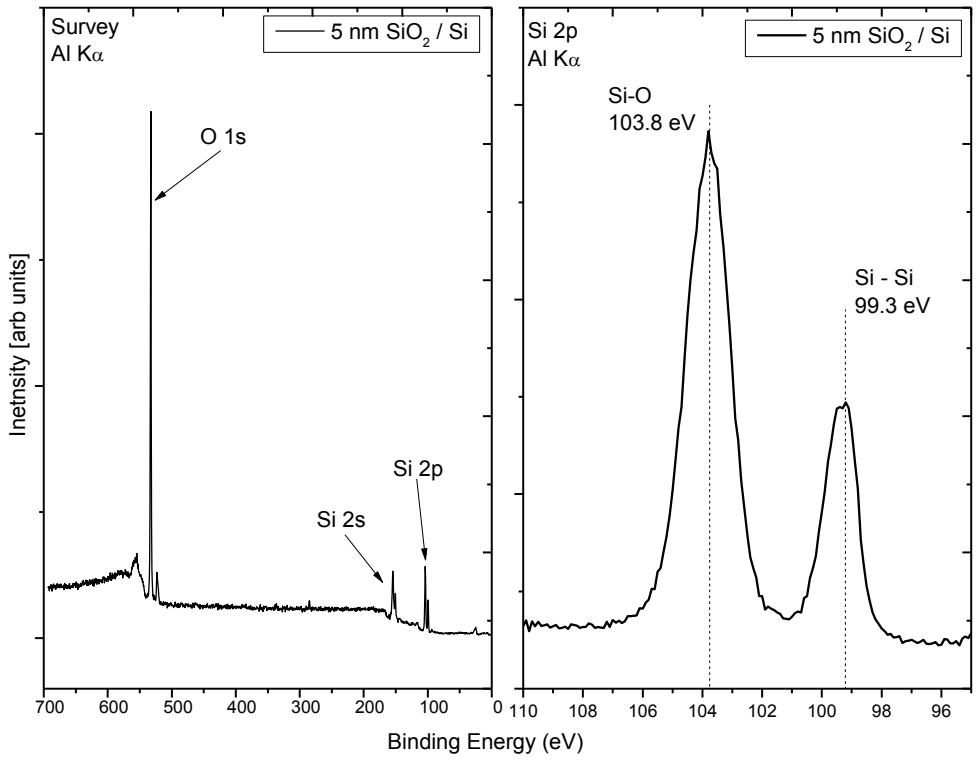

Figure 2.11: XPS survey and Si 2p spectra of 5 nm SiO_2 on Si substrate.

As can be seen from the survey spectra, a large O 1s peak is evident, attributed to the oxygen in the thin 5 nm over layer of SiO_2. Additional photoemission peaks are identified at lower binding energy (LBE) attributed to the Si 2s and Si 2p photoemission lines. A high resolution narrow window scan of the Si 2p spectrum reveals two component peaks. Due to the ultra-thin nature of the 5 nm SiO_2 film, signal from the underlying Si substrate is also acquired. The substrate Si, which is bonded to Si only (Si-Si bonds) appears at a binding energy position of 99.3 eV. The higher binding energy (HBE) component at a position of 103.8 eV is attributed to the over layer SiO_2, within which silicon is bonded to oxygen. This identification of chemical state bonding can be explained due to the fact that different elements have different electronegativity values. The effect of electronegativity values on chemical bonding is schematically shown in Figure 2.12.

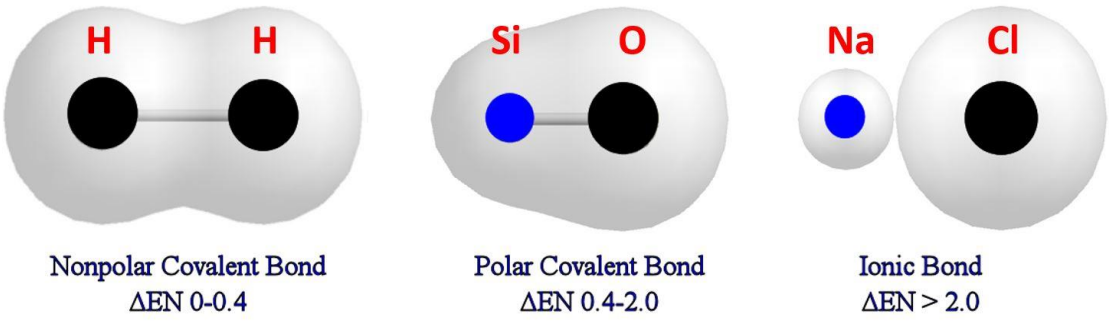

Figure 2.12: Electronegativity influence on chemical bonding showing changes in electron cloud densities [9].

As seen, two atoms of the same electronegativity (hydrogen for example) in a chemical bond, share the outer shell electrons equally in a perfectly covalent bonding arrangement. If two atoms of different electronegative values are involved in a chemical bond, a slight electron charge transfer is noted, with the majority of the negative charge residing around the atom with the highest electronegativity (in this case oxygen), thereby creating a slight positive charge around the atom with the lower electronegativity (in this example, silicon). If two atoms with a large difference in electronegativity bond, total charge transfer occurs, this is called ionic bonding and is demonstrated with the ionic bond NaCl, where the electronegative Cl receives the full share of the valence electron from the Na atom, thereby leaving the Na atom in an overall positive state. This explains the "chemical shift" of the SiO_2 peak in the Si 2p spectrum of Figure 2.11 relative to the Si-Si bonding of the substrate. As photoelectrons are emitted from the Si 2p orbital in the SiO_2 layer, they are being excited from a silicon atom in a slightly positive charge, lowering the KE value relative to the silicon-silicon bonds in the substrate. If the silicon atoms were bonded to an element of lower electronegativity than itself, a new peak would emerge at

a LBE position relative to the silicon-silicon bonding of the substrate. This "chemical-shift" allows XPS to not only perform elemental identification, but also identify the specific bonding environment for each element present. This property of XPS is heavily exploited in this thesis to understand the nature of chemical bond formation for barrier layers.

2.2.4 Additional Spectral Features

In addition to photoemission peaks, Auger lines and chemically shifted peaks, further spectral features can be seen within XPS spectra. Figure 2.13 shows the feature associated with a higher energy X-ray component in addition to the main Kα component used in conventional XPS which is present in spectra acquired by both of the commonly used Al and Mg anodes.

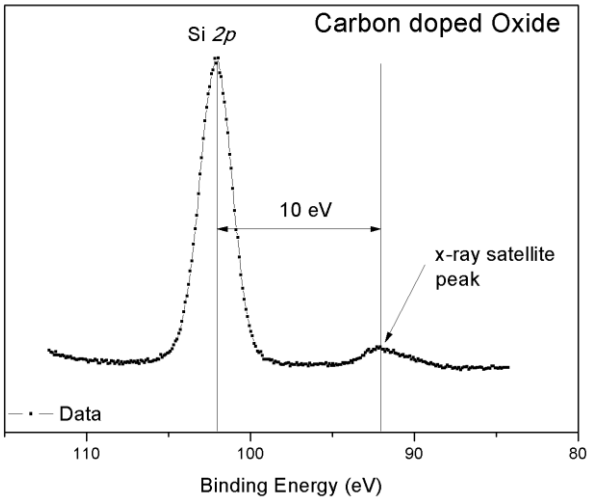

Figure 2.13: Si 2p spectrum showing X-ray satellite feature [2].

Due to the fact that higher energy X-ray components will produce photoelectrons with a higher kinetic energy, this will produce a small peak at lower binding energy relative to

the main photoelectron peak. This feature ~ 10 eV (typical position for strongest satellite peak using Al anode) at LBE can be problematic during peak fitting analysis (discussed in a later chapter) due to the fact that these satellite peaks may overlap with the main photoemission lines, for example in the Mn 2p spectra. The use of an X-ray monochromator eliminates these additional X-ray components (not available within this study). A list of satellite features and their relative intensities for both Al and Mg anodes are given in Table 2-1.

	$\alpha_{1,2}$	α_3	α_4	α_5	α_5	β
Mg displacement (eV)	0	8.4	10.1	17.6	20.6	48.7
Relative height (%)	100	8	4.1	0.6	0.5	0.5
Al displacement (eV)	0	9.8	11.8	20.1	23.4	69.7
Relative height (%)	100	6.4	3.2	0.4	0.3	0.6

Table 2-1: X-ray satellite features for both Al and Mg anodes [10].

Further to satellite features, shake-up features can also be seen within XPS spectra. Figure 2.14 shows these shake-up features in the Cu 2p spectra of various Cu species.

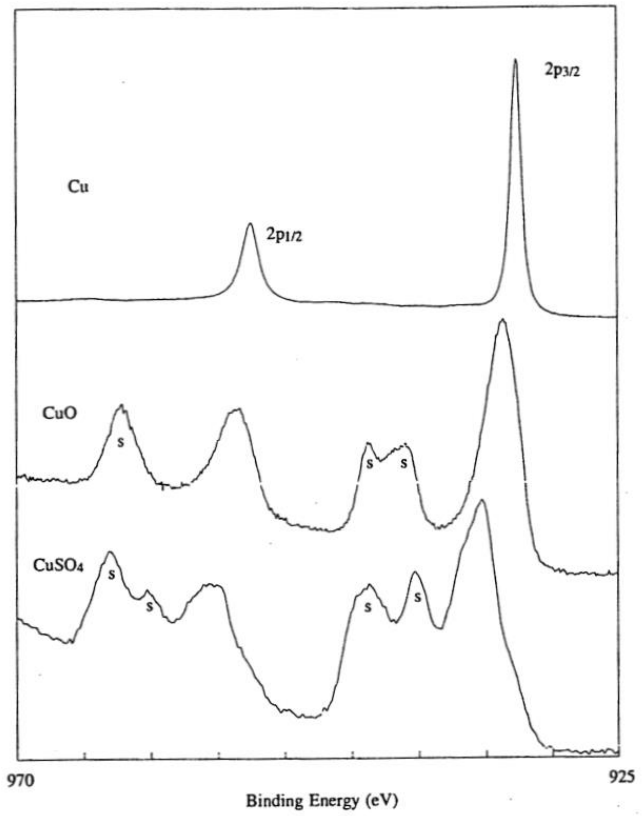

Figure 2.14: Shake-up features associated with Cu bonding states within the Cu 2p spectrum [11].

These spectral features are caused by coupling of the photoemitted electrons with valence states within the atom, thereby imparting energy to these states. The result is a lower kinetic energy emission, manifesting as a higher binding energy component.

2.2.5 Angularly Resolved XPS

In order to maximise the effective sampling depth into the material, the sample is typically placed at an angle of 90^{O} (normal emission) with respect to the analyser. Although at this angle, XPS is considered to be extremely surface sensitive, by rotating the sample off-

angle relative to the analyser, even greater surface sensitivity can be obtained as shown in Figure 2.15

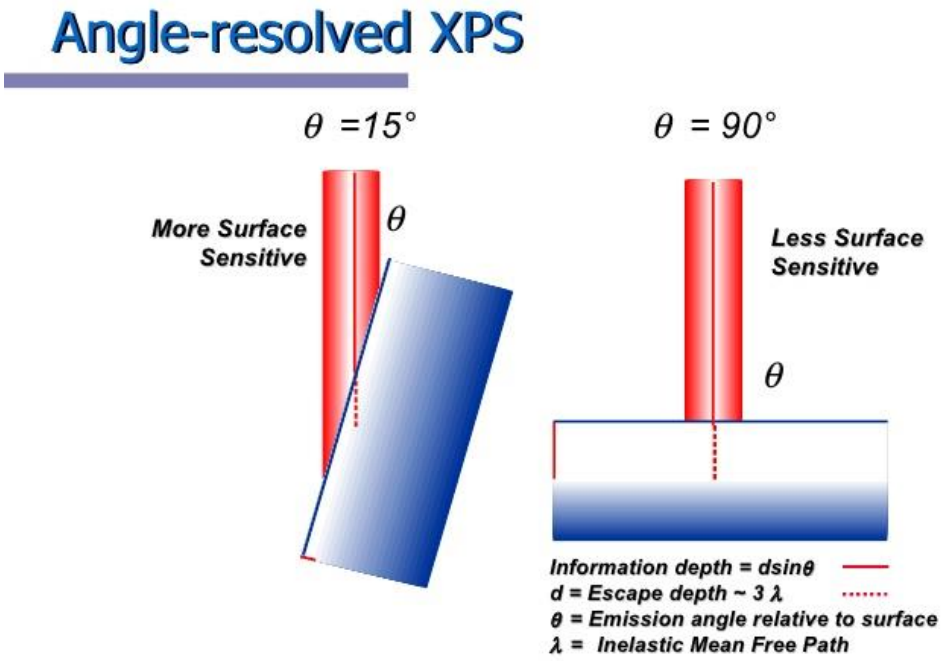

Figure 2.15: Angularly resolved XPS (ARXPS) and its impact on sampling depth [12].

As the sample is rotated relative to the analyser, increased surface sensitivity is gained due to the fact that sampling depth is effectively reduced. This effect is demonstrated in Figure 2.16, using a 5 nm thermal SiO_2 layer on a Si substrate showing that the surface localised oxide layer increases in intensity relative to the substrate silicon signal as the emission angle is changed from normal emission to 60^o off normal.

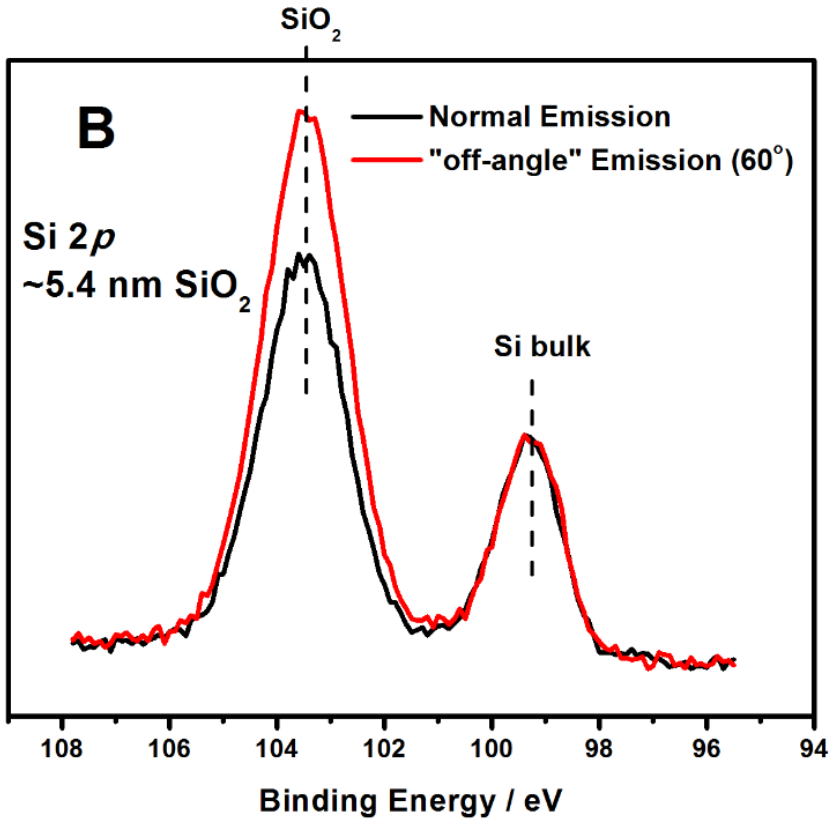

Figure 2.16: ARXPS demonstrated using 5 nm SiO_2 over layer on Si substrate

2.3 Electrical Measurements

Electrical characterisation of barrier materials is of great importance due to the electrical nature of the interconnect structures within which the barrier will reside. As stated previously, Cu has a tendency to diffuse into any surrounding ILD materials in the form of Cu^+ ions [7-10] [13-16]. Due to the charged nature of the diffusing Cu, electrical measurements sensitive to charge detection can be used to investigate Cu ion diffusion into ILD materials. Capacitance-voltage characterisation of MOS structures provides an ideal method to test for this Cu diffusion activity. In addition to CV measurements, current-voltage (IV) leakage measurements can also be used to study Cu diffused into ILD materials, due to the heightened leakage current associated with the presence of Cu in the dielectric material.

2.3.1 The MOS structure

In order to electrically characterise the effectiveness of barrier layer materials at preventing Cu ion diffusion, an electrical device must be fabricated, which allows the diffusion of Cu into a dielectric layer, and also allows the incorporation of a barrier layer between the Cu layer and ILD material. Cu ion diffusion into an ILD material is schematically shown in Figure 2.17.This indicates that if Cu^+ ions diffuse into a dielectric material, that dielectric will exhibit an overall positive charge.

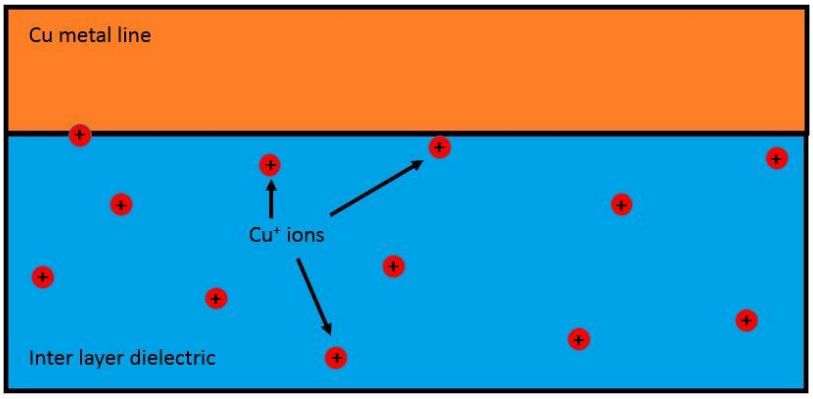

Figure 2.17: Schematic illustration of Cu ion diffusion into an ILD material.

Thus, if a technique can be developed to identify this charged state, a method of Cu ion diffusion detection can be realised. By fabricating a MOS structure with a Cu metal gate on a SiO_2 dielectric layer grown on adoped Si substrateas shown in Figure 2.18 (a), the effects of Cu ion diffusion into the dielectric can be detected by CV measurements.

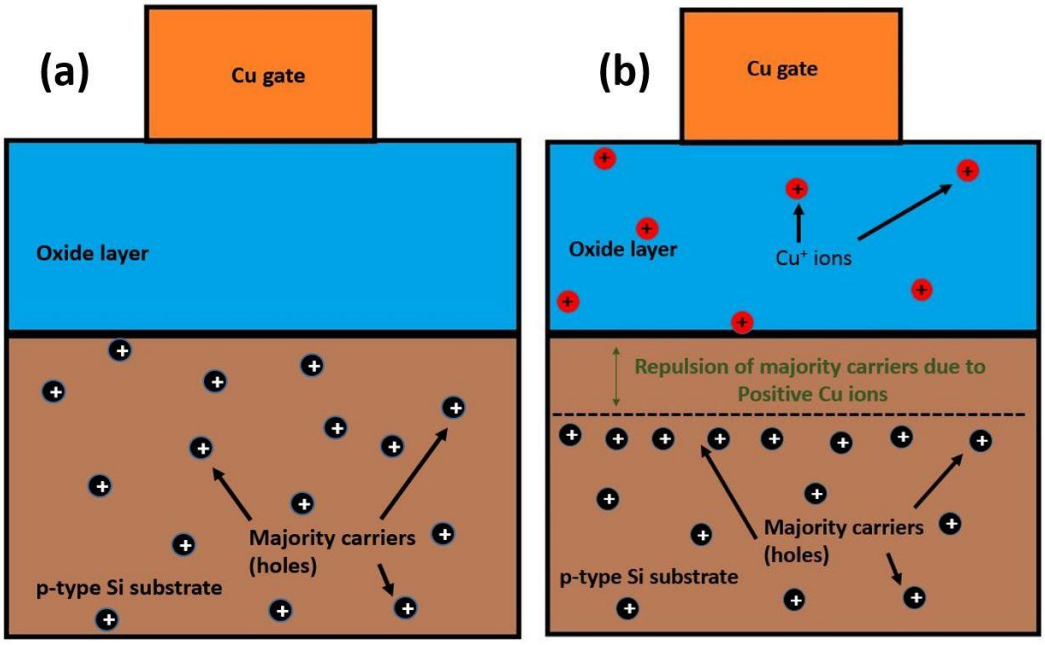

Figure 2.18: Cu MOS device (a) without Cu diffusion and (b) with Cu diffusion into the ILD.

As can be seen in Figure 2.18 (b), if Cu^+ ions diffuse into the dielectric material, they can repel the majority carriers of a p-type Si substrate (or attract majority electrons in a n-type substrate). This doped substrate is therefore sensitive to the presence of any charge build up in the oxide layer, making MOS structures ideal for detection of Cu ion diffusion. Additionally, any barrier layer under test can be deposited onto the dielectric layer before Cu gate deposition in order to test the effectiveness of the barrier at preventing Cu diffusion.

2.3.2 Capacitance-voltage sweep

The MOS structure can be viewed as a capacitor structure, due to the metal gate, dielectric layer and doped Si substrate. In contrast to a traditional metal-insulator-metal (MIM) structure (which has constant capacitance, irrespective of applied voltage), the MOS structure will have a variable capacitance, due to the fact that a semiconductor is used as one of the oxide electrical contacts. This can be explained via Figure 2.19, which shows an n-type Si MOS capacitor subjected to various gate voltages while grounding the Si substrate.

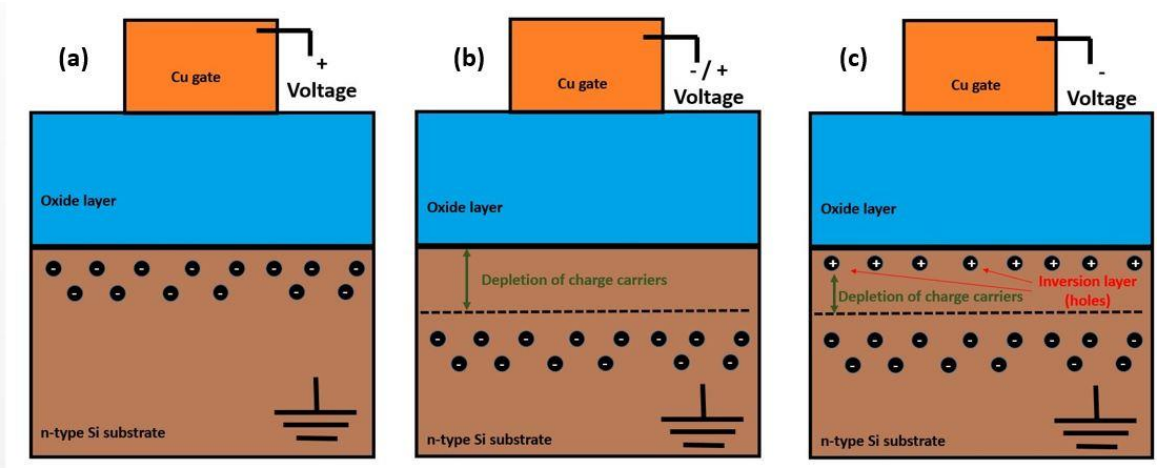

Figure 2.19: MOS capacitor subjected to (a) positive gate bias, (b) intermediate bias and (c) negative bias.

As can been seen in (a), when the gate voltage is positive, an accumulation of majority carriers (electrons in an n-type Si substrate) occurs at the Si/SiO_2 interface, thus the device acts as a typical capacitor structure, with the capacitance due to the oxide layer calculated as:

$$C_{ox} = \frac{k\varepsilon A}{d}$$

Equation 2.7: Oxide capacitance of a MOS structure in accumulation.

where k is the dielectric constant of the oxide layer, ε is the electrical permittivity of free space, A is the area of the gate electrode and d is the thickness of the oxide layer.

As the voltage is decreased towards negative values, a depletion layer (no charge carriers present) forms in the Si substrate. This depletion layer acts as an additional capacitor in series with the dielectric capacitance and can be calculated as:

$$\frac{1}{C_{total}} = \frac{1}{C_{ox}} + \frac{1}{C_{Dep}}$$

Equation 2.8: Capacitors in series relating to the dielectric capacitance and the capacitance associated with the depletion region.

where C_{Dep} is the capacitance due to the depletion layer formed, which can be calculated from Equation 2.7 using the k value of Si, and depletion width d.

As the voltage is decreased further, the depletion width reaches a maximum distance, and comes to an equilibrium position, similar to a PN diode junction. Further decreasing of gate voltage as seen in part (c), results in a phenomenon known as inversion. This phenomenon is the basis of transistor switching in IC circuits in order to create a conducting channel for current flow between the source and drain contacts. Essentially, minority carriers (holes in the case of an n-type Si substrate) build up at the Si / oxide interface due to the negative charge on the gate material. This phenomenon is known as inversion due to the fact that at this point, the region of the semiconductor at the Si / oxide interface, now acts as the opposite doping type compared to the bulk Si. Figure 2.20 shows a 1 MHz CV sweep for an n-type Si MOS structure, with the various components of (a) accumulation, (b) depletion and (c) inversion, all corresponding with parts (a), (b) and (c) of Figure 2.19.

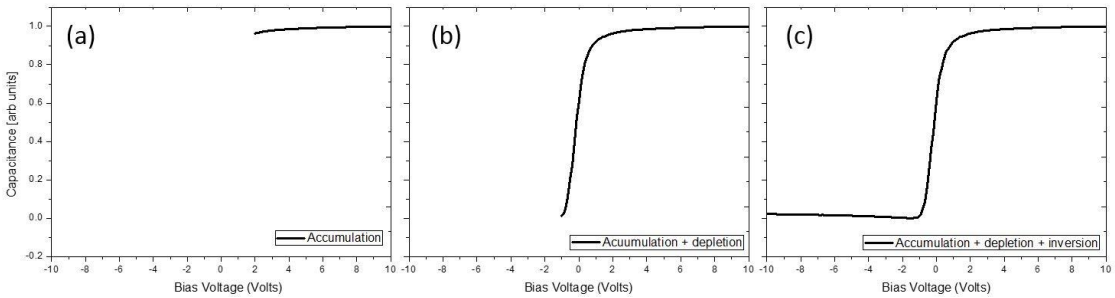

Figure 2.20: CV of an n-type MOS showing (a) accumulation, (b) depletion and (c) inversion regions.

The constant capacitance of accumulation can be seen in (a), reduction in capacitance in (b) due to the depletion width of the Si and inversion in (c). When examined closely, part (c) (inversion) of Figure 2.20, should show an increase in capacitance, after the decrease of depletion, due to minority charge carriers at the Si / oxide interface. This does not occur however in a 1 MHz frequency sweep, due to the fact that the minority carriers cannot respond fast enough to the fast switching AC signal probe. Figure 2.21 displays MOS CV data for both n-type and p-type Si using both low frequency and high frequency sampling signals. As can be seen, for both n and p-type, in the inversion region there is a rise in capacitance, due to the minority carrier response at low frequencies. In contrast the high frequency measurements remain at the C_{min} value due to the fact that at high frequency, the minority carriers cannot respond quickly enough to impact on the capacitance reading.

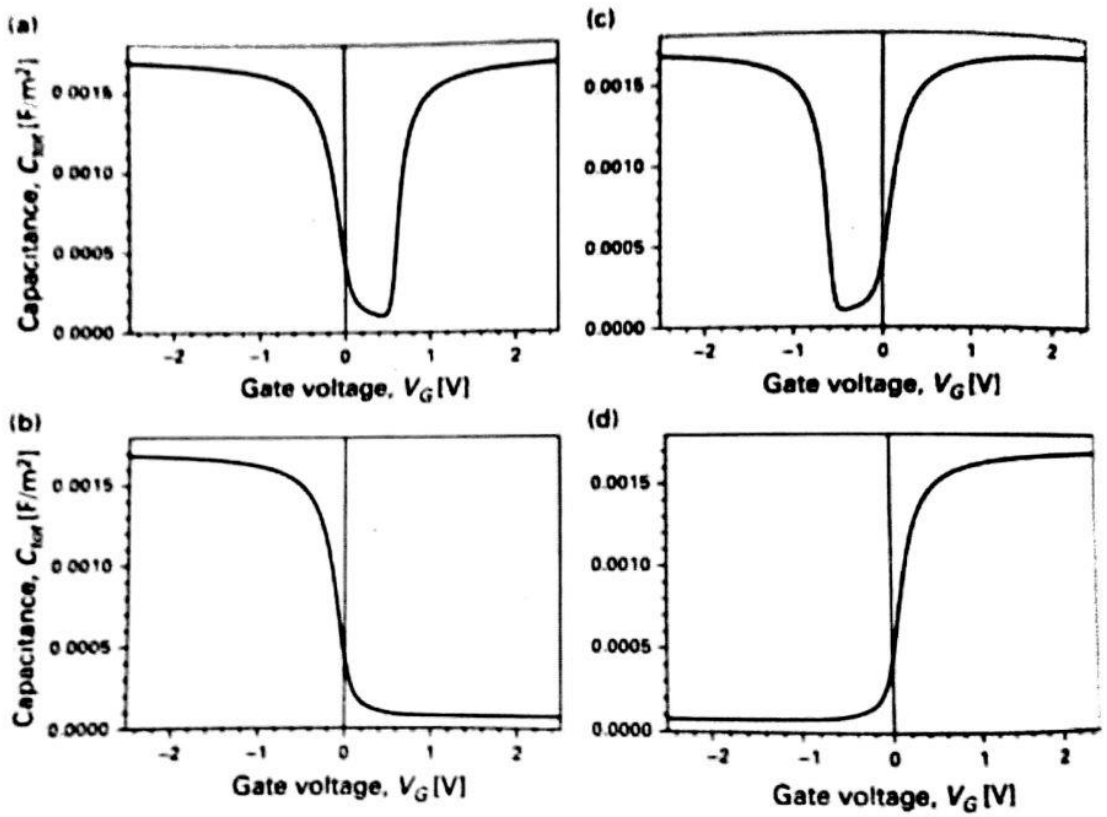

Figure 2.21: MOS CV sweeps of (a) low frequency p-type, (b) high frequency p-type, (c) low frequency n-type and (d) high frequency n-type [17].

Figure 2.22 displays the energy band diagrams of a p-type MOS structure when the gate is subjected to various levels of voltage biasing. As can be seen in (a), both the energy bands of the metal gate and p-type Si substrate are aligned. This is known as the flatband condition due to the fact that both energy band in the semiconductor and dielectric are flat. The flatband voltage point is an important reference voltage for a MOS structure in that it is the voltage which must be applied to flatten the bands. Accumulation of the MOS device as seen in (b), when a negative voltage is applied to the gate, results in an increase in the Fermi level of the metal gate relative to the Fermi level in the Si by the amount qV, where q is the fundamental charge (1.6×10^{-19} C) and V is the applied voltage. This creates a potential across the oxide layer, which induces band bending in the Si semiconductor

substrate. Upward band bending of the conduction and valence bands results in the Fermi level moving closer to the valence band

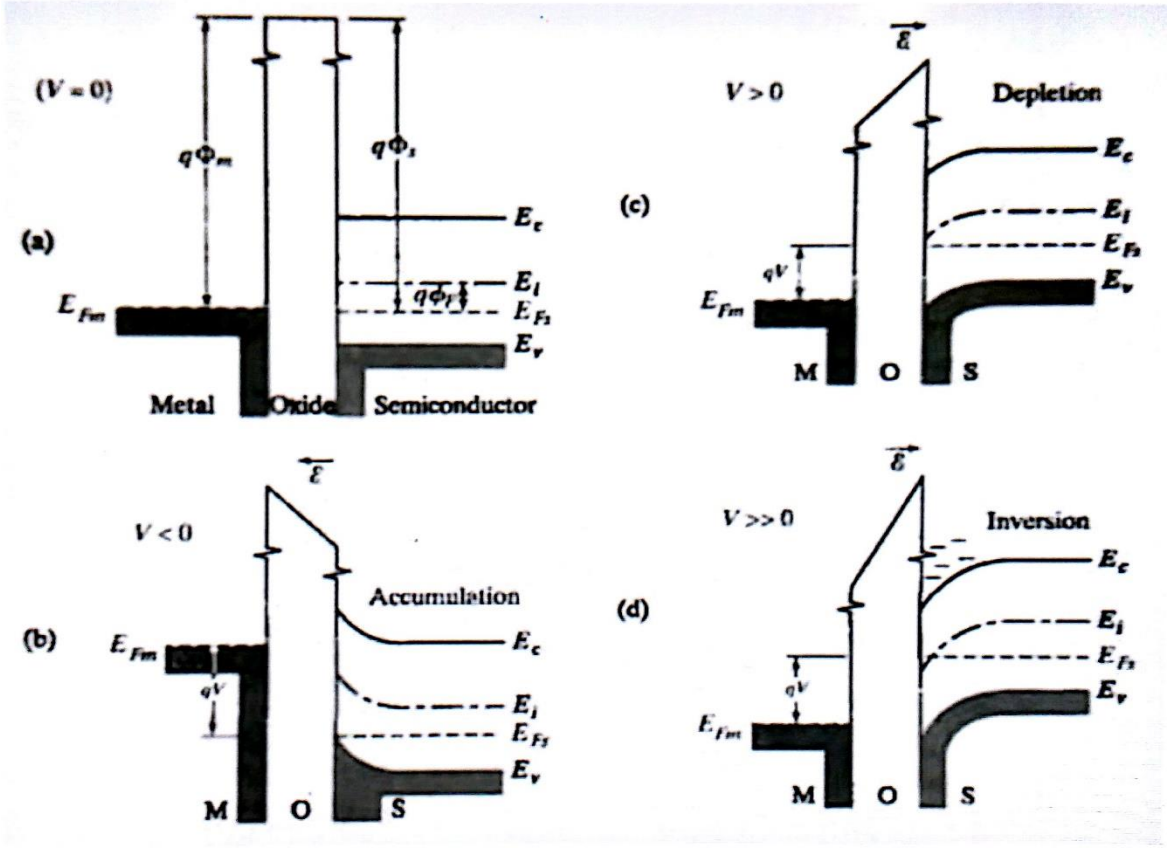

Figure 2.22: Energy band diagram of an ideal p-type MOS device during voltage biasing [18].

edge. This effect was previously shown in Figure 2.21 (b) as resulting in a maximum capacitance. When a positive voltage is applied to the gate the metal Fermi level moves below the Fermi level in the Si, again by the amount qV. This results in downward bending of the energy bands at the Si / SiO_2 interface and the creation of a depletion layer in the semiconductor. As the voltage is further increased on the metal gate, extreme band bending in the Si at the Si / oxide interface occurs. This results in the Fermi level of the Si being positioned near the conduction band, consistent with the creation of an n-type region in the Si substrate at the Si / oxide interface.

2.3.3 The Ideal MOS Device

While the ideal MOS structure can be thought of as a purely theoretical model, modern fabrication methods can produce very near to ideal device behaviour. The first requirement of an ideal MOS is to have zero leakage current through the oxide layer, in other words, the oxide layer must be a perfect electrical insulator. Secondly, both the metal gate and doped Si substrate must have the same workfunction value if a flat band condition is to be realised without an applied voltage. Additionally, within the oxide and Si / oxide interface, there must exist no charges, such as trapped charge or interface states. If the oxide layer within the MOS device was not a perfect insulator, the device would conduct a DC current under applied bias which if sufficiently large will make the capacitance measurements difficult to interpret.

The flatband condition exists in a MOS device when no band bending occurs at the Si / oxide interface as seen in Figure 2.22 (a). An ideal MOS device demands that both the metal and semiconductor substrate both have identical workfunctions, thereby giving the flatband position to be at exactly 0 V. When a workfunction difference exists between the metal and substrate, slight band bending occurs, even without an applied bias. If a large enough workfunction difference exists, the MOS device may actually be in an inverted state, even without an applied field, as demonstrated in Figure 2.23 (a) for a p-type substrate. Thus in order to achieve the flatband condition in a device with a gate / substrate workfunction mismatch, a positive or negative voltage must be applied to the device as seen in Figure 2.23 (b).

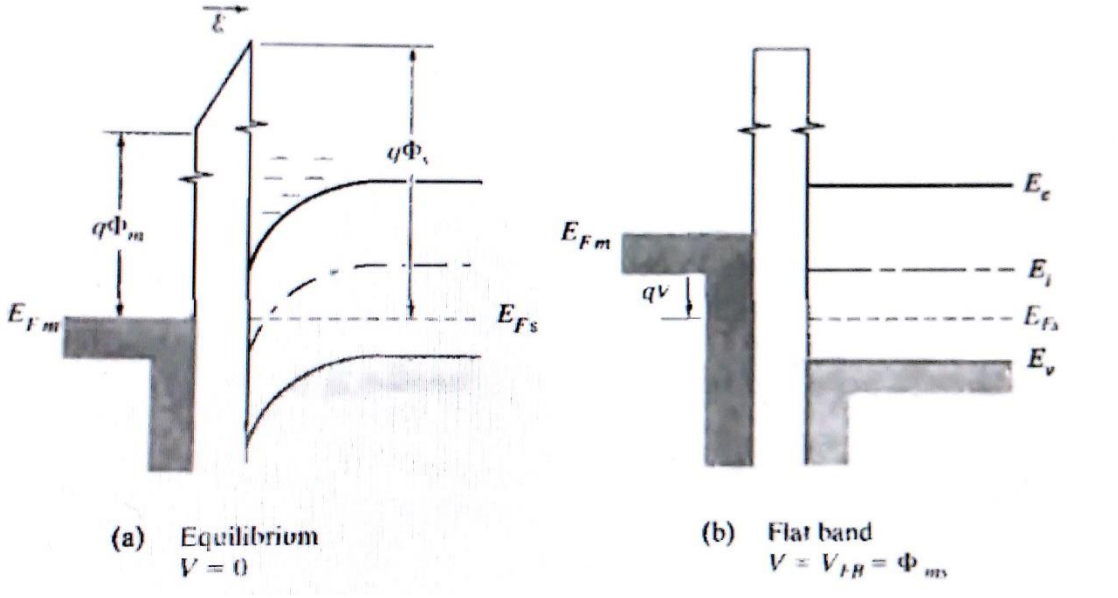

Figure 2.23: Effect of workfunction mismatch between metal gate and semiconductor substrate in a MOS device [18].

This then shows that in a non-ideal device, where the only non-ideal factor is a difference in workfunctions between the gate and substrate, the flatband voltage V_{FB} can be expressed as:

$$V_{FB} = {}^{\Phi}{}_{MS}$$

Equation 2.9: Flatband voltage of an ideal MOS, with different gate and substrate workfunctions.

where Φ_{MS} is the difference between the two workfuctions. A deviation from a non-ideal MOS device can also be as a result of charges within the oxide layer. A variety of charges can exist in the oxide layer, as schematically shown in Figure 2.24. Oxide trapped charges (Q_{ot}) are located in the bulk of the oxide layer, and have the ability to capture and release charge. The most common form of Q_{ot} is the oxygen vacancy in SiO_2 which can occur during the thermal growth of the oxide layer however,it is more prevalent when the oxide

layer is deposited via plasma enhanced chemical vapour deposition (PECVD) [17]. These charges can be passivated by annealing in a furnace at temperatures of ~ 500 ^{O}C in either pure N_2 or forming gas (typically 90% N_2, 10% H_2) [19]. The second type of charge in the oxide is the fixed oxide charge (Q_f). These charges are generally located either deep in the valence band or high in the conductance band of the semiconductor.

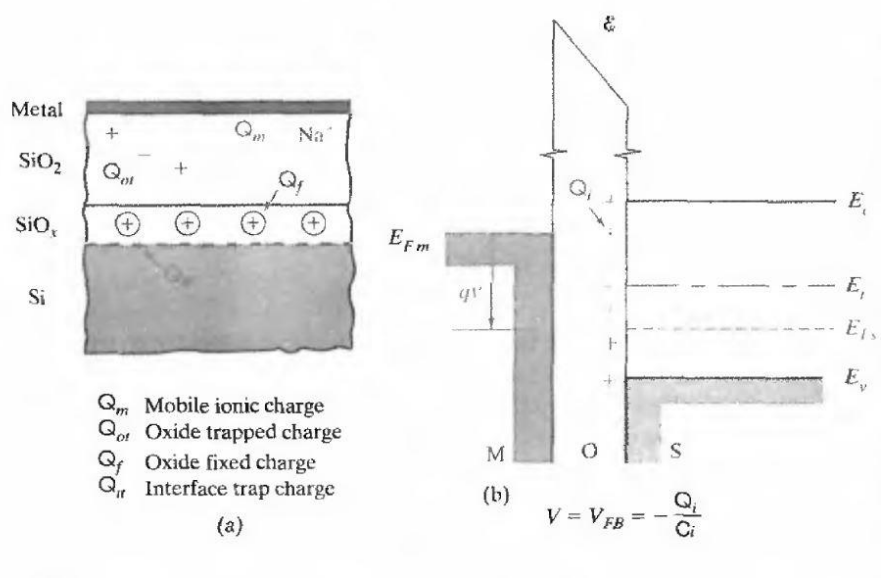

Figure 2.24: Various charges in an oxide layer of a non-ideal MOS structure [18].

Thus, they are generally not noticed under typical operating conditions. The third type of charge is known as interface states or interface charge (Q_{it}), generally formed as a result of the growth of a thermal SiO_2 layer from a Si substrate. The periodic Si surface layer of the Si substrate is distorted during the growth of an oxide layer which is amorphous in nature. This leads to defect sites and semi-oxidised Si (Si sub oxide states). These charge traps are found throughout the energy gap of the Si energy band diagram and are noticeable in a CV sweep as a “hump” that increases in size, as the frequency of the AC measurement signal is lowered, as seen in Figure 2.25.

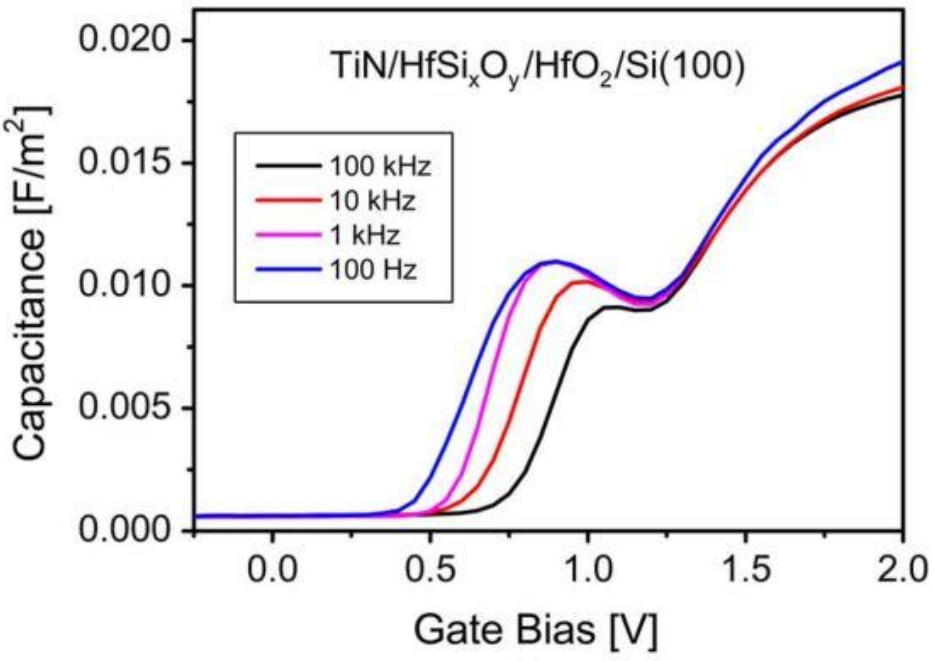

Figure 2.25: Interface state defects in a $HfSi_XOx$ dielectric layer [20].

The final type of charge within the oxide layer is a result of elemental contamination in the way of mobile ions. These ions, typically Na^+ ions, can be introduced into the dielectric during fabrication. Even a small quantity of ionic contamination can render a device useless, thus ultra-clean rooms are used in addition to stringent processing and wafer handling steps within semiconductor fabrication laboratories in order to reduce this issue. These ionic charges are usually mobile within the dielectric material, meaning that under an applied gate voltage, they can move toward or away from the Si / oxide interface. The result of introduction of a mobile positive charge species into the oxide material of a MOS is shown in Figure 2.26.

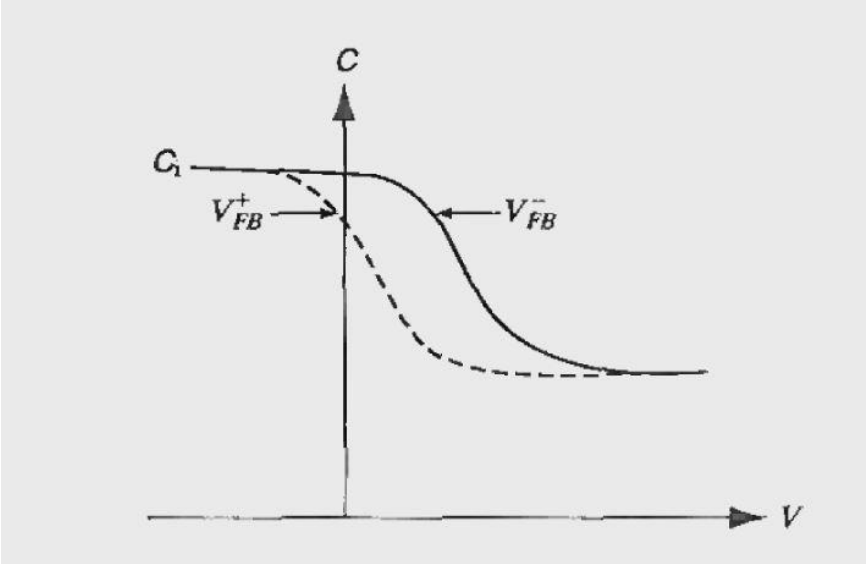

Figure 2.26: Mobile ion contamination effect on a MOS CV profile [18].

This indicates that during testing, the mobile ions can be repelled or attracted to the gate due to an applied voltage which then causes them to either move toward or away from the Si / oxide interface. If the ions are close to the Si / oxide interface, they will have a greater impact on the band bending due to the larger electrical flux the nearer they reside to the interface. This causes bending of the bands in both directions depending on the polarity of the CV sweep, giving a "double CV" profile with two distinct flatband voltages.

In order to calculate the amount of mobile ions within the dielectric, the MOS device must be stressed in order to push all ions towards the Si / oxide interface, thereby giving a maximum flatband shift (toward negative voltage values for positive ions and positive voltage values for negative ions). The device is then stressed in the opposite way in order to bias all mobile ions away from the Si / oxide interface, thereby reducing the effect of the ions on the flatband voltage. This difference in flatband voltage (ΔV_{FB}) can then be used to calculate the total amount of mobile ions within the dielectric (Q_m) as:

$$Q_m = C_{ox}(\Delta V_{FB})$$

Equation 2.10: Mobile ion concentration for a MOS device.

The effect of all these non-ideal charged states is to shift the flatband capacitance in addition to smearing or distorting of the CV profile (as seen in Figure 2.25). Thus in order to calculate the flatband voltage of a non-ideal MOS device with oxide defects, the total combination of charge defects in the oxide layer can be modelled as a single sheet of charge at the Si / oxide interface (Q_{total}) in order to simplify the calculations. This simplification then allows the flatband voltage of a MOS structure with oxide defects to be given as:

$$V_{FB} = -\frac{Q_{total}}{C_{ox}}$$

Equation 2.11: Flatband of a MOS device due to defects in the oxide material.

However, the flatband is also dependant on the workfunction of the material, thus giving the total flatband dependence as:

$$V_{FB} = \Phi_{ms} - \frac{Q_{total}}{C_{ox}}$$

Equation 2.12: Flatband voltage dependence due to non-ideal MOS characteristics.

2.4 Transmission electron microscopy

Transmission electron microscopy (TEM) is a useful imaging technique for nano-scale applications. The Rayleigh criterion sets the minimum resolution of a tradition light based microscope as:

$$\delta = \frac{0.61\lambda}{\mu sin\beta} \approx \frac{\lambda}{2}$$

Equation 2.13: Rayleigh criterion, limiting the resolution of optical microscopy.

Where δ is the resolution of the microscope and λ is the wavelength of light used in the microscope. Thus it shows that if a short wavelength of light such as UV (~ 320 nm) is used, then the best possible resolution obtainable is on the order of ~ 160 nm. This result indicates that traditional optical based microscopy techniques cannot be used to image ultra-thin films on the order of 10 nm or below. The de Broglie relation indicates that particles such as electrons have a wave-like nature associated with them, given as:

$$\lambda = \frac{h}{\sqrt{2meV}}$$

Equation 2.14: De Broglie relation for the wave nature of electrons accelerated by an applied voltage.

Where λ is the wavelength associated with an electron of mass m ($9.1x10^{-31}$ kg), e is the fundamental charge ($1.6x10^{-19}$ C), h is Plancks constant ($6.626x10^{-34}$ m^2kg/s) and V is the applied voltage which accelerates the electron. Thus it can be seen that if the applied voltage (V) is increased, the wavelength of the electron will decrease. By using state of the art electron lenses and high acceleration voltages (on the order of 100's of kV)

resolutions of 0.2 nm can be achieved [21]. In order to attain these ultra-high resolutions, a sample must be fabricated such that it is electron transparent to an incident electron beam. This is typically achieved by starting with a large planar sample (~1 cm x 1 cm) with a wafer thickness on the order of ~ 750 μm. A highly focused and energetic ion-beam (typically gallium) is then used to cleave a cross-section of the sample, which itself is thin enough to be electron transparent. This lamella structure is then loaded onto a TEM sample mount and can subsequently be used to image the cross section of the sample from substrate to sample surface. A typical TEM sample from these studies is shown in Figure 2.27, where initially, and optical microscope is used to image the sample holder and ultimately a view of the overall lamella structure. TEM is then used to further scale down to nanometre dimensions.

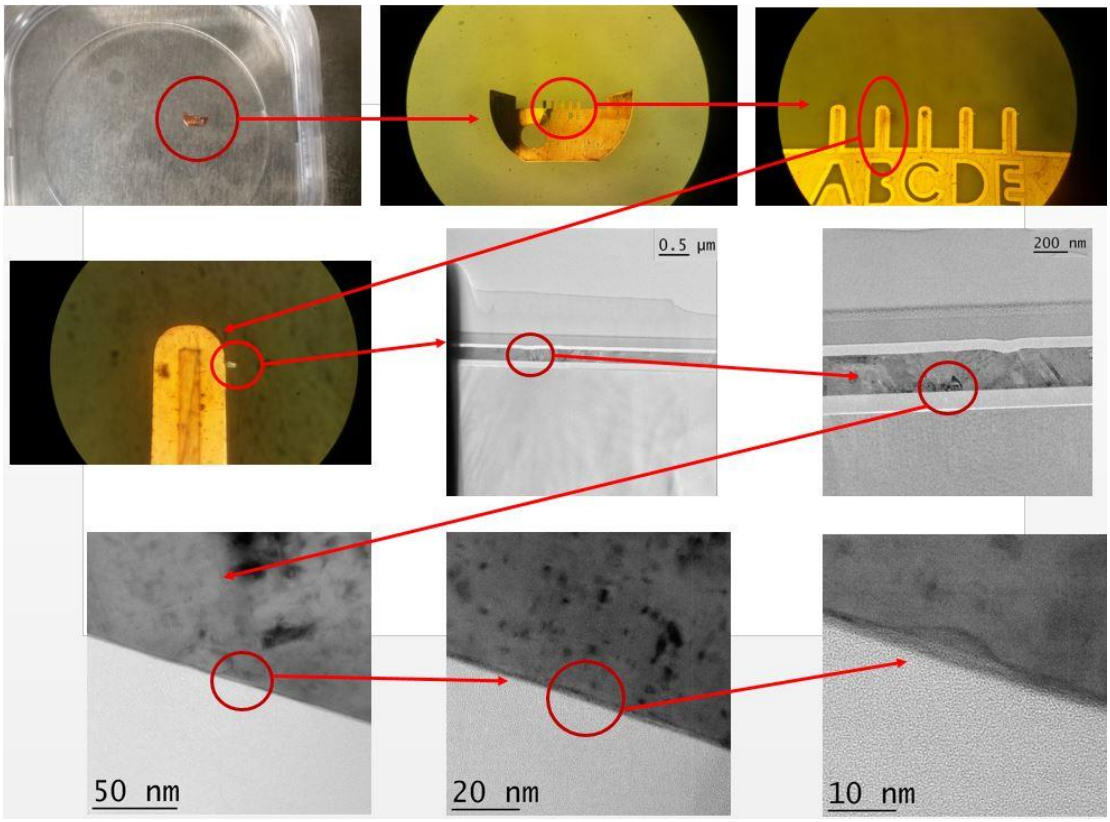

Figure 2.27: TEM lamella structure as seen from both optical and transmission electron microscopy techniques.

A schematic of a typical TEM is shown in Figure 2.28. As can be seen, in order to focus the high energy beam down to a sub nanometre probe size, a number of electron lenses are needed. Once the electron beam interacts with the electron transparent sample, it passes through onto a CCD camera where an image can be obtained.

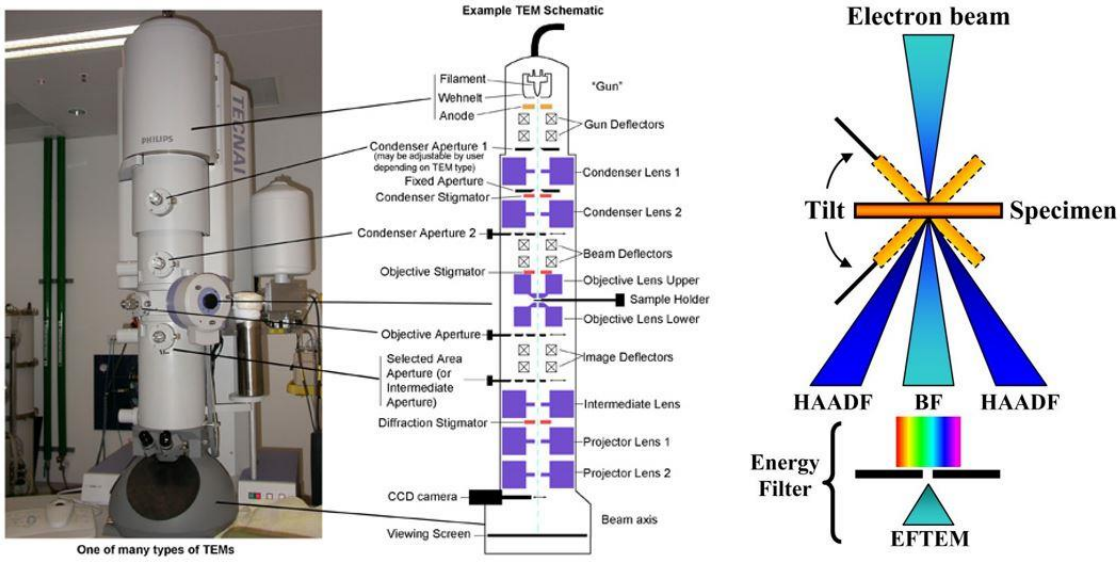

Figure 2.28: Diagram illustrating the components of a typical TEM system and both bright field (BF) and high angle annular dark field (HAADF) modes.

In addition, a high vacuum environment is required in order to reduce electron scattering from any ambient gasses. Various modes of TEM are used (Figure 2.28) such as bright field (BF) TEM, where the electron beam passes directly through the sample, and then a small aperture. This mode is sensitive to the thickness of the sample, with low density / low thickness areas appearing bright and thicker / higher density areas appearing darker. In addition crystalline structure can be determined due to diffraction patterns within the image. High angle annular dark field (HAADF) imaging utilises the scattered position of the beam once it has passed though the samples. A dark field detector is placed at a high angle relative to the primary beam and sample, thereby detecting only the scattered

electrons. This technique is highly sensitive to the atomic number of the elements in the sample, and thus gives a large contrast to the Z ratio of elements in a sample. In addition to HAADF mode which uses the scattered portions of the sample beam, other techniques can be used in parallel which utilise the un-scattered portion of the electron beam such as energy dispersive X-ray (EDX) spectroscopy or electron energy loss spectroscopy (EELS), thereby simultaneously giving elemental mapping capabilities to the technique.

2.4.1 Energy Dispersive X-ray Spectroscopy

As stated previously, a TEM not only has the ability to image a sample with atomic scale resolution, but it can also simultaneously perform elemental mapping of interfaces. EDX utilises a small electron beam probe size which can be scanned across a sample region of interest. As the electron beam passes through the scanned area of the sample, it interacts with the elements in the sample, with one such interaction being the ejection of an inner core electron within an atom of the sample due to the high energetic primary beam. This causes a core hole in the atom which can be filled by an electron from a higher energy state (higher orbit), similar to the previously described Auger process. As the electron fills the core hole, a photon, typically in the X-ray wavelength is emitted due to conservation of energy of a higher energy electron filling a lower energy state in the atom. This emitted X-ray photon is characteristic of the electron orbits involved in the process, which in turn is elementally characteristic, thereby a measurement of the emitted X-ray photon energies can give information to the elemental composition of a single point in the sample as defined by the electron beam spot size. Thus an elemental line profile of various interfaces in the sample can be obtained by scanning an electron probe beam across the interfaces and measuring the various photon energies emitted from the sample.

2.4.2 Electron Energy Loss Spectroscopy

EELS is a technique, capable of determining not only the elemental structure of a sample, but similar to XPS, the bonding environment within the sample. This is particularly useful when combined with the high resolution images obtained during TEM imaging, thereby allowing identification of the various elements across a number of interfaces to be obtained. The technique relies on a well energy defined electron beam to pass through the sample of interest, making this analysis method ideal for TEM systems. The electrons within the beam can in-elastically scatter within the sample, or promote various electrons to higher orbital states within the sample. The various energy loss states of the incident beam are characteristic of the material present within the sample, and thus an elemental map can be formed of the sample. Figure 2.29 shows a typical EELS spectrum, outlining the various features associated with energy loss due to electron beam / sample interactions. The zero loss peak is due to the primary electron beam which has passed through the sample, with no loss of energy. A large plasmon resonance peak can be seen which is due to the excitation of valence electrons within the sample. At higher energy losses, atomic-core loss lines can be seen. These energy loss lines are similar to XPS core level spectra, with the process involving removal of a core level electron from an atom, thus giving a characteristic loss peak due to the well-defined energy needed to remove an electron from an atomic orbital.

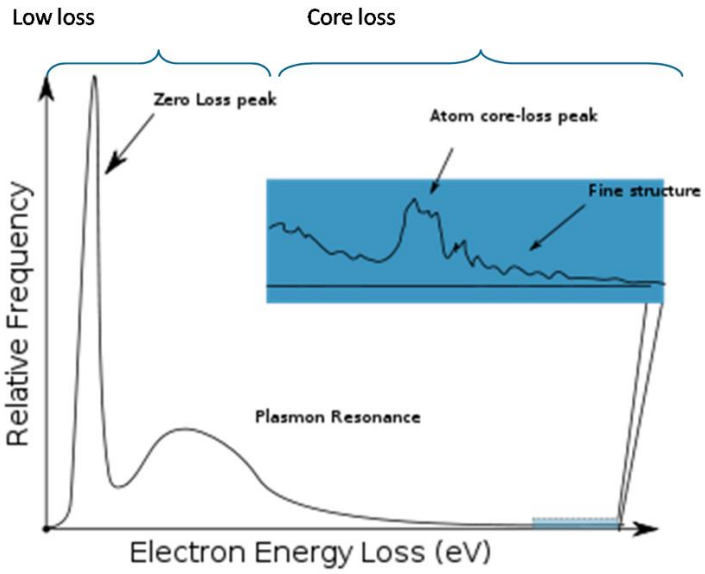

Figure 2.29: EELS spectrum showing the various characteristic energy losses within a sample.

2.5 Secondary Ion Mass Spectroscopy

Secondary ion mass spectroscopy (SIMS) is a highly surface sensitive technique used to track elemental changes throughout a sample [22]. An ion beam is used to sputter the top layers of a sample within a UHV environment. Sputtered fragments of the sample surface are then detected using a mass spectrometer, thereby giving elemental compositions of the sample surface, as schematically depicted in Figure 2.30. The ion beam can then be left to continuously sputter through the sample, thereby giving an elemental depth profile of the sample. Typically an ion beam composed of Ar^+ ions is used to sputter the sample surface, thereby allowing acceleration of the ions, due to the charge associated with the ionized Ar, whilst minimising chemical interactions of the ion beam with the sample due to the inert nature of Ar.

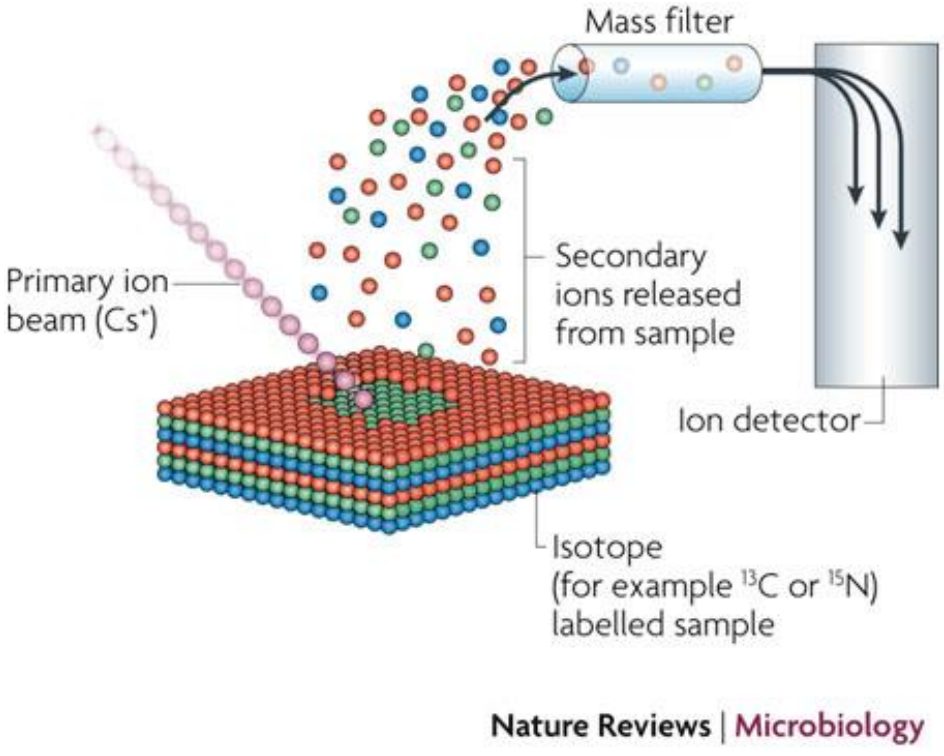

Figure 2.30: SIMS experimental set up [23].

Typically the ion beam used is focused to a small spot size and raster scanned across a larger area of the sample in order to create a crater during sputtering of the sample surface. Secondary ions can then be selectively analysed from locations within the centre of the crater, thereby minimising crater edge effects. If a small spot size is used, relative to the overall sampling area, an elemental image of the sample can be obtained. As the beam sputters deep into the sample surface, a three dimensional elemental map of the sample surface can also be obtained.

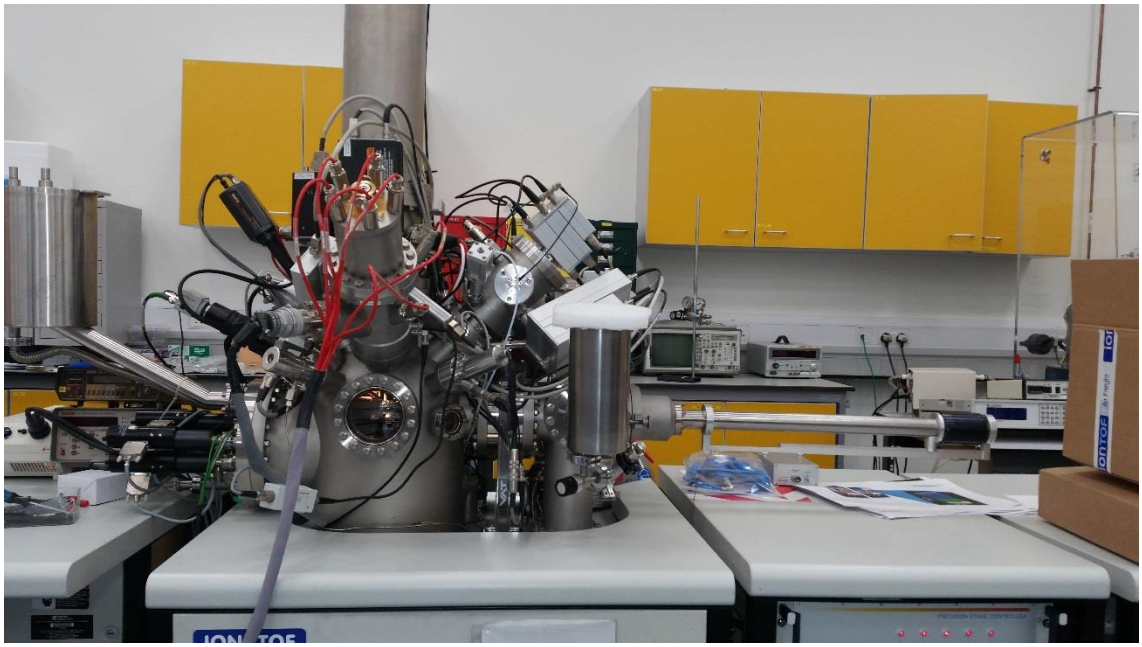

Figure 2.31: SIMS system in the National Physical Laboratory (NPL) in the UK, used in this study for the detection of Cu diffusion.

2.6 X-ray Absorption Spectroscopy

Fluorescent yield X-ray absorption spectroscopy (XAS) was performed on the Mn K-edge at room temperature using the NIST beamline (X23A2) at the National Synchrotron Light Source (NSLS) in Brookhaven. XAS is a technique which allows deep (in some configurations total sample) probing of the sample due to the high energy photons used. In order to perform an XAS measurement, a tuneable source of high energy photons is needed, typically achieved by using a facility such as a synchrotron in conjunction with a monochromator. A typical XAS measurement is shown in Figure 2.32 in addition to a typical XAS measurement set up.

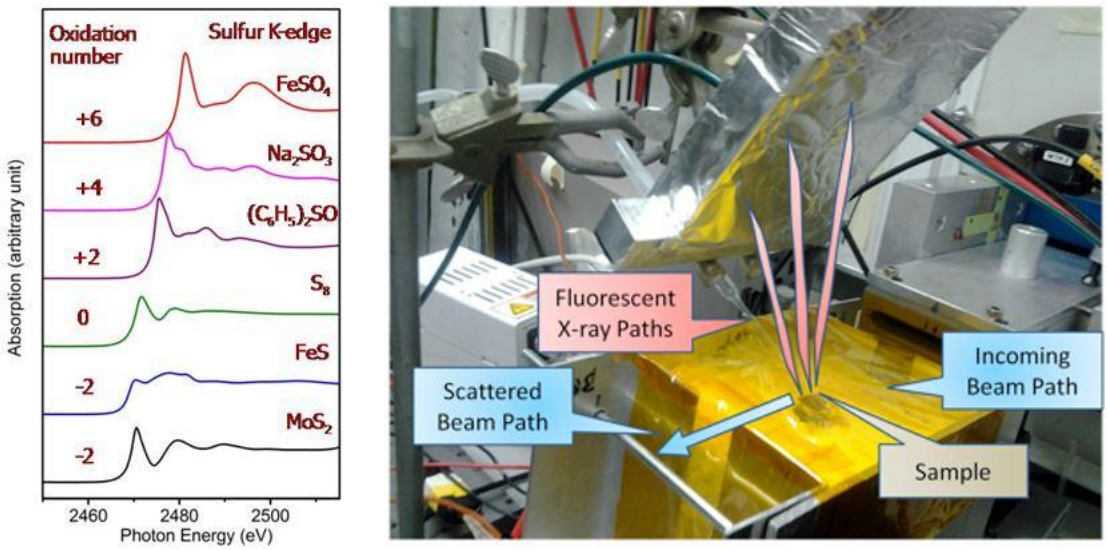

Figure 2.32: XAS Sulphur K-edge measurements and XAS fluorescent yield apparatus [24][25].

As can be seen from the sulphur K-edge data of various sulphur containing compounds, a strong difference exists in the spectra due to the change in oxidation state of the sulphur within the samples. This indicates that XAS is a useful technique to investigate the chemical state of various compounds within a sample. Various reference samples can be measured and compared to data acquired from a sample under investigation in order to

study the oxidation state of the material in question. Different elemental absorption edges can be used to examine a sample, depending on the elements present.

The absorption of an X-ray photon by a sample is dependent on the elements present within the sample. A flat background is typically observed as the photon energy is increased until a large absorption is noted, this is known as the absorption edge. Various absorptions edges can be probed, depending on the various electron orbitals within a sample which can absorb a photon of a given energy [26].

In this study the Mn K-edge was used in order to investigate the oxidation state of Mn when deposited on various dielectric materials. The Mn K-edge was examined by using a tuneable photon source between 6500 eV and 6650 eV.

2.7 References

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3 Experimental systems and methods

3.1 Introduction

A number of systems and methods are utilised throughout the course of this study including ultra-high vacuum systems, metal deposition techniques, XPS peak fitting procedures, electrical measurements and stressing of MOS devices. This chapter describes the process of using the techniques shown in the previous chapter in order to extract experimental results from a number of key systems.

3.2 Ultra-high vacuum systems

In order to perform XPS measurements, as described in the previous chapter, a requirement of an ultra-high vacuum (UHV) environment is imposed. This environment is necessary due to the mean free path of electrons and other gaseous molecules within a vacuum system being larger than at atmosphere conditions. XPS requires the measurement of the kinetic energy of electrons emitted from a sample which is irradiated by soft X-rays [1]. In order to measure the KE of the emitted electrons, they must pass into an electron energy analyser, without undergoing any collision events which would alter the KE energy ultimately measured by the analyser. Thus a UHV environment is necessary in order to remove as much gas from the space between the sample surface and the analyser as possible. The mean free path of an electron or gaseous molecule within a UHV environment (typically ~ $5x10^{-9}$ mbar) is on the order of ~ 40 km [2]. This means that any molecules within a UHV environment will travel on average 40 km before a collision with another gas molecule. Thus if the distance from sample surface to electron analyser is small relative to this large mean free path during XPS analysis, practically all

electrons emitted from the sample surface should traverse the relatively small distance from the sample surface to analyser without any collisions which could alter the KE of the electrons. This UHV environment is achieved by the use of various pumps and UHV compatible chambers in order to reduce the number of gas molecules within a vacuum vessel as much as possible. In addition to the increased mean free path of molecules and electrons within a UHV environment, the lower levels of chemical species such as oxygen or water vapour are necessary in order to avoid unwanted chemical reactions which would otherwise occur at atmospheric or low vacuum conditions. This enables the chemical reaction between a metal and dielectric substrate to be examined in-situ without any further reactions which would complicate the analysis. Further still, many components used such as X-ray sources or mass spectrometers could not operate at atmospheric or low vacuum conditions due to the sensitive nature of the components. Filaments within these devices would burn out if exposed to higher pressures and thus UHV is also required in order to run these systems without degradation in the lifetime of these UHV analytical components.

UHV environment is achieved by using a gas tight, stainless steel vacuum chamber to hold vacuum. Air is then pumped form this chamber, initially using roughing pumps. Once a rough vacuum is achieved in the chamber, additional pumps are used such as turbo molecular pumps or ion pumps in order to further reduce the pressure to HV / UHV conditions. Typically a bake is performed on the system during pump down in order to remove any water or other contaminants within the system which would otherwise slowly degas at room temperature, causing a larger background pressure.

3.3 XPS

The main technique used in this thesis is the in-situ approach of barrier layer formation using XPS analysis. This technique is realised by initially loading a substrate material of choice into the UHV system with XPS, thin film metal deposition and annealing capabilities. Once loaded, the sample is analysed via XPS. The sample is then heated or "degassed" to a temperature of typically ~ 500 ^{O}C in order to remove any organic or water vapour contamination from the surface which may occur prior to insertion into the UHV system. Once the sample surface is clean, XPS is then used again to analyse the pristine surface in order to obtain a reference data set of the substrate. A thin film (~ 2 nm) of a choice metal (Mn for example) is then deposited onto the sample surface within the UHV environment. XPS is again used to acquire data for the sample with this thin metal layer deposited onto the surface. A series of anneals typically takes place with XPS analysis performed after each anneal stage. These anneals are used to drive a chemical reaction between the deposited metal layer and the substrate material, in an effort to form a self-forming barrier. The fact that the whole experimental procedure is performed in the UHV system means that precise control is obtained during analysis. The metal deposition, being performed within UHV enables the deposition of pure metallic species with minimum oxygen present. Additionally, annealing within UHV allows the chemical reaction of the deposited metal and substrate to be observed without interference from contaminants.

Two XPS systems were primarily used in this study, in conjunction with a third XPS system which was used for backup support and ex-situ analysis of samples. The first system, named "XPS 1" is a UHV dedicated surface science chamber used in the study of Cu diffusion barrier layer materials. The system is equipped with a triple channel electron analyser in conjunction with a dual anode X-ray source (Al and Mg anodes). Thin film metal depositions can be performed in-situ using the Oxford Applied Mini

Electron Beam evaporator. This e-beam is a four pocket model, enabling the deposition of up to four metals, sequentially or simultaneously onto a sample surface. Annealing studies can be carried out in-situ by way of resistive heating of the sample stub. In addition the system has a mass spectrum analyser, used to monitor partial pressures of various species within the UHV environment and a thermal gas cracker, used to split molecular species such as O_2 to atomic species such as atomic O.

The second XPS system "XPS 2", is a UHV system with in-situ XPS, thin film deposition, annealing and secondary ion mass spectroscopy (SIMS) capabilities. Similar to XPS 1, this system features a triple channel electron analyser and dual anode x-ray source (Al and Mg) for XPS analysis. Thin film deposition is achieved by hot filament deposition of metal, typically by heating a tungsten filament with a metal of choice in contact with the filament until evaporation of the material occurs. SIMS can be carried out using both Ar^+ and N_2^+ ions.

3.3.1 XPS peak fitting

As stated previously, XPS can not only be used to identify elements in the top ~ 7 nm of a surface, but it can also show what chemical state each element is in, for example a spectra may indicate the presence of aluminium (Al), with a closer examination of the Al 2p line, the chemical bonding state of the Al can be deduced (metal Al, Al_2O_3, Al carbide etc.). Peak fitting analysis of XPS spectra is mainly needed when more than one peak overlap within the spectra, making identification of the individual chemical species present in the sample challenging. For example, within the Si 2p spectra of a 5 nm thermally grown SiO_2 layer on a Si substrate, there are two peaks that can be easily be identified within the spectra, as seen in Figure 3.1.

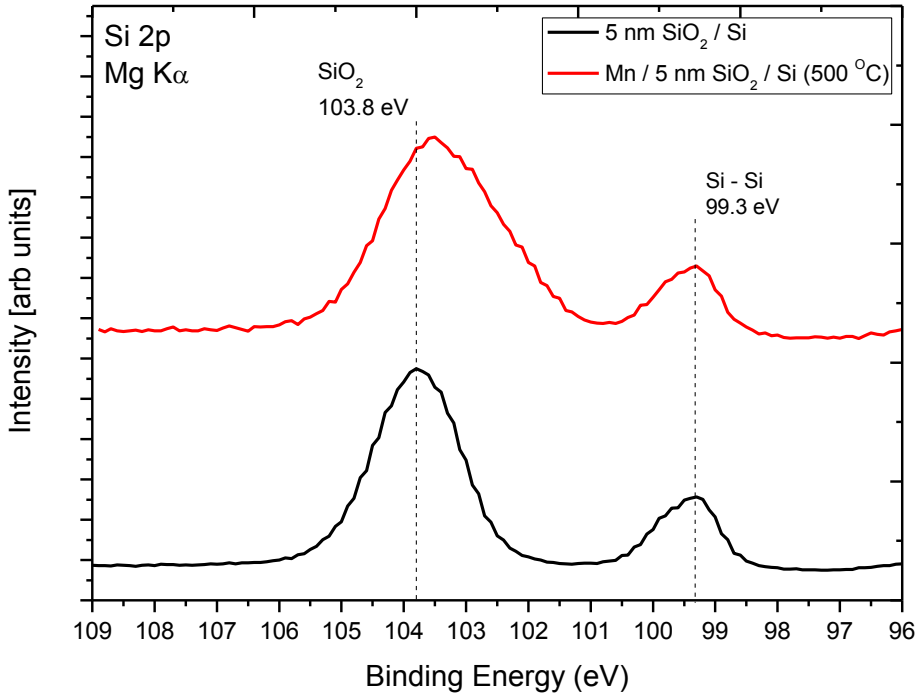

Figure 3.1: XPS Si 2p spectra of 5 nm SiO_2 and 5 nm SiO_2 with $MnSiO_3$.

When ~ 2 nm Mn is deposited and annealed on the 5 nm SiO_2 layer, a broadening of the SiO_2 related peak is noted. This is due to the growth of a new peak, at a LBE position to the original SiO_2 peak, which is attributed to the chemical bonding of Si in $MnSiO_3$. Both the SiO_2 and $MnSiO_3$ related peaks are too close in BE positions to be manifested as two separate peaks, thus peak fitting analysis must be performed in order to retrieve the parameters of the newly formed $MnSiO_3$ peak such as BE position and peak width. All peak fitting analysis in this study was carried out using AAnalyszer peak fitting software, as seen in Figure 3.2.

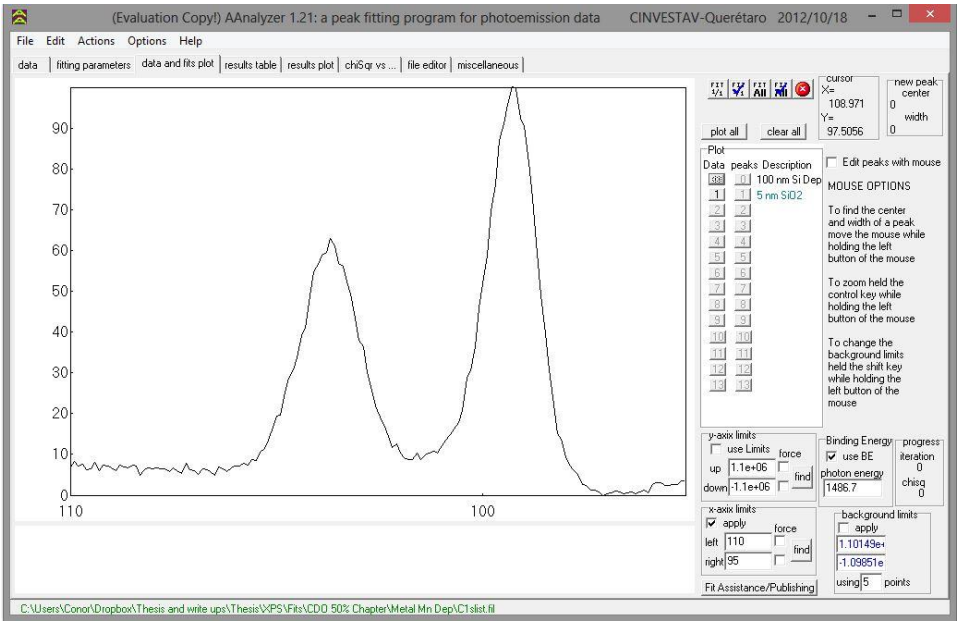

Figure 3.2: AAnalyser peak fitting software.

To peak fit spectra over the course of an experiment, initial parameters of the substrate spectra must be extracted, in order to use these in the more complex spectra at the end of an experiment as shown in Figure 3.1. All peak fitting analysis used in this study utilised a Shirley-Sherwood background in order to account for the rise in background of the spectra as a result of scattered electrons emerging from the sample surface during data acquisition. A number of different component peak profiles can be fitted to a spectrum, with the peak of choice in this study being a Voigt profile, consisting of a 3:1 Gaussian and Lorentzian profiles. The Lorenztian component of the peak is attributed to the core level lifetime and relates to the intrinsic width of the peak. The energy width of this peak is a result of the Heisenberg uncertainty principal which relates the uncertainty in energy to an uncertainty in the core hole lifetime. The major component which dictates the full width half maximum (FWHM) of the peak is the Gaussian component. This Gaussian component is related to instrumental broadening due to the energy width of the X-ray source and the limitations of the electron energy analyser. Peak fitting of a component

within a spectra also requires knowledge of the photoemission line which is being analysed, for example the Si 2p line is a doublet feature, this doublet however appears as a single peak due to the small separation of the two peaks (Si $2p^{1/2}$ and Si $2p^{3/2}$) at a value of 0.6 eV. Thus when fitting the Si 2p spectra, a doublet Voigt peak must be used. This doublet parameter can be reduced to a single peak shape in the case of the SiO_2 component peak due to the large FWHM and lack of asymmetry within the peak profile. As can be seen in Figure 3.3, peak fitting of the SiO_2 substrate requires the use of two peaks attributed to Si-Si bonds within the substrate and Si-O bonds within the SiO_2 layer which was thermally grown on the substrate.

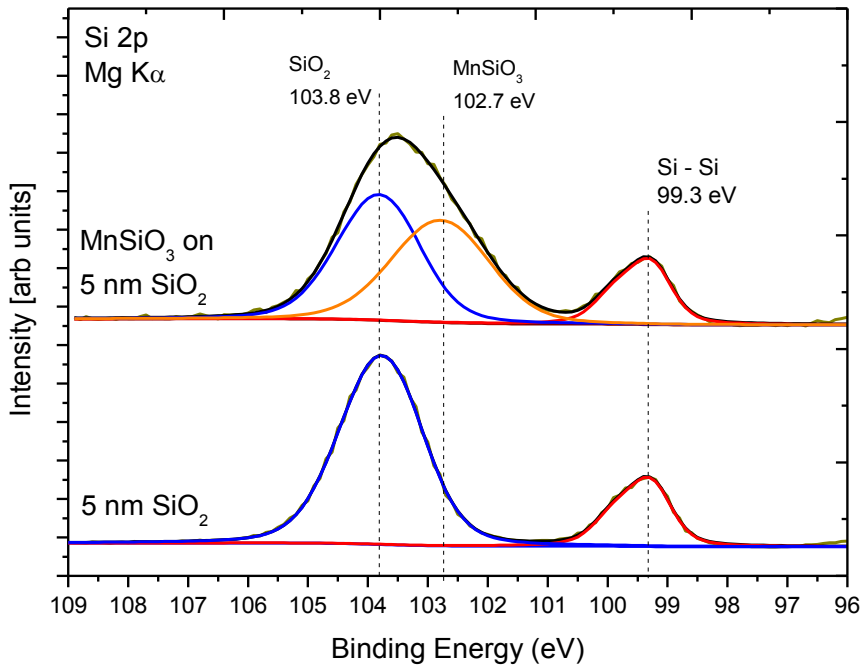

Figure 3.3: Peak fitting of 5 nm SiO_2 with $MnSiO_3$.

The peak parameters associated with the substrate were then fixed and used to peak fit the second spectra which contains a third chemical species attributed to $MnSiO_3$. When the original peak fit values are used, it is evident from broadening of the HBE peak that

a third peak must be included in the peak fitting analysis. This third peak at a position of 102.7 eV is attributed to the new chemical species $MnSiO_3$. Peak fitting values used in Figure 3.3 are displayed in Table 3-1.

Peak Fitting Parameters	Peak Position	Gaussian	Lorentzian	Orbital splitting
Si – Si	99.3 eV	0.67	0.25	0.6 eV
SiO_2	103.8 eV	1.48	0.25	N/A
$MnSiO_3$	102.7 eV	1.68	0.25	N/A

Table 3-1: Peak fitting parameters for $MnSiO_3$ on 5 nm SiO_2.

This fitting procedure can be applied to all peaks within the acquired XPS spectra at different steps in the experiment. Adopting a systematic approach to curve fitting where the fitting parameters are held fixed throughout the experimental sequence give credibility to the resulting analysis. This approach is used extensively in this study in order to identify evidence of any chemical reactions which take place during experimental analysis.

3.3.2 XPS layer thickness calculation

Thickness calculations using XPS spectra of ultra-thin films can be performed in order to give insight into the structural composition of a sample. Initially, a survey scan of the sample is taken in order to identify all elements within the sample. Narrow window – high resolution spectra of key elemental photoemission lines are then taken in order to gain additional information to the chemical species within the sample. Angularly resolved XPS can then be used to identify which elements and chemical species are surface

localised, assuming that the sample is in a layered form and not homogenous. Two variations of thickness measurement are possible. The first method uses the relative signal of the substrate peak and over layer in order to calculate the thickness of the over layer. This method works best when the peaks used from both layers are from the same photoemission line, for example the Si 2p line in both Si-Si and Si-O, as seen in the 5 nm SiO_2 sample presented in Figure1.3. If the IMFP of the over layer and substrate are known and can be approximated by a single term, then a thickness of this layer can be calculated. By assuming comparable binding energy and IMFP values, a simplified calculation of over layer thickness is given as:

$$\mathrm{d} = \lambda . \ln(1 - \frac{I(L)}{I(s)+I(L)})$$

Equation 3.1: XPS thickness determination.

Where d is the thickness of the over layer in nanometres, λ is the IMFP of the electron, I(L) is the signal of the over layer and I(S) is the signal of the substrate. A different approach to thickness measurement of an over layer can be to use software available such as the NIST Electron EAL database [3]. The method used in this software works well with the in-situ approach taken in this study, where initially a substrate is loaded and analysed with XPS. A thin metal layer is then deposited onto the substrate and the sample is again analysed using XPS. The attenuation of the substrate signal can then be used to give the thickness of the over layer, assuming the IMFP of the over layer material is known. This allows the thickness of various over layers to be calculated, in contrast to the previously discussed method which relies on similar BE positions and mean free paths within the sampling depth.

3.3.3 XPS elemental composition

Elemental composition of a sample can be achieved during XPS analysis. This can be particularly useful when the stoichiometry of a sample is to be analysed. In order to determine the elemental composition of the top surface of a sample via XPS, the sample must be homogenous at the surface in terms of elemental composition and not in a layered form within the XPS sampling depth. In addition, values for the sensitivity factors for each element and photoemission lines must be available in order to carry out the necessary calculations. Different elements and electron orbits within the atoms of the top surface of the sample will have varying probabilities of undergoing a photoemission process via irradiation of the X-ray source. This is determined by the energy of the radiation (anode selection) and photo-ionisation cross sections for the various electron orbitals within an atom. In addition, the KE of the out coming electrons will be different for each element present, and thus must also be factored into any such values.

When all the necessary information is obtained, a table of relative sensitivity factors (RSF) can be produced. These tables are freely available [3-5] and describe the various sensitivity values of each element within an XPS spectrum. Although this method is traditionally labelled as semi-quantitative, the real strength of this method is seen when two samples are analysed side by side, in a direct comparative sense, thereby reducing processing errors to identify elemental composition differences between both samples. Typically in order to calculate the elemental composition of a sample, XPS survey spectra are acquired in order to identify all elements present within the sample. This is useful as within the survey scan, all elemental photoemission lines are acquired using the same scan parameters, thereby allowing a good comparison between peak areas. Once the elemental lines are acquired, the strongest line from each element is chosen, and peak

fitted in order to compare the area of each elemental photoemission peak. The following formula can then be used to normalise the peak area to a standard ratio, by modifying the area via the RSF factor of that peak:

$$A_E = \frac{Peak\ Area}{RSF}$$

Equation 3.2: Modification of elemental peak area via relative sensitivity factor.

Where A_E is the modified elemental peak area, REF is the relative sensitivity factor for that elemental photoemission line and Peak Area is the calculated peak area from the acquired XPS data.

Once all elemental peak areas have been modified by the appropriate RSF for each elemental photoemission line, a chemical composition can be calculated by:

$$E_1 = \frac{A_{E1} + A_{E2} \ldots . + A_{EN}}{N}$$

Equation 3.3: Calculation of the elemental ratios within a sample.

Where E_1 is the element under investigation, AE is the modified peak area of an elemental line and N is the number of elemental lines used in the calculation. Thus a total percentage breakdown of the elemental composition within a sample can be achieved via XPS analysis.

3.4 Metal Oxide Semiconductor Fabrication

MOS fabrication was necessary in order to electrically test barrier layer performance in this study. The fabrication of electrical devices is extremely challenging due to the sensitivity of devices to external contaminants and process defects [6,7]. MOS structures in this study were fabricated in two locations. The first location was the Tyndall National Institute, Cork, where both pure copper (Cu) and CuAl alloy (90:10 % wt) MOS structures were fabricated on n-type Si wafers with a 100 nm SiO_2 dielectric layer, in a dedicated clean room fabrication facility. The second location for fabrication of MOS devices took place in the XPS 1 UHV system described above. The process of fabrication of MOS devices within a UHV environment allows the use of ultra-clean interfaces and metal depositions in addition to the added benefit of utilising in-situ XPS characterisation throughout the fabrication process. Initially, a 2 cm x 1 cm n-type Si substrate which had 100 nm thermally grown SiO_2 was placed on a sample stub with a 1 cm x 1 cm Si mask (see Figure 3.4) over half the sample, held in place with screw fixtures.

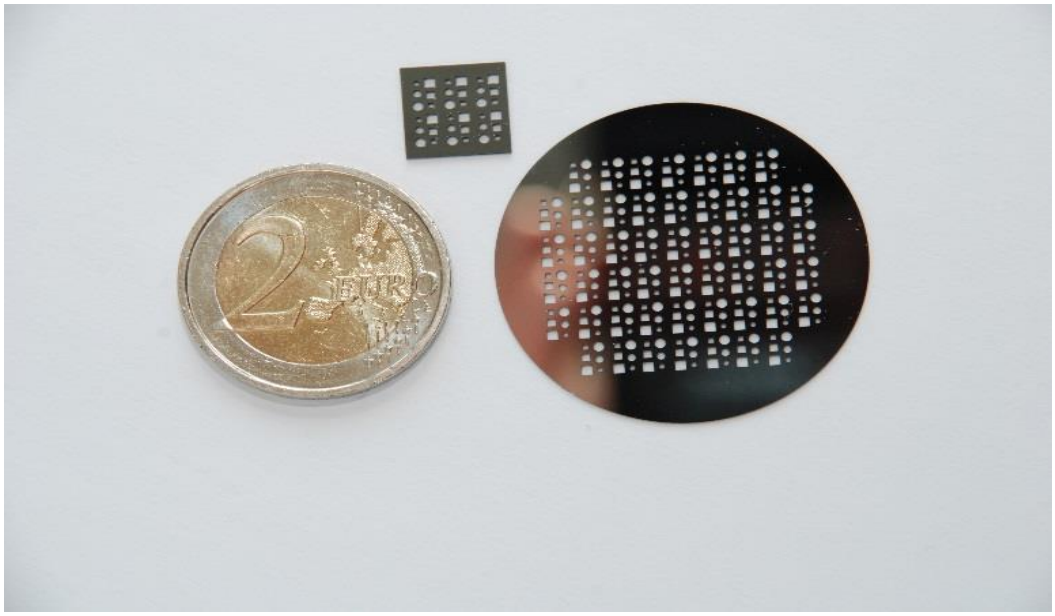

Figure 3.4: Si shadow masks used for fabrication of MOS devices.

This set up allowed a secure fitting of the mask to substrate, thereby eliminating movement of the mask during experimentation. The use of a sample stub with in-situ heating capabilities allowed the samples to be degassed prior to experimentation in order to form an ultra-clean interface and also to anneal the sample during barrier layer formation. The sample half covered by the Si mask allowed the fabrication of MOS devices, while the blanket portion of the sample allowed the use of XPS to characterise the interface chemistry. Due to the fact that the whole sample (MOS and XPS portions) are on the same sample stub, any metal depositions or anneal treatments will affect the entire sample identically, thus allowing the parallel study of interface chemistry with MOS fabrication. Improper alignment of metal depositions in the direction of the shadow mask results in shadowing the gate materials as seen in Figure 3.5.

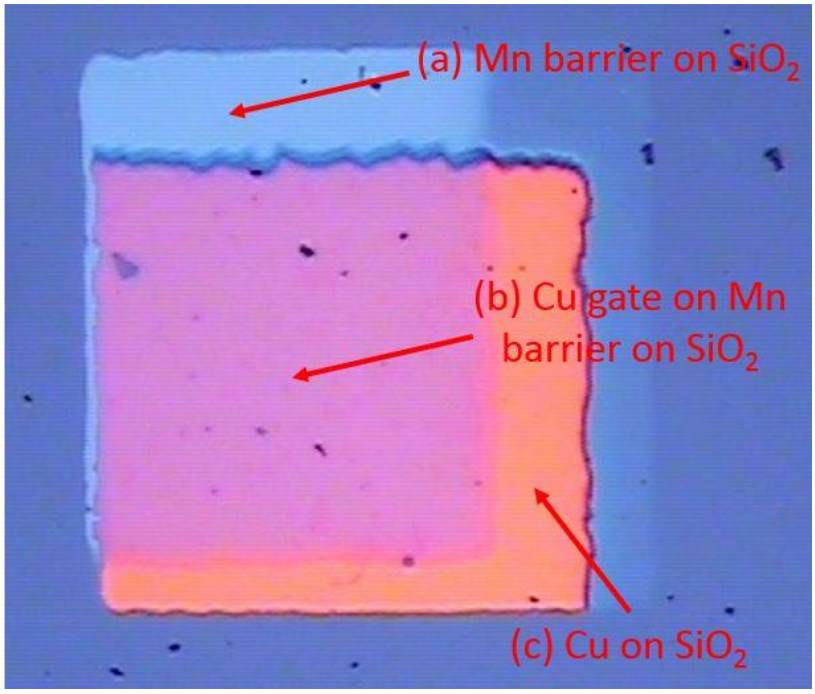

Figure 3.5: Optical microscope image of a MOS structure showing shadowing of the metal layers within the gate.

As can be seen in Figure 3.5, a blue colour rectangular region can be seen in the top left portion of the gate area, this is attributed to the ultra-thin Mn barrier which was deposited prior to the Cu gate. Three distinct colour regions can be seen in the image (a) a light blue portion, attributed to Mn on the SiO_2 substrate, (b) a pink colour region which is attributed to Cu on top of the Mn barrier region and (c) a brown region, attributed to Cu on the SiO_2 substrate with no barrier material underneath. Thus the barrier layer formed on the substrate, which could well prevent Cu diffusion, is rendered ineffective, as some of the Cu gate resides directly on the SiO_2 layer, thereby allowing this portion of the gate to diffuse into the dielectric. In addition, a thick Cu gate must be deposited in order to electrically contact the structure without the electrical probe penetrating through the gate material. These processing challenges were successfully solved and fabrication of MOS devices was undertaken within the UHV system in order to electrically characterise $MnSiO_3$ as a Cu diffusion barrier layer candidate.

3.5 Electrical testing of MOS devices

The main electrical test performed on MOS devices was capacitance-voltage sweeps, outlined in the previous chapter. This enables the detection of Cu ions which can diffuse into the dielectric layer under stressing of the devices [8-12]. MOS devices were stressed in two ways. The first stress is a pure thermal stress test where devices are subjected to a high temperature anneal in a tube furnace in either N_2 flow or atmosphere in order to deliberately drive the diffusion of Cu into the underlying dielectric material. MOS devices with a barrier layer were simultaneously stressed in order to test the effectiveness of the barrier layers formed. The second stress experiment performed was the bias temperature stress (BTS) measurement. This measurement involves applying a bias voltage to a device during thermal stress in order to generate (and bias) Cu ions into the underlying dielectric.

3.5.1 Probe station and characterisation equipment

Two probe stations were employed to study the fabricated MOS devices electrically. The first probe station used needle tip probes which could be put into contact with the MOS gates under observation through an optical microscope. The second probe station used allowed probing a sample under rough vacuum conditions in addition to heating the sample to temperatures of up to 150 ^{O}C whilst simultaneously applying a voltage to the gate contact of the device under test. Three separate electrical test meters were used to study the MOS characteristics. These included a Keithley 4200 electrometer which allowed the measurement of leakage currents through the MOS devices down to a level of $1x10^{-12}$ A. The second piece of electrical test equipment was a 1 MHz Boonton 72b CV meter which was electrically interfaced to the Keithley 4200 in order to facilitate data acquisition during capacitance voltage sweeps. This fixed 1 MHz CV meter enabled rapid CV profiles to be obtained. The third piece of electrical apparatus used was an Agilent

4240A LCR meter which had a variable frequency measurement capability for CV acquisition between 20 Hz to 10 MHz. This was interfaced to a PC for rapid data acquisition. The use of variable frequencies during CV analysis enables the detection of interface states within a MOS device.

3.5.2 Thermal stressing of MOS devices

A tube furnace (as seen in Figure 3.6) in a class 1000 clean room was employed to thermally stress MOS devices under different ambient conditions. High temperature annealing of MOS devices up to 500 ^{O}C could be carried out in either an N_2 flow or atmosphere environment. This allowed controlled oxidation of the MOS metal gates to take place which can act to promote Cu diffusion.

Figure 3.6: Tube furnace used to stress MOS devices.

3.5.3 Bias thermal stressing of MOS devices

BTS of MOS devices involves applying a positive voltage (~ 1 MV/cm) to the gate of the MOS structures whilst the device is at an elevated temperature (~ 150 ^{O}C). This experiment was performed in a custom build probe station as seen in Figure 3.7.

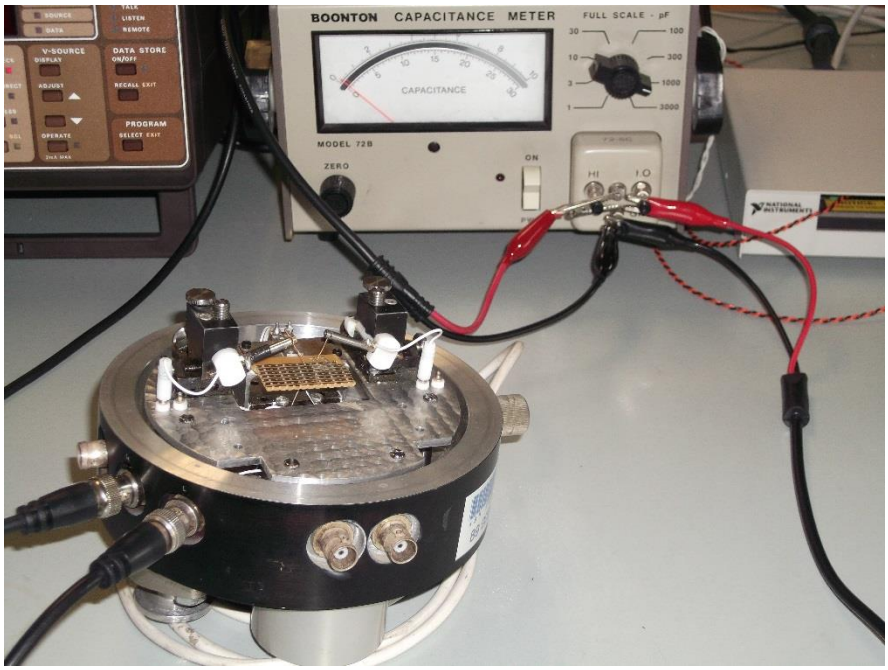

Figure 3.7: BTS probe station with Boonton 72b CV meter in background.

Devices were placed in the probe station where a CV trace was initially taken in addition to leakage current measurements through the structure. A voltage was then applied to the device whilst it was heated to a temperature of 150 ^{O}C for ~ 600 s. The applied voltage remained on the device as it cooled down. The leakage current through the device was simultaneously measured during the applied voltage in order to track any increase in leakage current during the stressing stage. Once the device had cooled to room temperature, further CV and IV data were taken and compared to the initial data taken before stressing.

3.6 References

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4 In situ parallel fabrication and interface characterisation of metal oxide semiconductor barrier layer test structures

4.1 Introduction

Downward scaling of devices, as applied through Moore's law has proved challenging in relation to materials, materials growth and device characterisation [1] . Copper (Cu) has replaced aluminium (Al) as the metal of choice for on chip interconnect lines for IC production due to the benefits of lower resistivity, reduced RC time delay, decreased power consumption and increased resistance to electromigration failure [2]. With the advantages to the change in Cu also came a number of disadvantages, most notably the diffusion of Cu into any surrounding silicon based inter layer dielectric (ILD) material which causes device degradation and ultimately device failure [3,4]. As shown in previous sections, the metal manganese (Mn) has emerged as a possible self-forming barrier candidate to replace the relatively bulky Ta/TaN barrier currently in use. Previous studies have shown that when Mn (or a CuMn alloy) is deposited on a SiO_2 dielectric and annealed, the over layer (or alloying element) chemically reacts with the dielectric in a self-limiting fashion (~ 3 nm) to form a new chemical species which has been identified as manganese silicate ($MnSiO_3$) [5-7]. In order for a barrier candidate material to be considered, it must fulfil certain criteria such as:

(a) Prevent Cu diffusion into the surrounding ILD.

(b) Promote adhesion between the Cu line and the ILD (as Cu is known to have poor adhesion to silicon oxide based ILDs).

(c) Be thin enough to allow Cu to fill most of the interconnect line, thereby decreasing resistance of the line.

The interface chemistry of barrier layer formation has been examined by the DCU SIRG in an ultra-high vacuum environment, thereby allowing the use of XPS analysis in addition to thin film metal deposition and annealing capabilities, without the need to break vacuum and expose samples to atmospheric contamination which could interfere with chemical species formed [6-8]. A common approach in the wider literature is to deposit the metals needed to form a barrier on a dielectric material, typically within a chemical vapour deposition chamber, or deposition of an alloy of Mn and Cu directly onto the substrate dielectric [5]. The sample is then exposed to atmosphere where ex-situ characterisation is used such as XPS, transmission electron microscopy (TEM) or secondary ion mass spectroscopy (SIMS) [8-10]. Additionally, electrical testing of barrier materials are commonly tested via the fabrication of metal oxide semiconductor (MOS) structures, which require the patterned deposition of metal gate areas on a dielectric material, typically with and without a barrier layer for comparative purposes [11,12]. The issue associated with fabrication of these devices is the lack of control and real time monitoring of the barrier formation process.

This chapter focusses on a novel technique developed in the surface science and interfaces group in DCU. Both fabrication of MOS structures and interface chemical analysis of the reactions that occur at the interface during MOS fabrication have been developed within a UHV environment with XPS, thin film Mn deposition, annealing and thick Cu capping depositions capabilities. This process allows the fabrication of MOS structures, both with and without a $MnSiO_3$ barrier in order to test the barrier effectiveness, which in previous

studies has only focused on interface chemistry studies. Sample fabrication within a UHV environment allows the fabrication of ultra-clean interfaces and ultra-low levels of oxygen ambient, thereby allowing the direct correlation of interface chemistry with electrical performance of fabricated devices. Ex-situ analysis techniques can also be used, and correlated back to the initial XPS results, thereby imparting confidence to any results obtained. Electrical data taken include capacitance voltage sweeps of the fabricated MOS devices throughout a series of ex-situ anneals designed to stress the devices in order to test any barrier layers formed. Transmission electron microscopy TEM and secondary ion mass spectroscopy SIMS are also employed to gain additional information in order to correlate all data back to initial XPS analysis during barrier layer formation.

4.2 Experimental details

High quality silicon dioxide films were thermally grown to a thickness of 100 nm on n-type Silicon <100> wafers in the Tyndall National Institute, Cork. Individual samples were then cleaved from these wafers with dimensions 2 cm x 1 cm. To facilitate the fabrication of MOS devices in parallel to XPS analysis, a 1 cm x 1 cm laser diced Si shadow mask with both circular and square gate areas of 500 μm x 500 μm, 750 μm x 750 μm and 1 mm x 1mm was used to cover half of the sample as shown in Figure 4.2 .

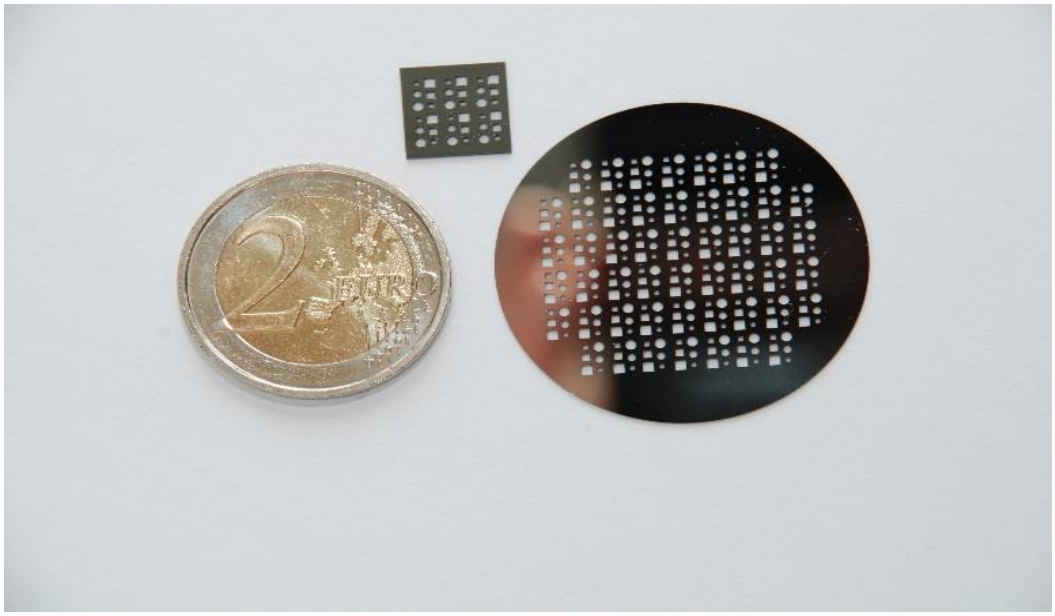

Figure 4.1: Si shadow masks used to define MOS gate areas during metal depositions.

This enabled parallel interface chemistry studies by XPS on the uncovered section of the sample. These samples were loaded into a UHV chamber (base pressure of $5x10^{-10}$ mbar) and degassed to a temperature of 500 ^{O}C prior to any metal depositions in order to create a contaminant free SiO_2 surface. Metallic Mn was deposited in-situ in a highly controlled fashion using an Oxford Applied Research EGC04 mini electron beam evaporator at a pressure of $5x10^{-9}$ mbar using HCl etched Mn chips with a purity of ~ 99.9%. XPS analysis of the chemical interactions between the deposited Mn and the dielectric surface was undertaken as a function of thermal annealing cycles leading to $MnSiO_3$ formation. The photoelectrons were excited using a conventional Al Kα ($h\upsilon$ = 1486 eV) X-ray source in conjunction with the electron energy analyser operating at a pass energy of 20 eV, yielding an overall resolution of 1.2 eV. High temperature annealing studies were carried out at a pressure better than $5x10^{-9}$ mbar with the sample held at its target temperature for 60 minutes. The XPS core level spectra were peak fitted using Voight profiles composed of Gaussian and Lorentzian line shapes in a 3:1 ratio whilst using a Shirely-Sherwood type background.

Once these studies were complete, a thick Cu capping over layer was deposited on the whole sample from a tungsten filament evaporator at a pressure better than $1x10^{-8}$ mbar with a Cu source metal of 99.99% purity prior to removal from the UHV system as seen in Figure 4.2.

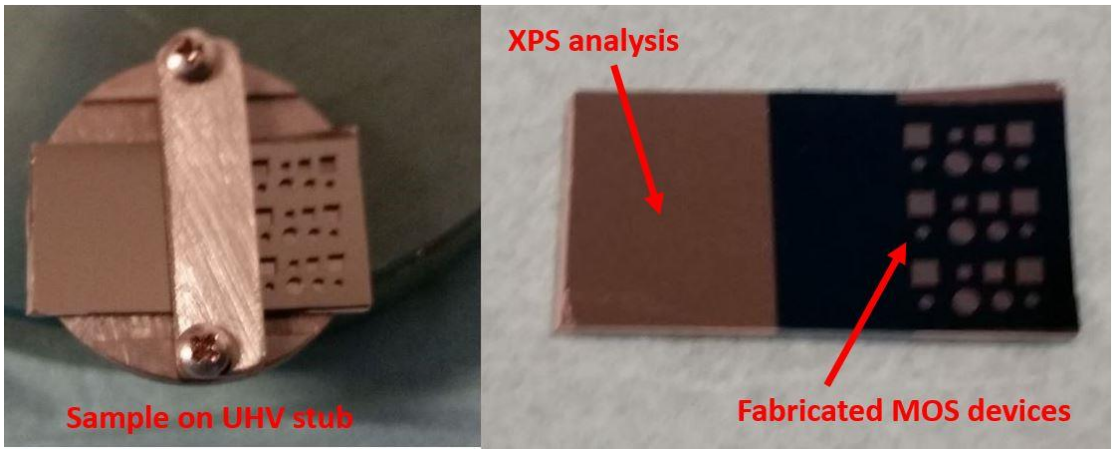

Figure 4.2: Samples fabricated using Si shadow masks.

Capacitance voltage sweeps of the fabricated MOS structures were carried out using a Boonton model 72 b 1 MHz CV meter interfaced to a Keithley 4200 electrometer. Voltage sweeps ranged from + 10 V to – 10 V with a step of 0.1 V and hysteresis was tracked by applying a reverse -10 V to + 10 V CV sweep immediately following the initial CV sweep. A hold time of 300 s at + 10 V (applied to the fabricated Cu gate contact) was used prior to all CV sweeps in order to bias any mobile ions within the dielectric layer towards the Si/SiO_2 interface to maximise any flatband voltage shifts within the CV profile. Both N_2 flow and atmosphere anneals of the MOS structures were carried out in a tube furnace in a class 1000 clean room. Samples were held at the desired temperature for 60 minutes during anneal stages. Ten devices across each sample set were tested, however for clarity the results for only one device from each set is presented as there was very good reproducibility across the sample.

4.3 Pure Cu & $MnSiO_3$ barrier MOS fabrication

Figure 4.3 displays the XPS survey spectra during the course of fabrication of the $MnSiO_3$ barrier layer MOS devices. As can be seen following degas procedure, the only elements present in the top surface of the SiO_2 dielectric are silicon and oxygen, reflecting the clean surface obtainable in the UHV environment. Following degassing, a thin ~ 1.2 nm metallic Mn film was deposited onto the sample surface, after which an anneal was performed at 500 ^{O}C for one hour, in order to drive a $MnSiO_3$ reaction between the ultra-thin Mn layer and underlying dielectric layer. As can be seen during the course of barrier formation, no excess carbon, oxygen or other contaminants were detected, reflecting the high levels of control over the course of barrier layer formation. Finally a thick Cu capping layer was deposited onto the sample surface, protecting the interface prior to removal from the UHV environment and creating Cu gate electrical contacts for the MOS devices.

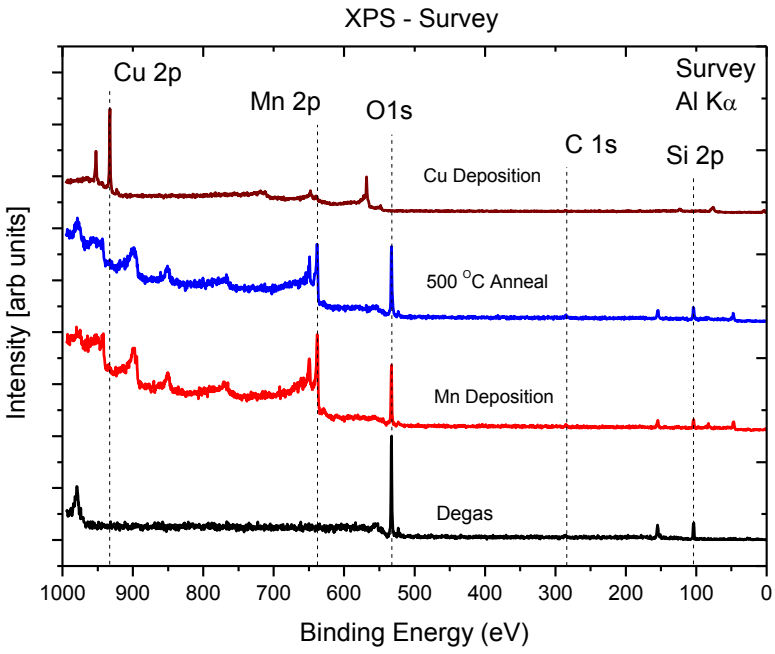

Figure 4.3: XPS survey spectra displaying over the course of in-situ MOS $MnSiO_3$ barrier MOS devices.

As can be seen in the survey spectrum of the thick Cu film deposited, the only element present is Cu, indicating the purity of the deposited film.

Figure 4.4 displays Si 2p core level spectra during the formation of $MnSiO_3$ on the dielectric surface.

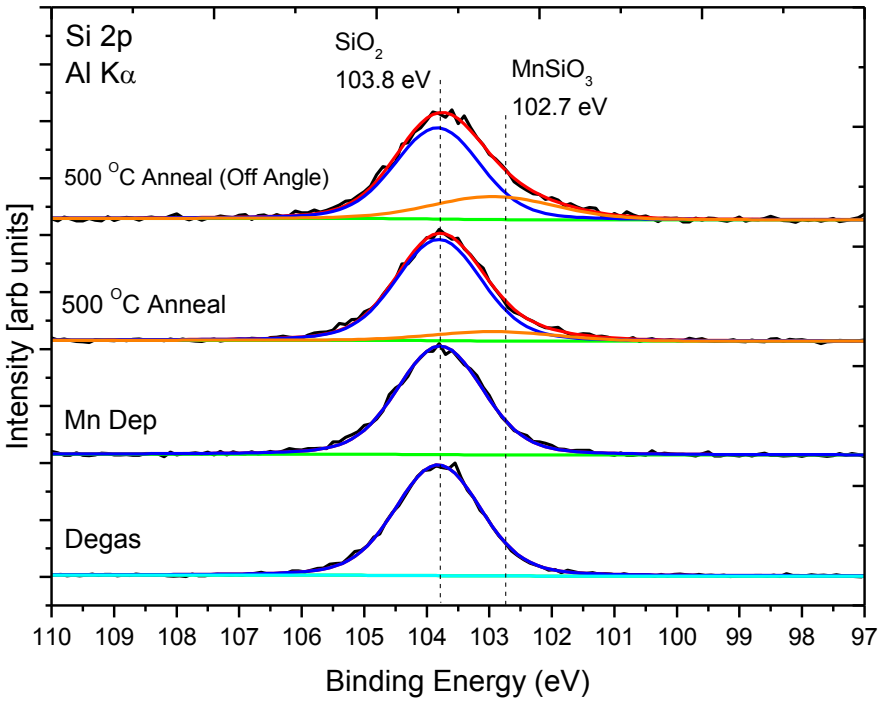

Figure 4.4: XPS Si 2p spectra during the experimental procedure of $MnSiO_3$ formation.

As can be seen following Mn deposition and annealing procedures, a lower binding energy (LBE) peak emerges at a position of 102.7 eV relative to the SiO_2 substrate peak at 103.8 eV. Off angle XPS (60 ^{O} from normal emission) indicates that the new species formed is surface localised relative to the substrate SiO_2.

Figure 4.5 displays O 1s core level spectra during the course of MOS device fabrication.

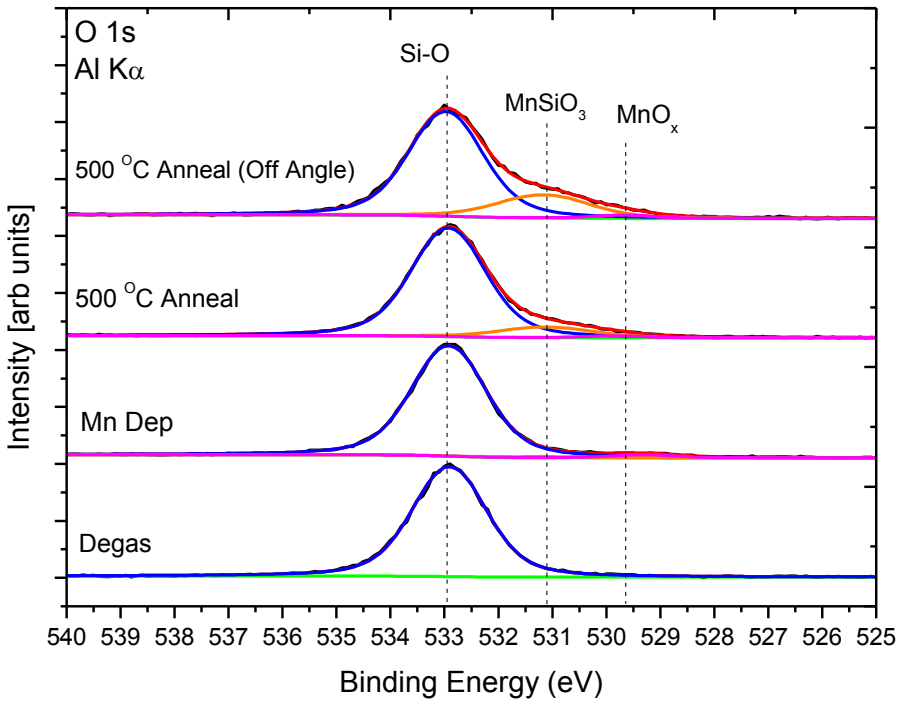

Figure 4.5: XPS O 1s spectra during the formation of $MnSiO_3$.

Similar to the Si 2p spectra, a LBE peak emerges at a position of 531.2 eV relative to the SiO_2 substrate position of 533 eV. The off angle XPS (60 ^{O} from normal emission) spectrum again indicates that the new species formed is surface localised relative to the substrate SiO_2. An important point to note is the lack of Mn oxide formed during barrier layer formation, again reflecting the high levels of control available within the UHV environment. Figure 4.6 displays the Mn 2p core level spectra following Mn deposition and annealing stages. A shift to higher binding energy is noted overall following annealing in addition to an oxidised component at ~ 642 eV. Off angle XPS indicates no

change in the Mn 2p spectra, indicating that the ultra-thin layer is homogenous in its chemical composition.

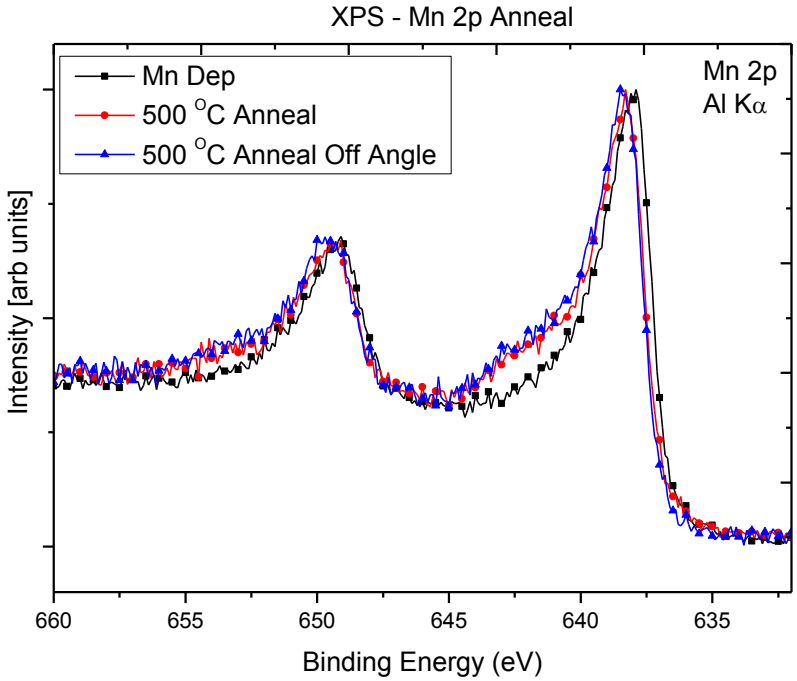

Figure 4.6: XPS Mn 2p spectra during the formation of $MnSiO_3$.

The growth of peaks at LBE energies of 102.7 eV for the Si 2p and 531.2 eV for O 1s spectra in addition to shifting to HBE and growth of an oxidised Mn feature at ~643 eV in the Mn 2p spectra following Mn deposition and annealing on SiO_2 is consistent with the formation of a self-forming barrier layer composed of $MnSiO_3$, in agreement with previous studies [13,14].

4.4 Adhesion promotion of $MnSiO_3$ barrier

Following in-situ Cu capping of MOS devices, samples were removed from the UHV environment in order to electrically test the fabricated structures. MOS devices were probed on an electrical probe station using needle tip probes under an optical microscope.

Probing of the pure Cu reference structures during electrical testing show scratch marks due to the needle tip probes contacting the Cu gate metal residing on the SiO_2 substrate, as seen in Figure 4.7 (a). This result indicates that Cu has poor adhesion to the dielectric material due to the ease at which the gate material could be removed during testing. In contrast, the MOS devices with a $MnSiO_3$ barrier (shown in Figure 4.7 (b)) show no indication of scratching during electrical probing with the needle tip probes.

Due to the fact that the two samples were fabricated separately, a processing error could account for the drastic difference in adhesion, thus it was decided to fabricate a third sample where the $MnSiO_3$ barrier would only partially cover the defined area of the MOS gates. This sample was fabricated by tilting the sample off-normal to the e-beam during Mn deposition, thereby inducing shadowing of the Mn onto the sample surface. Once the $MnSiO_3$ barrier was formed, the thick Cu layer was deposited as normal. Thus a dual barrier / non-barrier sample was created which allowed the direct comparison of the $MnSiO_3$ barrier layer relative to no barrier layer. Figure 4.7 (c) displays the optical microscopy images of the dual barrier / non-barrier sample. The needle tip probe was used to contact across the whole gate area of the MOS structures in order to test adhesion, whereupon it was found that the area with a $MnSiO_3$ barrier was not scratched during testing, in contrast to the area with no barrier layer which was easily scratched during testing.

In order to fully test the adhesion of both samples, tape test experiments were perfomed on both samples. This test involved placing a layer of scotch tape of the MOS structures of each sample set and removing the tape. As can be seen following the tape test for the non-barrier sample in Figure 4.7 (d), removal of the Cu gate is noted, indicating poor

adhesion to the SiO_2 substrate. This results is in contrast to the $MnSiO_3$ barrier sample which passed the tape test as seen in Figure 4.7 (e) due to the fact that the gate material was not removed even following multiple tape tests.

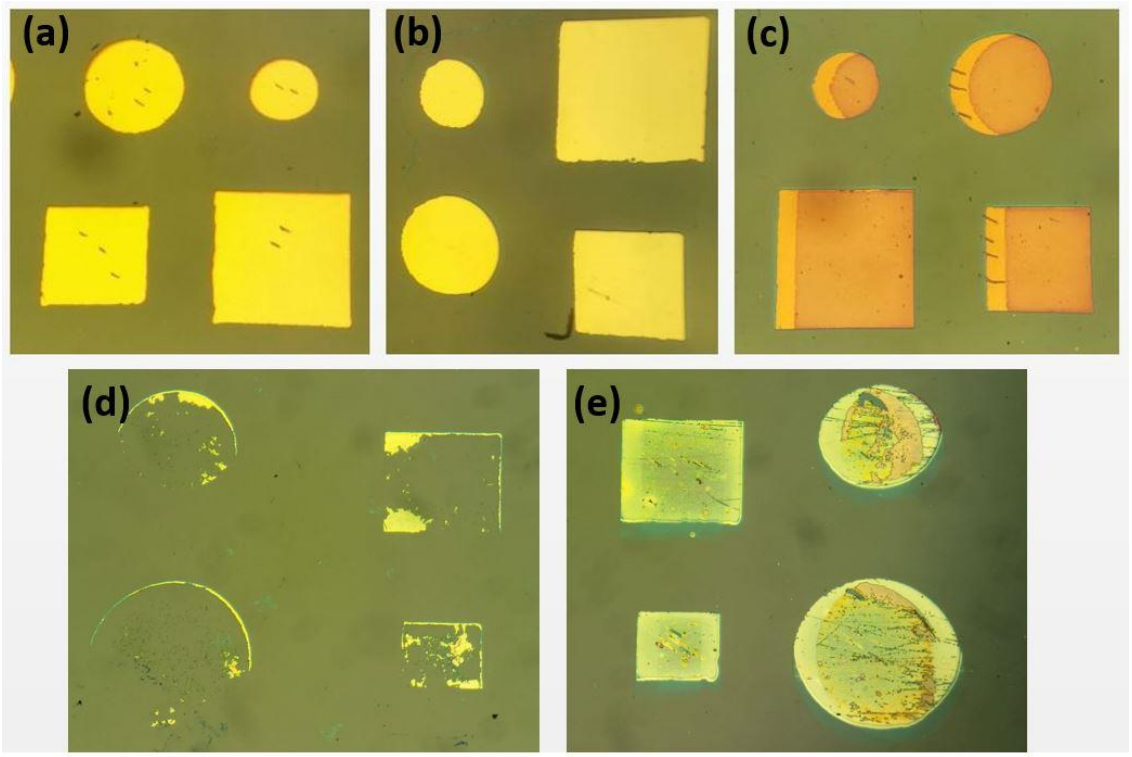

Figure 4.7: Optical microscopy images of fabricated MOS gate contacts for (a) pure Cu reference (b) $MnSiO_3$ barrier (c) dual barrier / non-barrier structures, (d) pure Cu reference following tape test and (e) $MnSiO_3$ barrier sample following tape testing.

4.5 Electrical characterisation

In order to test the barrier effectiveness of the $MnSiO_3$ layer at preventing Cu diffusion into the dielectric, MOS structures with and without a barrier layer were tested via capacitance voltage measurements during each sample anneal stage. Samples were initially annealed in an N_2 flow tube furnace at 400 ^{O}C in order to remove trapped charge in the dielectric material, most likely as a result of the thermal growth of the high quality

oxide layer. Once the samples displayed ideal behaviour in terms of MOS activity, a second anneal was performed at 300 ^{O}C for 30 minutes in atmosphere in order to stress both samples thermally. Willis et al [15] has suggested that the origin of Cu^{+} ions in SiO_2 following Cu MOS stressing is due to oxidation of the Cu gate metal, thereby producing Cu^{+} ions which penetrate into the dielectric layer. Thus annealing of the samples in atmosphere should produce Cu^{+} ions which allow testing of the $MnSiO_3$ barrier layer sample relative to the pure Cu reference sample.

In order to test the impact of the $MnSiO_3$ barrier layer on the overall resistance of the Cu gate, four point probe testing was performed on both samples in order to gain additional information as to the impact of the barrier layer on the pure Cu over layer.

4.5.1 Capacitance voltage

Figure 4.8 displays CV data for the pure Cu reference MOS for as deposited, 400 ^{O}C N_2 tube furnace anneal and following a 300 ^{O}C atmosphere anneal. As can be seen from the as deposited CV sweep, clear accumulation, depletion and inversion regions in the CV sweep are observed, indicating good stability of the MOS device. Non-ideal behaviour however is noted due to the position of the flatband voltage being at negative voltage values, which can be attributed to a positive charge build up in the dielectric layer, which most likely occurs during the thermal growth of the oxide layer. Following a 400 ^{O}C N_2 flow anneal, the device remains stable with the additional improvement of the flatband voltage position shifting to a value close to 0 V, indicating that the MOS device is now acting as an ideal MOS structure. Thus due to the ideal nature of the device following N_2 flow anneal, it can be concluded that this is the initial starting point to stress the device in order to test for Cu diffusion. In order to thermally stress the device, an anneal was performed at 300 ^{O}C in atmosphere. As seen in Figure 4.8, post atmosphere anneal, a shift

of flatband voltage is noted to negative voltages, indicating a build-up of positive charge in the oxide layer. Hysteresis is also noted, consistent with movement of mobile charges within the dielectric material. This result is consistent with previous reports of Cu^{+} ion diffusion into the dielectric material, causing device failure [3,16-18] and displays the instability of Cu on SiO_2, thus showing the need for a barrier layer between the ILD and Cu conducting line.

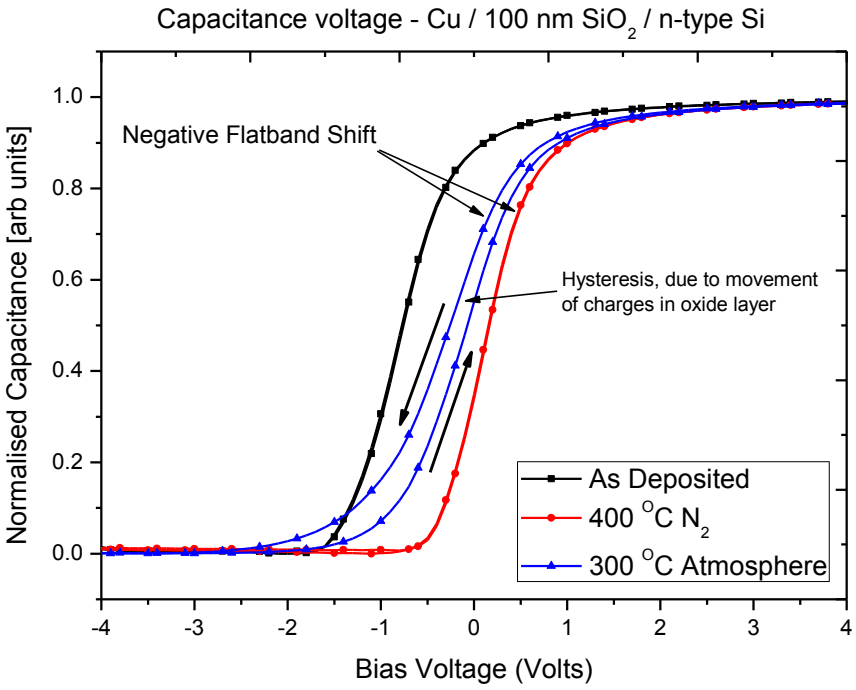

Figure 4.8: Capacitance voltage sweeps of pure Cu MOS during the experimental steps.

Figure 4.9 displays CV data for the $MnSiO_3$ barrier layer MOS devices during the course of experimental procedure. As can be seen from the as deposited CV sweep, a build-up of positive charge is evident in the oxide layer, similar to the pure Cu reference MOS devices. Following N_2 flow anneal, the voltage flatband of the device shifts to ~ 0 V, consistent with ideal MOS behaviour. The $MnSiO_3$ MOS devices were subjected to the same 300 ^{O}C atmosphere anneal at the same time as the Cu reference MOS. It is clear

from the CV profile shown in Figure 4.9, following atmosphere anneal, that the barrier has prevented failure of the device.

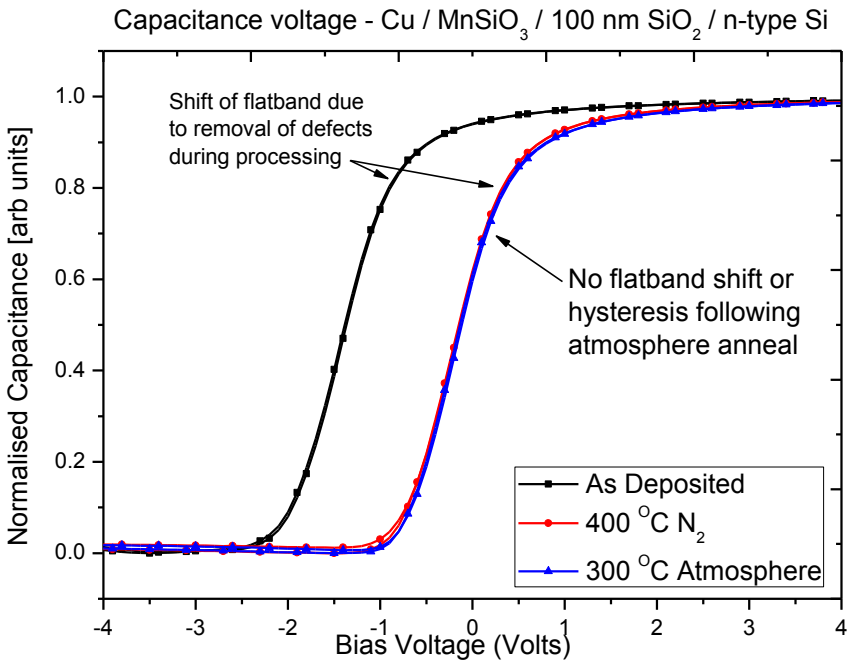

Figure 4.9: Capacitance voltage sweeps of MnSiO3 barrier MOS during experimental procedure.

4.5.2 Four point probe

Previous reports of Mn in Cu metal systems have shown that excess metallic Mn can diffuse through the Cu film, to the top surface of the film [19]. This Mn then oxidises via ambient exposure, passivating the layer and preventing Cu oxide formation [19]. This upward diffusion of Mn could negatively impact the conductivity of the Cu film, thus in order to ascertain if the $MnSiO_3$ barrier has negatively impacted the conductivity of the overlying Cu layer, four point probe measurements were performed and compared to that of the pure Cu reference sample.

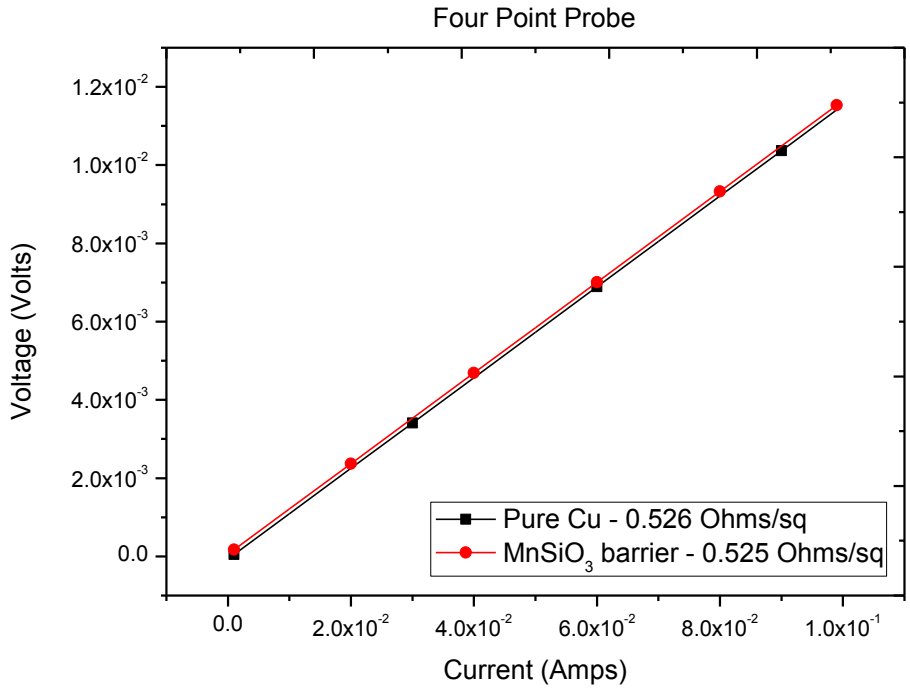

Figure 4.10: Four point probe measurements of both pure Cu and $MnSiO_3$ samples.

As can be seen from Figure 4.10, both samples appear to have the same sheet resistance values. This is an important result when viewed in conjunction with the adhesion results and CV data displayed previously. Thus it is shown that the ultra-thin $MnSiO_3$ barrier has not negatively impacted upon the resistance of the over layer Cu film.

4.6 XPS analysis post atmosphere anneal

As stated above, previous reports indicate that excess metallic Mn could diffuse to the surface of the Cu film, passivating the film, preventing Cu oxidation. This could explain the stability of the $MnSiO_3$ sample, not due to the barrier layer formed at the interface but due to passivation of the surface layer, preventing Cu oxide formation and thus Cu^+ ions which could migrate into the dielectric layer as seen in the pure Cu reference sample. Thus in order to test for the surface passivation of the $MnSiO_3$ sample via surface

localised Mn, post atmosphere anneal XPS was performed on both pure Cu reference and $MnSiO_3$ barrier samples.

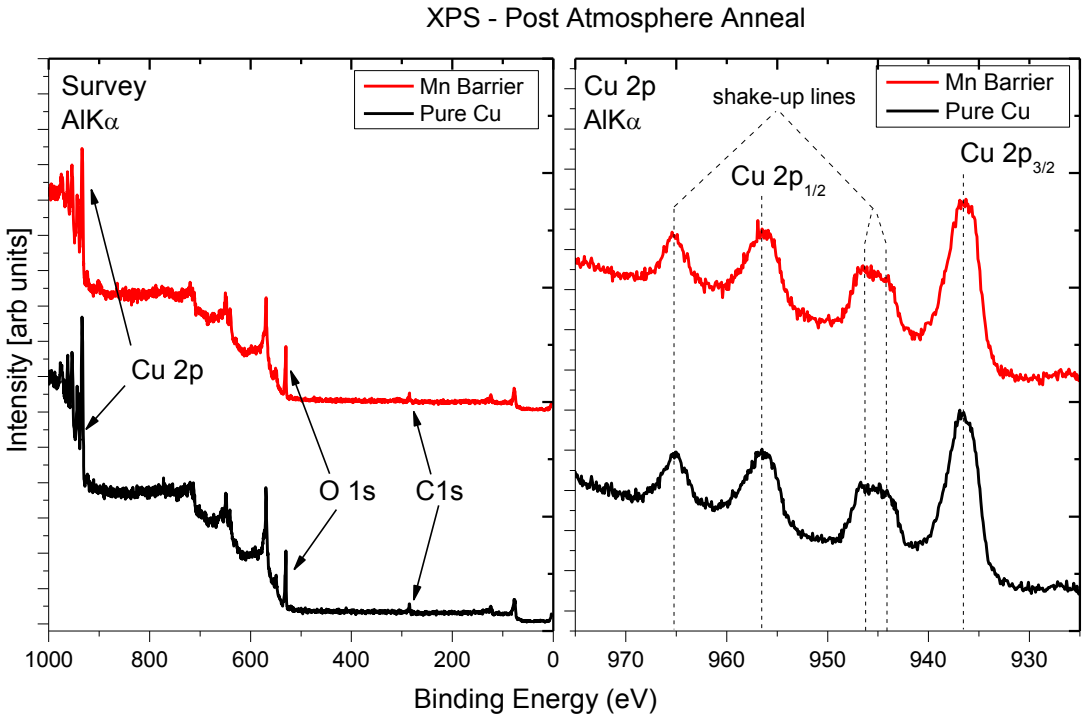

Figure 4.11: XPS of both pure Cu reference and $MnSiO_3$ barrier samples post atmosphere anneal.

Figure 4.11 displays XPS survey spectra in addition to narrow window Cu 2p spectra for both pure Cu reference and $MnSiO_3$ barrier sample post atmosphere anneal. As can be seen from the pure Cu reference sample, the Cu in the top surface of the sample has oxidised, evident from the presence of the O 1s photoemission peak in the survey spectra. Narrow window Cu 2p spectra also show the evidence for Cu oxide due to broadening of the photoemission lines relative to the as deposited metallic Cu, seen in initial XPS data during device fabrication. The presence of strong shake-up features in the Cu 2p spectra indicate that the chemical species at the surface is CuO [20]. As seen in the survey spectra

of the $MnSiO_3$ barrier sample, no Mn is present, with the spectrum mirroring the pure Cu reference sample. Narrow window Cu 2p scans of the $MnSiO_3$ sample indicate that the Cu in the surface of the sample is in the same chemical state as that in the pure Cu reference sample, CuO. This result combined with previously shown four point probe data strongly suggest that the stability of the $MnSiO_3$ sample is due solely to the ultra-thin $MnSiO_3$ layer formed during sample fabrication.

4.7 Transmission electron microscopy

Transmission electron microscopy (TEM) was carried out in the Tyndall National Institute to image both the pure Cu reference (non-barrier) and $MnSiO_3$ barrier sample, post atmosphere anneal stress, and the images are displayed in Figure 4.12 (a) and (b) for the pure Cu reference and $MnSiO_3$ samples respectively.

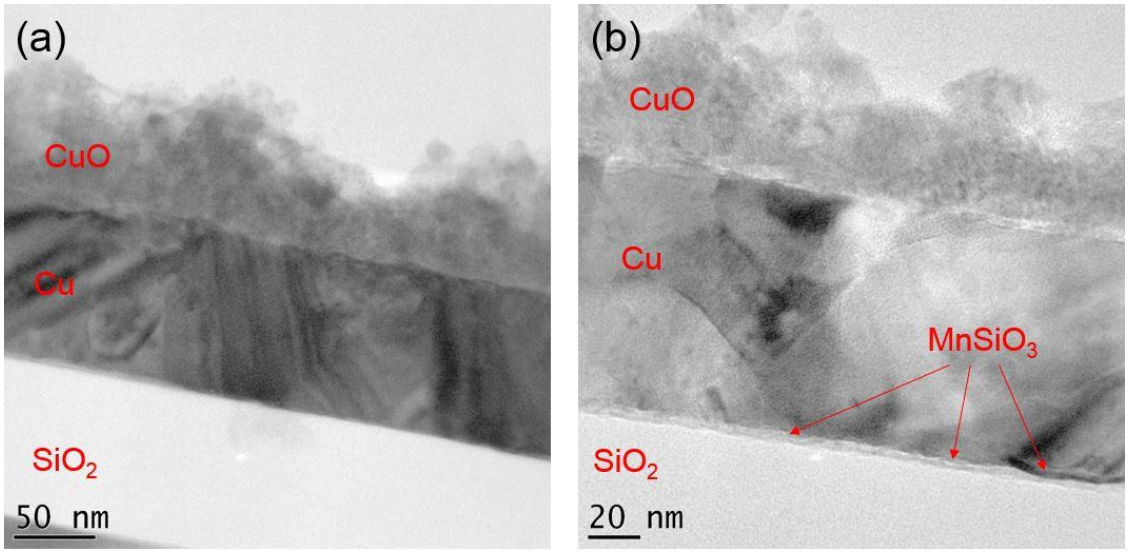

Figure 4.12: TEM images of (a) pure Cu reference (non-barrier) and (b) $MnSiO_3$ sample.

As can be seen from the pure Cu reference (a), the SiO_2 dielectric and Cu metal layer are clearly seen in the TEM image, in addition to a Cu oxide layer on the surface of the

sample. When the $MnSiO_3$ barrier layer sample (b) is examined, so too can the SiO_2, Cu metal and Cu oxide layers clearly be seen, with a distinct addition of a layer of average thickness 3.6 nm between the Cu and SiO_2 layers. This layer is attributed to the $MnSiO_3$ layer formed during fabrication of the barrier sample, consistent with previous TEM reports of barrier layers [7,21,22]. The $MnSiO_3$ layer is therefore effective in keeping the Cu and the SiO_2 physically separated, maintaining an abrupt interface. When the Cu / SiO_2 interface of the pure Cu reference sample is examined further, at higher magnification, as seen in Figure 4.13 (a) and (b), a less well defined transition region is observed.

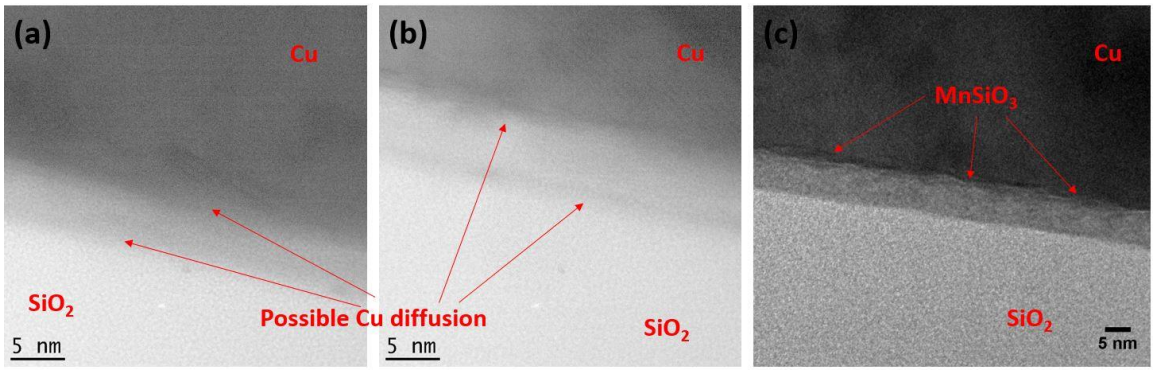

Figure 4.13: high magnification TEM imaging of the Cu / SiO_2 interface for the pure Cu reference sample and (c) $MnSiO_3$ interfacial layer on $MnSiO_3$ barrier sample.

This graded interface is consistent with the diffusion of Cu into the SiO_2 layer following thermal stressing. Definitive evidence of diffusion would require high resolution EELS analysis of the interface chemical profile which was not available in this TEM instrument.

4.8 Secondary ion mass spectroscopy

Secondary ion mass spectroscopy was used to depth profile both the $MnSiO_3$ barrier and non-barrier samples following thermal stress treatments on a SIMS instrument in the National Physics Laboratory in the UK which yielded both elemental depth profiling and 3D imaging of the sample interfaces. The SIMS depth profile for the non-barrier (Cu / SiO_2 / Si) sample is displayed in Figure 4.14. As can be seen from the spectrum, there is a considerable concentration of Cu oxide at the surface of the sample, in agreement with post thermal stress XPS results. The intensity of the Cu oxide signal decreases towards the Cu / SiO_2 interface as metallic Cu signal increases in intensity. The Cu signal is detected well into the 100 nm SiO_2 dielectric layer which is consistent with Cu diffusion. This result is in agreement with CV analysis reported above and with previous reports of Cu diffusion studies by SIMS depth profiling [15,3,23].

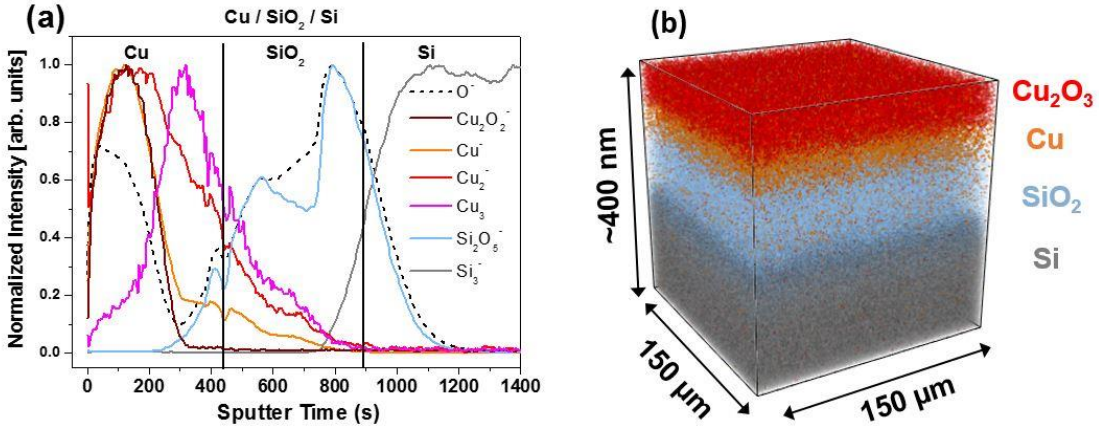

Figure 4.14: (a) SIMS depth profiling of non-barrier reference sample and (b) 3D imaging of SIMS depth profiling.

SIMS depth profiling of the Cu / $MnSiO_3$ / SiO_2 / Si barrier sample is presented in Figure 4.15. In agreement with the non-barrier sample and post thermal stress XPS analysis, a surface layer of Cu oxide is present, due to oxidation of the Cu gate following tube furnace

annealing. This Cu oxide signal decreases with a concurrent increase in the metallic Cu signal as the Cu / SiO_2 interface is approached. Further depth profiling into the film shows a rapid decrease in Cu counts and a corresponding increase in a $MnSiO_3$ signal at the metal / SiO_2 interface. Further depth profiling shows that no Cu is found within the SiO_2 layer. This sharp decrease in Cu signal at the interface with no evidence of Cu diffusion into the oxide layer, is in agreement with electrical data which showed that the $MnSiO_3$ barrier sample was stable and prevented the diffusion of Cu into the underlying dielectric material, in contrast to the failure of the pure Cu non-barrier reference sample.

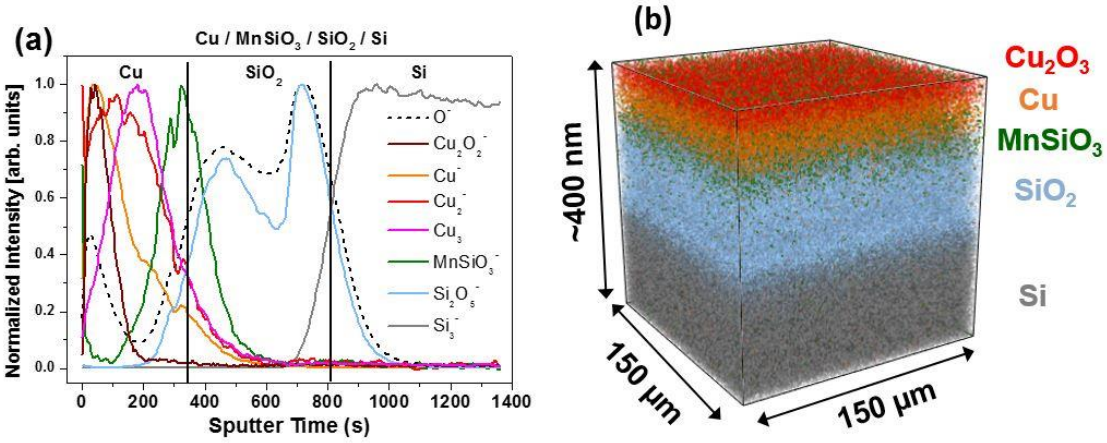

Figure 4.15: (a) SIMS depth profiling of $MnSiO_3$ barrier sample and (b) 3D imaging of SIMS depth profiling.

4.9 Conclusions

A novel approach to in-situ fabrication and interfacial characterisation of $MnSiO_3$ Cu diffusion barrier MOS devices has successfully been developed. Cu / SiO_2 / Si MOS structures both with and without an ultra-thin $MnSiO_3$ barrier layer at the metal / oxide interface were fabricated within a UHV system with XPS used to track the interfacial chemistry during fabrication. This enabled the fabrication of ultra-clean interfaces with precise control over the barrier formation process. The requirements of future barrier layers outlined at the start of this chapter were:

a) Prevent Cu diffusion into the surrounding ILD
b) Promote adhesion between the Cu line and the ILD (as Cu is known to have poor adhesion to silicon oxide based ILDs)
c) Be thin enough to allow Cu to fill most of the interconnect line, thereby decreasing resistance of the line

These requirements have been shown to be satisfied with the formation of an ultra-thin $MnSiO_3$ barrier layer at the metal / oxide interface, characterised with in-situ XPS analysis. Adhesion promotion was shown to occur on barrier samples which were resistant to scratching during electrical testing, in contrast to non-barrier samples which displayed poor adhesion. Capacitance voltage sweeps of pure Cu (non-barrier) samples show the need for a barrier at the metal / oxide interface due to diffusion of Cu^+ ions into the oxide layer following thermal stress treatments. $MnSiO_3$ barrier MOS devices were shown to be stable following identical thermal stress treatments, highlighting the barrier effectiveness at preventing Cu diffusion into the dielectric. Four point probe data in conjunction with post atmosphere annealing XPS analysis of both barrier and non-barrier

samples indicate that the $MnSiO_3$ has not interacted with the over layer of Cu, as no increase in the sheet resistance of the corresponding Cu layers was detected. SIMS depth profiling showed evidence of the diffusion of Cu within the dielectric layer of the non-barrier sample in contrast to the sharp decrease in Cu counts at the metal / SiO_2 interface of the barrier sample. Thus it has been shown that the excellent stability of the $MnSiO_3$ barrier sample, relative to the instability of the non-barrier reference sample, was solely due to the ultra-thin $MnSiO_3$ barrier, formed and characterised in-situ with XPS analysis.

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5 Manganese silicate barrier formation on different porosity carbon doped oxide dielectrics

5.1 Introduction

The metal manganese (Mn) has emerged as a possible candidate for future use as a self-forming barrier material on inter-layer dielectrics (ILD) used in interconnect fabrication [1-3]. Previous photoemission studies investigating Mn interactions with SiO_2 dielectric layers show that upon anneal treatments Mn chemically interacts with the dielectric layer in a self-limiting fashion, forming an ultra-thin (~ 3 nm) barrier composed of manganese silicate ($MnSiO_3$) [4,5]. Further in-depth XPS and TEM studies using SiO_2 dielectric layers show that partially oxidised manganese (MnO_x) can be used to form more silicate upon anneal treatments, relative to metallic Mn [1].

As Moore's law continues to push device geometries towards smaller and smaller dimensions, new dielectric materials are needed to overcome the parasitic capacitance between interconnect lines [2]. Carbon doped oxides (CDO) have emerged as candidates to replace SiO_2 as ILD materials for future integration [3,4]. The advantage of replacing Si-O with Si-C bonds is to reduce the electrical polarisability of the material, lowering the k value and thus lowering the overall resistance-capacitance (RC) time delay of the interconnect lines. In contrast to the advantages of lower RC time delay, disadvantages of using CDO materials include the possible chemical interaction of the carbon in the dielectric layer with the deposited Mn during barrier formation resulting in the formation of metal-carbide species as reported in previous studies, [5]. In addition to unwanted chemical reactions during barrier formation, CDO materials have been shown to have a

lower Young's Modulus than SiO_2, making these dielectrics susceptible to damage during processing of interconnect structures [6]. Further reduction in k value of CDO materials can be achieved via the incorporation of pores within the dielectric layer [7]. Porosity is generally achieved by introducing a labile species into the dielectric layer during deposition. Following anneal treatment, the labile species decomposes from the dielectric layer leaving nanometre sized pores in the film. Due to the relatively low k value of a void (~ 1), the pores within the material impact the overall k value by reducing it, tending overall to a k value of 1 (total void, no material present) as the porosity of the film increases. This increase in porosity however has unwanted effects such as increased surface roughness, lower Young's Modulus and high levels of diffusion of materials into the dielectric layer due to the facile diffusion paths caused by the pores [13-15]. Formation of barrier layers on these ultra-low k, high porosity dielectrics is of considerable interest for future iterations of IC fabrication, however, they pose significant fabrication challenges [8,9].

This chapter focuses on the chemical and structural investigation of manganese silicate barrier formation on prototype high carbon content dielectric materials, fabricated using the same chemical back bone but with different porosities. XPS and XAS studies were used to investigate the interface chemistry and chemical compound formation, respectively, while TEM measurements in conjunction with EELS profiles provided additional chemical and structural information on the barrier formation region. In order to make as direct a comparison as possible between the different dielectric materials, XPS studies of interface formation between the deposited Mn and the dielectric surfaces were carried out simultaneously on the highly porous (50% added porosity) and the low porous (0% added porosity) substrates. In order to eliminate the possible effects of sample

charging during the XPS measurements, an absolute binding energy referencing method of depositing elemental silicon on the dielectrics was used. Studies involving the deposition of both metallic manganese and partially oxidised manganese on the different porosity CDO substrates were undertaken. These latter experimental with manganese oxide also allowed investigation of the use of the oxygen 1s signal as a referencing method for the identification of manganese silicate on the CDO substrates.

5.2 Experimental details

CDO dielectric materials were obtained from an external vendor, which supplied both a 50% porous high carbon content CDO layer and reference 0% porous layer which contained the same chemical backbone. In order to use the 0% porous sample as a direct reference to the 50% porous sample, both 50% and 0% porous samples were loaded onto a single sample stub within a UHV system for XPS analysis. Both samples could then be exposed to identical metal depositions and anneal stages whilst also giving the capability of isolating the samples spatially during XPS analysis.

Hydrochloric acid etched Mn chips (~99.9% purity) were used as a source material for the deposition of Mn in the UHV system using an Oxford Applied Research EGC04 mini electron-beam evaporator. Si was deposited via the same Oxford Applied Research EGC04 mini electron beam evaporator using a Si source material of 99.99% purity. Oxidised Mn was deposited in a similar fashion to metallic Mn with the evaporation taking place in a $5x10^{-8}$ mbar partial pressure of oxygen. X-ray absorption measurements were carried out in the National Synchrotron Light Source (NSLS) in Brookhaven. Transmission electron microscopy (TEM) measurements were performed in the Advanced Microscopy Laboratory (AML) Crann, in Trinity College Dublin, by preparing

a sub 100 nm lamella structure from the initial CDO samples and analysed in a FEI Titan TEM system.

5.3 XPS binding energy referencing of 50% and 0% porous CDO

Previous XPS studies of CDO dielectric layers show that the binding energy positions of the CDO core level photoemission peaks shift with increasing carbon content in the dielectric material [10]. For example, as the carbon content is increased relative to pure SiO_2, the oxidised Si 2p peak position shifts towards lower binding energy positions. This shift in peak position, which is a consequence of the decreased polarity of the Si-C bond compared to the Si-O bond, is problematic for the unambiguous identification of Mn silicate growth.

In addition to shifting of peaks due to carbon incorporation within the dielectric material, the photoemission peaks may also shift due to differential charging during XPS analysis. As the photoemission process inherently results in electrons being emitted from the sample surface, the sample is left in a positive charge state. Due to the difference in porosity of both the 0% and 50% CDO materials, differential charging may be observed which could obscure the binding energy referenceing. Thus accurate binding energy positions of photoemission peaks must be taken in order to confidently identify the growth, if any, of Mn silicate upon these industrially relevant CDO substrates.

5.3.1 Deposited Si as an XPS binding energy referencing for porous CDO dielectrics.

|In XPS studies, the main photoemission peak used to identify Mn silicate growth is the Si 2p spectrum [11,12]. As seen in previous studies of Mn on pure SiO_2 substrates, a lower binding energy peak emerges relative to the oxidised Si 2p substrate peak following

Mn deposition and annealing [13,1]. This peak at a binding energy of 102.7 eV is attributed to the chemical bonding of Si in $MnSiO_3$. Due to the overlapping nature of some CDO Si 2p peaks with this Mn silicate peak position, it is essential that accurate peak positions are acquired for the identification of Mn silicate. The Si 2p peak for pure Si is well established and accepted to be at a binding energy of 99.3 eV. Therefore, by depositing a thin layer of silicon in situ on a CDO surface, an absolute binding energy reference can be obtained for the Si 2p peak position of the CDO material relative to pure Si.

A 0% and a 50% porous CDO samples were loaded into a UHV system with in situ Si deposition and XPS capabilities. Following degassing and XPS analysis of the as loaded samples, ~2-3 nm of Si was deposited onto both sample surfaces. As can be seen from the resulting photoemission spectra in Figure 5.1 , when deposited Si is used as a BE reference, the position of the Si 2p peak in the CDO 50% sample is found to be at a position of 102.5 eV while for the 0% porous sample, the referenced BE position is at 101.7 eV.

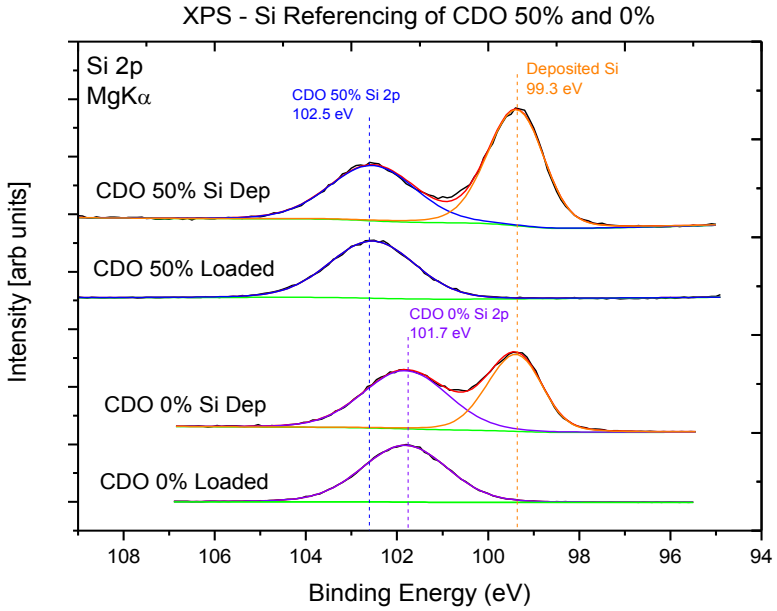

Figure 5.1: XPS binding energy referencing of Si 2p CDO 0% and 50% porous dielectrics.

Given that both CDO materials have the same chemical composition, with only difference being the porosity, it is not obvious from a chemical shift perspective why there is such a considerable difference in BE position. A possible explanation for the difference in B.E. may relate to the chemical impact of introducing porosity into the CDO film. The 0% CDO layer contains no porosity and thus there exists a high degree of crosslinking of the polymer network within the film, resulting in very low amounts of termination groups within the film. In comparison, the 50% film, contains a high degree of porosity, and such is expected to have a lower crosslinking of the polymer network, due to the presence of the pores throughout the film. If the 50% sample has lower crosslinking of the backbone film, then it must have a higher amount of termination at the end of each polymer chain where the network has been "interrupted" by the presence of pores. If these termination groups are more electronegative than the crosslinking chains, then they will cause any silicon within the layer to appear at higher binding energy relative to silicon in a non-porous sample where comparatively a reduced number of silicon atoms exist in a network terminated fashion.

Figure 5.2 displays Si 2p BE referencing data for both 0% and 50% CDO materials in comparison to the BE position of $MnSiO_3$ which was formed on a 5 nm thermally grown SiO_2 substrate.

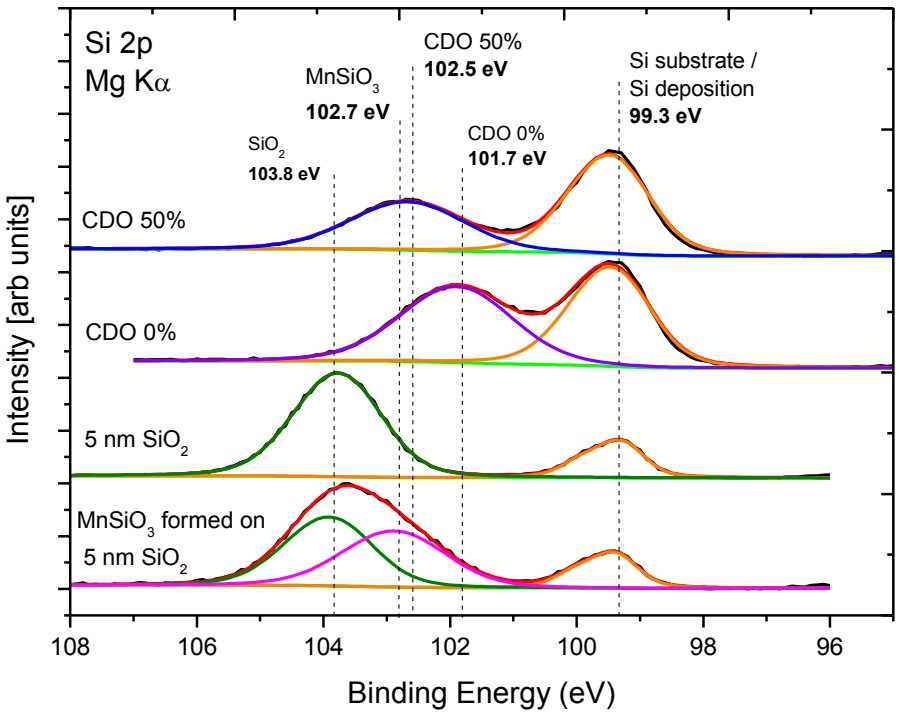

Figure 5.2: XPS Si 2p spectra displaying the BE positions of both CDO Si 2p peaks relative to the B.E. position of $MnSiO_3$.

As can be seen, there is considerable overlap between the $MnSiO_3$ BE peak position and that of both the 0% and 50% Si 2p substrate peaks. Additionally, a larger FWHM for both CDO 0% and 50% (1.9) is noted relative to pure SiO_2 (1.2). These results indicate that the Si 2p spectra cannot be unambiguously used to identify the presence of Mn silicate on either 0% or 50% substrates due to the overlapping nature of the peak positions.

5.3.2 Deposited Mn oxide as a XPS binding energy reference for 0 % and 50% porous CDO

An alternative approach to identifying the presence of Mn silicate would be to use other photoemission peaks characteristic of its formation which have been identified in previous studies. The O 1s photoemission core level could potentially be used to identify

the presence of Mn silicate, however as with the Si 2p spectra, careful B.E. referencing of these peaks must be undertaken in order to accurately identify the growth, if any, of Mn silicate species.

Figure 5.3 shows the O 1s photoemission spectra for SiO_2, CDO 0% and CDO 50%, all following the in-situ deposition of Mn oxide.

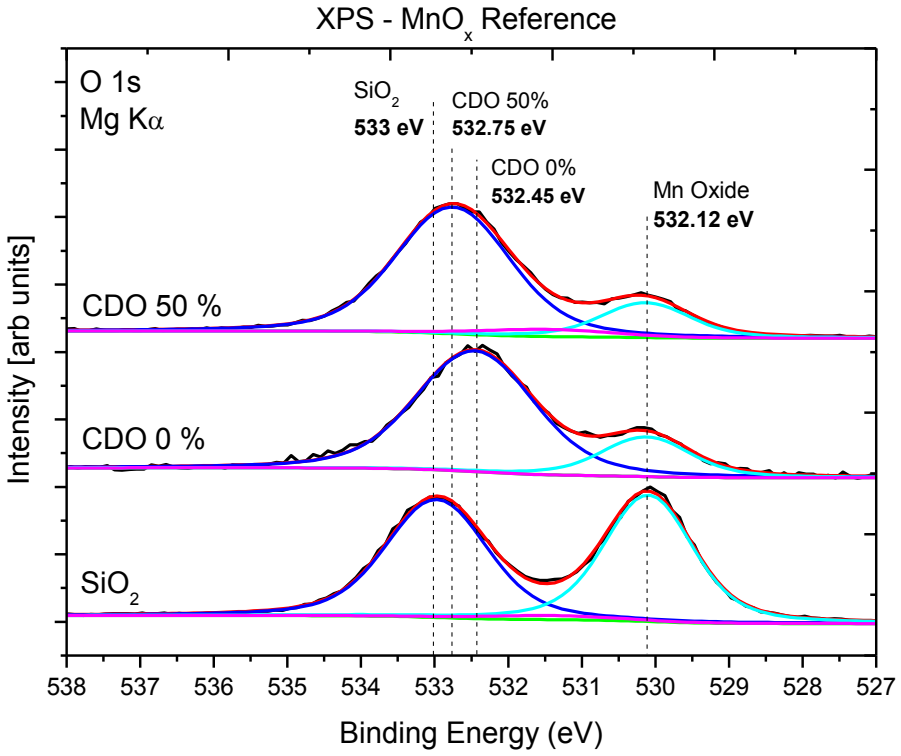

Figure 5.3: XPS O 1s spectra of Mn oxide referencing of both 0% and 50% CDO materials.

The well-known B.E. position of the SiO_2 O 1s substrate peak of 533 eV can be used to accurately reference the position of the deposited Mn oxide signal. In turn, once the BE position of the Mn oxide layer has been identified, it can be used to BE reference the substrate O 1s peak positions of both the CDO 0% and CDO 50% dielectric materials. As can be seen from Figure 5.3, the BE position of the Mn oxide peak relative to the 533 eV

BE position of the SiO_2 substrate was found to be 532.12 eV. Using this peak position as a reference on the CDO substrates, the BE position of the CDO 0% film is 532.45 eV and that of the CDO 50% is 532.75 eV indicating a small BE difference.

Figure 5.4 displays the O 1s spectra during the formation of $MnSiO_3$ on 5 nm thermal SiO_2 following a 500°C anneal of a Mn oxide deposited layer. Having the established BE position of Mn oxide, an accurate peak position of $MnSiO_3$ related O 1s signal can be obtained relative to the BE position of Mn oxide.

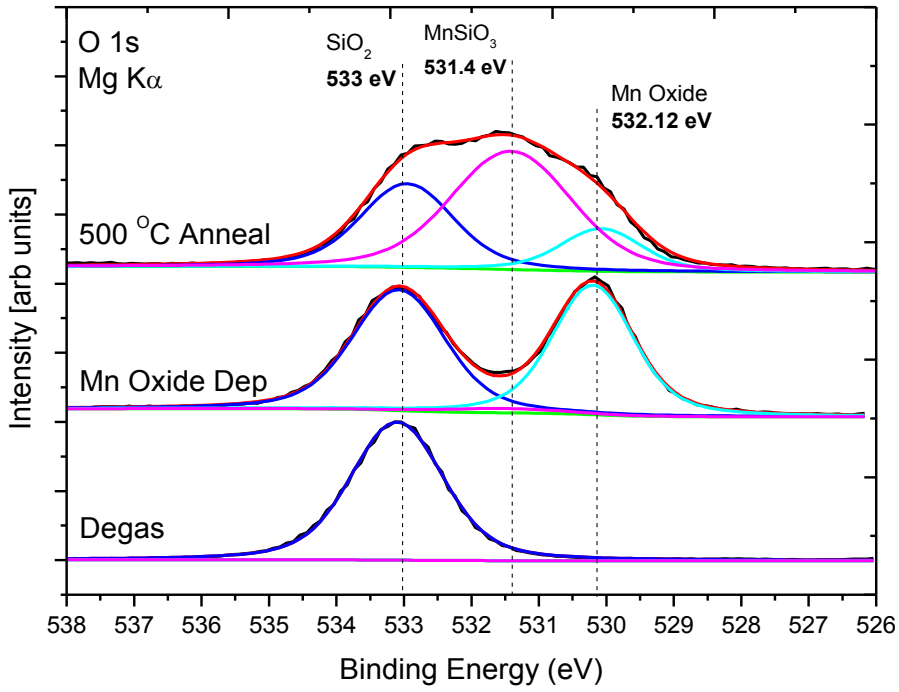

Figure 5.4: XPS O 1s spectra of $MnSiO_3$ formation on 5 nm thermal SiO_2.

This allows the identification of Mn silicate on both the 0% and 50% CDO materials within the O 1s spectra as seen in Figure 5.5.

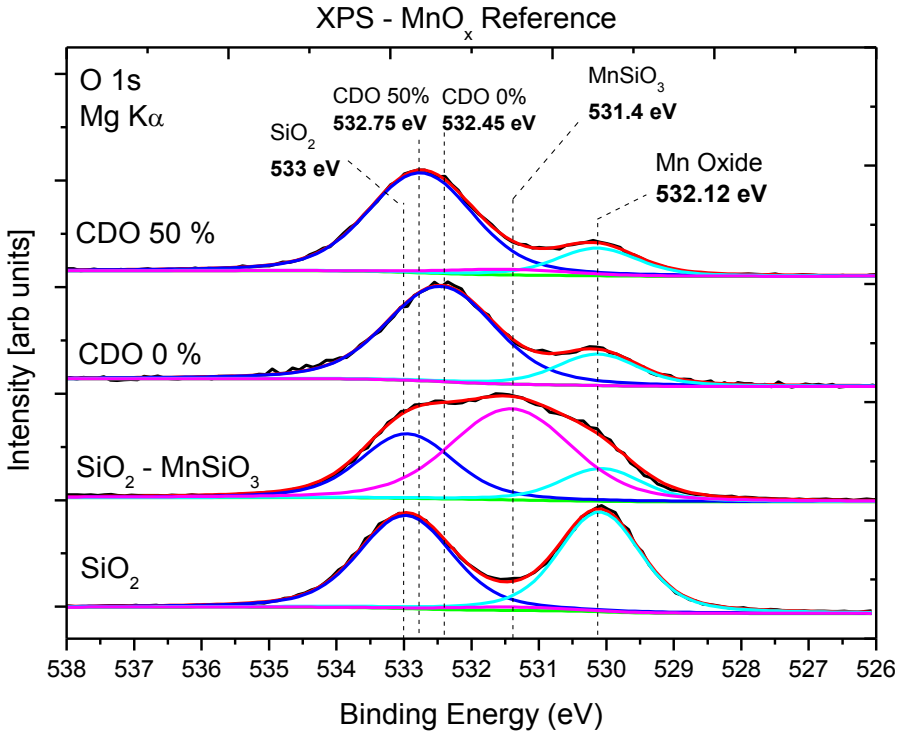

Figure 5.5: XPS O 1s spectra displaying the BE position of $MnSiO_3$ relative to the BE referenced CDO 0% and 50% dielectrics.

5.4 Mn deposition for barrier formation on 0% and 50% porous CDO

In order to study the growth of Mn silicate on both 0% and 50% porous CDO, both samples were simultaneously mounted on the same sample holder and inserted into a UHV chamber with in-situ Mn deposition and XPS capabilities. XPS spectra for both samples in the as loaded state were taken prior to degassing of the samples at a temperature of 500 ^{O}C for one hour as shown in Figure 5.6. The calculated elemental composition values, determined using standard elemental sensitivity factors, before and after the 500 ^{o}C degas anneal are displayed for each sample.

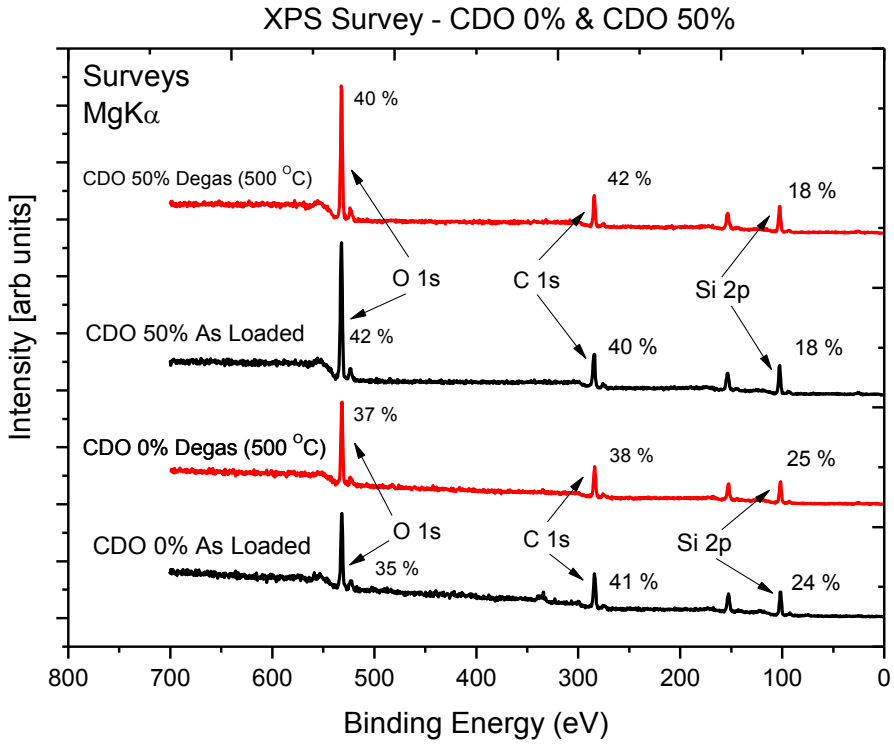

Figure 5.6: XPS survey spectra of CDO 0% and 50% both as loaded and degas.

Both 0% and 50% as loaded CDO samples have different elemental compositional ratios as displayed in Table 5-1**.** The CDO 0% reduces in carbon following the degas procedure, typical of the removal of adventitious carbon contamination from the surface of the material. In contrast, the CDO 50% sample initially has a slightly lower amount of carbon in the as loaded state, relative to the CDO 0%. Following the degas procedure of the CDO 50%, the carbon signal increases, with a corresponding decrease of oxygen in the film. This result is consistent with removal of water vapour from the pores of the CDO 50%, thereby reducing the oxygen signal. Finally after degas, both films still appear to have slightly different elemental ratios, with the CDO 50% having more carbon and oxygen relative to the reference CDO 0% film. This increase in oxygen for the CDO 50% film,

could help to explain why the Si 2p peak position is found to be at a higher binding energy relative to the lower oxygen content CDO 0% film (as seen in section 5.3.1), due to the fact that oxygen has a high electronegativity value.

Elemental % and ratio	Si	C	O
As Loaded:			
CDO 0% (percentage)	24 %	41 %	35 %
CDO 0% (ratio to Si)	1	1.7	1.45
CDO 50% (percentage)	18 %	40 %	42 %
CDO 50% (ratio to Si)	1	2.21	2.33
Degas:			
CDO 0% (percentage)	25 %	38 %	37 %
CDO 0% (ratio to Si)	1	1.52	1.48
CDO 50% (percentage)	18 %	42 %	40 %
CDO 50% (ratio to Si)	1	2.33	2.22

Table 5-1: Elemental percentages and ratios for CDO 0% and 50% both as loaded and degas.

Following degas of the samples, ~ 2-3 nm of Mn was deposited simultaneously onto both 50% and 0% CDO substrates as displayed in Figure 5.7.

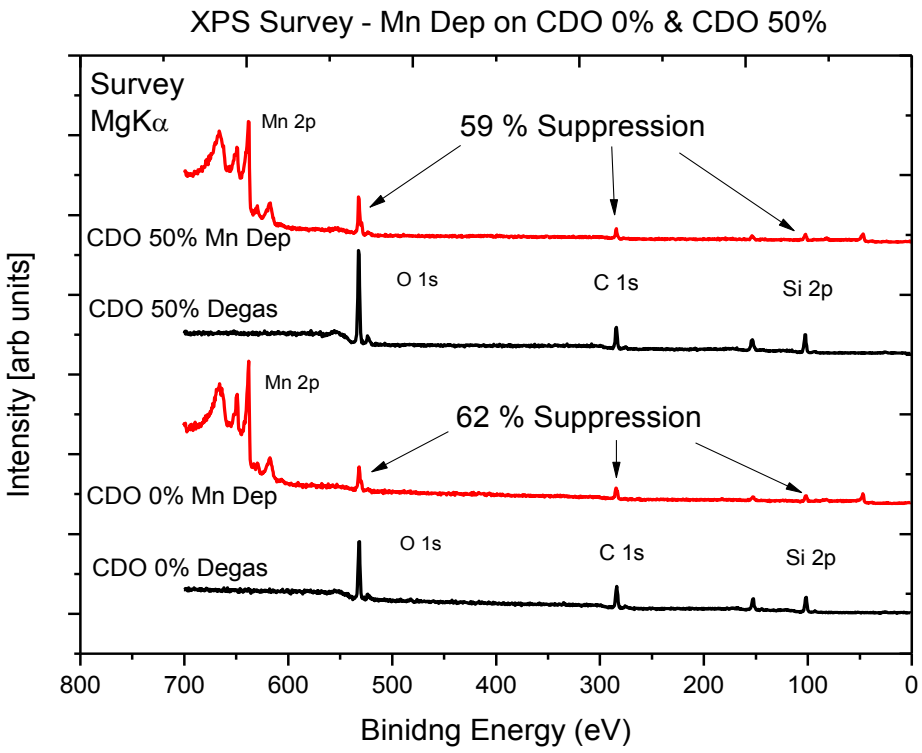

Figure 5.7: XPS Survey spectra of CDO 0% and 50% both degas and Mn dep.

The calculations of the suppression of the substrate peak intensities included in Figure 5.7 show that the 0% porosity substrate signal has been attenuated by 62 % of its original value following the Mn deposition. The equivalent suppression of the 50% porosity substrate is to 59 % of its original intensity. This difference is consistent with the porous nature of the 50 % porous CDO substrate when compared to the 0% porous material as the simultaneous Mn deposition would be expected to attenuate both substrates by the same amount. It suggested that the Mn has diffused into the pores of the 50% CDO during deposition, thereby decreasing the suppression of the substrate relative to the 0% porous sample. Figure 5.8 displays the XPS Mn 2p spectra for both the CDO 0% and CDO 50% following Mn deposition. As can been seen, the intensity of the Mn 2p signal on the 50%

sample is lower relative to the 0% control sample. This result agrees with the difference in suppression of the substrate signals for both 0% and 50% substrates as seen in Figure 5.7, due to the porous nature of the 50% CDO, the Mn 2p signal is diminished, possibly due to diffusion of Mn into the porous network of the substrate. This is in contrast to the 0% control sample with which the deposited Mn should be entirely surface localised, thereby giving a larger signal count during XPS analysis.

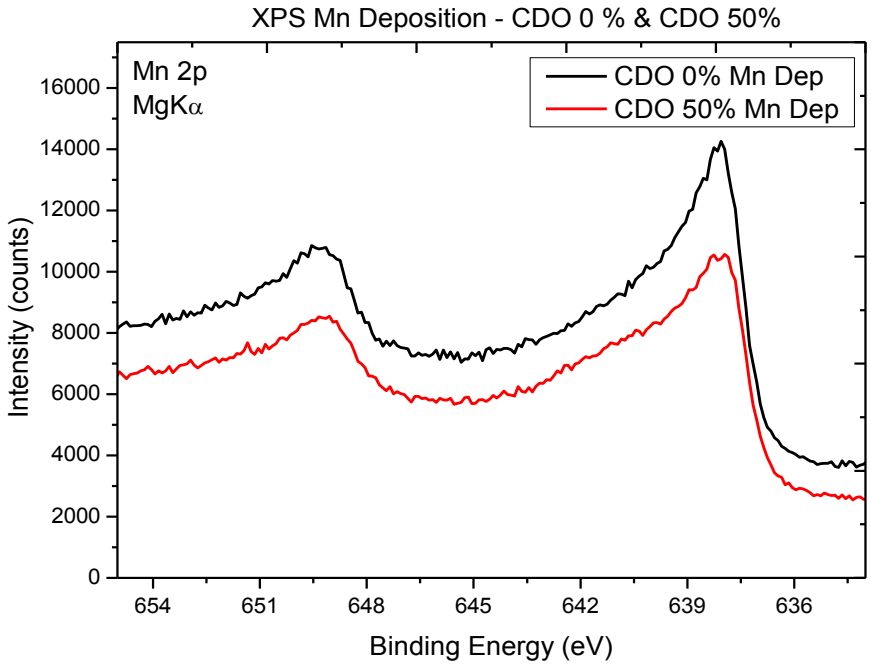

Figure 5.8: XPS Mn 2p spectra of Mn deposition on CDO 0% and CDO 50%.

Following Mn deposition, both CDO 0% and CDO 50% were thermally annealed to 500 ^{O}C in order to track any chemical interaction between the deposited Mn and substrate materials.

Figure 5.9 displays the Si 2p spectra for both CDO 50% and 0% layers throughout the course of the experimental procedure. No significant change is observed in peak profile with both the position and width of each Si 2p peak remaining constant throughout the course of the experiment. The result is consistent with the observation made in Section

5.3.1 where it was shown that the B.E. position of Mn silicate overlaps considerably with both Si 2p peaks of CDO 0% and 50% substrates.

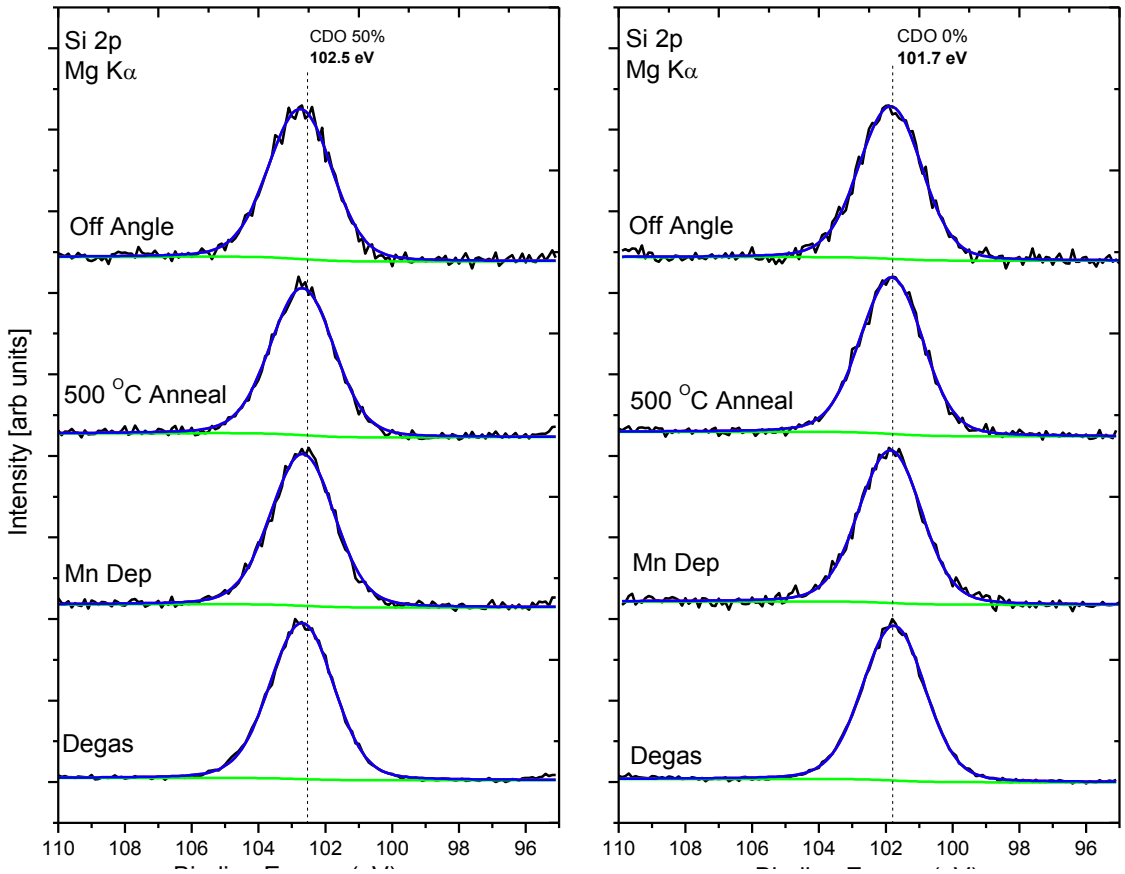

Figure 5.9: XPS Si 2p spectra of both 50% and reference 0% CDO dielectrics during experimental procedure.

Figure 5.10 displays the C 1s XPS spectra for both CDO 50% and reference CDO 0% over the course of the experimental procedure. Similar to the Si 2p and O 1s BE positions for both materials, a difference is noted in BE position (0.5 eV) for the C 1s spectra between both samples. As can be seen following Mn deposition, a lower binding energy peak appear on both spectra, consistent with previous reports of the formation of Mn carbide [5].

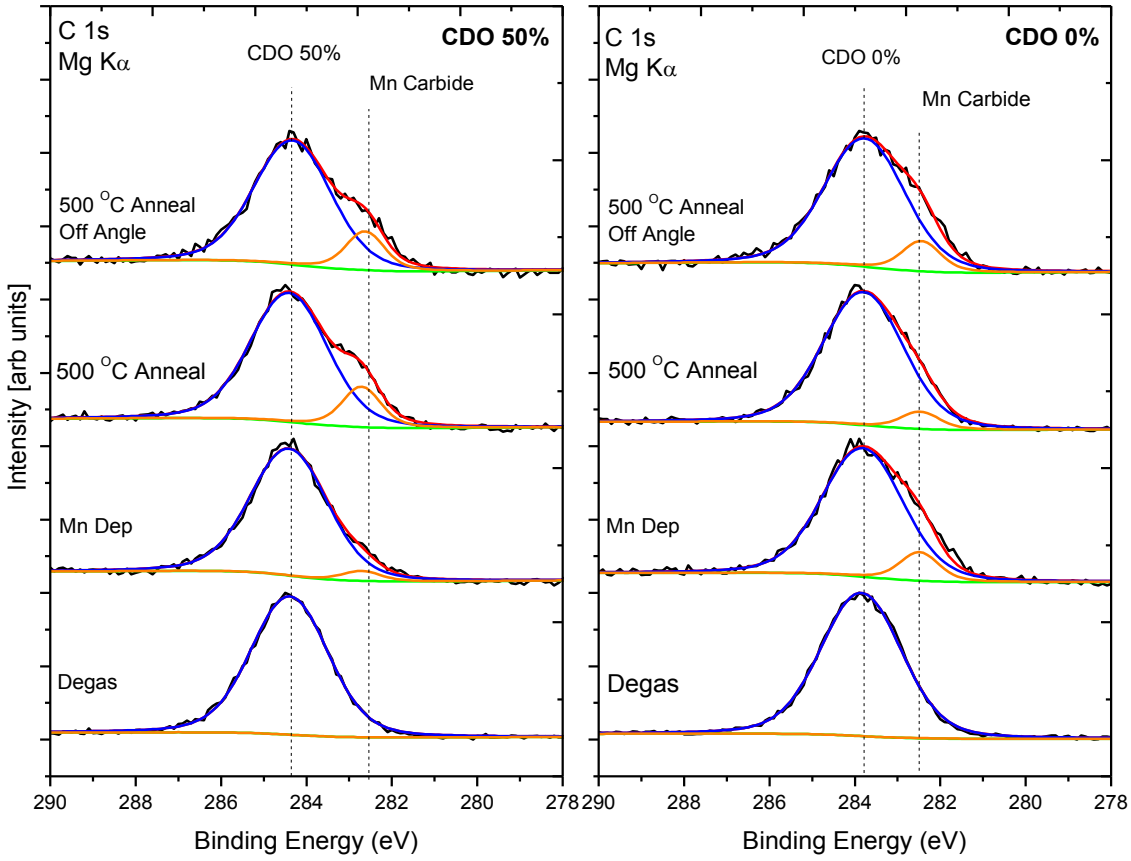

Figure 5.10: XPS C 1s spectra for both CDO 50% and reference 0% during experimental procedure.

Following the 500 ^{O}C anneal stage, an increase in Mn carbide is seen on the 50% CDO in contrast to a reduction in the 0% CDO sample. Off angle spectra indicate that the Mn carbide is predominantly surface localised on both samples. When the spectra for the CDO 50% and 0% post 500 ^{O}C anneal are examined, it is seen that there is more Mn carbide formation on the 50% CDO material relative to the 0% film. This result is consistent with the increased chemical interaction between the deposited Mn and the 50% porous sample resulting for greater in-diffusion of the Mn into the porous structure than is possible on the 0% CDO.

Figure 5.11 displays the O 1s core level spectra during the Mn deposition and anneal cycle. As can be seen in both the 50% and 0% spectra, the deposition of Mn results in the observation of a Mn oxide component peak identified by the O1s component peak at a B.E. of 530.12 eV.

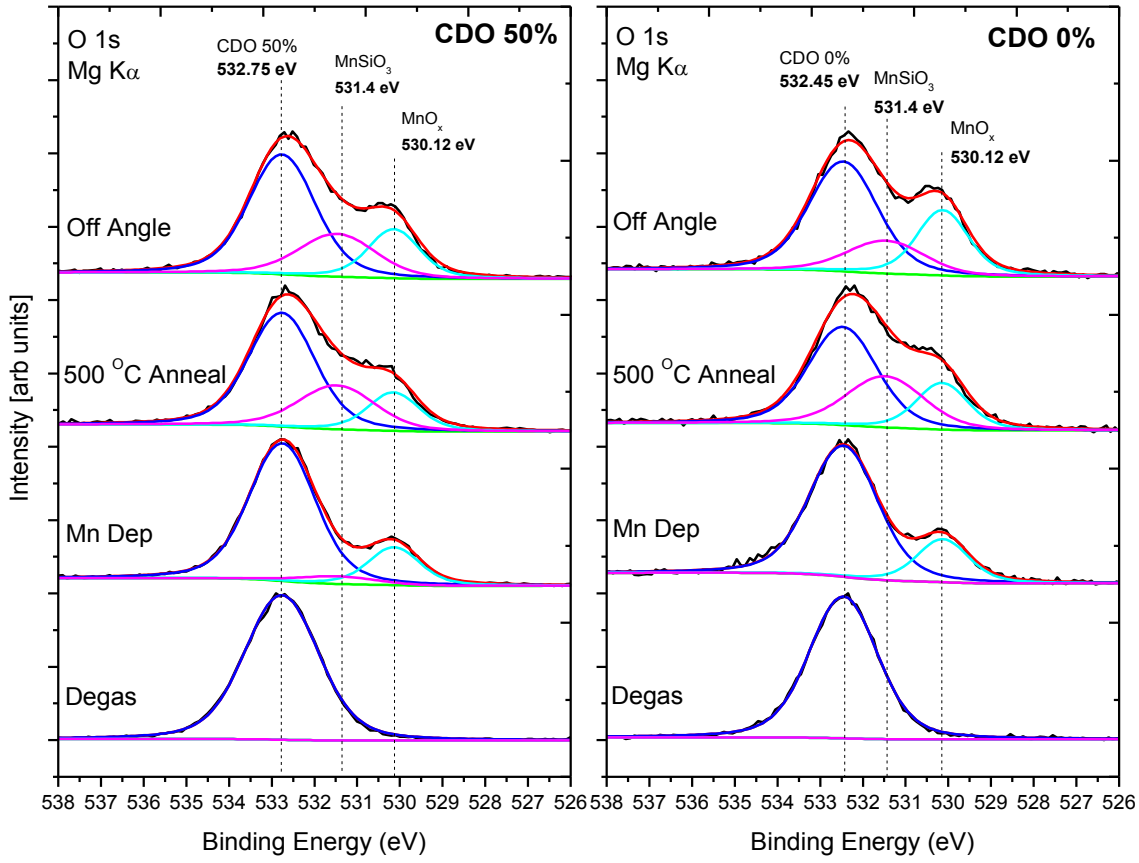

Figure 5.11: XPS O 1s spectra of both 50% and reference 0% CDO dielectrics during the Mn deposition and anneal cycle.

Following a 500ºC anneal, a third peak emerges between the substrate and Mn oxide peaks for both 50% and 0% films at a B.E of 531.4 eV. The B.E. referencing work outlined in section 5.3.2, suggests that this peak can be attributed to the growth of a

$MnSiO_3$, component. Off angle scans following the 500 ^{O}C anneal indicate that the Mn oxide peak is more surface localised than the newly formed peak attributed to Mn silicate. This angular dependence of the two component peaks is more pronounced on the 0% porosity substrate compared to the 50% sample. Again this is consistent with a greater chemical interaction depth perpendicular to the surface on the 50% sample due to the porosity. The chemical interactions results in Mn silicate layer formation on the 0% porosity sample are more surface localised. Typically, a ratio of the O 1s silicate component peak to the substrate O 1s peak could be used for each sample to give a direct comparison of the amount of silicate formed on both the 0% and 50% CDO materials. This calculation however assumes that both substrates have the same amount of Mn deposited. Even though both substrates were simultaneously exposed to the same Mn deposition, it was outlined above that following XPS scans post deposition, more Mn signal was seen in the surface area of the 0% relative to the 50%. Thus the above calculation can be misleading when trying to compare the silicate growth on both substrates. A better comparison is by dividing the silicate peak area by the sum of the Mn oxide and Mn silicate peak areas, thus giving information about the total amount of silicate formed in each sample from the total amount of Mn oxide present on each sample. This calculation shows that for the total Mn oxide and $MnSiO_3$ peak areas, 60.7% of the area is due to $MnSiO_3$ for the 0% reference sample and 61.6% for the 50% CDO sample. It is thus shown that similar amounts of Mn oxide to $MnSiO_3$ reside on the surface of each CDO sample. This however can be misleading as it is potentially limited by the sampling depth of the XPS system used, thereby not taking into account any Mn which has diffused further into the CDO 50% substrate, and potentially forming more $MnSiO_3$. In order to further investigate the chemical species formed at the interface on these different porosity

samples, following XPS characterisation, both samples were capped with a thick Cu layer prior to removal from UHV in order to protect the interface from atmosphere exposure.

5.5 XAS of CDO 0% & 50%

Due to the difficulty in peak fitting the Mn 2p spectra using conventional XPS and the fact that only the O 1s photoemission spectra was used to identify and characterise the formation of $MnSiO_3$, additional chemical information on the nature of the precise chemical species formed at the Mn/dielectric interface was obtained via x-ray absorption spectroscopy measurements (XAS). The high surface sensitivity of conventional XPS enables the acquisition of chemical information from typically the top ~ 7 nm of the sample. In contrast, the XAS measurements performed in this study have a sampling depth into the material which is significantly larger than the region of chemical interaction. This is because a fluorescence method of detection was used in these measurements. This is particularly interesting due to the porous nature of the 50 % sample, whereby it is possible that any deposited Mn on the surface could diffuse into the bulk of the material, below the sampling depth of conventional XPS, however it would still be detected via XAS measurements.

Figure 5.12 displays XAS data of the Mn K-absorption edge at 6545 eV from both the 50% and 0% CDO materials following Mn deposition and anneal showing significant differences in the absorption profile above the edge.

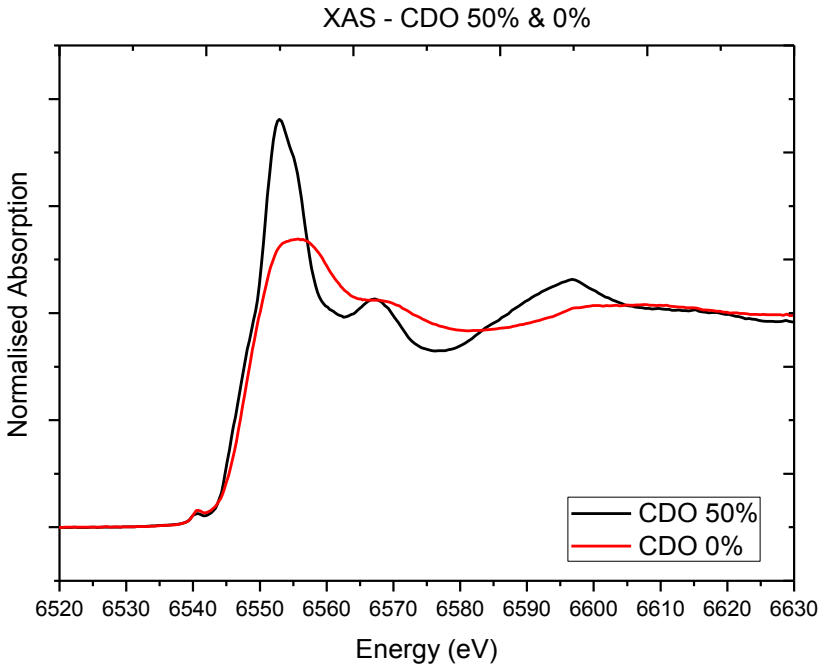

Figure 5.12: XAS Mn K edge of both CDO 50% and reference 0%.

The CDO 50% sample has more pronounced spectra features than the 0% sample. In an attempt to identify the origin of these spectral differences XAS absorption spectra of various reference Mn oxide compounds including Mn_3O_4, Mn_2O_3, MnO_2, MnO and $MnSiO_3$ were acquired on the same instrument and are displayed in Figure 5.13.

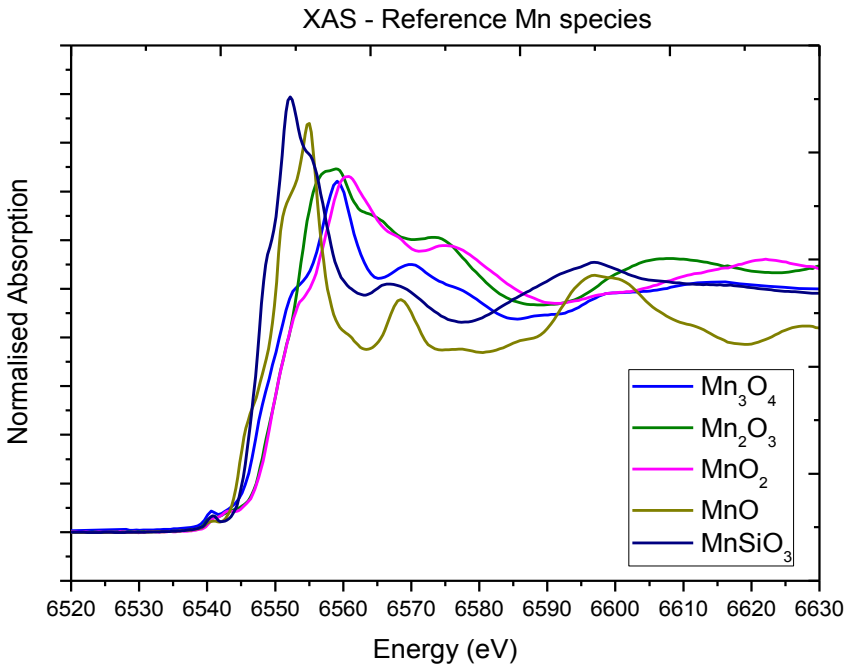

Figure 5.13: XAS Mn K edge of Mn reference species.

Distinctive differences are apparent for the different oxidation states. This is in sharp contrast to what would be observed in the corresponding XPS spectra of different Mn oxidation states. In particular, very distinctive differences are observed in the XAS absorption spectra of MnO and $MnSiO_3$, two compounds which have the same 2^+ oxidation state and therefore extremely difficult to distinguish by XPS measurements, if even possible. Fitting the XAS Mn k-edge absorption spectra for both CDO 50% and 0% samples was performed by way of a linear combination of the reference spectra. Figure 5.14 displays the reference CDO 0% dielectric data which was subjected to a linear fit using all Mn chemical species reference data.

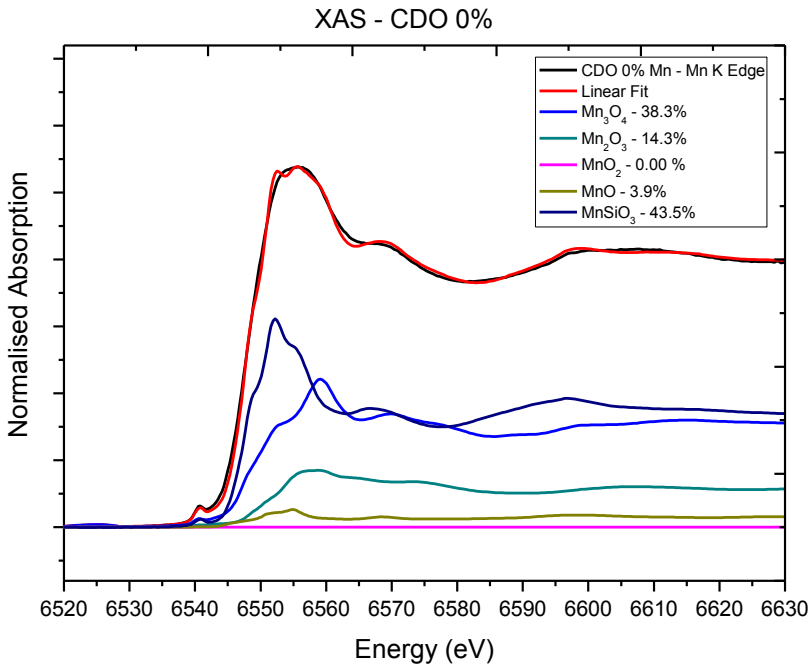

Figure 5.14: XAS linear fitting of reference CDO 0%.

The linear fit agrees well with the data however a number of slight discrepancies are noted. Relative amounts of different Mn in oxidation states can be extracted from the linear fit which indicate that the main species of Mn present in the 0% sample is $MnSiO_3$ (43.5%) followed by Mn_3O_4 (38.3%) in addition to traces of other Mn oxide species. Mn_3O_4 is the most thermodynamically stable Mn oxide and forms on metallic Mn after prolonged air exposure. This would suggest that the deposited Cu overlayer on the Mn treated CDO substrates didn't act as an oxygen barrier. These results suggest that the main Mn chemical species present are Mn silicate and Mn oxide, which is in agreement with the XPS data taken during barrier layer formation on the 0% sample.

XAS linear fits for the CDO 50% sample shown in Figure 5.15 indicates that the $MnSiO_3$ at 88% is the predominant chemical species followed by MnO (11.6%). While the agreement with the raw data is not as good as for the 0%, it does support the finding of

the XPS study that $MnSiO_3$ is the dominant chemical species formed at the Mn/CDO interface.

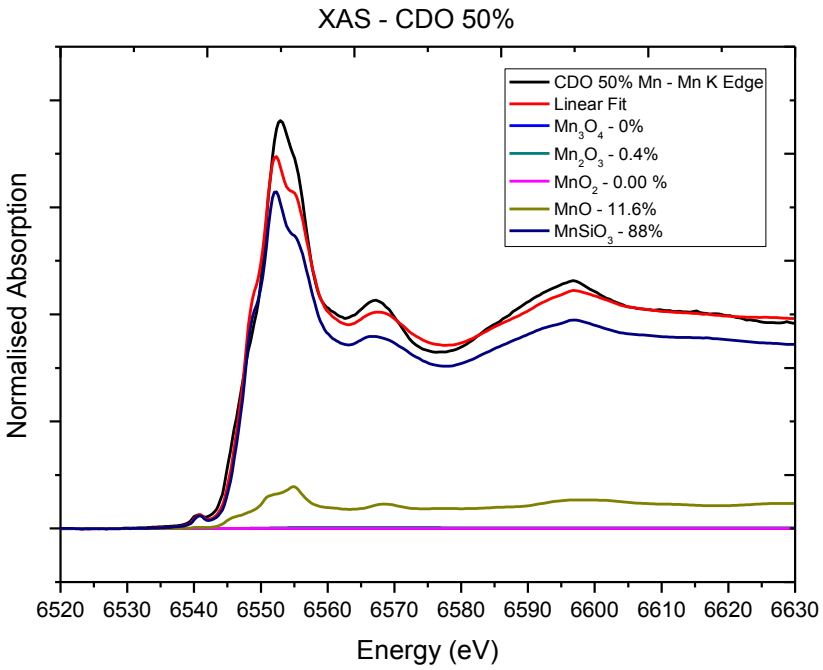

Figure 5.15: XAS linear fitting of CDO 50%.

Discrepancies in the linear fit of both the CDO 0% and 50% samples may also be due to the fact that no metallic Mn or Mn carbide species reference XAS measurements were taken or used in the linear fits of the CDO samples. As seen in the XPS analysis, Mn carbide was formed on both the CDO 0% and 50% samples, in addition a small amount of metallic Mn may also have been present. These unknown species may account for the discrepancies seen in the linear fits, however given the fit accuracy overall, it is noted that these species are most likely to be only minor components within both samples.

5.6 TEM of CDO 0% & 50%

In order to gain structural information of the barrier layers formed on both 50% and 0% CDO materials, the samples which were fabricated with in-situ XPS and subsequent XAS measurements were subsequently subjected to transmission electron microscopy analysis. Both 50% and 0% CDO TEM lamella structures were prepared by a gallium focused ion beam (FIB) in order to produce an electron transparent, sub-100 nm cross section of the interfaces. This preparation enabled the use of TEM in scanning transmission electron microscopy (STEM) mode, in addition to a high angle annular dark field detector to produce a Z contrast image. Electron energy loss spectroscopy (EELS) was employed within the TEM system to elementally map the interfaces of the samples. Figure 5.16 displays the TEM images of both (a) CDO 0% and (b) CDO 50%. The thickness of the CDO film calculated from the TEM measurements were 98 nm and 66 nm respectively for CDO 0% and 50% dielectric layers. It is apparent from the images that the Mn / CDO interface for the 0% CDO sample is flat and sharp, indicating that the deposited Mn is surface localised and continuous, consistent with the fact that the 0% CDO has no associated surface porosity. In contrast, the Mn / CDO interface of the 50% porosity sample is significantly rougher with difficulty to identify a discrete Mn layer, consistent with the highly porous nature of this dielectric material.

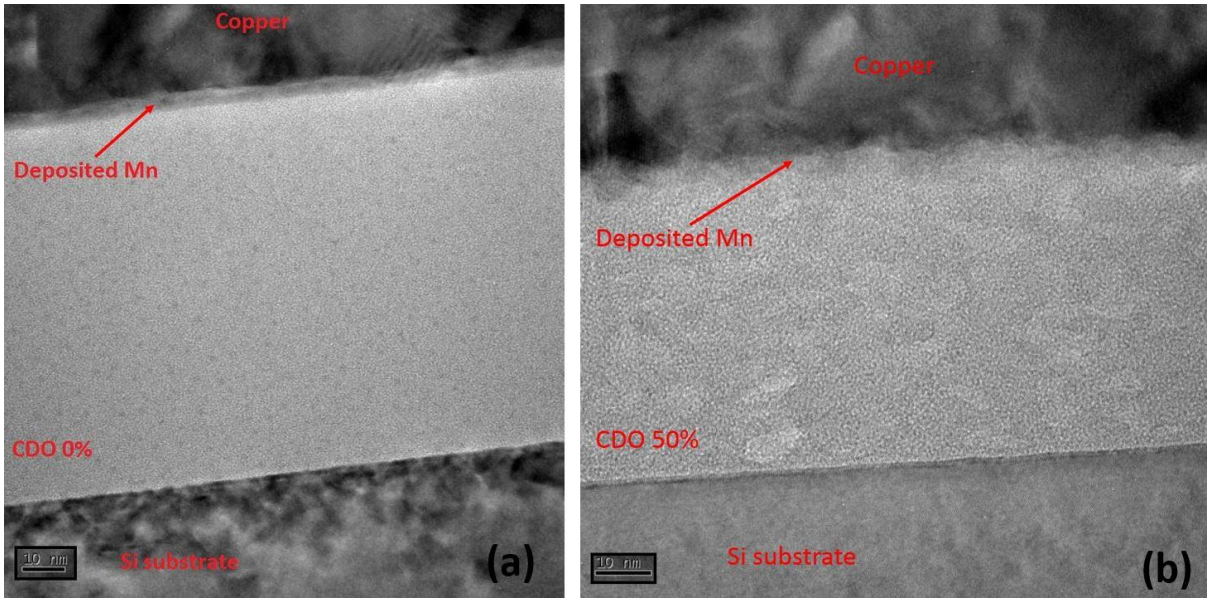

Figure 5.16: TEM images of (a) 0% CDO and (b) CDO 50% dielectrics following barrier formation studies.

Figure 5.17 displays the TEM elemental mapping of the CDO 0% sample. As can be seen from the data, the Mn layer appears to be surface localised with the thick Cu capping layer on top. The CDO layer beneath displays silicon, carbon and oxygen as confirmed via initial XPS scans of the substrates. The chemical composition of the barrier region consists of Mn, O and Si again consistent with the XPS and XAS studies.

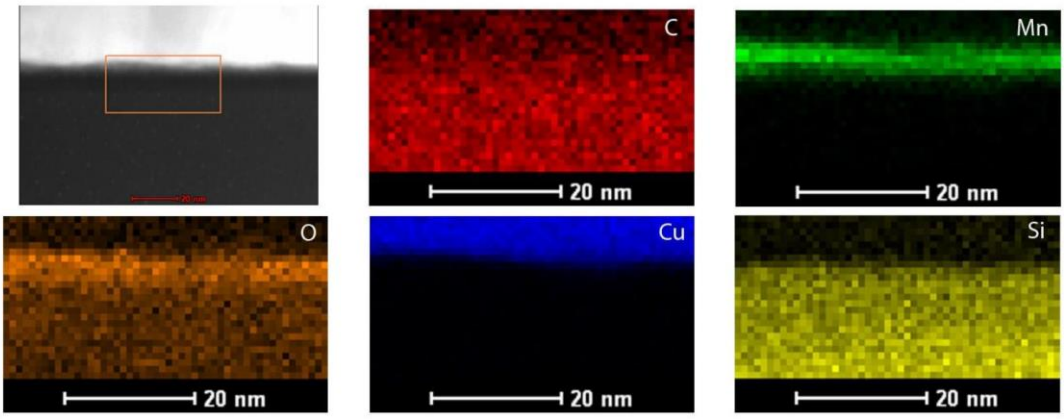

Figure 5.17: TEM elemental mapping of CDO 0%.

Figure 5.18 displays EELS elemental mapping data for the CDO 50% sample. In contrast to the CDO 0%, the Mn layer is less surface localised and appears to extend further into the substrate consistent with Mn diffusion into the dielectric material. This uneven interface is replicated in higher roughness in the Cu capping layer of the 50% porous sample. The elemental composition of the barrier layer region is again indicative of Mn silicate formation.

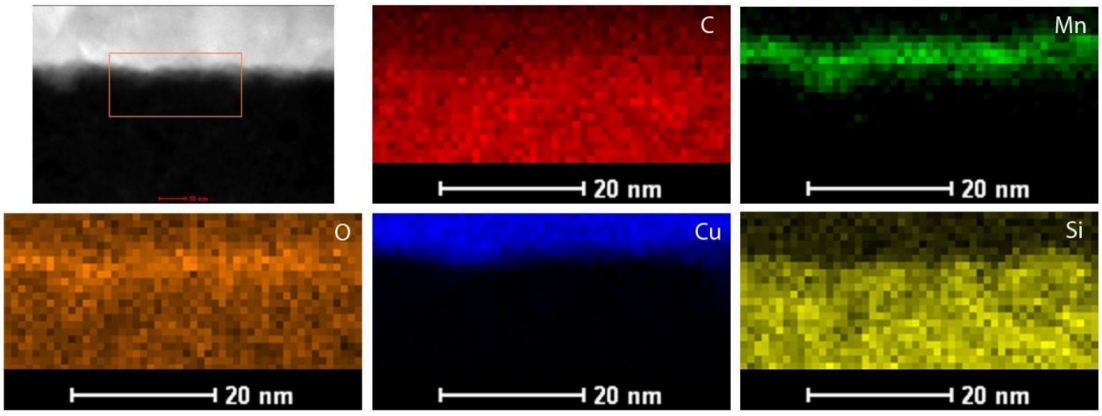

Figure 5.18: TEM elemental mapping of CDO 50%.

The measured thickness of the Mn over layer for the 0% CDO was found to be ~4 nm in contrast to the CDO 50% sample which was found to be ~6 nm thick. It is worth re-stating

at this point that both samples were exposed simultaneously to the same Mn deposition. Therefore the most likely explanation for the contrasting results in the Mn layer thickness is the diffusion of Mn into the porous structure of the 50% sample. This is evident in the XPS results as a decrease in Mn signal with a simultaneous increase in substrate signal, due to the fact that as the Mn diffuses through the porous network, it possibly diffuses beyond the XPS sampling depth, whilst simultaneously not supressing the under layer substrate signal.

EDX profiles across the barrier layer region for the CDO 0% presented in Figure 5.19 confirm the elemental composition evident from the 2-dimension maps.

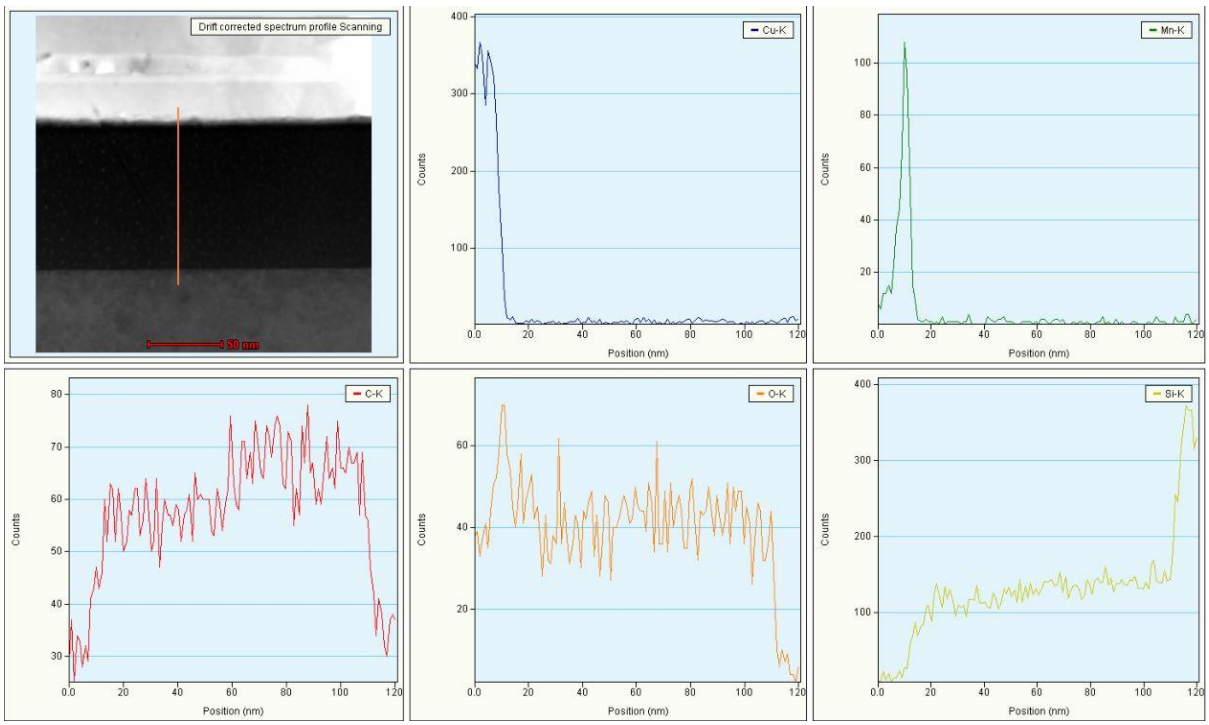

Figure 5.19: EDX profiles across the Mn / CDO / Si interfaces of the CDO 0% sample.

The localised nature of the oxidised Mn layer between the Cu and the CDO is clearly apparent. The higher oxygen signal in the barrier region than in the CDO dielectric is consistent with the oxygen rich $MnSiO_3$ composition of the interfacial layer. In addition,

the lack of Cu signal in the dielectric substrate confirms the effectiveness of the barrier at preventing Cu diffusion. Figure 5.20 displays the EDX profiles of the CDO 50% sample confirming the surface localised distribution of the Mn in an oxidised state.

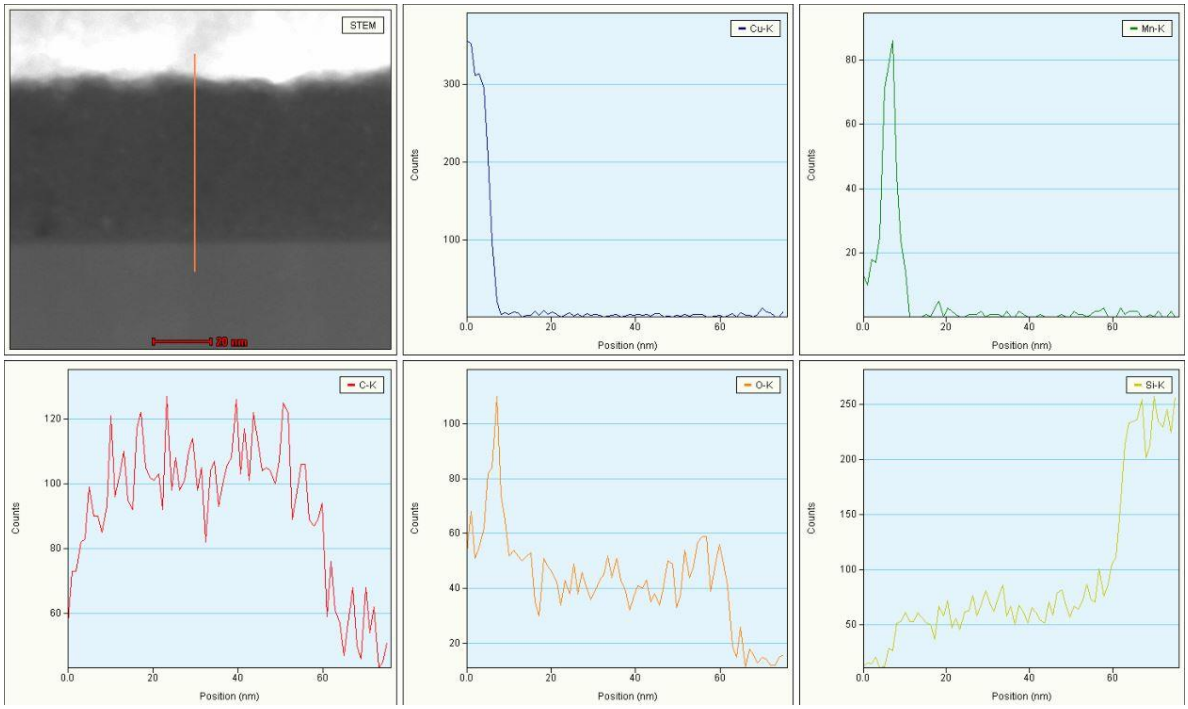

Figure 5.20: EDX profiles across the Mn / CDO / Si interfaces of the CDO 50% sample.

As with the 0% sample, the Cu appears to be fully surface localised, indicating that none of the Cu capping layer has diffused into the 50% CDO dielectric layer. These TEM studies indicate that for both dielectric materials, a Mn based barrier layer forms which is effective in preventing Cu diffusion. The thicker barrier layer in the case of the 50% porous dielectric reflects the fact that Mn has diffused further into the dielectric than in the case of the chemically identical 0% porosity substrate.

5.7 Chapter conclusions

Both 0% and 50% porous carbon doped dielectric samples were investigated in relation to Cu diffusion barrier layer formation. Initial XPS binding energy referencing of the CDO peaks indicate that the Si 2p, which traditionally is the primary identifier of $MnSiO_3$, could not be used in this study due to the overlapping nature of the CDO peak positions with that of $MnSiO_3$. The O 1s spectra were successfully referenced for both the 0% and 50% CDO materials, thereby allowing the identification of $MnSiO_3$ during XPS analysis. The simultaneous deposition of a thin Mn layer on both 0% and 50% substrates gave evidence for the diffusion of Mn into the porous structure of the 50% porosity CDO sample from XPS analysis. Post in-situ annealing reveals that $MnSiO_3$ is formed on both the 0% and 50% CDO materials, in addition to Mn carbide. XAS measurements confirmed the presence of $MnSiO_3$ on both dielectrics, with a larger amount appearing on the 50% CDO sample. TEM was also employed to give structural and elemental mapping across the Mn / CDO / Si interfaces for both sample. Thickness measurements of the Mn deposited on both samples agree with XPS results indicating that diffusion of Mn had occurred into the surface pores of the 50% sample. No Cu from the Cu capping layer was detected in the dielectric of either 0% or 50% samples, indicating the effectiveness of the barrier layer at preventing Cu diffusion.

This chapter highlights the difficulty in controlling the barrier layer thickness on highly porous CDO materials to the 2-3nm target thickness for future generations of interconnect technology. In addition to the formation of Mn carbide at the interface following Mn deposition and annealing, the surface porosity of the 50% CDO presents serious challenges due to diffusion of the barrier layer material into the surface of the dielectric, which seems to be inherently related to the dielectric structure. This diffused material

may have a negative impact on the k-value of the material, thereby making the successful integration of highly porous dielectrics into device fabrication very challenging.

5.8 References

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6 CuAl (90:10 % wt) alloy for use in BEOL IC interconnect technologies

6.1 Introduction

Aluminium (Al) is an attractive metal to use in BEOL processes of IC production due to its previous use as the interconnect metal of choice. This well studied metal has been replaced by copper (Cu) as the conducting material due to the lower resistivity and increased resistance to electromigration offered by Cu interconnect schemes [1]. With the change to Cu as the interconnect metal of choice also came a number of disadvantages, most notably the diffusion of Cu into any surrounding ILD material [2-6]. Aluminium however has a high thermodynamic favourability to form a stable metal oxide, which could potentially be of use as a self-forming barrier candidate [7]. In order to test this principle, this chapter addresses the issue of alloying Cu with Al for possible Cu seed layer applications in future interconnect technology schemes. It has been shown previously that when Al is alloyed with Cu, it has a beneficial impact of supressing electromigration of Cu interconnects [8,9]. Thus, this chapter studies an alloy of Cu and Al (Cu:Al 90:10 % wt) in order to determine its effectiveness as an interconnect seed layer for BEOL applications. The main properties of such an alloy should include [10]:

(a) Expulsion of the alloy element from the bulk material following anneal treatments.
(b) Interaction of the expelled alloying material with any surrounding ILD material, consistent with a self-forming barrier process

(c) Passivation of the surface of the material via oxidation of the alloying element in order to prevent oxidation of the Cu within the film.

(d) Good adhesion between the material and any surrounding ILD material as Cu is known to have poor adhesion to dielectric materials, in addition to low surface roughness.

(e) Prevent Cu diffusion into any surrounding ILD material.

6.2 Experimental details

Blanket Cu and CuAl alloy (90:10 % wt) films were sputter deposited from dedicated sputter targets onto both 100 nm, 10 nm thermally grown and 100 nm PECVD deposited SiO_2 substrates in the Tyndall National Institute, Cork. In addition, a number of MOS structures were fabricated on both 100 nm thermal and PECVD SiO_2 substrates using Cu, Al and CuAl alloy gates in order to electrically test the effect of the alloying element Al on the Cu metal gate.

In subsequent experiments, thin film SiO_2 layers (~ 3nm) were deposited by e-beam deposition onto blanket layers of Cu and CuAl alloy. XPS analysis and thermal anneals were carried out in the same XPS systems previously described.

Electrical measurements were carried out on a Keithley 4200 for IV analysis and a Boonton 72b 1 MHz capacitance meter interfaced to the Keithley 4200 for CV analysis.

6.3 XPS referencing of Cu, Cu oxide, Al & Al oxide

In advance of undertaking an XPS study of the CuAl alloy, reference spectra were acquired from pure Cu and Al films. This was necessary due to the overlapping nature of the Al 2p and Cu 3p core level peaks within the acquired XPS spectra of the CuAl alloy. Reference samples were studied in order to accurately peak fit the complex Cu 3p/Al 2p spectra associated with the CuAl alloy sample.

Figure 6.1 shows XPS reference scans of both metallic Al and Al oxide. Metallic Al was deposited from a tungsten wire filament within an UHV system at a pressure better than $1x10^{-8}$ mbar onto a 100 nm SiO_2 substrate. XPS was then performed on the sample immediately after deposition. Survey scans of the deposited layer reveal that no O 1s peak was present within the sampling depth of XPS, thus the deposited Al was thick enough to reduce the substrate signal to zero and leave a pure metallic Al film. Once the reference spectra were acquired, the sample was removed from the UHV system and stored in a desiccator for 2 days to oxidise in atmosphere. The sample was then re-loaded into the UHV system and reference data taken for ambient oxidised Al were acquired. As can be seen in Figure 6.1, the pure metallic Al reference spectrum for the Al 2p photoelectron core level at a BE position of 72.9 eV is asymmetric, requiring fitting using an asymmetric profile, in contrast to conventional Voigt profile fits. The ambient exposed sample, used as an Al oxide reference spectrum, reveals that a broad peak to a higher binding energy of 75.5 eV appears on the Al 2p spectra following atmosphere exposure. This peak has been attributed to Al oxide due to the concurrent growth of an O 1s peak in the survey spectra. Although the oxide peak within the Al 2p spectra is clearly seen, so too is the

metallic Al peak, indicating that the oxide layer grown due to atmosphere exposure is smaller than the sampling depth of XPS.

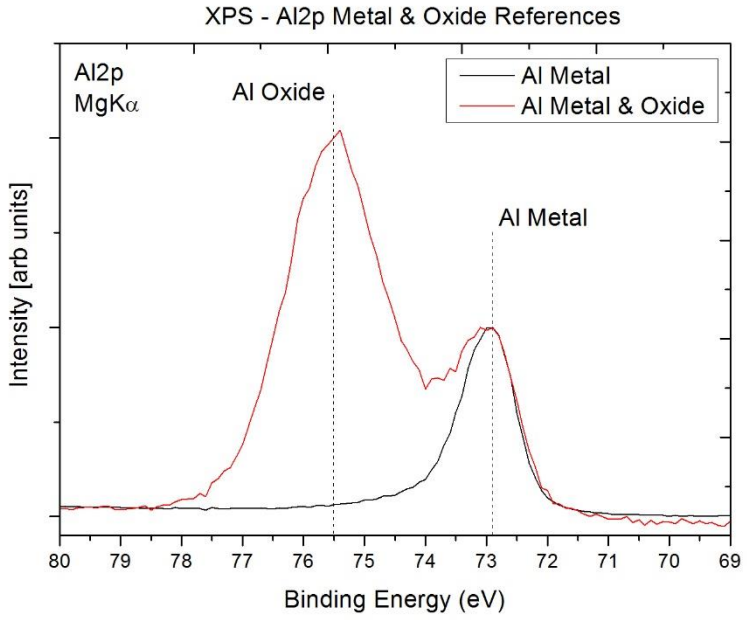

Figure 6.1: XPS Al 2p spectra of metal Al and Al oxide reference data.

Cu reference material scans were taken on the same XPS system in order to recreate similar environments and data acquisition parameters. As with the reference Al films, Cu was thermally evaporated onto a 100 nm SiO_2 substrate in the UHV system at a pressure better than $1x10^{-8}$ mbar. Immediately following deposition the deposited Cu layer was examined using XPS. Survey spectra reveal that no O 1s peak was present, indicating that the Cu layer was thick enough to eliminate the substrate signal and also that the Cu was in a pure metallic state. After the metallic Cu reference data was taken, the sample was removed from the UHV environment and stored in a desiccator for one month to oxidise. Following the atmosphere exposure, the Cu film was reloaded into the UHV system and rescanned using XPS. The survey spectrum displays an O 1s peak indicating that the Cu

has oxidised. Cu 3p high resolution narrow window scans show that after atmosphere exposure, the peak is broader relative to the metallic Cu reference as seen in Figure 6.2.

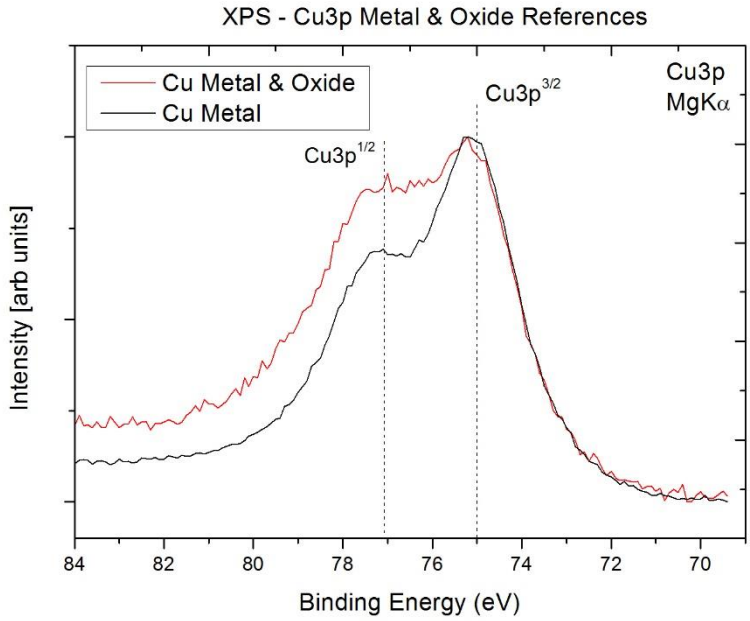

Figure 6.2: XPS Cu 3p spectra of metal Cu and Cu oxide references.

Al2p/Cu3p Fit Parameters	Gaussian	Lorentzian	B.E Position	Doublet Separation	Doniach Sunjic
Al Metal	0.64	0.24	72.9	0.45	0.16
Al Oxide	1.64	0.24	75.55	0.45	N/A
Al Sub-Oxide	0.91	0.24	73.78	0.45	N/A
Cu Metal	1.16	1.63	75	2.4	0.06
Cu Oxide	1.9	1.63	76.67	2.4	0.06

Table 6-1: Peak fitting values derived from reference Al 2p and Cu 3p data.

As can be seen from Table 6-1, three peaks were fitted with an asymmetric peak shape using a Doniach-Sunjic value of 0.16 for the Al metal peak and 0.06 for both metal Cu and Cu oxide. The Al oxide and sub oxide peaks were found to be symmetrical and thus was fitted using a standard Voigt profile. Shirley-Sherwood background corrections were used in all peak fitting analysis, consistent with previous studies [11-13]. The resulting peak fits using the parameters for both elements are shown in Figure 6.3.

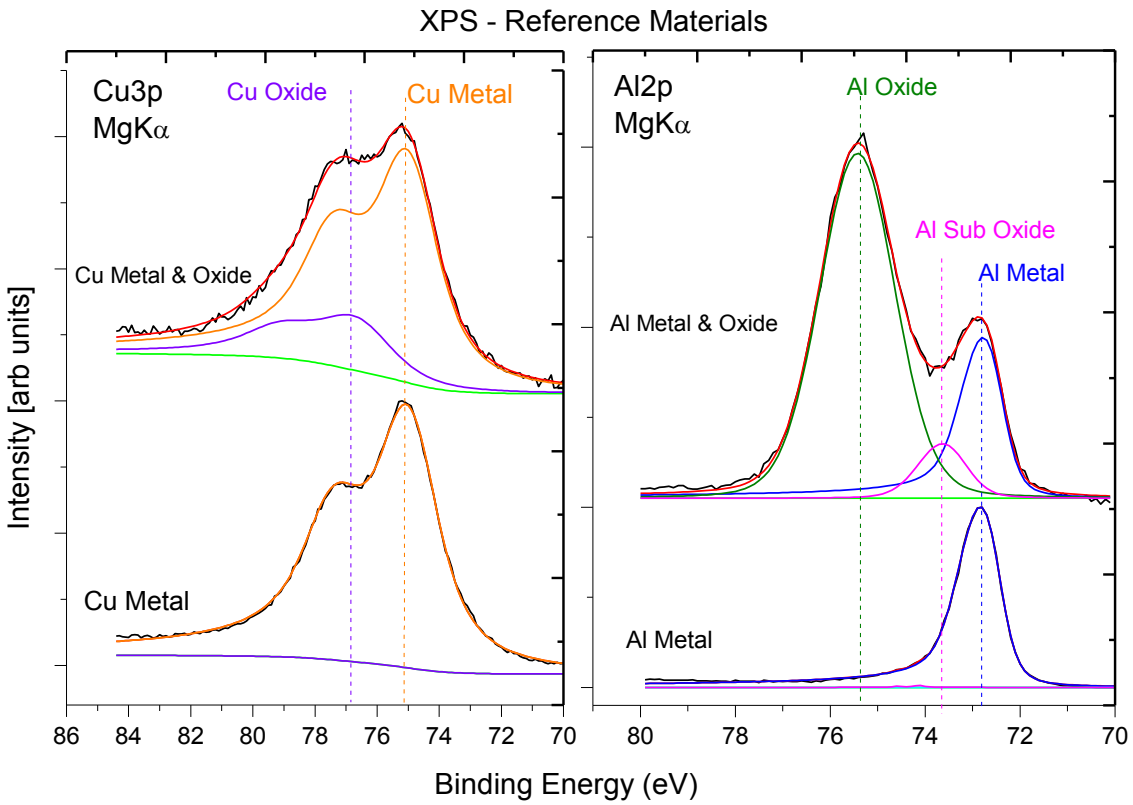

Figure 6.3: XPS peak fitting of reference materials.

6.4 In-situ annealing of CuAl alloy

XPS was employed to study the effect of thermal anneal treatments on the CuAl alloy in order to ascertain if the Al can segregate from the bulk of the alloy towards the surface making it suitable for use in self-forming barrier applications. Once loaded into the UHV environment, XPS was used to analyse the sample in the as loaded state following which it was subjected to a series of anneals within the UHV system and held at the target temperatures for one hour. Figure 6.4 displays survey scans for as loaded and annealed CuAl alloy.

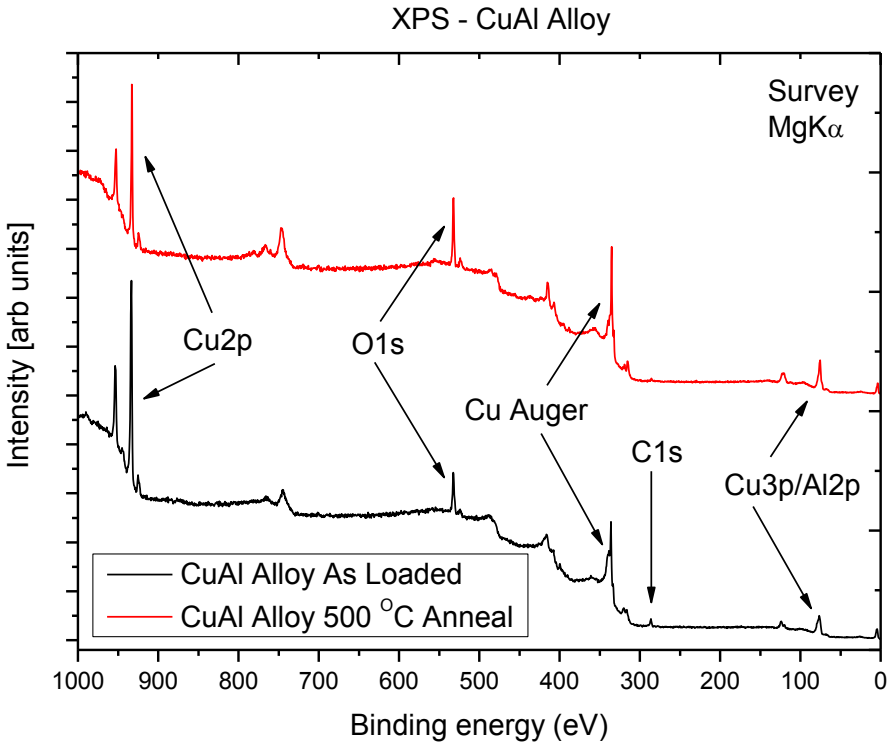

Figure 6.4: XPS survey spectra of CuAl alloy as deposited and annealed.

As can be seen in the as loaded survey scan, the only elements present in the top surface of the alloy are copper, oxygen, traces of aluminium and traces of adventitious carbon. Upon in-situ annealing, a decrease in Cu 2p signal is noted in addition to an increase in oxygen and aluminium signals. A decrease in C 1s signal is also noted following anneal indicating the partial removal of surface contamination. Figure 6.5 displays the Cu 3p/Al 2p photoemission peaks for the as deposited and annealed CuAl alloy.

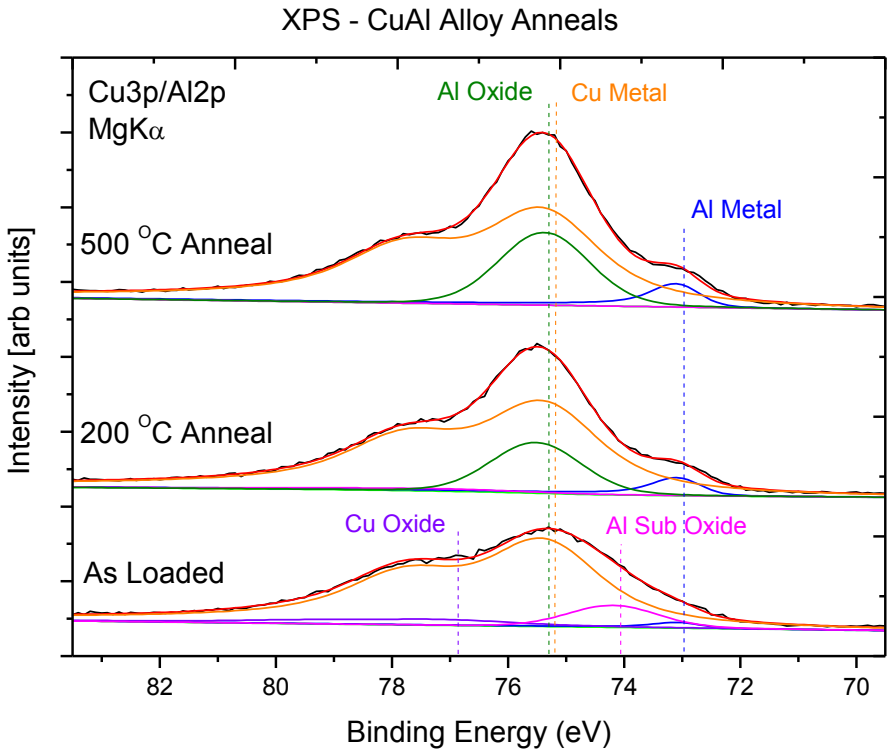

Figure 6.5: Cu 3p/Al 2p XPS narrow window scans as a function of thermal anneal.

All peaks in the Cu 3p/Al 2p windows were fitted using the reference peak fitting values obtained in section 6.3. As can be seen in Figure 6.5, the as loaded state of the CuAl alloy contains Cu metal, Cu oxide and a small quantity of Al in a sub-oxide and metallic state. Upon anneal, the Cu oxide signal vanishes with the concurrent growth of both metallic

Al and Al oxide peaks. This is consistent with the expulsion of Al from the bulk. As the aluminium is expelled through the Cu oxide region, it reduces the Cu oxide to form metallic Cu and Al oxide. It should be noted that growth of Al oxide is also consistent with oxidation of metallic Al within the UHV system due to degassing of sample stub and the high temperatures associated with the in-situ anneal. Figure 6.6 displays the O 1s photoemission peak of the CuAl alloy both as loaded and following anneal stages.

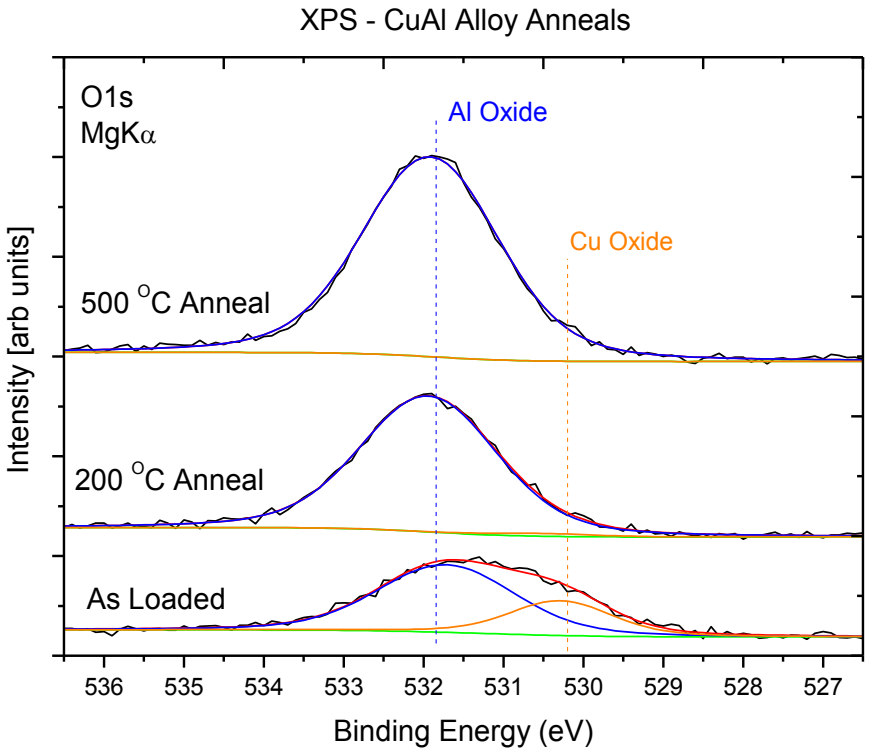

Figure 6.6: O 1s narrow window scan of CuAl alloy as a function of thermal anneal.

As can be seen in the as loaded scan, there exists two O 1s peak components which have been attributed to Cu oxide and Al oxide. Following annealing in the UHV system, the Cu oxide peak is completely attenuated, as seen in the Cu 3p/Al 2p spectra also. The

reduction of Cu oxide in the film is an important point to note as not only does it decrease the resistance of the film, but according to Willis et al [14], it could also inhibit the diffusion of Cu into any surrounding dielectric materials.

6.4.1 HAXPES of CuAl alloy

In addition to conventional XPS, High Energy XPS (HAXPES) measurements were performed at the National Synchrotron Light Source, in Brookhaven Laboratory, USA. The photon energy used in this study was 2200 eV which enabled acquisition of the Al 1s photoemission line which is unobtainable using conventional Mg and Al anodes in XPS systems. Figure 6.7 displays spectra of the Al 1s / Cu 2p and Cu 3p / Al 2p spectra regions for the as loaded and 450 ^{O}C annealed CuAl alloy sample.

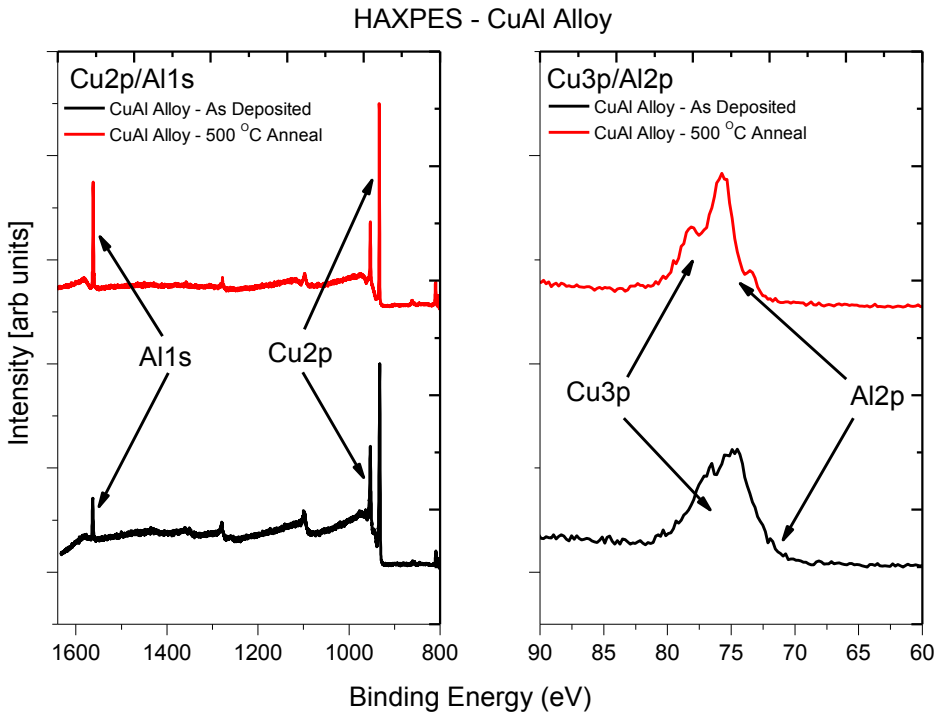

Figure 6.7: High energy XPS of both Al 1s / Cu 2p and Cu 3p / Al 2p core levels of the CuAl alloy as loaded and annealed

The intensity of the Al 1s peak grows following the 450 ^{O}C anneal with respect to the Cu 2p, consistent with segregation of the aluminium from the bulk material. In addition the Cu 3p / Al 2p spectra shows clearer evidence of Cu oxide removal and growth of metallic Al, relative to conventional XPS spectra as seen in Figure 6.5.

6.4.2 Secondary ion mass spectroscopy

Secondary ion mass spectroscopy was used to depth profile the Al concentration at surface of the CuAl alloy both as deposited and annealed in-situ at a temperature of 500 ^{O}C with the data displayed in Figure 6.8.

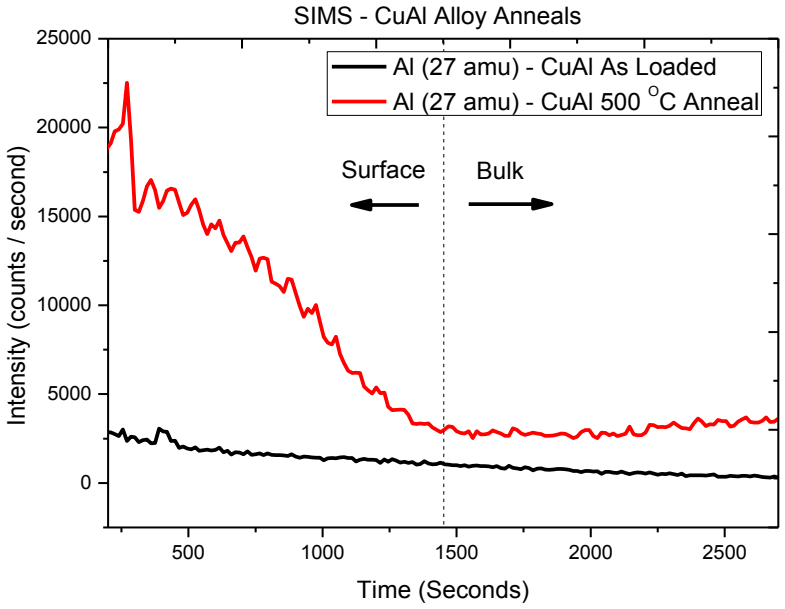

Figure 6.8: SIMS data of CuAl alloy both as deposited and annealed.

As can be seen from the SIMS data for the as deposited CuAl alloy, the Al counts at the surface and into the bulk of the material are almost. This is in contrast to the annealed CuAl alloy which shows a build-up of Al at the surface, which decreases further into the

film. This increase of Al at the surface of the film is in agreement with both the XPS and HAXPES data.

6.5 Barrier formation of CuAl / 3 nm SiO_2

In order to identify evidence of barrier layer formation between the CuAl alloy and a dielectric material it was necessary to probe the chemical interactions between the alloy and a suitable dielectric material. Typical XPS experimentation for the formation of barrier layers via the interaction of a metal and dielectric layer involve the in-situ deposition of metals or semi oxidised metals onto dielectric substrates [15-17], however given that the sampling depth acquisition of XPS in the 10 nm range, and the thickness of the CuAl alloy layers in this study were ~ 100 nm, it was necessary to invert the typical barrier formation. Thus a thin dielectric layer was deposited onto the relatively thick CuAl alloy substrate in order to characterise the barrier layer formation between the CuAl alloy and the over layer dielectric material. Figure 6.9 displays the survey spectra for the 3 nm SiO_2 / CuAl alloy stack both as loaded and following vacuum anneal. As can be seen from Figure 6.9, the as loaded state is similar to the bare CuAl alloy as seen previously but with the addition of both a Si 2p and Si 2s photoelectron peaks as a result of the deposited SiO_2 layer. An increase in the O 1s peak is also noted which is consistent with the dielectric over layer.

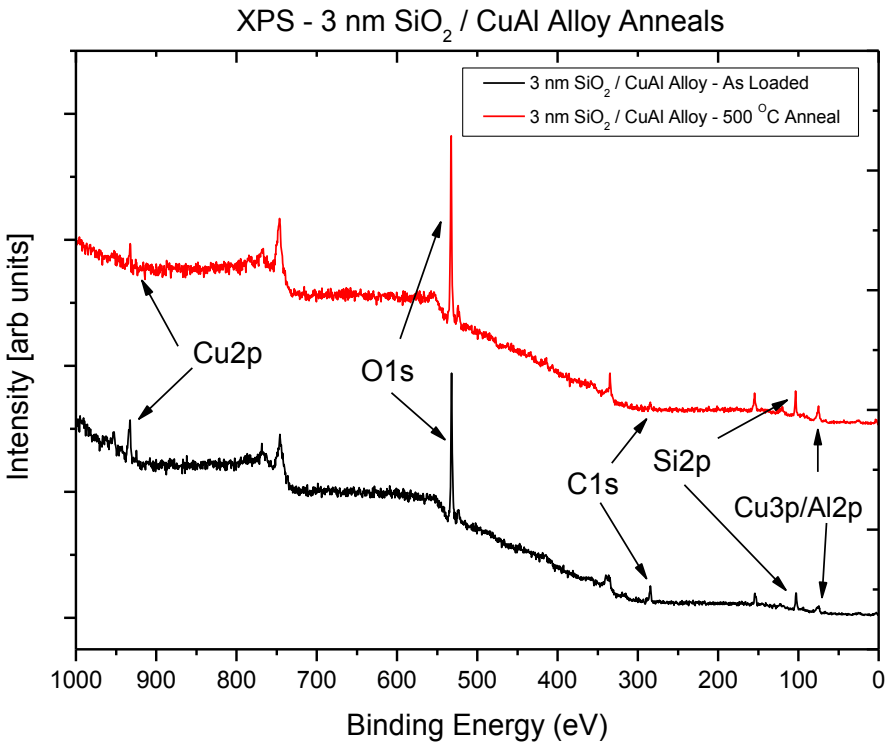

Figure 6.9: Survey spectra of CuAl alloy / 3 nm SiO_2, as loaded and annealed.

The overall intensity from the CuAl alloy substrate is reduced compared to the bare CuAl alloy due to the presence of the dielectric over layer. Following annealing within the UHV system, it is evident from Figure 6.9 that there is a reduction in the intensity of the Cu signal which is consistent with expulsion of Al towards the top surface of the alloy / SiO_2 interface. Figure 6.10 displays the Cu 3p/Al 2p photoemission data for the 3 nm SiO_2 /

CuAl alloy stack for as loaded, 500 ^{O}C anneal and using angularly resolved XPS (ARXPS) at a take-off angle of 50 ^{O} from normal emission.

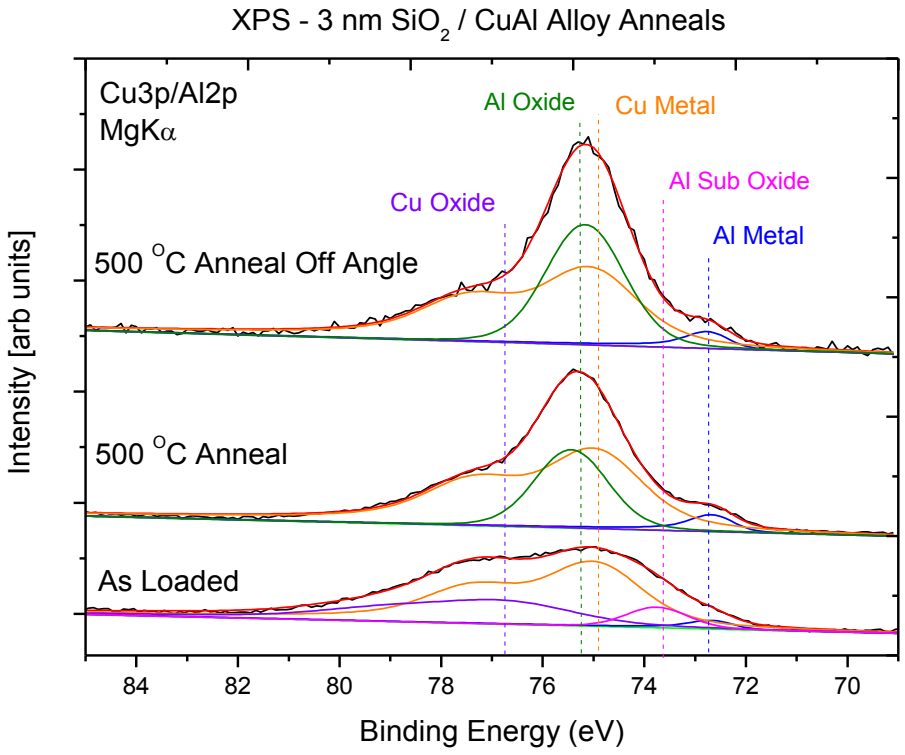

Figure 6.10: XPS of the Cu 3p / Al 2p spectra from the CuAl alloy capped with 3 nm SiO_2 as loaded and annealed.

As can be seen in the as loaded state, the substrate is composed of Cu metal, Cu oxide, Al in a sub oxide state and a limited quantity of Al metal. After a UHV anneal at a temperature of 500 ^{O}C there is an increase in the Al signal as seen by an increase in both the Al oxide peak and Al metal peak intensity. Off Angle scans show that the Al oxide peak is more surface localised than both the metallic Al and metal Cu signal. This is consistent with the formation of barrier layer at the interface of the alloy/dielectric layer, composed of aluminium oxide. Figure 6.11 shows the Si 2p spectra of the SiO_2 / CuAl

alloy stack for as loaded, 500 ^{O}C anneal and 50 ^{O} off angle emission following UHV anneal.

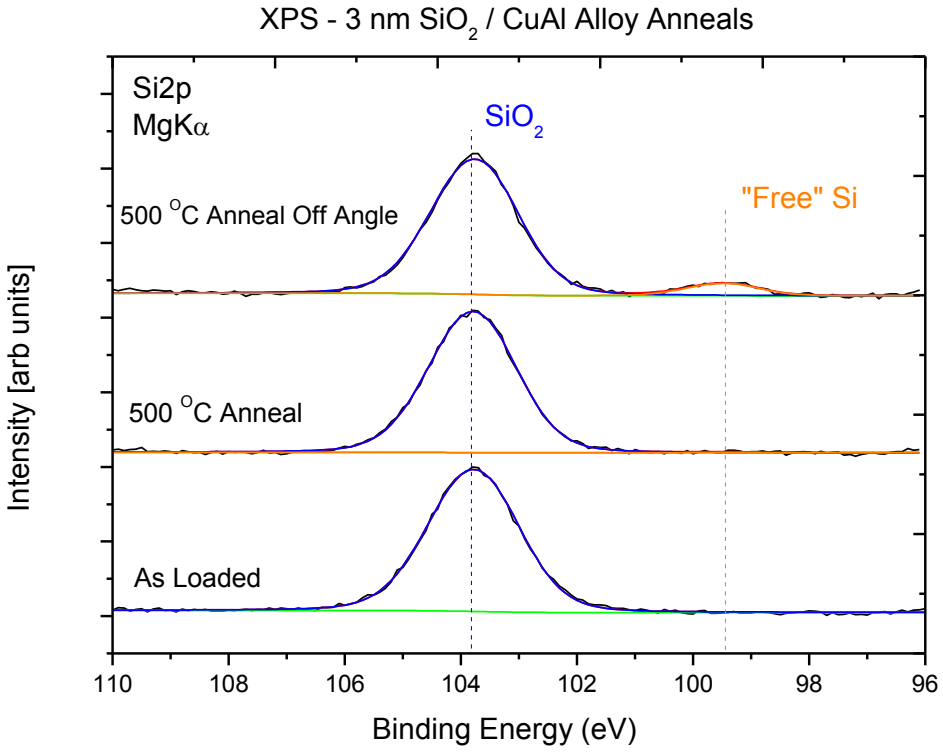

Figure 6.11: XPS Si 2p spectra of 3 nm over layer dielectric on CuAl alloy, as deposited and annealed.

The as loaded spectrum, indicates that the silicon appears to be in a fully oxidised and single chemical state consistent with a SiO_2 layer. Following anneal at 500 ^{O}C, the Si 2p peak appears unchanged, however when examined off angle, a lower binding energy component peak emerges at 99.3 eV binding energy, consistent with the formation of "free" (non-bonded) Si. This additional peak was not seen in off angle scans of the as loaded sample (not shown), and thus has been attributed to be as a result of the annealing process. Previous studies on the interaction of in situ deposited metallic aluminium with SiO_2 dielectric layers which were brought through a series of UHV anneals reveal that

the aluminium chemically interacts with the dielectric layer, reducing the SiO_2 to form aluminium oxide and "free" Si [7][18]. Thus, examining the above "free" Si peak in relation to this experiment, the following argument can be made. As seen in previous sections, Al migrates from the CuAl alloy bulk towards the interfaces of the bulk, including the top most surface. As the Al migrates toward the surface, it reduces the Cu oxide at the surface to form Al oxide. However an Al oxide layer is also formed at the interface, by reduction of the SiO_2 with the resulting release of free silicon.

6.6 Electrical characterisation of CuAl alloy

6.6.1 Four point probe measurements

Four point probe measurements were used to study the resistance of both CuAl alloy blanket layers and pure Cu layers (used as a reference material) for a range of vacuum anneal temperatures. Samples were annealed in vacuum at pressures better than $1x10^{-6}$ mbar with the samples being held at the target temperature for one hour. Figure 6.12 displays the four point probe data for both the CuAl alloy and pure Cu blanket layers which were subjected to anneal treatments in vacuum conditions.

Table 6-2 displays the sheet resistance values from the four point probe data, derived from Figure 6.12. As can be seen in Table 6-2, the Cu film decreases in sheet resistance from 0.029 Ω/sq to 0.022 Ω/sq, which is calculated to be a 25% reduction in resistance following vacuum annealing at 500 ^{O}C. This decrease in sheet resistance is consistent with the crystallisation of the Cu film, acting to increase the conductivity of the film by reduction of electron scattering sites [19]. CuAl alloy resistance values are shown to decrease from an as deposited value of 0.23 Ω/sq to 0.12 Ω/sq following annealing at 500 ^{O}C in vacuum, calculated to be a 50% decrease in sheet resistance.

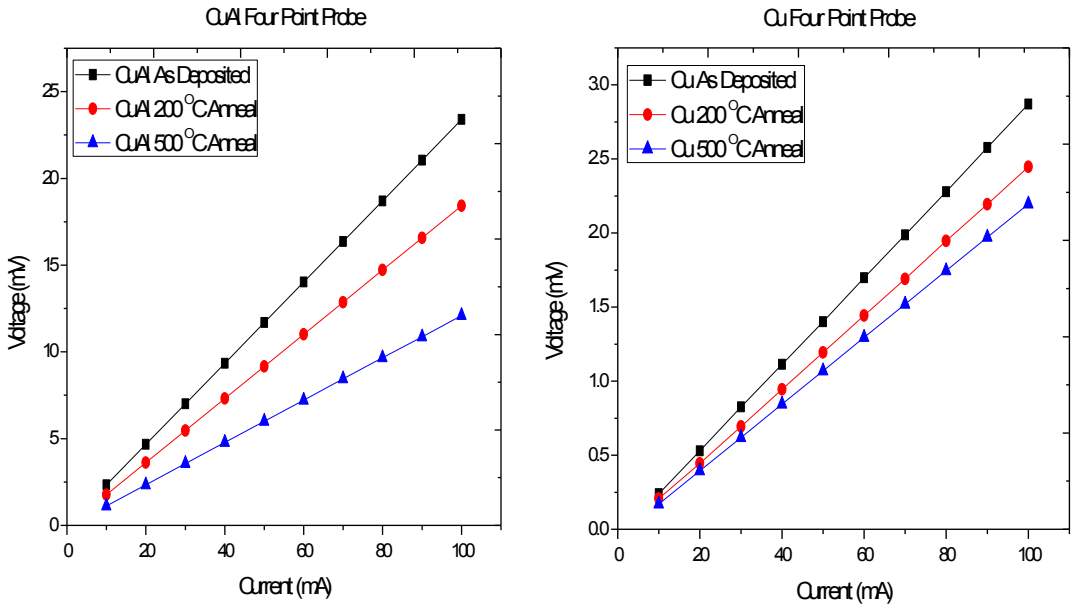

Figure 6.12: Four point probe data for CuAl alloy and Cu blanket layers, as deposited and annealed.

As with the pure Cu film, a drop in sheet resistance is expected due to crystallisation of the film, however a larger decrease in resistance is noted for the CuAl alloy relative to the Cu film. This larger decrease in resistance is consistent with the expulsion of Al from the alloy bulk, which acts as an impurity, causing a larger sheet resistance in the as deposited film [20]. Once the Al begins to be expelled from the alloy bulk, there is less impurity within the bulk and thus a larger decrease in sheet resistance is noted relative to the Cu reference.

A larger resistance overall of the CuAl alloy relative to the pure Cu film is noted (~ 10X increase in resistance). This high resistive property of the alloy would potentially negate any benefit of using it as an interconnect metal due to the fact that it would increase the

RC time delay of any interconnect scheme it was utilised in. Thus this alloy material may instead be used as a thin Cu electrodeposition seed layer and / or a capping layer for metal interconnect structures; thereby allowing maximum fill of pure Cu metal in the interconnect whilst still maintaining the benefits of the alloy properties at the critical interfaces.

Four Point Probe	**Cu**	**CuAl Alloy**
As Deposited	0.029 Ω/sq	0.23 Ω/sq
200 ^{O}C Anneal	0.024 Ω/sq	0.18 Ω/sq
500 ^{O}C Anneal	0.022 Ω/sq	0.12 Ω/sq

Table 6-2: Resistance measurements derived from four point probe data.

6.6.2 Capacitance voltage measurements

PECVD deposited SiO_2 dielectric with a thickness of 100 nm on n-type Si substrates were used to fabricate capacitor structures which were subjected to vacuum anneal treatments in order to electrically characterize the effect of the alloying element Al in the Cu bulk while using pure Cu and Al metal gates as references. It is known that the flatband position of a MOS structure under CV analysis is dependent on the difference in workfunction of the metal gate and silicon substrate. Figure 6.13 shows capacitance voltage scans of all three MOS variants both before and after a 500 ^{O}C anneal in vacuum at a pressure better than $1x10^{-6}$ mbar. Trapped charge in the oxide is noted in the as deposited samples which is attributed to damage caused by sputter deposition of the metal gates manifesting as a smearing of the CV profiles. Following a vacuum anneal at 500 ^{O}C

the sputter damage is removed, leaving a sharp transition between accumulation, depletion and inversion regions.

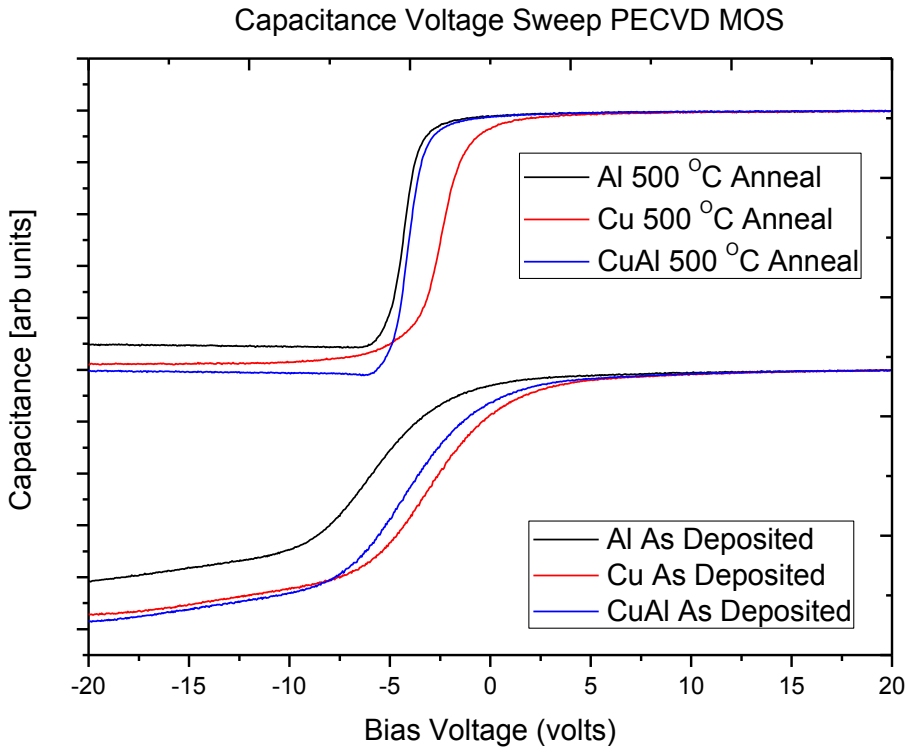

Figure 6.13: Capacitance voltage sweeps of MOS structures with Cu, Al and CuAl alloy gates both before and after vacuum anneal

As can be seen for the as deposited samples both the Cu and CuAl alloy have similar flatband voltage positions and characteristics, mainly due to the fact that the CuAl alloy is 90% Cu and 10% Al, as seen in previous studies [3]. Following vacuum annealing, a shift in the flatband voltage position of the CuAl alloy in noted from a more Cu like value to a more Al like value. This shift in flatband is consistent with the migration of Al from the CuAl bulk towards the metal/dielectric interface, modifying the difference in work function between the metal gate and n-type Si substrate, manifesting in a flatband shift to pure Al like values, similar to the result was reported Tsui et al on the work involving

binary alloys [21]. This is consistent with both XPS and HAXPES results indicating that at elevated temperature, Al is expelled from the alloy bulk towards all interfaces of the bulk metal.

6.7 Transmission electron microscopy

Transmission electron microscopy (TEM) was used to image the Cu and CuAl alloy layers both as deposited and following a 500 ^{O}C anneal in vacuum. Figure 6.14 displays the cross sectional TEM images of (a) pure Cu and (b) CuAl alloy following the 500 ^{O}C anneal in vacuum.

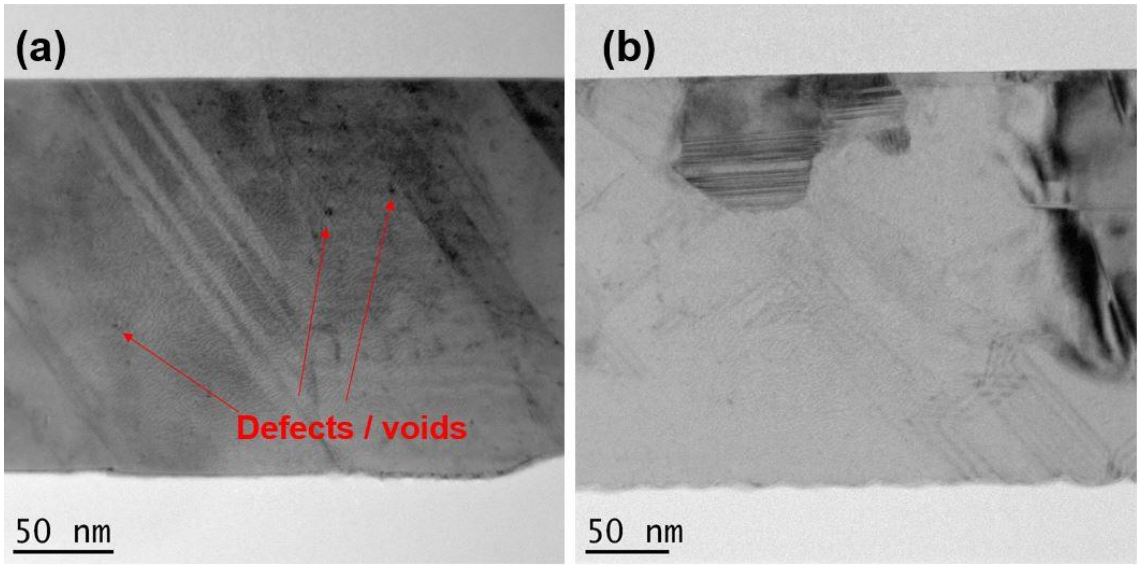

Figure 6.14: TEM images of (a) pure Cu and (b) CuAl alloy following a 500 ^{o}C anneal in vacuum.

As can be seen from the pure Cu film in (a), defects which appear as voids in the film are visible. When the CuAl alloy image (b) is examined, no such pin holes or defects are observed within the film. This result indicates that at low dimensions of interconnect lines, pin holes or voids in a pure Cu line could be problematic, however these appear to not be an issue using the CuAl alloy. Figure 6.15 displays TEM images of the CuAl alloy both (a) as deposited and (b) vacuum annealed at 500 ^{O}C for one hour. As can be seen in

the TEM image of the as deposited CuAl alloy (a), there is an abrupt interface between the two distinct regions attributed to the CuAl alloy and SiO_2 dielectric layer. When the vacuum annealed CuAl alloy interface image (Figure 6.15 (b)) is examined there appears to be an interfacial layer which is consistent with barrier formation [22].

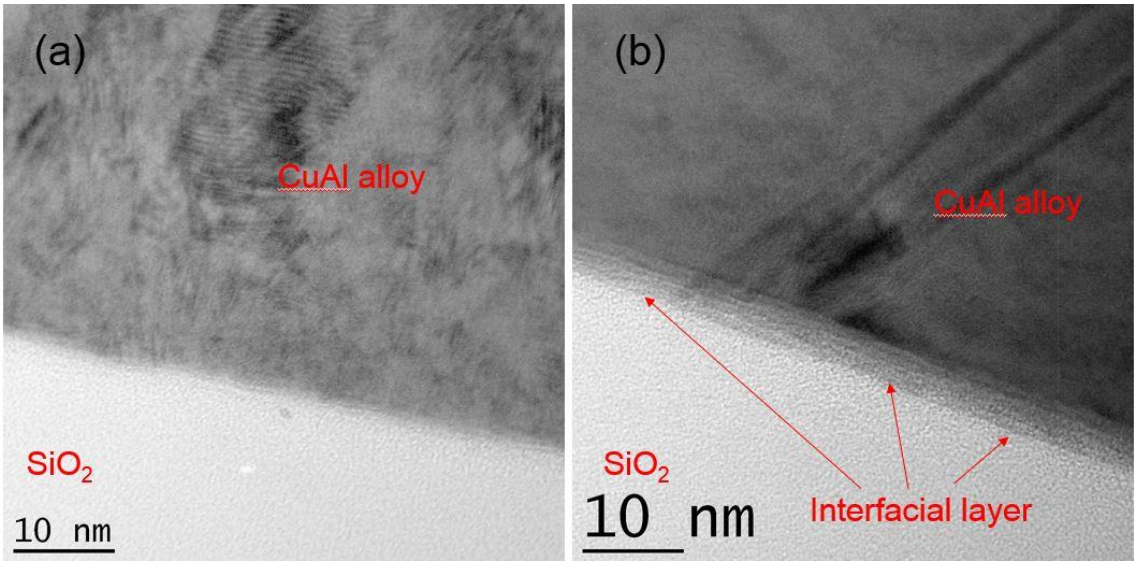

Figure 6.15: TEM cross sectional images of CuAl alloy (a) as deposited and (b) 500 ^{O}C annealed in vacuum.

Figure 6.16 displays TEM images of the pure Cu film at the metal / oxide interface following vacuum anneal at 500 ^{O}C for one hour. As can be seen from the 50 nm scale image of Figure 6.16 (a), a rough interface is noted with the addition of small protrusions into both the Cu layer and oxide region. The red circle marked area in image (a) is the area shown in image (b). This region shows particular intermixing of the two layers to a thickness of ~ 5 nm. This intermixing and roughening of the interfacial region between the metal Cu layer and the SiO_2 oxide layer is consistent with the diffusion of Cu into the oxide layer following vacuum anneal at 500 ^{O}C.

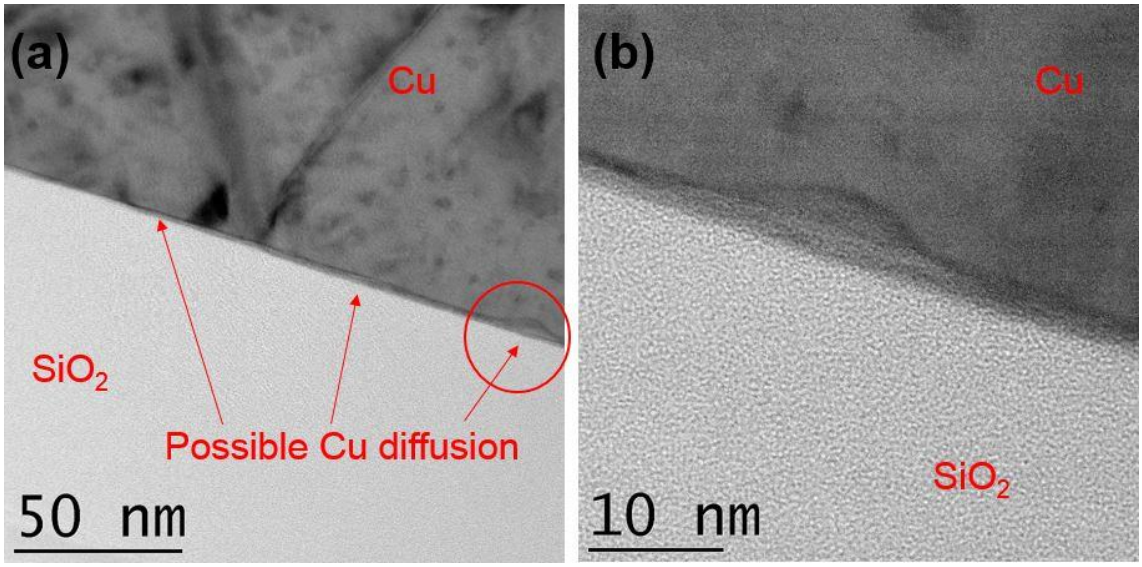

Figure 6.16: TEM imaging of the pure Cu / SiO2 interface following 500 ^{o}C vacuum anneal.

In addition to bright field imaging, high angle annular (HAADF) TEM images were taken in order to characterise this interface further. HAADF images are more sensitive to the z-ratio of the sample, in other words they are very sensitive to the elemental composition within the image, with high mass elements appearing brightest compared to low mass elements which will appear darker. HAADF TEM imaging of the Cu metal / SiO_2 oxide interfacial region following 500 ^{O}C vacuum anneal are presented in Figure 6.17. The same region was simultaneously imaged in bright field (BF) (a) and HAADF mode (b) in order to gain additional information at the metal / oxide interfacial region.

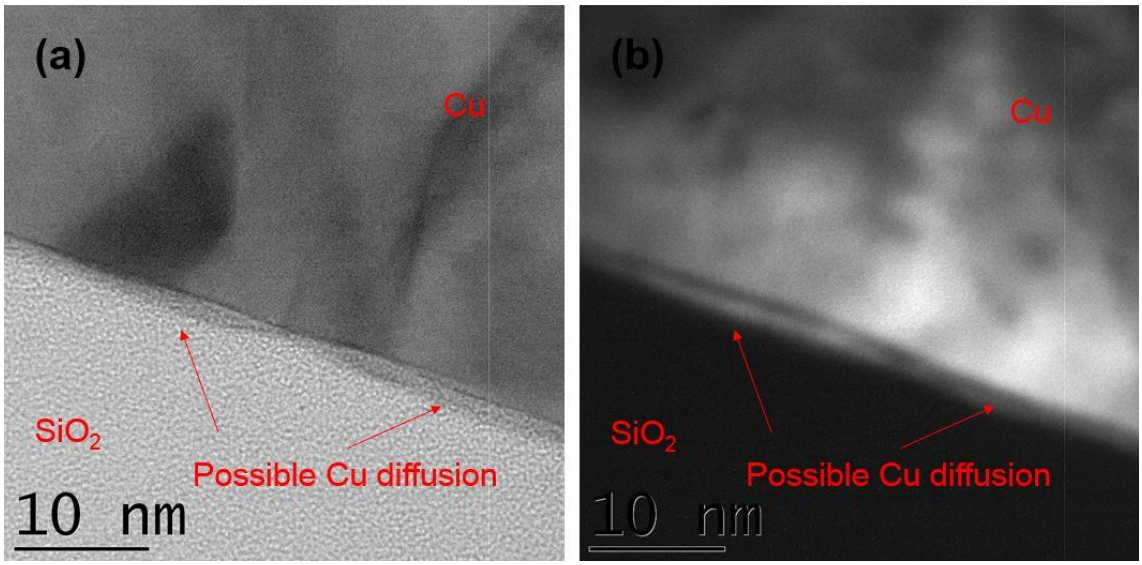

Figure 6.17: TEM imaging of Cu / SiO2 interface using (a) bright field and (b) high annular angle dark field imaging.

As can be seen in Figure 6.17 (a), the BF TEM image shows possible diffusion of Cu metal into the SiO_2 region of the interface. When the HAADF image of the same region (Figure 6.17 (b)) is examined, it is seen that the Cu metal layer appears brighter relative to the dark region associated with the SiO_2 layer. When the interface at the Cu / SiO_2 region is examined further, bright areas are seen to be apparently diffused into the oxide region. These bright areas match the position of the possible Cu diffusion areas of Figure 6.17 (a), which is the BF image counterpart to Figure 6.17 (b). This result strongly suggests that Cu has diffused into the top most region of the oxide layer following vacuum anneal at 500 ^{O}C. No such Cu diffusion was seen in the CuAl alloy interface both as deposited or vacuum annealed. In contrast to the pure Cu vacuum annealed sample, an interfacial layer is seen to have formed in the CuAl alloy sample post anneal in vacuum. This layer is attributed to a self-forming barrier which, as seen in TEM results to have prevented the diffusion of Cu into the dielectric layer.

6.8 Conclusions

A CuAl alloy has been investigated for use in BEOL interconnect schemes. XPS peak fitting analysis was used to successfully peak fit reference metal Cu, metal Al, Cu oxide and Al oxide reference spectra in order to accurately peak fit the complex overlapping peaks associated with the CuAl alloy. XPS analysis of the CuAl alloy which was annealed in-situ shows the presence of additional Al at the surface of the alloy, consistent with the segregation of the alloying element form the bulk material. HAXPES spectra was used to probe the Al 1s core level, which does not overlap with any other photoemission peaks in the spectra, conclusively showing the increase of Al at the surface of the CuAl alloy upon thermal anneal treatments. SIMS measurements of the surface of the CuAl alloy both as deposited and annealed also indicate a build-up of Al at the surface of the material. An ultra-thin over layer of SiO_2 deposited onto the surface of the CuAl alloy was used to successfully induce an interaction between the Al which was expelled during thermal anneal and the over layer, consistent with the process of a self-forming barrier. Additional four point probe data shows a larger decrease in resistance of the CuAl alloy relative to a pure Cu film, consistent with previous results of expulsion of the alloying element form the metal bulk. Capacitance voltage analysis of MOS structures with Cu, Al and CuAl alloy gates were analysed both as fabricated and vacuum annealed. A shift in flatband capacitance of the CuAl form more Cu like values to more Al like values was noted, consistent with the migration of Al towards the metal / ILD interface, indicating as in previous results that the alloying element not only migrates to the top surface but also to the underlying surface, where a self-forming barrier process can take place. Finally TEM images of Cu and CuAl alloy layers both as deposited and annealed indicate that Cu had diffused into the top region of the oxide layer in the pure Cu sample following vacuum anneal treatment at 500 ^{O}C. In contrast to the pure Cu sample, the CuAl alloy sample

shows the formation of an interfacial region between the metal and oxide layer post vacuum anneal. This layer has been attributed to the self-forming barrier mechanism of Al which migrated to the oxide interface following vacuum anneal where it chemically reacted with the oxide layer forming a stable Al oxide barrier which could potentially prevent cu diffusion into the oxide region.

Thus, the experimental work in this chapter has shown that a CuAl alloy (90:10 % wt) can function as a seed layer in BEOL processes for interconnect applications. The expulsion of Al from the metal bulk allows Al to migrate up into a Cu line which can be deposited onto the alloy seed layer, thereby improving electromigration aspects of a Cu interconnect structure. As stated in the introduction a number of criteria must successfully be met, which have shown to be satisfied by the CuAl alloy including:

(a) Expulsion of the alloying element (Al) from the bulk material following anneal treatments.
(b) Interaction of the expelled Al with a dielectric material, consistent with a self-forming barrier process.
(c) Passivation of the surface of the film via oxidation of the alloying element at the surface of the film.

Further criteria needed to be satisfied including (d) good adhesion of the material to any surrounding ILD layers, including low surface roughness and (e) prevention of Cu diffusion into any surrounding ILD material will be outlined in the following chapter.

6.9 References

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7 CuAl alloy barrier layer properties for future Interconnect applications

7.1 Introduction

Prevention of Cu diffusion into the surrounding ILD material is of major importance for future BEOL processes in IC production [1,2]. As stated previously, the current Ta/TaN barrier stack will become too bulky in future iterations of interconnect technologies [3]. Self-forming barriers have been proposed as an alternative to the relatively bulky Ta/TaN barrier currently in use [4-8]. In addition adhesion between the Cu line and surrounding ILD material must be strong in order to decrease delamination of any metal / dielectric layers [9]. Roughness of the film must also be kept to a minimum due to the aggressive scaling of devices, which can be compromised by large roughness values of materials [10]. As seen in the previous chapter, a CuAl (90:10 % wt) alloy displays a number of properties which could make it suitable for integration into BEOL IC fabrication strategies. The main points of note included:

(a) The expulsion of Al from the alloy bulk upon thermal anneal.

(b) Self-forming barrier reaction between the expelled alloy and a SiO_2 layer.

(c) Surface passivation of the film due to oxidation of the Al which acts to prevent oxidation of the Cu within the material.

In addition to the above benefits, further properties must also be studied if this material system is to be considered to future integration within BEOL structures, these include:

(d) Good adhesion between the metal layer and any surrounding dielectric material, in addition to low surface roughness.

(e) Prevent Cu diffusion into any surrounding dielectric material.

The last two properties, both (d) and (e) will be explored in this chapter.

7.2 Experimental details

In addition to blanket films of Cu and CuAl alloy as introduced in the previous chapter, a number of metal oxide semiconductor (MOS) devices were fabricated using lift off lithography. These MOS devices were fabricated using PECVD and thermally grown SiO_2 layers with a thickness of 100 nm on n-type <100> Si substrates. Cu, Al and CuAl alloy gates were sputter deposited through photoresist pattern defined features on each substrate yielding MOS gate structures. These MOS devices were then electrically tested via capacitance-voltage (CV) sweeps and leakage current-voltage sweeps (IV). Stressing of MOS devices was undertaken in two separate experiments, the first consisting of a bias thermal stress (BTS) test whilst the second stress being a purely thermal stress, both stress procedures are explained in detail in chapter 3. All MOS structures studied received a 500 ^{O}C anneal in vacuum at pressures better than $1x10^{-6}$ mbar in order to remove sputter damage to the oxide layers which occurred during metal gate deposition and also to "activate" the alloying element Al in the CuAl alloy to segregate from the bulk to all surfaces including the underlying dielectric interface, as seen in chapter 6.

7.3 Bias Thermal Stress of Cu & CuAl alloy MOS devices

Bias thermal stress (BTS) testing of MOS devices was undertaken in order to test the effectiveness of the CuAl alloy at preventing Cu diffusion into the underlying dielectric material. A pure Cu sample was used as a reference to demonstrate failure due to Cu diffusion into the underlying dielectric material whilst subjecting the CuAl alloy to identical stress parameters in order to test the effectiveness of the alloy at preventing Cu diffusion. It should be noted that multiple devices were tested, but for clarity only one

data set for one device per sample is shown due to the fact that all samples displayed similar results. BTS stressing is a particularly relevant experiment to perform when investigating the barrier performance of a material. This is due to the fact that both an electric field and temperature are applied to the device simultaneously, similar to operating temperatures and electric fields experienced by an IC chip during operation. In this study the temperature ranged from room temperature to 100 ^{O}C, which is typically the maximum temperature of operation. Applied voltages on the gate of the MOS structures were + 5 V (similar to chip operation voltages) and + 10 V in order to maximise the stress to the device. Figure 7.1 displays the stages over the course of BTS experimentation.

The initial stage comprises of a CV and IV sweep in order to establish the initial quality of the MOS device. Following initial characterisation a BTS step consisting of applying a bias voltage at room temperature is performed. The bias voltage used is + 0.5 MV/cm, which equates to + 5 V for the 100 nm PECVD SiO_2 substrates used in this study, with the positive voltage being applied to the gate of the MOS structure in order to drive any Cu^+ ions into the dielectric material. The bias period lasts for 600 s, during which the leakage current through the MOS device is also recorded. Following the bias stage, a second set of CV and IV sweeps are taken in order to track any resulting changes. Further stages of biasing using either elevated temperature and / or electric field are then carried out on the MOS device (again with the leakage current being recorded during biasing) in addition to CV and IV data being recorded after each stage. It should also be noted that the dielectric of choice for these MOS structures was a PECVD deposited SiO_2. Due to the deposition method of the dielectric layer in the MOS devices, a large amount of trapped charge is seen within the CV profiles. This however is found to be acceptable as

all devices tested exhibited clear accumulation, depletion and inversion regions, with the only non-ideal MOS trait seen as a shift of flatband voltage from 0 V to negative values.

Figure 7.1: Bias temperature stress (BTS) test stages.

7.3.1 BTS of Cu reference MOS

Figure 7.2 displays CV data from a pure Cu MOS device over the course of BTS testing. As can be seen via the initial CV trace, the MOS device appears stable with clear accumulation, depletion and inversion regions seen in the sweep.

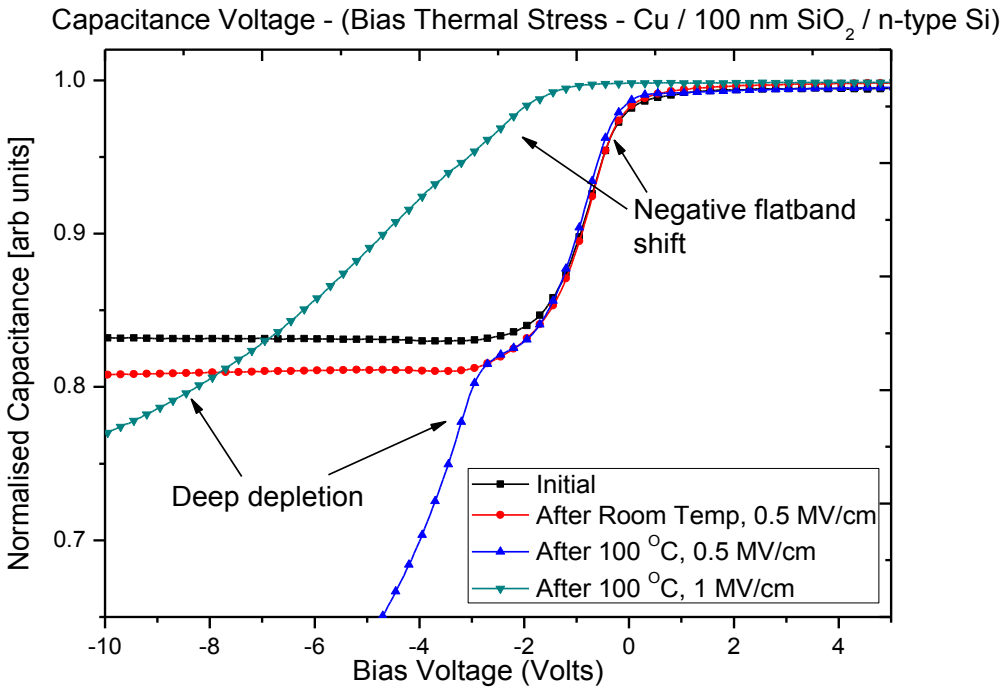

Figure 7.2: CV data for pure Cu MOS during BTS testing.

Following the various BTS stages, as outlined in Figure 7.1, it is seen that the CV profile degrades. This degradation can be seen as both a shift of flatband voltage position to

negative values, in addition to "deep depletion" activity, a phenomenon which occurs when no inversion region can be observed in the CV profile. Leakage current (IV) measurements on the MOS device was also recorded after each BTS stage and are presented in Figure 1.3. As can be seen via the initial IV sweep, low levels of leakage are seen with the leakage current in the $1x10^{-11}$ A range. Following the various BTS stages, degradation of the device is noted with a maximum leakage current value following the final 1 MV/cm at 100 ^{o}C BTS stage of ~ $1x10^{-4}$ A.

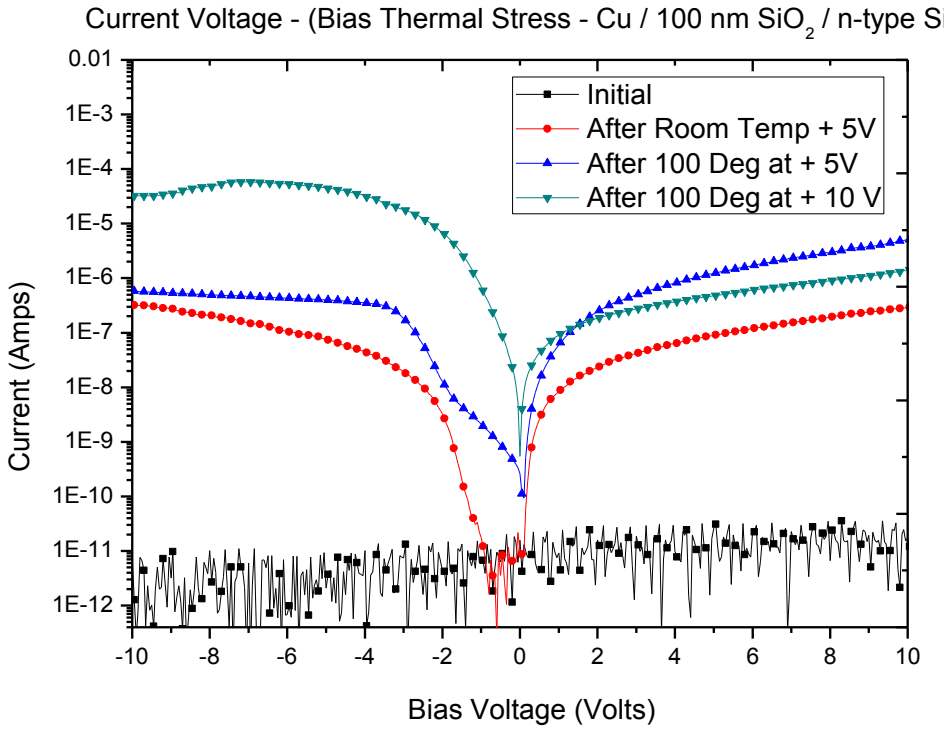

Figure 7.3: IV leakage current data for pure Cu MOS during BTS testing.

As stated previously, when a bias is applied to the gate of the MOS devices during BTS, the leakage current through the device can be measured. The leakage current during stressing for the pure Cu MOS device is shown in Figure 7.4. The first BTS stage of stressing with an applied bias of + 0.5 MV/cm on the Cu gate at room temperature shows

negligible leakage current. Throughout the remaining stress stages at 0.5 MV/cm and 1 MV/cm, the leakage current increases with each subsequent stress stage at 100 ^{O}C. The maximum current noted is during the 600 second stress of 1 MV/cm at 100 ^{O}C was ~ $4x10^{-4}$ A.

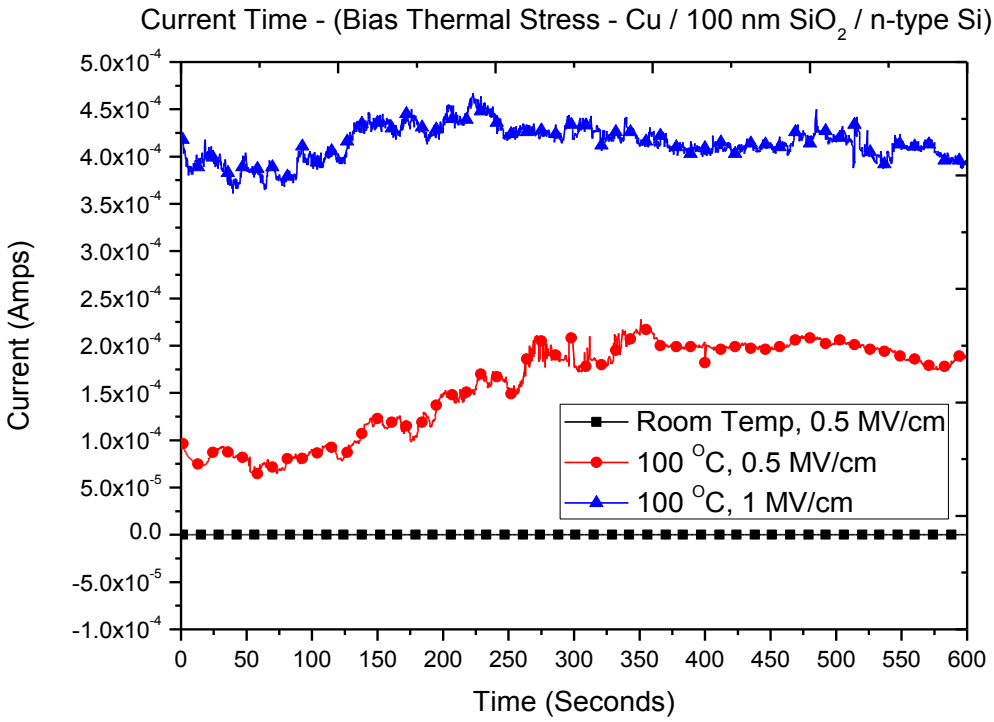

Figure 7.4: Leakage current for pure Cu MOS during device stressing.

The results obtained with BTS experimentation of pure Cu MOS devices as shown above are consistent with the diffusion of Cu into the underlying dielectric material during BTS [11-13]. Temperature appears to have a detrimental effect on the leakage current of the MOS device, as indicated by the low levels of leakage at room temperature in contrast to the higher levels of leakage (eight orders of magnitude increase) using the same 0.5 MV/cm bias at a heightened temperature of 100 ^{O}C.

7.3.2 BTS of CuAl alloy MOS

Figure 7.5 displays CV profiles for the CuAl alloy MOS structure over the course of BTS testing. As can be seen from the initial CV trace, the MOS device exhibits stable characteristics with clear accumulation, depletion and inversion regions.

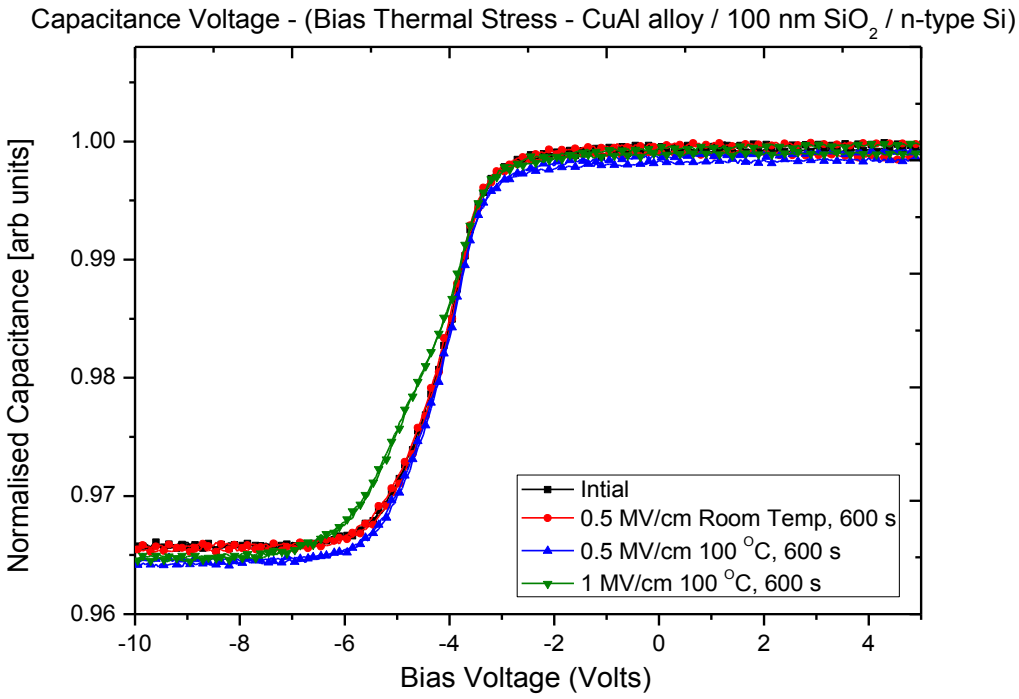

Figure 7.5: CV data for CuAl MOS during BTS testing.

Throughout the course of the BTS testing, the CV sweeps remain stable, even after the maximum step of 1 MV/cm at 100 ^{O}C which resulted in severe degradation of the pure Cu MOS structures. It should be noted also that a slight stretching of the CV profile is seen in the CuAl MOS following the 1 MV/cm at 100 ^{O}C BTS stress stage. This slight behaviour has been reported in previous BTS studies and has not been attributed to any failure due to Cu diffusion into the underlying dielectric material [14]. Figure 7.6 displays the IV leakage current data for the CuAl MOS over the course of BTS testing.

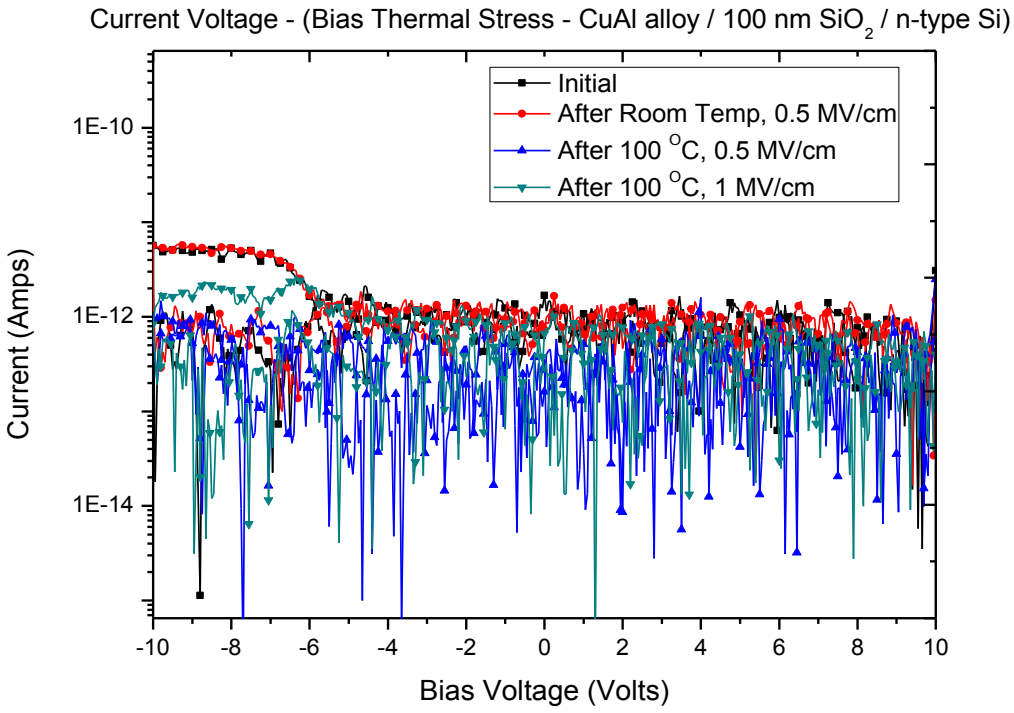

Figure 7.6: IV leakage current data for CuAl MOS during BTS testing.

As can be seen from the initial to final IV taken after the maximum stress stage, the leakage current remains low, ~ $1x10^{-12}$ A which is the limit of the current sensing of the Keithley 4200 used in this study. This result is in direct contrast to the pure Cu MOS which shows severe leakage current throughout the course of the BTS testing. Figure 7.7 displays the corresponding leakage current through the CuAl alloy MOS device during the bias temperature stress stages of 0.5 MV/cm at room temperature and both 0.5 MV/cm and 1 MV/cm at 100 ^{O}C which again shows no significant increase in leakage is detected throughout the measurement sequence.

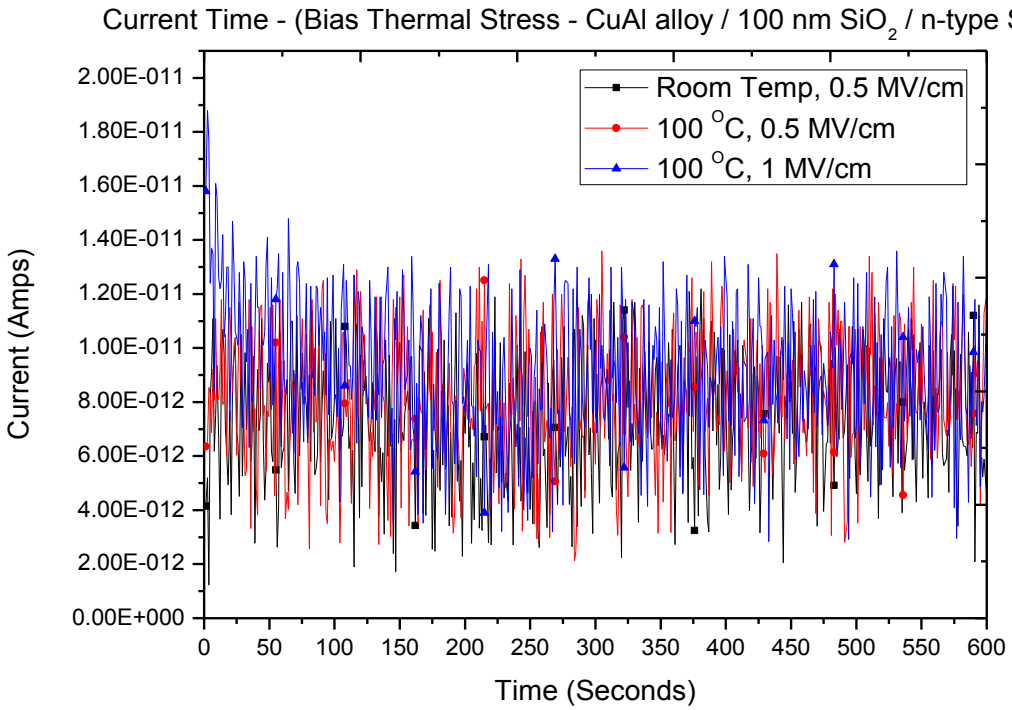

Figure 7.7: Leakage current for pure CuAl MOS during device stressing.

The stability of the CV data, in combination with both low current leakage levels during and after each stress stage indicate that the CuAl alloy is stable over the course of the BTS testing. This indicates that no Cu has diffused into the dielectric layer of the MOS device, in contrast to the pure Cu reference, which exhibits negative voltage flatband shift in the CV profiles, in addition to high levels of leakage both during and after each stress stage, which is consistent with the diffusion of Cu into the dielectric layer of the pure Cu reference MOS device.

7.4 Thermal stressing of Cu and CuAl alloy MOS

As seen in section 7.3, pure Cu MOS devices were shown to exhibit failure following BTS testing, consistent with the diffusion of Cu into the dielectric of the MOS device. This is in contrast to the CuAl alloy MOS devices which exhibit no such Cu diffusion characteristics. In order to test the CuAl alloy further, pure thermal stress treatments were performed in a tube furnace within a class 1000 clean room with both the pure Cu reference MOS and CuAl alloy MOS devices undergoing thermal stressing. In order to avoid unwanted charges within the oxide layer, a thermally grown SiO_2 layer was used instead of the PECVD deposited SiO_2 layer, as used in the BTS testing, which exhibited far less trapped charge, yielding very near to ideal MOS characteristics prior to thermal stressing. Both N_2 gas flow and atmospheric anneals were used to thermally stress the MOS devices up to a maximum temperature of 500 ^{O}C, with an initial vacuum anneal of 500 ^{O}C used for all samples, as stated in section 7.2 with all samples being held at the target temperature for one hour. As with the BTS results, large numbers of devices and samples were tested (>10); however for clarity only one set of data for each sample is shown due to the fact that all devices showed similar behaviour across the sample set. All CV profiles were recorded following a + 10 V hold for 300 s on the gate of the MOS structure in order to bias any mobile ions towards the Si / SiO_2 interface.

7.4.1 Pure Cu reference MOS thermal stress

Figure 7.8 shows CV profiles for the pure Cu MOS sample throughout the course of the thermal stress tests. As can be seen from the initial CV profile following the 500 ^{o}C vacuum anneal, the CV profile exhibits no hysteresis or other non-ideal MOS traits.

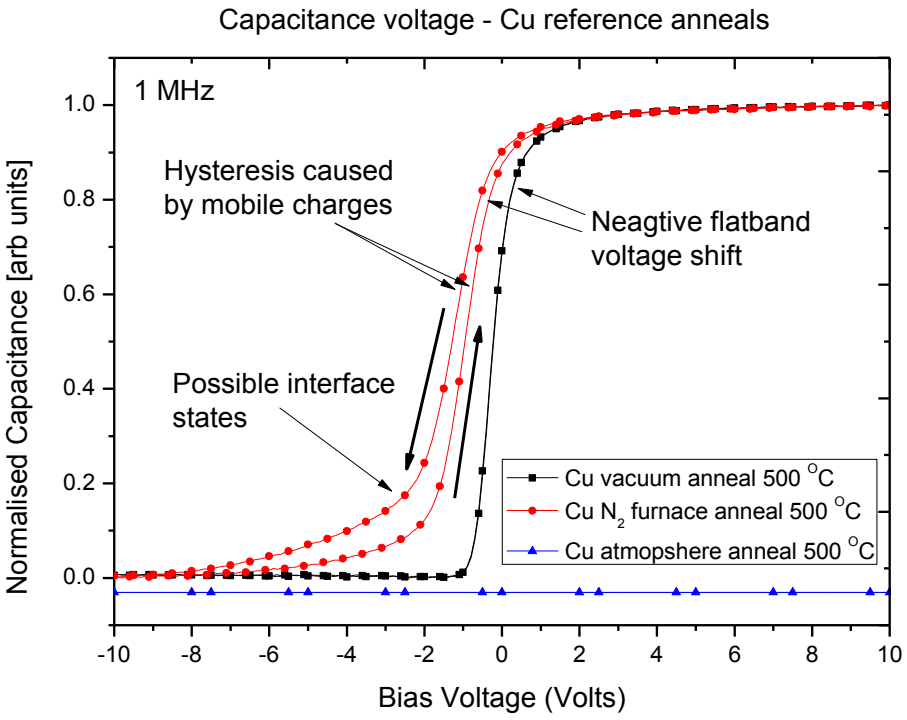

Figure 7.8: CV profiles of pure Cu reference MOS throughout thermal stress testing.

Following initial electrical characterisation, the Cu reference sample was annealed in the tube furnace within a class 1000 clean room at a temperature of 500 ^{O}C under N_2 flow. Following this anneal the CV profile shifts to negative voltage values in addition to the introduction of hysteresis within the profile. On closer examination a more extended transition from depletion to inversion regions within the CV profile could indicate the existence of interface states at the Si / SiO_2 interface. A final anneal at a temperature of 500 ^{O}C was then performed in the same furnace, with the exception that this anneal was performed in atmospheric conditions. Following this anneal stage it was not possible to read any capacitance values from the Cu gates which appeared heavily oxidised and were beginning to delaminate from the SiO_2 substrate in large flakes. Figure 7.9 displays the leakage current through the pure Cu reference MOS throughout the course of the thermal

stressing. In contrast to the BTS testing, the initial current is low (~ $1x10^{-12}$ A) and remains low following both the N_2 and atmosphere anneals at 500 ^{O}C. As stated previously, the atmosphere anneal caused delamination of the gate material, and thus reliable electrical contact could not be made to the MOS gate.

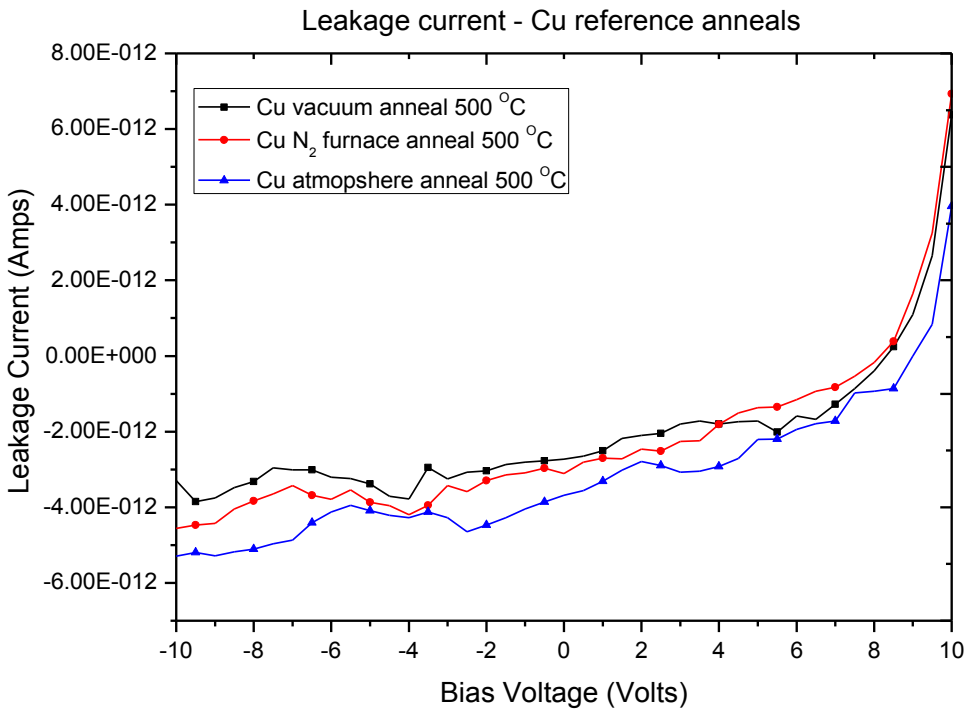

Figure 7.9: IV leakage current for the pure Cu reference throughout thermal stressing.

The negative flatband voltage shift and hysteresis as seen following the 500 ^{O}C N_2 anneal within the CV profile is consistent with the diffusion of Cu^{+} ions into the underlying dielectric material [13-16]. Further stressing at 500 ^{O}C in atmospheric conditions leads to total destruction of the pure Cu gate material, indicating total failure of the device.

7.4.2 CuAl alloy MOS thermal stress

CuAl alloy MOS devices were simultaneously subjected to the same anneal sequence as the pure Cu reference device, to ensure identical conditions from which to draw conclusions. Figure 7.10 displays the CV profiles of the CuAl MOS device throughout the course of the thermal stress test.

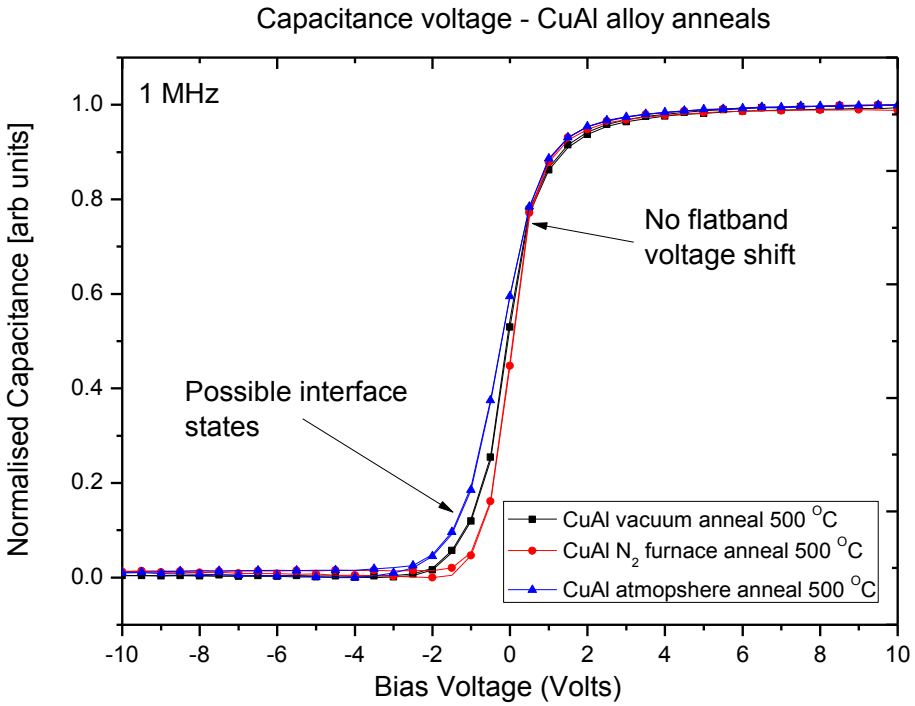

Figure 7.10: CV profiles of CuAl alloy MOS throughout thermal stressing.

As can be seen from the initial CV profile following vacuum anneal at 500 ^{O}C, the device is stable with clear accumulation, depletion and inversion regions and no non-ideal MOS traits present. Following the 500 ^{O}C anneal in N_2 flow, the CV profile becomes sharper in terms of the transition from accumulation to inversion. This is possibly due to the removal of any small amount of trapped charge residing in the oxide layer post vacuum anneal. No hysteresis or flatband shifts within the post N_2 anneal profile are noted.

Following the atmosphere anneal at 500 ^{O}C, the CV profile displayed a near ideal-MOS profile. There is however a slight broadening out of the profile at the depletion / inversion region which could be due to interface states at the Si / SiO_2 interface. Figure 7.11 displays the leakage current through the CuAl alloy MOS device throughout the thermal stress testing.

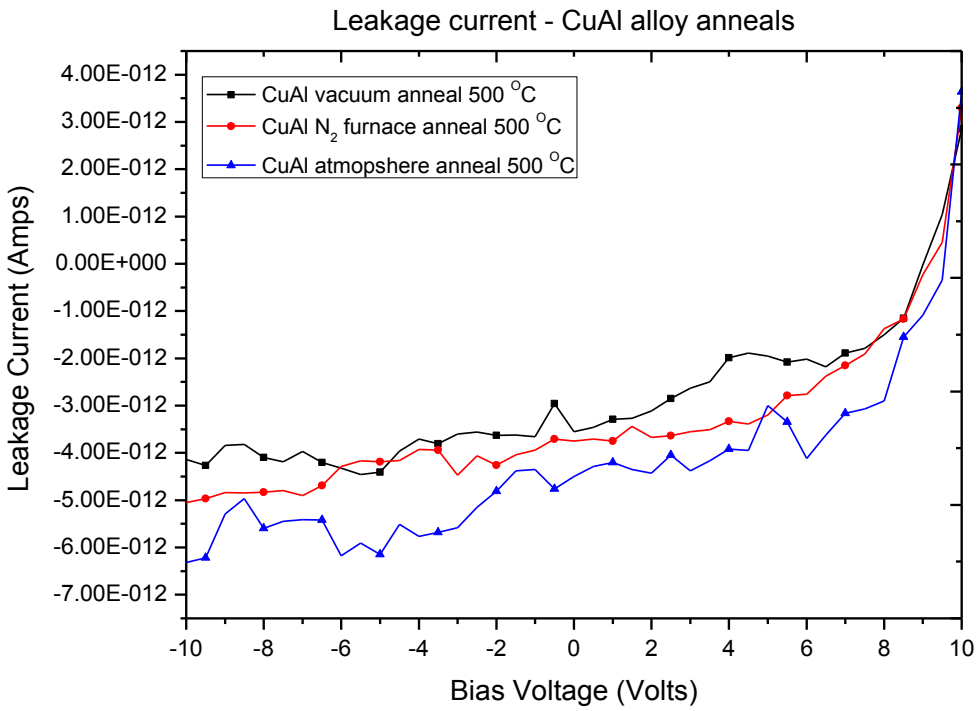

Figure 7.11: IV leakage current of CuAl MOS throughout thermal stressing.

As with the pure Cu reference MOS, no large increase in current is noted following thermal stressing, even following the extreme 500 ^{O}C atmosphere anneal. Therefore it can be seen that substantive differences exist between the pure Cu and CuAl alloy MOS devices post 500 ^{O}C atmosphere anneal.

7.4.3 Low frequency CV analysis of thermal stress

In order to test for interface states following the 500 ^{O}C N_2 anneal for both the Cu reference and CuAl alloy MOS device, a 10 kHz CV measurement was performed on each device. As stated in the experimental techniques chapter, low frequency CV allows the identification of interface states as seen by a "hump" in the CV profile [17]. Figure 7.12 displays the 10 kHz CV profiles of both the Cu and CuAl 1 MHz profiles as seen in Figure 7.8 and Figure 7.10 respectively, following the 500 ^{O}C N_2 thermal stress stage.

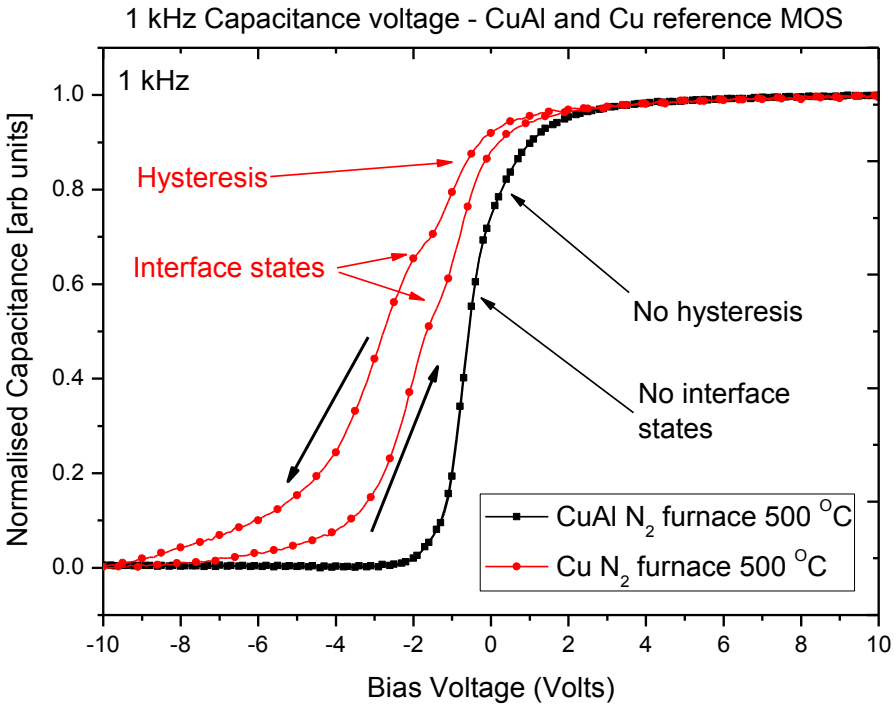

Figure 7.12: 10 kHz CV profiles of both Cu and CuAl MOS devices following the 500 ^{o}C thermal stress.

As can be seen from the two profiles, a large amount of hysteresis is noted for the pure Cu reference device, in addition to a hump in the CV profiles, consistent with the movement of charge within the oxide layer [18,19] in addition to interface states at the Si

/ SiO_2 interface. This is in contrast to the CuAl device which exhibits no hysteresis or interface states within the 10 kHz CV profile.

7.4.4 Flatband voltage shift of pure Cu MOS following thermal stress

As shown in Figure 7.8, a negative flatband voltage shift of the pure Cu MOS devices is noted following the 500 ^{O}C nitrogen anneal. Stated previously in the experimental details of the thermal stressing section (section 7.4) all CV profiles were recorded following a + 10 V hold for 300 s on the gate of the MOS structures in order to bias any mobile ions within the dielectric towards the Si / SiO_2 interface. In addition to this hold time, a number of other hold times and voltages were used on both the Cu and CuAl MOS devices. The hysteresis noted in Figure 7.8 following N_2 anneal at 500 ^{O}C is consistent with the movement of charges within the dielectric material of the pure Cu MOS device. If these ions are truly mobile, then applying various voltage biases to the gate of the MOS device for various time periods should alter the flatband voltage to different degrees, due to the fact that the closer the ions are to the Si / SiO_2 interface the greater the flatband shift, and the closer they reside to the metal gate, the less impact they will have on the band bending at the Si / SiO_2 interface. Figure 7.13 displays the CV profile for the Cu MOS device, which exhibited Cu diffusion characteristics from Figure 7.8, but with various hold times used before recording the CV profile. Although a dual sweep CV profile was recorded, and indeed showed large hysteresis as seen in Figure 7.8, only the + 10 V to – 10 V portions of the CV sweep are shown here both for clarity and to highlight the flatband shifting of the Cu MOS device.

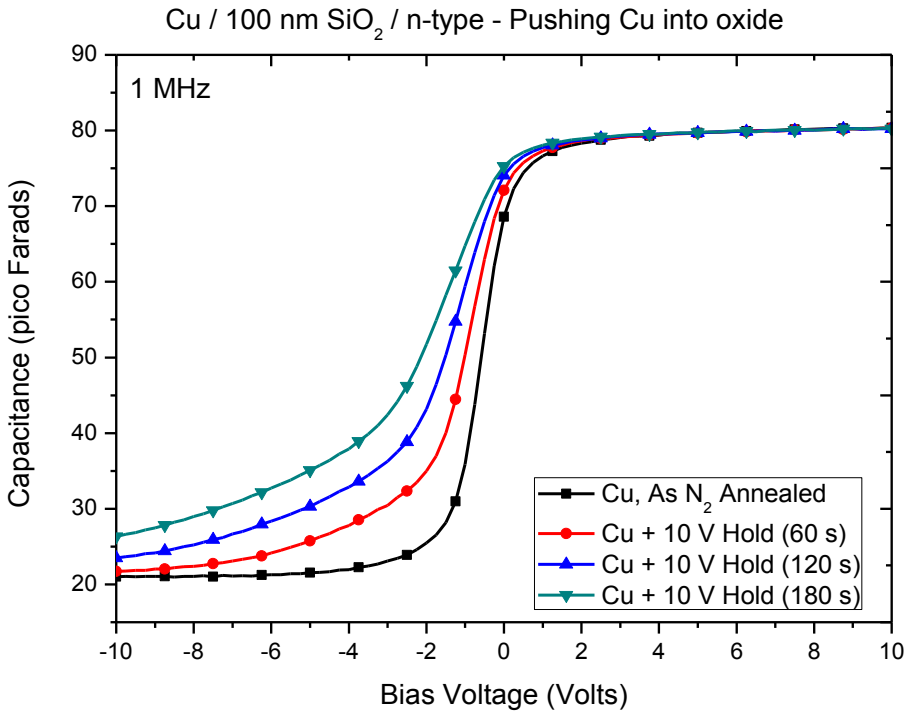

Figure 7.13: CV profiles of Cu MOS for various positive voltage hold times.

As can be seen from the initial CV profile which did not receive any hold time, the Cu device appears stable (a small amount of hysteresis however was noted). Subsequent CV profiles were then recorded using a + 10 V hold on the gate of the structure in order to bias any Cu^+ ions into the dielectric material for varying amounts of time. As can be seen from the various hold time CV profiles, a gradual negative flatband voltage shift is noted as the hold time is increased from 0 s to 180 s. The final 300 s hold time is omitted as it is shown in Figure 7.8 previously. Once a large flatband shift had been achieved, a negative hold voltage of – 10 V was applied to the gate in order to bias any mobile Cu^+ ions toward the metal gate and away from the Si / SiO_2 interface. These negative voltage CV profile hold time are shown in Figure 7.14.

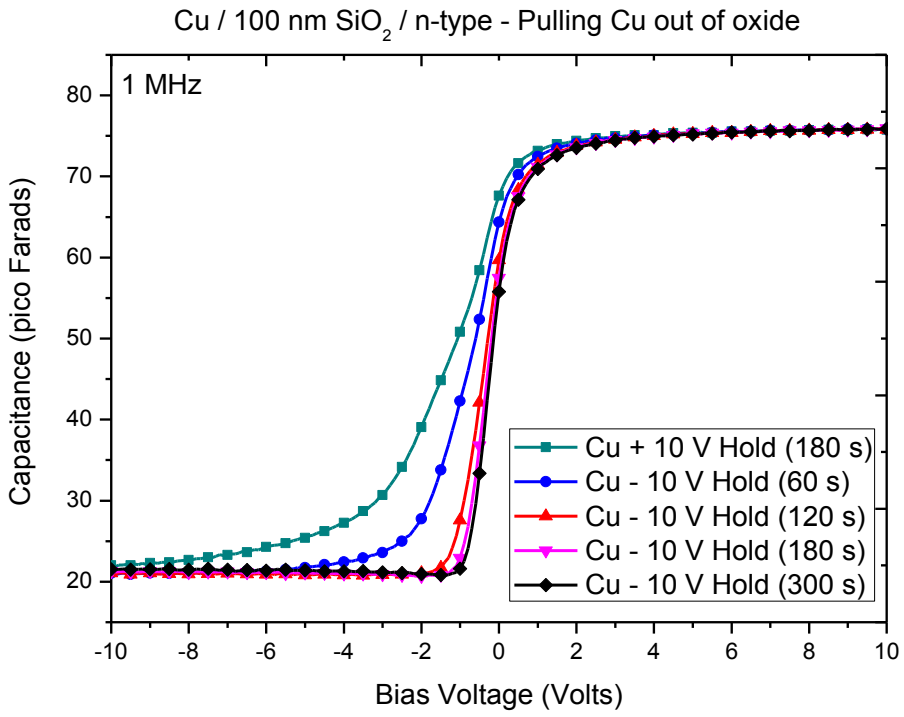

Figure 7.14: CV profiles of Cu MOS for various negative voltage hold times.

As can be seen via the – 10 V hold times on the gate of the Cu MOS device, a shift of flatband voltage is noted towards the original position of the intial state as seen in Figure 7.13. A final – 10 V hold for 300 s seconds is then applied to the gate, where it is then found that the CV profile appears as a very near ideal MOS. Thus it is shown that the flatband of the device can be altered by applying a positive or negative voltage for a set time, thereby showing that the charge which is causing this flatband voltage shift is mobile and a "tuneable" flatband position can be achieved. This result indicates the difficulty in identifying any diffused Cu^{+} ions within a dielectric material using CV profiles of fabricated MOS devices. If the correct CV parameters such as hold time and hold voltage are not used, then it is possible that no flatband voltage shift will be detected.

Thus a full in depth study must be completed as shown above in order to identify any flatband shifts associated with Cu diffusion into any surrounding ILD material.

7.4.5 Imaging of Cu and CuAl MOS throughout thermal stressing

In addition to electrical data, optical, atomic force microscopy (AFM) and scanning electron microscopy (SEM) images were obtained from the Cu and CuAl MOS devices following various anneal stages. Optical microscopy photographs for both Cu and CuAl MOS devices are presented in Figure 7.15.

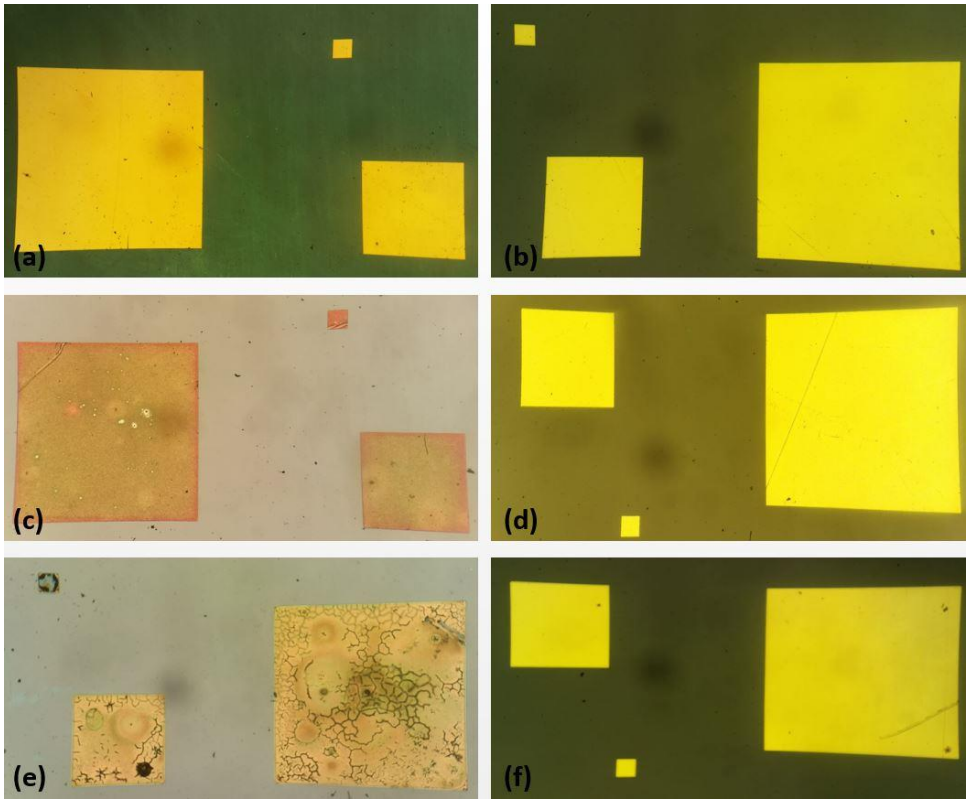

Figure 7.15: Optical microscopy photographs of Cu (a,c,e) and CuAl (b,d,f) following the three anneal stages of the thermal stressing (vacuum, N_2 flow, atmosphere at 500 ^{O}C).

As shown in Figure 7.15, the Cu and CuAl MOS devices following vacuum anneal at 500 ^{O}C ((a) and (b) of Figure 7.15 respectively) do not seem to be damaged or oxidised to any

large extent, most likely due to the fact that the anneal took place in high vacuum conditions better than $1x10^{-6}$ mbar. Following the 500 ^{O}C anneal in N_2 for the Cu and CuAl MOS devices ((c) and (d) of Figure 7.15 respectively), oxidation of the Cu samples appears to have taken place due to the discolouring of the gate metal. This is in contrast to the CuAl (d) which exhibits no such damage. Finally following the 500 ^{O}C anneal in atmosphere for the Cu and CuAl MOS devices ((e) and (f) of Figure 7.15 respectively), extreme discolouration and cracking / delamination of the Cu gates (e) is noted, as stated previously this delamination of the gate material made it impossible to obtain any electrical data from the devices. This again is in contrast to the pristine gate structures of the CuAl MOS devices following the 500 ^{O}C atmosphere anneal stage, which show excellent CV profiles in contrast to the pure Cu sample. It is worth restating at this point that both Cu and CuAl alloy MOS devices were annealed simultaneously in the same anneal and thus the large contrasting difference noted can be interpreted as being due to the alloying of Al within the CuAl sample, relative to the failure of the pure Cu reference.

Atomic force microscopy (AFM) were used to image the samples further. The surface roughness of the samples was calculated by taking the 3D surface area of the sample and dividing that value by the projected area of the AFM image (2 μm x 2 μm image area); thus a low value of surface area divided by projected area (with 1 by definition being the lowest) indicates low roughness and a higher value indicates high levels of surface roughness [20]. Figure 7.16 displays both 2D and 3D AFM images of the Cu MOS devices both post 500 ^{O}C vacuum anneal and post 500 ^{O}C N_2 anneal ((a) and (b) of Figure 7.16 respectively).

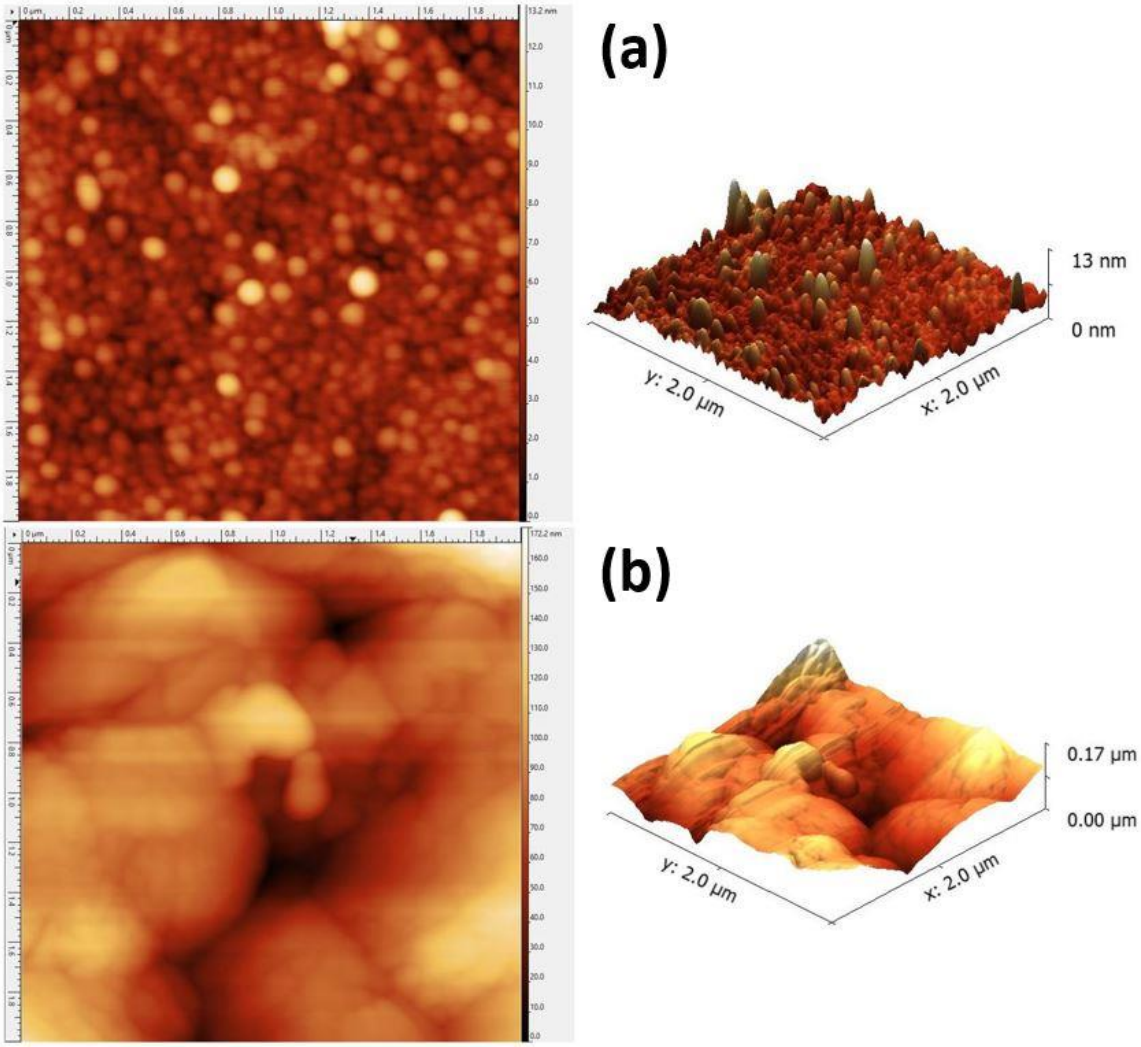

Figure 7.16: AFM images (2D and 3D) of Cu MOS following (a) 500 ^{o}C vacuum anneal and (b) 500 ^{o}C N_2 anneal.

As can be seen from the AFM images, the post vacuum anneal surface appears to be flat, with a surface/projected area of 1.0018. Following the 500 ^{O}C N_2 anneal stage the surface appears to roughen significantly which is shown by a surface/projected area of 1.0294. This increase in surface roughness cannot be tolerated in BEOL interconnect fabrication [9]. Figure 7.17 displays 2D and 3D AFM images of both CuAl post 500 ^{O}C vacuum anneal and post 500 ^{O}C N_2 anneal ((a) and (b) of Figure 7.17 respectively).

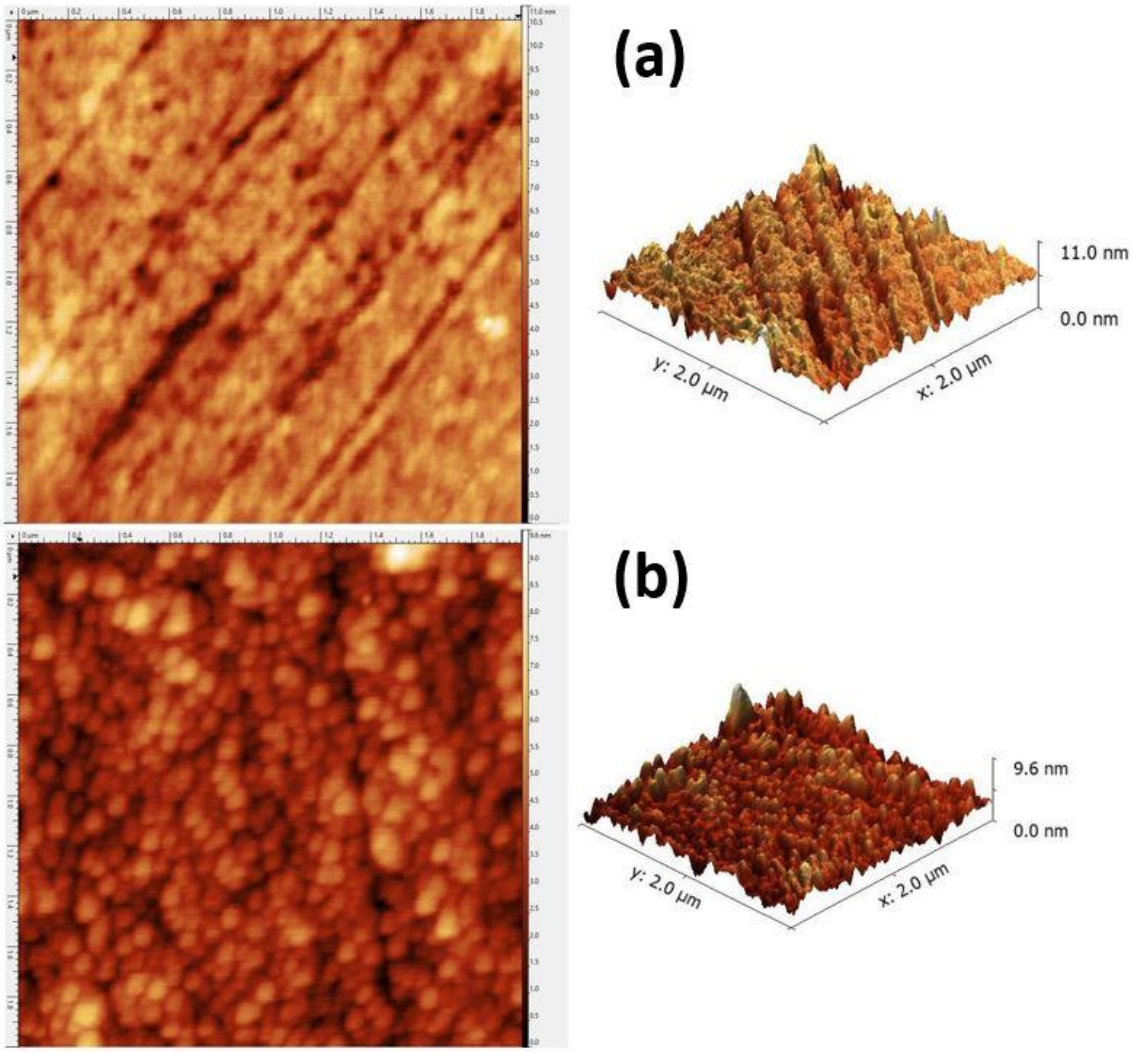

Figure 7.17: AFM images (2D and 3D) of CuAl MOS following (a) 500 ^{o}C vacuum anneal and (b) 500 ^{o}C N_2 anneal.

As can be seen form the AFM images of the CuAl alloy MOS gate, the surface is very smooth following the vacuum anneal stage with a surface/projected area of 1.0015. Following the 500 ^{O}C N_2 anneal stage, the surface still appears smooth with a surface/projected area of 1.0013. This is in contrast to the pure Cu reference which foloowing the 500 ^{O}C N_2 anneal increased in surface roughness drastically.

Scanning electron microscopy was used to image the surface of both the Cu and CuAl alloy MOS devices over the course of thermal stress treatments. All SEM images are presented in Figure 7.18.

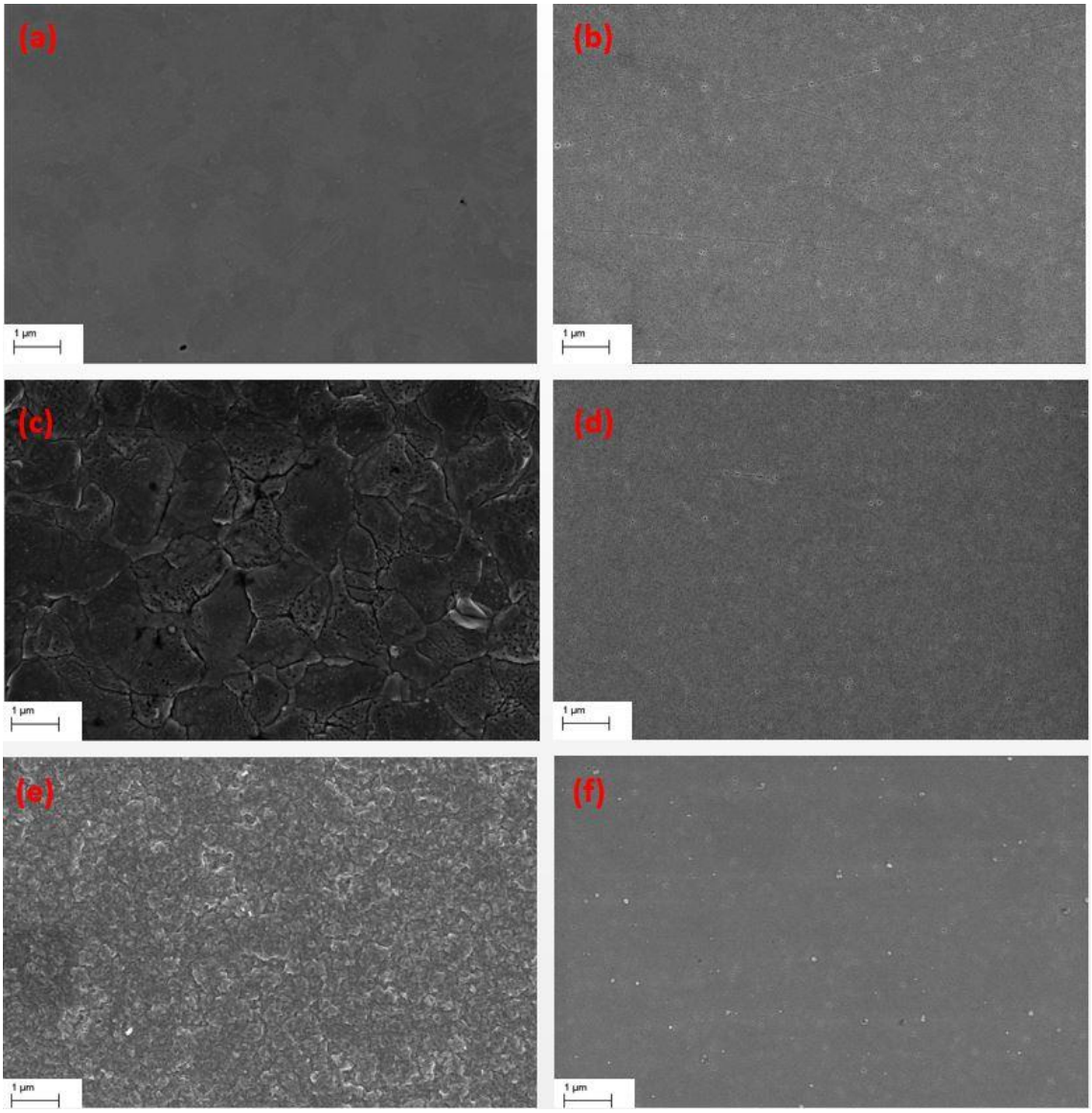

Figure 7.18: SEM images of Cu (a,c,e) and CuAl alloy (b,d,f) over the course of thermal stress treatments.

As can be seen from Figure 7.18 (a) and (b) for the Cu and CuAl alloy vacuum anneals respectively, both surfaces appear smooth and relatively featureless following vacuum anneal, in agreement with AFM analysis, indicating that the vacuum anneal does not

damage the morphology of the metal gates. Following the N_2 500 ^{O}C anneal for Cu (c) and CuAl alloy (d), a large difference in surface morphology is noted, as seen via AFM also. The SEM images of the N_2 anneal give great detail to the cracking and surface defects, not immediately obvious for the Cu N_2 anneal when imaged via AFM. In contrast the CuAl alloy N_2 500 ^{O}C anneal surface appears smooth and relatively featureless compared to the pure Cu surface of the same thermal stress, in agreement with previous reports [8,21]. The final 500 ^{O}C atmosphere anneal SEM images for Cu (e) and CuAl alloy (f) are shown in the lower portion of Figure 7.18. As can be seen via the Cu 500 ^{O}C atmosphere anneal (e), the surface appears to be heavily cracked, with more surface features relative to the N_2 anneal. In contrast the CuAl alloy 500 ^{O}C atmosphere anneal (f) appears smooth and featureless. Small features are noted in image (f), however these have been attributed to Si dust which may have contaminated the sample surface during sample cleaving prior to insertion within the microscope.

When the optical, AFM and SEM images are examined in combination, it is clear that the pure Cu samples degrade over the course of thermal stress by way of increased surface cracking a roughness, in addition to total gate failure by way of partial delamination and flaking of the gate material following the 500 ^{O}C atmosphere anneal. In contrast the CuAl alloy appears to remain smooth and relatively featureless over the course of the thermal stress measurements, even after the 500 ^{O}C atmosphere anneal which proved to be destructive to the pure Cu sample.

7.5 Secondary Ion Mass Spectroscopy

Secondary ion mass spectroscopy was used to depth profile the Cu reference MOS devices which exhibited failure following thermal stressing. Three samples were analysed, the first was an as fabricated MOS device which received no anneal treatment and was thus used as a reference for further samples that were annealed. The second device tested was a Cu MOS device which had received a 500 ^{O}C anneal in vacuum. Finally a Cu MOS device which had received both a 500 ^{O}C anneal in vacuum and subsequent 500 ^{O}C anneal in N_2 was analysed due to the fact that this device exhibited signs of Cu diffusion into the oxide layer, as seen in Figure 7.8. Figure 7.19 displays the SIMS depth profiling of the Cu MOS device as fabricated (no associated anneals or treatments). As indicated in the plot, three distinct regions in the graph are visible, the first being the Cu metal layer, the second layer consists of the SiO_2 dielectric and the final layer the underlying Si substrate. When examined closely there exists however extra detail at the metal / SiO_2 and SiO_2 / Si interfaces. A sharp drop off in Cu_3 signal at the metal / oxide interface indicates that the interface is abrupt in addition to the lack of Cu being "pushed" into the oxide layer during the ion bombardment of the SIMS procedure [22,23]. This sharp drop off in Cu signal indicates that no Cu has diffused into the oxide material. When the SiO_2 / Si interface is examined however, a rise in Cu signal from the background counts of ~ 50 counts is noted. This increase could be due to partial "knock in" of the Cu gate material during the ion bombardment, or possibly due to implantation of Cu during the sputter deposition of the gate material. In addition, a rise in the background signal for CuO and CuO_3Si signals are noted at the metal / SiO_2 interface. This result indicates that a possible reaction has taken place between metal Cu and the underlying SiO_2 to form CuO and CuO_3Si species.

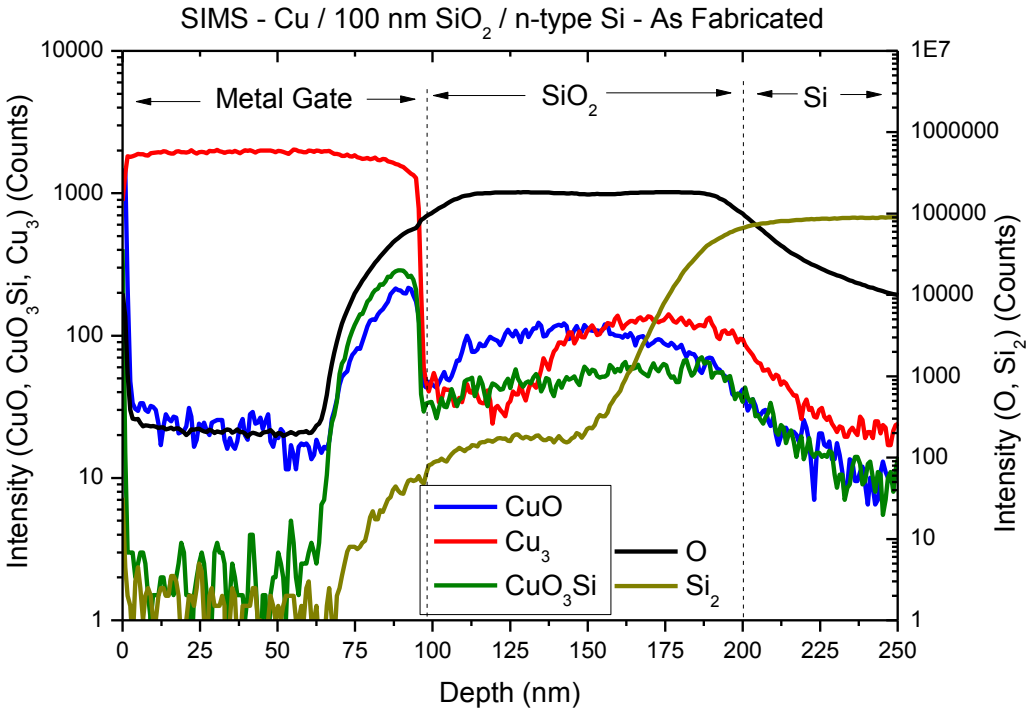

Figure 7.19: SIMS depth profile of Cu MOS as fabricated.

Figure 7.20 displays SIMS depth profiling of Cu MOS following a 500 ^{O}C anneal in vacuum. As can be seen, a large change in spectra is seen from the as fabricated structure of Figure 7.19 to the vacuum annealed in Figure 7.20 with evidence of the diffusion of Cu into the underlying SiO_2 layer.

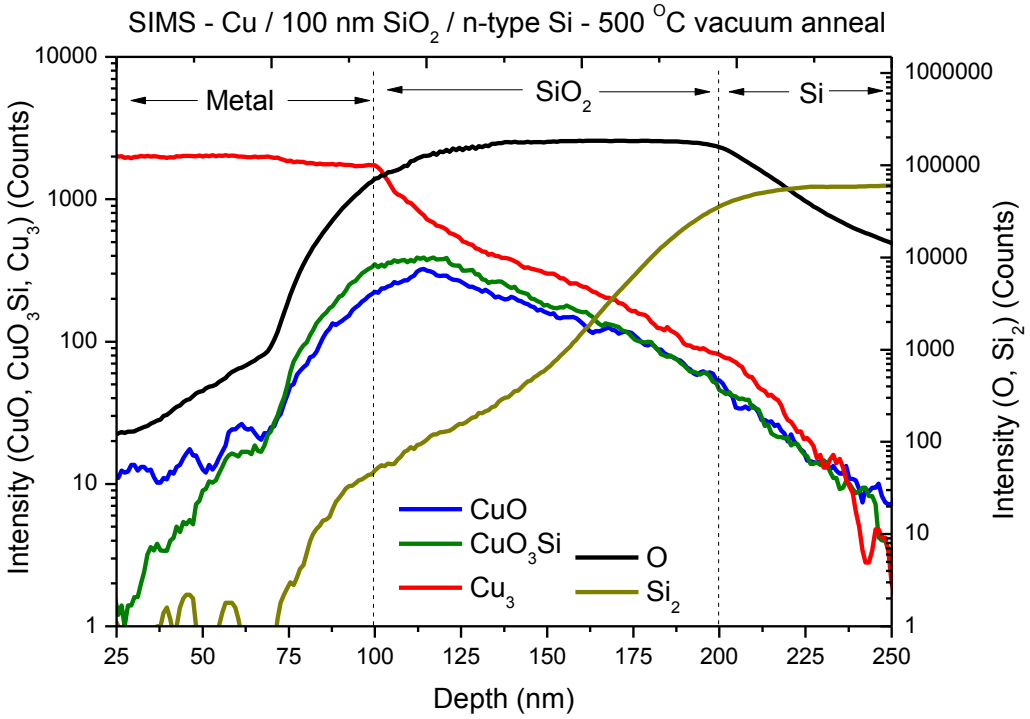

Figure 7.20: SIMS depth profile of Cu MOS following 500 ^{o}C vacuum anneal.

In addition to a broadening of the Cu metal signal into the oxide layer, a broadening of both CuO and CuO_3Si signals is also noted into the oxide layer, consistent with TEM imaging as seen in the previous chapter. This results is unexpected considering the sharp, near ideal MOS CV profile obtained for the vacuum annealed Cu sample, as seen in Figure 7.8. Cu MOS SIMS depth profiling spectrum for the 500 ^{O}C N_2 sample is presented in Figure 7.21. As can be seen from the depth profile, a large CuO signal is seen both up to the metal / SiO_2 interface and into the dielectric layer. This large CuO signal is most likely as a result of oxidation of the metal Cu gate due to a partial oxygen atmosphere during the N_2 tube furnace anneal at 500 ^{O}C, consistent with decolouration of the gate material as seen in the optical photographs displayed in Figure 7.15. In addition to an increase of CuO signal, an increase of CuO_3Si and Cu_3 signals are seen within the region

of the spectrum associated with the SiO_2 dielectric layer. This increase of Cu diffusion into the dielectric layer is consistent with the failure of the CV profile a seen in

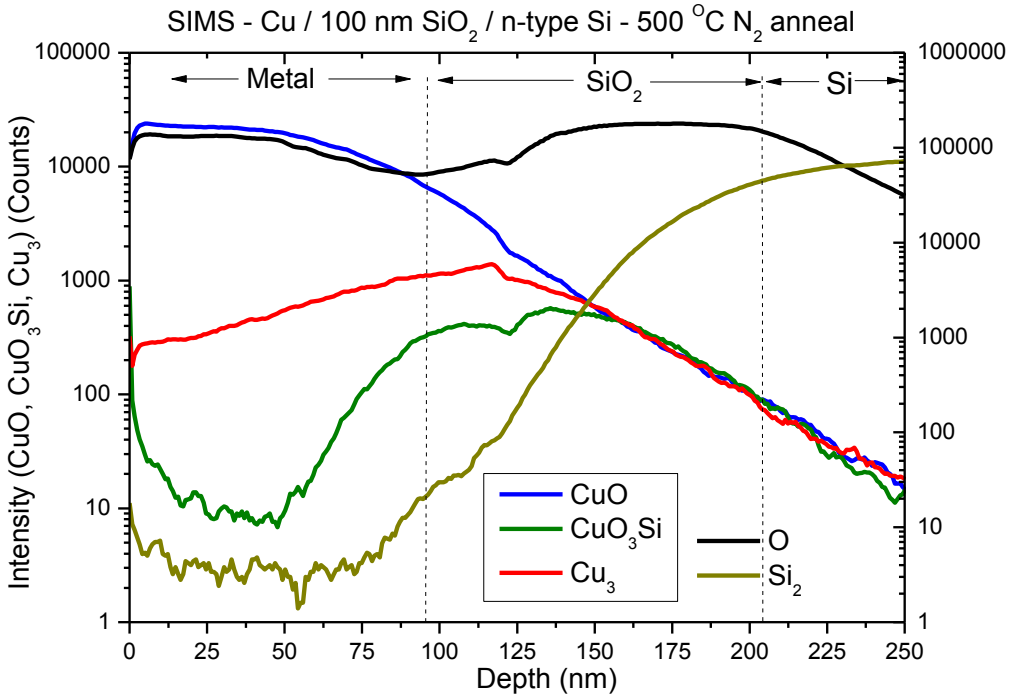

Figure 7.21: SIMS depth profile of Cu MOS following 500 ^oC N_2 anneal.

Figure 7.8**.** Thus the SIMS depth profiling has shown that changes in the CV profile for the Cu MOS device which was annealed in N_2 at a temperature of 500 ^OC can be related to the diffusion of Cu into the oxide layer of the device, as seen in previous studies of Cu diffusion analysed by SIMS [14,15,24].

7.6 Conclusions

As stated in the introduction to this experimental chapter, a number of conditions must be satisfied in order to consider a CuAl alloy for use in future BEOL interconnect strategies. Conditions such as:

(a) The expulsion of Al from the alloy bulk upon thermal anneal.

(b) Self-forming barrier reaction between the expelled alloy and a SiO_2 layer.

(c) Surface passivation of the film due to oxidation of the Al which acts to prevent oxidation of the Cu within the material.

were shown to be satisfied in the previous experimental chapter involving the CuAl alloy. This chapter has shown that the remaining conditions, namely:

(d) Good adhesion between the metal layer and any surrounding dielectric material, in addition to low surface roughness.

(e) Prevent Cu diffusion into any surrounding dielectric material.

have been satisfied by the use of a CuAl (90:10 % wt). BTS and thermal stress tests using both a pure Cu reference and CuAl alloy MOS devices show the failure of pure Cu by way of distortion of the CV profile in addition to negative flatband voltage shifts, attributed to the diffusion of Cu into the underlying oxide layer. The flatband of Cu MOS devices has shown to be "tunable" by way of an applied bias prior to acquiring the CV profile. This was shown to be in stark contrast to the CuAl alloy which showed no evidence of Cu diffusion or device failure, thereby satisfying condition (e) outlined above. Further experimentation by way of optical, AFM and SEM imaging of the thermally stressed MOS devices indicate the failure of the pure Cu devices by way of increased surface roughing and cracking, in addition to partial delamination of the gate material following the 500 ^{O}C atmosphere anneal stage. This again is in contrast to the thermal stability of the CuAl alloy as indicated by the relatively smooth and undamaged surfaces

even following the 500 ^{O}C atmosphere anneal stage. This result satisfies the demand imposed by condition (d) outlined above, indicating that a CuAl alloy has been shown to satisfy all conditions necessary for integration in future BEOL strategies for IC fabrication.

7.7 References

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8 Conclusions and future work

8.1 Conclusions

8.1.1 $MnSiO_3$ as a Cu diffusion barrier

A procedure for in-situ fabrication of Cu / SiO_2 / Si MOS structures both with and without a $MnSiO_3$ barrier at the Cu / SiO_2 interface has successfully been developed; thus allowing the comparison of interfacial chemistry and electrical performance to be compared. Results show that the in-situ deposition of a thin layer of metallic Mn (~ 1.5 nm) on a SiO_2 substrate in addition to in-situ annealing at 500 ^{O}C results in the formation of an ultra-thin (< 1.5 nm) layer of $MnSiO_3$. Electrical measurements on both the $MnSiO_3$ and non-barrier reference sample indicate the diffusion of Cu into the underlying dielectric layer of the reference sample and the stability of the $MnSiO_3$ barrier sample at prevention of Cu diffusion into the dielectric layer. Poor adhesion of the non-barrier sample is noted as removal of the Cu material following tape tests in contrast to the $MnSiO_3$ samples which showed superior adhesion due to the ultra-thin $MnSiO_3$ barrier at the Cu / SiO_2 interface. Further characterisation as seen via TEM and SIMS measurements conclusively show the diffusion of Cu into the underlying SiO_2 layer of the non-barrier reference sample, in contrast to the stability of the $MnSiO_3$ barrier sample. The results outlined in this chapter indicate that an ultra-thin layer of $MnSiO_3$ at the interface of a Cu / SiO_2 structure prevents diffusion of Cu into the SiO_2 layer, whilst simultaneously promoting adhesion between the two layers, thereby making this material system suitable for integration into BEOL processes for IC production.

8.1.2 $MnSiO_3$ formation on 0% & 50% porous industrially relevant dielectric materials

Simultaneous in-situ deposition of thin layer Mn (~ 2.5 nm) films on both 0% and 50% porous low-k CDO materials was successfully demonstrated; thereby allowing the investigation of $MnSiO_3$ formation on a highly porous substrate to observed relative to a non-porous substrate. In-situ annealing reveals that $MnSiO_3$ forms on both 0% and 50% porous substrates. XAS measurements indicate a larger formation of $MnSiO_3$ on the 50% porous dielectric (~ 88% $MnSiO_3$) relative to the non-porous 0% dielectric (~ 44%). TEM measurements in conjunction with EELS mapping of the metal / dielectric interfaces reveal that the deposited Mn has diffused into the 50% porous substrate, in agreement with the highly porous nature of the material. This observation is in agreement with the in-situ XPS analysis which also indicates diffusion of the Mn into the highly porous substrate. The results in this chapter indicate that $MnSiO_3$ can form on industrially relevant dielectric materials and that porosity does have an impact on the formation of $MnSiO_3$. This impact can be seen via XAS measurements which indicate ta larger formation of $MnSiO_3$ on the 50% porous dielectric relative to the non-porous reference material in addition to the problematic in-diffusion of the deposited Mn as seen via TEM and in-situ XPS measurement on the 50% porous dielectric material.

8.1.3 CuAl (90:10 % wt) alloy for use in BEOL IC strategies

A CuAl alloy material was investigated for use as a material candidate for BEOL interconnect applications. In-situ XPS and ex-situ HAXPES measurements show the growth of Al metal and Al oxide in the surface region of the alloy following anneal treatments, indicating the expulsion of Al form the alloy bulk, the first requisite necessary for consideration of a self-forming barrier alloy candidate. A thin layer of SiO_2 was deposited onto the alloy surface and annealed, which shows the interaction of the expelled

Al from the alloy with the overlying SiO_2 layer, consistent with the formation of a self-forming barrier at the surface of the alloy material. TEM imaging of reference pure Cu and CuAl alloy layers was performed following vacuum annealing which indicate a continuous interfacial layer forms between the CuAl alloy and SiO_2 substrate, consistent with the formation of a self-forming barrier. This results is in contrast to the pure Cu reference which indicates Cu diffusion into the underlying SiO_2 layer. Four point probe data indicates that the resistance of the CuAl alloy decreases following vacuum anneal, consistent with the expulsion of Al from the alloy bulk; however even following a 500 ^{O}C anneal in vacuum, the resistance of the alloy is noted to be ~ 10 x higher than the pure Cu reference material. The results obtained in this chapter indicate that a CuAl alloy has potential as a self-forming barrier candidate due to the expulsion and self-forming barrier reactions of the alloy following anneal; however given the relatively high resistance of the alloy, integration of this material candidate may not be suitable as a whole metal interconnect material but may instead be considered in a thin film form, such as a highly enriched seed layer.

8.1.4 Barrier layer properties of a CuAl (90:10 % wt) alloy

Following on from preliminary work outlined in the initial CuAl alloy chapter, more in-depth analysis was performed on the alloy as to its use in prevention of Cu diffusion into any surrounding dielectric material. Both bias thermal stress and pure thermal stressing of CuAl and reference Cu MOS structures was undertaken. These results show the stability of the CuAl alloy in contrast to the instability if the reference Cu MOS structures which indicate Cu diffusion into the underlying dielectric material following stressing. Further stressing in atmospheric ambient conditions show the total failure of the pure Cu reference material by way of oxidation and delamination of the Cu gate material from the

SiO_2 substrate in contrast to the stability of the CuAl alloy which remained stable throughout the various thermal stress stages. Capacitance voltage measurements of the pure Cu MOS structures following thermal stressing in an N_2 flow environment show the movement of Cu^+ ions within the underlying dielectric material. It was found that these ions could be biased towards or away from the SiO_2 / Si interface of the MOS device via the application of an electric field. Optical and SEM imaging of the metal gates throughout the course of thermal stressing shows the degradation of the pure Cu reference material with corresponding stability of the CuAl alloy. SIMS analysis reveals that Cu has penetrated into the dielectric of the reference Cu MOS samples throughout the course of thermal stressing. The results in this chapter indicate the usefulness of the CuAl alloy at prevention of Cu into the underlying dielectric layer of the fabricated MOS devices. Surface passivation of the alloy is noted due to the thermal stability of the CuAl alloy which is attributed to the surface layer of Al oxide which was shown to form on the alloy following anneal treatments.

Indeed, since the completion of this study, manufacturers of semiconductor IC components have announced the use of alloying Cu seed layers with manganese in manufacturing processes as an electromigration (EM) dopant [1]. In addition, Al is also in use as an EM dopant as indicated by Intel Corporation [2]. Thus with both Mn and Al currently in use in high volume manufacturing as EM dopants, both metals could also be used as barrier layer materials in a self-forming barrier approach presently or in the near future.

Low-k carbon doped oxides still prove challenging in relation to stability and barrier formation, especially when porosity is introduced [3,4], as seen in this study. The need

for pore sealing or pore “stuffing” of the porous materials is evident from the diffusion of the barrier layer material into the dielectric upon deposition. Electrical measurements combined with in-situ chemical analysis and ex-situ characterisation methods such as SIMS and TEM have shown to yield a high return of data in relation to Cu diffusion barrier layer studies. This approach will be adopted in future studies as outlined below.

It can be seen from the results outlined above, that the use of Mn in a self-froming barrier capacity shows great promise. The incorporation of an ultra-thin (< 1.5 nm) layer of $MnSiO_3$ at the interface of a Cu / SiO_2 sample has shown to prevent the in-diffusion of Cu into the dielectric layer, with the additional benefit of promoting adhesion between the two layers. $MnSiO_3$ was successfully formed on industrially relevant 0% and 50% porous low-k CDO materials, again indicating that Mn can be successfully incorporated into future BEOL interconnect strategies.

A CuAl alloy has also shown promise for use in BEOL strategies. The alloy has shown to prevent Cu diffusion into the underlying SiO_2 layer, with the added benefits of increased adhesion of the metal to the underlying SiO_2 and surface passivation of the metal film due to the formation of an Al oxide layer at the surface. Four point probe data reveals that the alloy is ~ 10 x higher in resistance than the pure Cu reference used in this study, thereby eliminating any benefit gained from the alloy for use as an interconnect metal. Thus the CuAl (90:10 % wt) alloy could potentially find use as a thin seed layer for Cu electroplating applications or as a surface capping layer for future Cu interconnect applications.

8.2 Future work

Due to the success of the work undertaken in this study in relation to both Mn and Al as barrier layer candidates, future work in this area appears promising in order to successfully implement one or both of these metals into high volume manufacturing in a self-forming barrier capacity.

Future work directly following on from this study shall include:

(a) Chemical and electrical characterisation of Al as a self-forming Cu diffusion barrier layer candidate on low-k CDO materials with and without associated porosity.

(b) Thickness reduction of barrier layers in order to ascertain the thinnest barrier possible in order to prevent Cu diffusion and thus drive Moore's law forward.

(c) A CuMn alloy would prove useful for experimentation due to the excellent properties observed using a CuAl alloy. This alloy can then be used to study barrier properties and thin film integrity, as seen via the CuAl alloy in this work, on a wide variety industrially relevant dielectric materials.

(d) Further expansion of experimental techniques such as X-ray reflectivity (XRR) in order to study film thickness and density of these industrially relevant porous CDO materials.

(e) Electromigration testing using small channel structures on dielectric materials with both Mn and Al based barrier in order to test adhesion and Cu diffusion characteristics of these barriers in a more industrially focused manner.

(f) Fundamental studies of Cu diffusion in relation to plasma and other manufacturing process damages should be undertaken, after which barrier layers can be tested from a more industrially relevant stand point.

(g) Atomic layer deposition is a key deposition technique for future studiesdue to the high industrial relevance of the technique.

(h) Atomic layer etch has also emerged as a potentially useful technique in BEOL manufacturing.

In addition to barrier layers, the topic of low-k dielectrics is of great interest to industry in relation to deposition, etch, integration and stability [5]. Porous CDO layers are also of major importance as seen in this study, and thus the issue of pore stuffing or sealing of the dielectric layers if of great importance [6]. Surface assembled monolayers (SAMS) have been suggested as a possible candidate to pore seal the surface of these highly porous layers [7,8], thereby facilitating barrier layer formation on the surface of the dielectric layer without inward diffusion of material as seen in this study. Thus SAMS can be investigated in relation to the pore sealing ability and surface modification in order to facilitate barrier layer formation on the surface of these challenging dielectric materials.

8.3 References

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