Time Dependent Dielectric Breakdown and Stress Induced Leakage Current Characteristics of 8Å EOT HfO_2 N-MOSFETS

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***Abstract*—In this work we present the time dependent dielectric breakdown (TDDB) characteristics of LaO capped HfO_2 layers with an equivalent oxide thickness of 8Å. The layers show maximum operating voltages in excess of 1V. Such high reliability can be attributed to very high Weibull slopes. We examine the origin of the high slopes by a detailed study of the evolution of the stress induced leakage current with time, temperature and stress voltage.**

Keywords- Hafnium oxide; High-k dielectric; stress induced leakage current, CMOS reliability, time dependent dielectric breakdown.

I. INTRODUCTION

High-k dielectrics to replace SiO_2 have been successfully incorporated at the 45-nm complementary metal-oxide-semiconductor (CMOS) technology node. However, continued research into the scaling of the high-k layer below 1nm equivalent oxide thickness (EOT) is necessary in order to adhere to the technology roadmap. At present there appear to be several barriers to further scaling including film uniformity, significant negative bias temperature instability (NBTI) , and uncertain time dependent dielectric breakdown (TDDB) and stress induced leakage current (SILC) characteristics [1,2,3].

This work focuses on the time dependent dielectric breakdown (TDDB) of LaO capped HfO_2 layers with an equivalent oxide thickness of 8Å. The layers show exceptionally high operating voltages, greater than 1V. In section III we show that this high reliability can be attributed to very high Weibull slopes. We examine the origin of the high slopes in section IV by a detailed study of the evolution of the stress induced leakage current behaviour, and evidence suggests that a defect level deep in the silicon bandgap is responsible for the breakdown in these layers.

II. EXPERIMENT

Two identical gate stacks were considered in this work with one having Si as the substrate material and the other SiGe. The dielectrics were grown on 300mm (100) Si-wafers using a metal inserted poly-Si process (MIPS). The gate stack was formed with an initial IMEC clean followed by 36 cycles of atomic layers deposition (ALD) HfO_2. A LaO capping layer was used to control the work function. The gate was formed by 5nm physical vapour deposition (PVD) TiN followed by 2nm PVD Si.

All experiments were performed on square gated transistors with areas of $1x10^{-8}$ cm^2 and $4x10^{-8}$ cm^2. This processing resulted in an EOT of 7.8Å and 8.1Å for the Si and SiGe substrates respectively. These values were extracted from Hauser fitting of C-V curves at 100 kHz to 100MHz [4]. The transmission electron microscope (TEM) image from a sample with almost identical processing in figure 1 shows no detectable interfacial layer and a physical thickness of ~2nm.

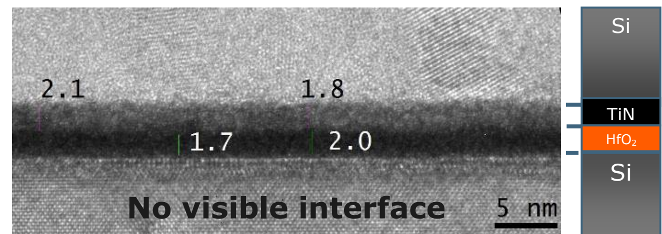

Figure 1. TEM image of a layer from the same lot as the wafers in this work with 2nm TiN gate. No interfacial SiO_2-like layer is observed.

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III. Time Dependent Dielectric Breakdown

The initial TDDB evaluation was carried out at 125°C and voltages from 2.2-2.5V. The devices measured were 1µm x 1µm transistors. The time-to-breakdown (t_{BD}) Weibull distributions were fitted with the maximum likelihood method, to ensure accurate extraction of the Weibull slope (β) and the 63%-value (η). Figure 2a shows the resulting TDDB distributions. Using a soft breakdown criterion of a current jump of 10µA, a Weibull slope of 1.54 is extracted for the 7.8Å layer and 1.82 for the 8.1Å case. Such slopes are well in excess of the ~0.8-1 that is commonly reported in the literature for layers of similar thickness [5].

Due to the positive impact of a high Weibull slope when scaling the TDDB distribution to smaller device areas and to the low percentile failure region, the power-law reliability extrapolation in figure 2b shows 10-year maximum operating voltages of 1.24 and 1.3V for the Si and SiGe substrates respectively.

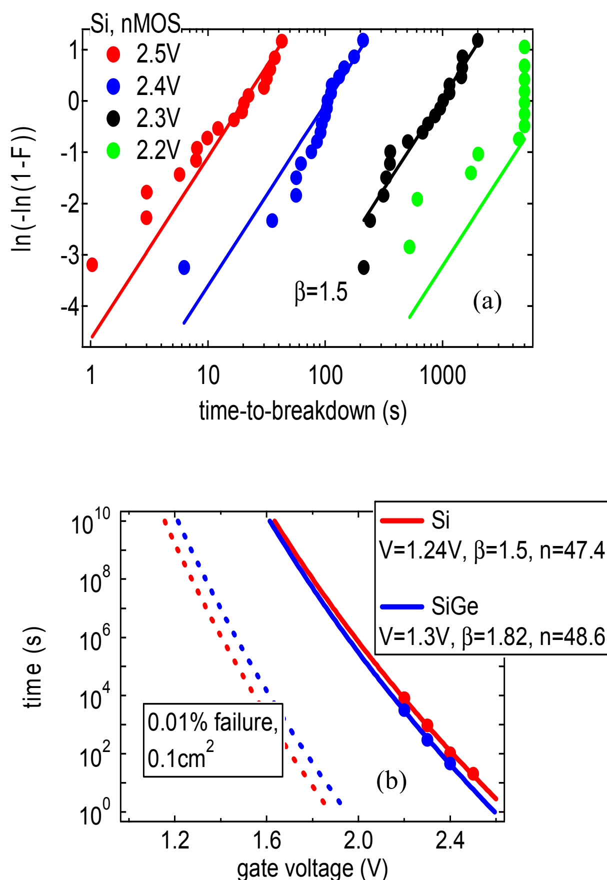

Figure 2. (a) Weibull plot of the tddb distribution for the Si substrate devices showing a Weibull slope of 1.5. (b) Power law lifetime extrapolation scaled to 0.1% failure rate and 0.1cm2. Operating voltages of >1V are forecasted.

The percolation model of oxide degradation [6] shows that the t_{BD}-distribution is Weibull distributed with slope $\beta = m.\beta_{ot}$ where 'm' is the logarithmic trap generation rate and β_{ot} is equal to the number of traps in the path

Thus, a high Weibull slope is caused either by more traps being required to trigger the breakdown or a higher trap generation rate. The model suggests that for SiO_2 layers of equivalent physical thickness to those under consideration here, 3 traps should be required to cause breakdown [7]. If the percolation distance is taken to be the same for HfO_2 it would mean that for a 3-trap path (with β=1.82) the 8.1Å layer would have a defect generation rate of 0.61, much higher than the 0.35-0.4 commonly seen in the literature [8]. However, it is commonly accepted that due the reduced barrier height of the high-k compared with SiO_2 the effective capture cross section of a high-k defect is larger than that of an SiO_2 defect, meaning that the percolation distance is more likely to be reduced in the high-k [9]. If anything then, we should expect that 2 well placed traps or perhaps 3 poorly aligned traps is the maximum needed to cause breakdown in these layers.

IV. Stress Induced Leakage Current Analysis

The I-t traces used to evaluate the TDDB reliability in the SiGe devices are shown in figure 3 and display a significant SILC component which emerges during the device lifetime. To further investigate the possibility of a high defect generation rate in these devices we examined the I-t traces during stress.

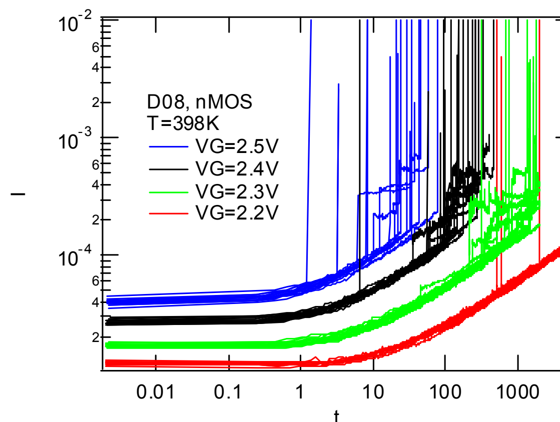

Figure 3. I-t traces measured during constant voltage time dependent dielectric breakdown show significant SILC of up to 5x initial leakage at breakdown for the stress voltage considered.

It has been shown that subtracting the initial charging component from the I-t trace, the pure leakage during the stress can be extracted [10]. This is shown in figure 4a for the SiGe devices. These measurements are performed on larger 2µm x 2µm FETs to maximise the SILC at low stress voltages.

The extracted SILC generation rate from the slope of these curves is 0.63 in line with that suggested by a 3 trap TDDB model with high trap generation rate. Note however that the current in the region of the fit is in the micro-amp range, suggesting that 2-trap conduction is already dominant. If this is the case then, as shown by Degraeve et al [10], the SILC generation rate would be twice the TDDB trap generation rate.

Probing of lower SILC levels with this method is not possible as illustrated schematically in figure 4b. Directly fitting the I-t trace to factor out the charging component is not

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correct because the I-t trace in this region is partly made up of SILC generated early in the stress from single traps; the region where the logarithmic trap generation rate and the SILC generation rate are the same. This is the reason why the power law fit in figure 4a fails in the low SILC regime.

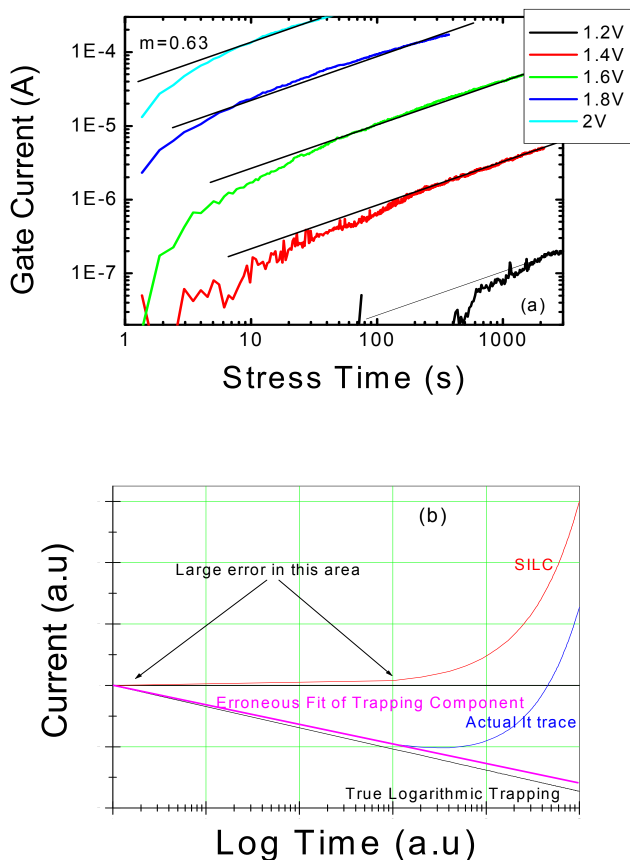

Figure 4. (a) Pure leakage current component extracted from the I-t trace by fitting and subtracting the charging component. (b) Schematic diagram of the error introduced in the single trap regime by directly fitting the I-t trace. The blue curve represents the real I-t trace. Fitting the trace with the pink line does not take into account the presence of single trap SILC early in the stress.

Commonly, SILC measurements involve stressing the dielectric at high field and measuring the increase in leakage current either 'on the fly' as detailed above, or by interrupting the stress and sensing at a fixed voltage close to the operation condition, which may or may not be favourable for tunneling through traps created during the stress. For an nMOSFET, the chosen voltage is typically ~0.5V, which represents a band alignment where resonant tunneling through defects at, or slightly below the silicon conduction band is the dominant trap assisted conduction mechanism. In such a case, the Fermi level is aligned with these defects whereas defects with other energy positions will not contribute significantly to the SILC at this gate voltage.

Measuring the SILC using a stress-and-sense methodology where the stress is interrupted and a full I_gV_g curve is taken allows sensing defects across the bandgap by direct tunneling where the on-the-fly method will only sense deeper defects by valence band tunneling and is insensitive to resonance effects [11], which is far removed from the operation condition as illustrated in fig. 5.

Furthermore the possibility exists to perform a discharge between the stress and sense conditions to minimise the effect of oxide charging. The stress and sense method was employed for a range of gate voltages and temperatures up to 175°C. Fig. 6 shows the SILC in these thin layers is relatively unaffected by discharging steps indicating that it is largely an irreversible process. Nonetheless, in all stress-and-sense measurements detailed in this work, the discharge step is performed.

There still exists in the literature some confusion over whether SILC is mediated through empty states or if a site needs to trap a carrier to enable it to become involved in the SILC process [12]. In this work the thickness of the layers is such that one would not expect significant trapping, though the SILC component still remains after the discharge indicating that it is mediated through neutral electron traps. However, further work needs to be done to understand the link (if any) between the traps which cause SILC and those which contribute to BTI effects.

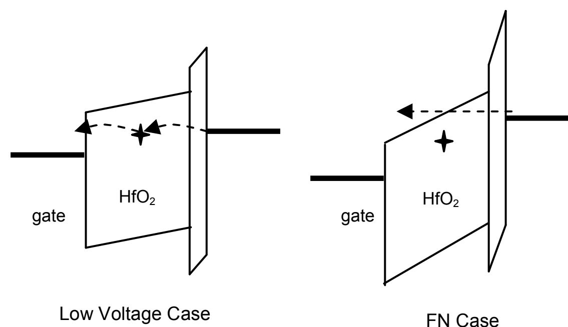

Figure 5. When sensing in the direct tunneling regime the Si Fermi level is resonant with defects in the HfO_2 bandgap, whereas the band alignment when directly measuring from the I-t trace may not sense the created defects efficiently.

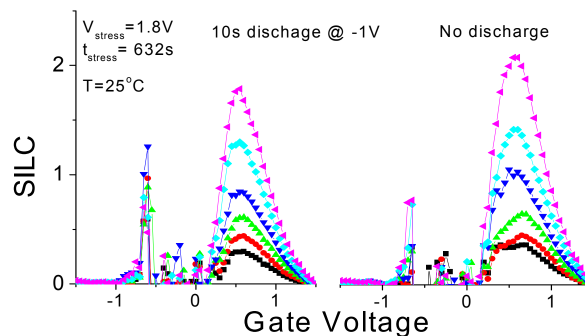

Figure 6. SILC profile for devices stressed with and without a 10s discharge at -1V prior to each stress phase. The discharge step removes less than 10% of the total 'bulk' SILC indicating that the SILC is mediated through empty defect states which remain in the oxide after the discharging step.

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Figure 5 shows the evolution of the SILC as a function of time for several stress conditions at a sense voltage of 0.5V. In this case we see a strong dependence of the SILC generation rate on voltage (fig 5a) and indeed temperature (fig. 5b) which disagrees with the model proposed in [12]. However, even the gentlest stress in the single trap regime only yields a SILC generation rate of 0.32 which cannot explain the TDDB results and so an increased bulk HfO_2 trap generation rate seems unlikely.

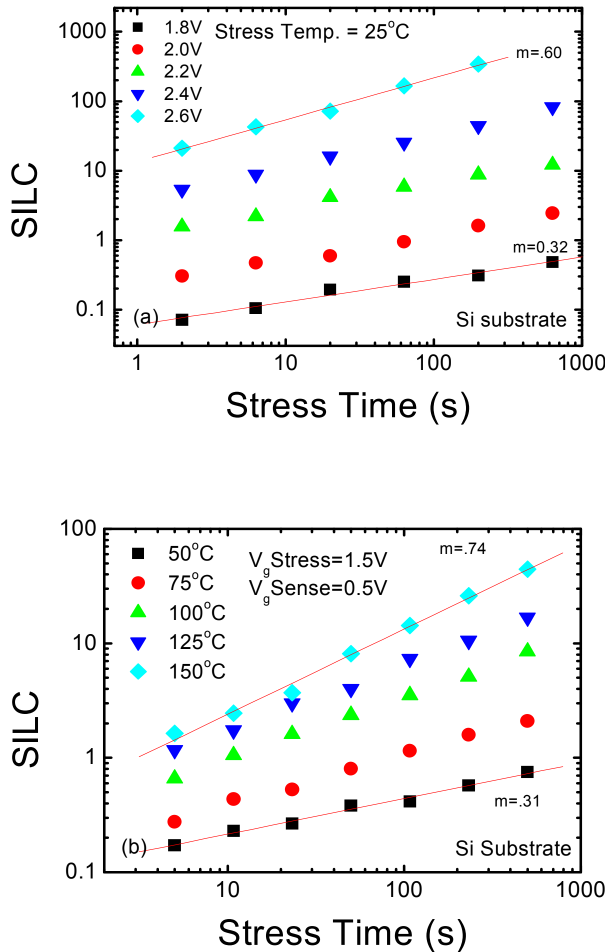

Figure 7. SILC generation as a function of (a) voltage for a series of stresses at 25°C and (b) temperature for a series of stresses at V_g=1.5V. A sense voltage of 0.5V is used in both cases. The SILC generation rate is dependent on both temperature and voltage.

Previous work [11] has shown that a sense voltage just below V_{FB} is resonant with a defect band close to the Si/SiO_2 interface. In order to examine the degradation rate close to the interface, we took the same stresses as above but changed the sense voltage to -0.7V. The kinetics are compared in figure 8 for sense voltages of (a) 0.5V and (b) -0.7V. The SILC generation rate is found to be 0.59 even at the lowest stress condition in the -0.7V case where the leakage increase after 1000s is 2nA and single trap conduction is dominant, rising to 1.4 at very high stress conditions. As for the case of 0.5V sense voltage, the sensitivity to stressing gate voltage is evident showing the transition from one-trap to two-trap SILC during the stress.

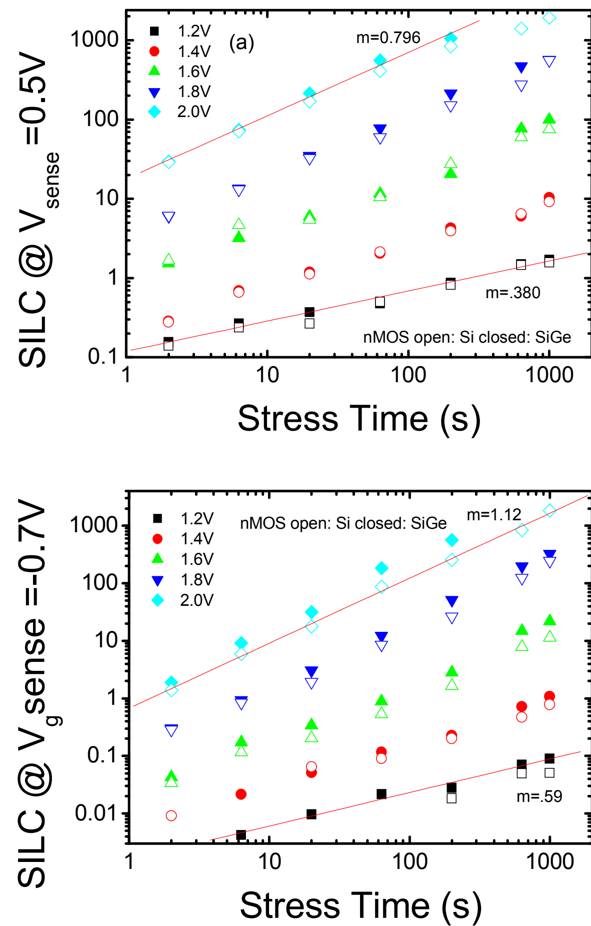

Figure 8. Comparison of the SILC generation behvaiour for a sense voltage of (a) 0.5V and (b) -0.7V. The measured SILC generations rates at -0.7V are much higher than those at 0.5V indicating a higher defect generation rate deep in the bandgap close to the interface.

As mentioned earlier, previous work has shown that SILC sensed at ~ -0.7V in high-k stacks with an SiO_2 interfacial region is linked to defects in the SiO_2. However the TEM image in figure 1 displays no visible interfacial region indicating that in this case, the defect level must result from the HfO_2 layer. Substrate hot electron stresses showed that the defect generation at -0.7V is not increased any more than elsewhere in the SILC spectrum for intensive interface stressing, indicating that the defect level is indeed present through the bulk HfO_2.

The TDDB statistics we have obtained can be explained if these traps are the ones responsible for the breakdown behavior. As shown in figure 8b, a trap generation rate of 0.6 is measured at the lowest stress condition. Thus a 3 trap breakdown path with this generation rate would result in a Weibull slope of 1.8, in line with the value we have measured.

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Further investigation of this defect level shows an increased sensitivity to temperature. Measurements show an activation energy of 0.6eV for a sense voltage of -0.7V compared with 0.4eV at 0.5V sense. Figure 9 shows the SILC generation rate as a function of temperature for the two sense voltage during a 100s stress at a number of stress conditions. At room temperature and the lowest stress condition, both sense voltages show a SILC generation rate of ~0.4. This consistent with the Weibull slope of a TDDB distribution at room temperature of 1.22 and again indicates a 3-trap breakdown.

For the 125°C case, the single trap SILC generation rate at the lowest stress condition is again consistent with the defect at -0.7V resulting in the breakdown of the oxide, and at 175°C we can see single trap SILC dominant for both sense conditions at low stress voltage, and the dominance of 2-trap SILC at V_{stress}=1.4V where the SILC generation rate in each case is 2x the trap generation rate. The emergence of new defect generation mechanisms at elevated temperature in high-k materials has previously been reported in [13] and the current results show the effect is still apparent in thinner high-k layers without an interfacial SiO_2.

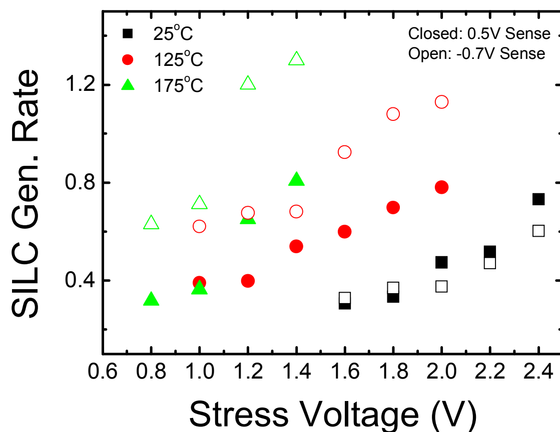

Figure 9. SILC GENERATION RATES EXTRACTED FROM A 100S STRESS AS A FUNCTION OF TEMPERATURE FOR TWO DIFFERENT SENSE VOLTAGES. THE DEFECT SENSED AT -0.7V IS MORE TEMPERATURE SENSITIVE THAN THAT AT 0.5V.

V. CONCLUSION

TDDB studies of high-performance HfO_2 based nMOSFETs show maximum operating voltages in excess of 1V. Within error-bar, the SiGe substrate devices show identical reliability to those with Si substrates. SILC measurements to analyze the defect generation behavior show a voltage and temperature dependent SILC generation rate and suggest that the defect which causes the breakdown is located deep in the silicon bandgap and is highly temperature sensitive. The high trap generation rate associated with this defect leads to an increased Weibull slope during TDDB experiments which in turn drives the high maximum operating voltage.

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