Degradation and breakdown characteristics of thin MgO dielectric layers

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MgO has been suggested as a possible high-*k* dielectric for future complementary metal-oxide semiconductor processes. In this work, the time dependent dielectric breakdown (TDDB) characteristics of 20 nm MgO films are discussed. Stress induced leakage current measurements indicate that the low measured Weibull slopes of the TDDB distributions for both *n*-type and *p*-type devices cannot be attributed to a lower trap generation rate than for SiO_2. This suggests that much fewer defects are required to trigger breakdown in MgO under voltage stress than is the case for SiO_2 or other metal-oxide dielectrics. This in turn explains the progressive nature of the breakdown in these films which is observed both in this work and elsewhere. The reason fewer defects are required is attributed to the morphology of the films. © *2010 American Institute of Physics.* [doi:10.1063/1.3265434]

I. INTRODUCTION

Magnesium oxide has recently garnered attention as a possible mid-*k* material to serve as the gate dielectric in complementary metal-oxide semiconductor (CMOS) processes, both on Si and III-V substrates.[1] Among the attractive properties of the material are its wide band-gap (7.3–7.8 eV) which is important to maintain a sufficient barrier to carrier tunneling, its high dielectric constant (up to 10)[2] and breakdown field (12 MV/cm) and most interestingly its ability to form a high quality abrupt interface with Si without the presence of an interfacial silicon oxide which has the potential to minimize the equivalent oxide thickness.[3] In this work, we examine the electrical characteristics of thin (20 nm) MgO films fabricated into both *n*- and *p*-type capacitors on silicon substrates. The study focuses on the time dependent dielectric breakdown (TDDB) behavior of the films under constant voltage stress (CVS). Miranda *et al.*[4] have shown that the possibility for progressive breakdown exists in identical 20 nm MgO based capacitor structures and the possible reason for this is identified.

For any material to be considered as a possible gate dielectric for future CMOS processes, it is vitally important that during accelerated lifetime tests it displays breakdown characteristics that will ensure a lifetime in excess of 10 years when extrapolated back to the low oxide field range which the layer will be subject to during operation. In the next section, the growth process for the MgO based capacitors used in the study, and the experimental methodology used in the TDDB evaluation are outlined. In Sec. III, we present the results of the study for both *p*-type and *n*-type devices and discuss the significance of the observed TDDB behavior and the very different behavior of the MgO layers when compared to conventional SiO_2 or metal oxide based high-*k* layers.

II. EXPERIMENTAL

n-type and *p*-type (100) silicon wafers with a dopant density of $10^{15}/cm^3$ were dipped in a 5% HF solution, rinsed with deionised water and dried in nitrogen to achieve a clean hydrogen terminated silicon surface. The wafers when then loaded to the deposition chamber where 20 nm MgO films where deposited by e-beam deposition from polycrystalline 99.99% pure MgO pellets at 180 °C and 1×10^{-6} mbar. The growth rate was 0.2 Å/s. MOS structures were formed using a fully silicided (FUSI) gate process where the MgO was capped with 100 nm of amorphous silicon to prevent ambient exposure of the film. Nickel was then deposited onto the amorphous silicon using *ex situ* e-beam evaporation to a thickness of ~80 nm through a patterned resist mask and subsequent lift off process. The FUSI gates were then formed by a rapid thermal anneal process at 500 °C for 30 s in an N_2 ambient. A transverse electron microscope (TEM) image of the 20 nm MgO is shown in Fig. 1. The image shows an abrupt interface between the silicon substrate and the bulk MgO film with no interlayer formation. The measured physical thickness of the MgO film is 21.7 nm with good thickness uniformity.

TDDB measurements were performed on both the *p*- and *n*-type capacitors. The devices were square gated capacitors with an area of 1.6×10^{-5} cm^2. In both cases 16 capacitors were subjected to CVS in accumulation at 4 different stress voltages to ensure accurate extraction of the TDDB Weibull slope and to allow a reliable lifetime extrapolation to be made. Only devices whose initial leakage was within ~10% of the mean value were included in the statistical analysis to
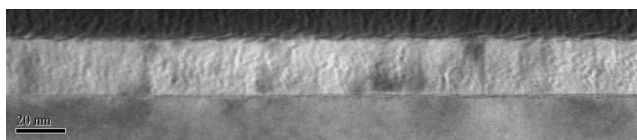

FIG. 1. TEM image of the 20 nm layers used in this work, showing a small interfacial oxide region and good thickness uniformity.
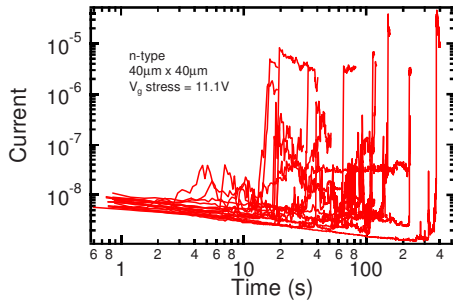
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FIG. 2. (Color online) *I-t* traces for 20 nm MgO layers during a CVS at V_g=11.1 V. The devices exhibit progressive breakdown behavior, usually not seen for layers >5 nm thick.

ensure that thickness uniformity effects were minimized. The use of 64 samples allows for an error of less than 10% in the accuracy of the extraction of the TDDB Weibull slope.[5]

III. RESULTS AND DISCUSSION

Figure 2 shows a set of current-time (*I-t*) traces from CVS measurements made at V_g=11.1 V on an *n*-type capacitor. Each *I-t* trace features an initial current decrease attributable to the trapping of negative charge during the stress which is described by a power law. As the stress continues the generation of defects in the layer becomes evident and the decline in leakage current slows due to the stress induced leakage current (SILC) component.[6] As this continues, the formation and wearout of leakage paths in the film leads to an eventual catastrophic breakdown.

Such progressive breakdown is not ordinarily seen in layers of this thickness. In the case of SiO$_2$ layers with a thickness in excess of ~5 nm, the *I-t* trace generally consists of the charging phase then a sudden hard breakdown with a current rise into the milliamp range corresponding to the formation of a leakage path and almost instantaneous thermal runaway.[7] The progressive breakdown behavior (also reported in Ref. 4) for such a thick layer suggests differences in the defect generation mechanism in MgO.

A complete TDDB Weibull distribution for an *n*-type device is shown in Fig. 3. Due to the progressive nature of the breakdown, we used a current step algorithm where the first current jump of a given magnitude in the *I-t* trace acts as trigger for the breakdown detection. During this process, the software filters out single point current spikes which will

lead to erroneous detection of the breakdown. In the case of Fig. 3, a current step trigger of 40 nA is taken as breakdown trigger which, as can be seen from Fig. 2, corresponds to a level where most samples have undergone hard breakdown.

The time-to-breakdown (t_{BD}) Weibull distributions were fitted with the maximum likelihood method, to ensure accurate extraction of the Weibull slope (β) and the 63%-value (η). The exponent of the power law fit to this data is defined as the voltage acceleration factor (γ). For the case of the *n*-type capacitors, the Weibull slope of the distribution is 1.01 which is very low for a layer of 20 nm thickness. For SiO$_2$ of similar thickness, a Weibull slope in range of 11–15 can be expected, as explained in the next section.

To further understand the origin of the low β, it is necessary to understand its physical significance. According to the percolation model of oxide defect generation,[8] breakdown times in the gate dielectric are statistically distributed, because traps are formed within the layer at random locations and so there is a distribution in the total trap density at which a conductive filament from anode to cathode will form. It is evident that this distribution is controlled by both the trap generation rate and the number of traps required to form the conductive filament.

The trap density D_{ot}, at which breakdown occurs is Weibull distributed with a slope β_{ot} equal to the number of traps in the path. Furthermore, it is assumed that $D_{ot}=c \cdot t^m$, with m as the (logarithmic) trap generation rate and "t" as the stress time. With this formula it is easily proven that the t_{BD}-distribution is Weibull distributed with slope $\beta=m \cdot \beta_{ot}$. For conventional SiO$_2$ layers, m is between 0.5 and 0.7, and β_{ot} is a function of oxide thickness. The percolation model suggests that the "percolation distance" of a single trap is ~0.9 nm and so for our 20 nm layers, a β_{ot} of ~22 (a 22 trap chain should be required to trigger the breakdown) would be expected and when combined with a trap generation rate of ~0.5−0.7 this yields an expected Weibull slope of between 11 and 15.

The reason for the unusually low measured β in this case can thus be explained in two ways. Either the trap generation rate in MgO is much lower than that for SiO$_2$, or the number of traps required to cause breakdown in the MgO layer is lower. In order to discriminate between these two possibilities, a further investigation of the low Weibull slope was carried out by performing the statistical analysis for a number of different breakdown triggers. During the buildup of traps in a dielectric, the prebreakdown Weibull slope is characterized by the number of traps in the percolation paths within the oxide.[9–11] For example, very early in a stress where the trap generation rate is 0.5, conduction through single trap conduction paths dominates and consequently the measured t_{BD} Weibull slope will be 0.5. As the stress continues and the leakage current increases, the Weibull slope will reflect the onset of conduction through chains of 2 or more traps and if we examine several subsequent current steps, we can construct a plot of β versus current step height as shown schematically in Fig. 4(a).[12]

The experimental data for the 20 nm MgO layers used in this work is shown in Fig. 4(b). The Weibull slope increases in a single step from ~0.6 for the smallest current step to 1
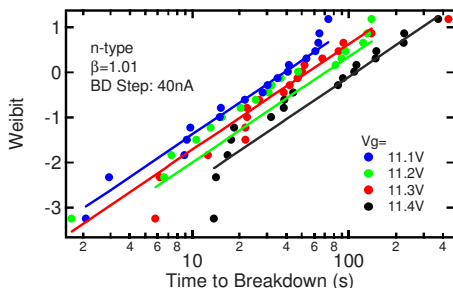

FIG. 3. (Color online) Time to breakdown distribution for the *n*-type devices using a current step height of 40 nA to trigger the breakdown. The Weibull slope of the distribution is 1.01, much lower than the expected value of 12–15.
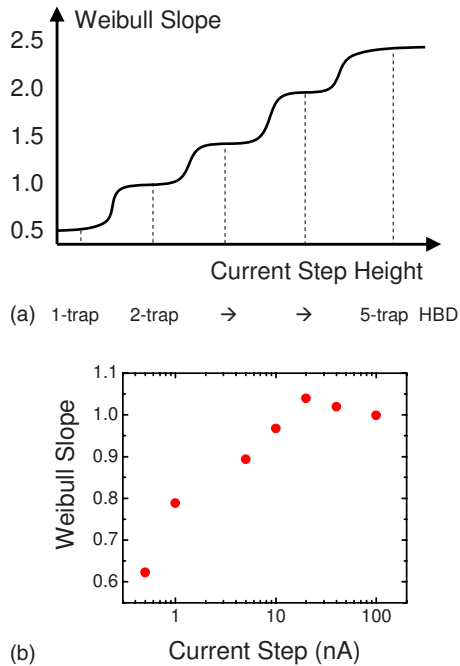
FIG. 4. (Color online) (a) Schematic diagram of the Weibull slope increase as a function of breakdown step height showing plateaus in the region where single trap and two-trap conductions dominate the gate current, as predicted by the percolation model. (b) β vs current step height for our samples showing the increase of β from 0.6 to 1 in a single step indicating a single transition from single trap to two-trap conduction, where hard breakdown occurs.

for hard breakdown. This behavior is illustrative of a two-trap hard breakdown path, significantly less traps than are required in conventional gate dielectric materials.

To verify this observation we examined the SILC in the MgO layers. The SILC is known to provide a reliable measurement of the buildup of neutral electron traps in the dielectric during stress and so can be used to identify the trap generation rate.[6] To extract the trap generation rate we take the *I-t* trace for a CVS and normalize the gate current to the $t=0$ value. We then correct for the charge trapping component by subtracting the straight line tangential to it as shown in Fig. 5(a). The resulting curve [Fig. 5(b)] is the pure leakage current through the layer as a function of time and the slope of this curve represents the SILC generation which as mentioned, is used as a measure of neutral trap generation in the oxide.

Figure 6 shows the resultant curves for three stress voltages for the *n*-type capacitors. They display a consistent generation rate, independent of stress voltage of ~0.5. Similar values were also extracted for the *p*-type capacitors. This measurement verifies that the defect generation rate in MgO is very close to that measured in SiO_2 and consequently that the two-trap breakdown suggested by the Weibull slope as a function of current step correctly describes the t_{BD} data.

The possible explanation for so few traps being required to break the oxide lies in the TEM image in Fig. 1. The bulk MgO takes on a columnar grained morphology and it is likely that the grain boundaries which form between the columns are conductive as is the case with other crystalline high-*k* materials. Several studies[13,14] have shown that MgO films adopt this structure even when grown by other methods
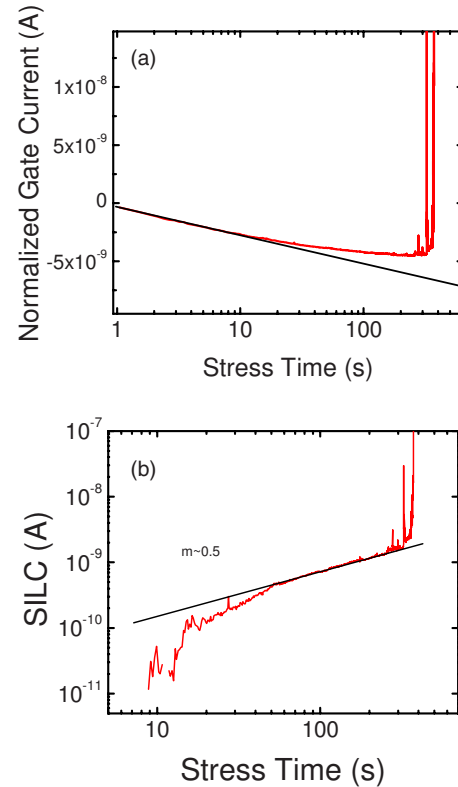

FIG. 5. (Color online) To extract the pure SILC component from the *I-t* trace, (a) the charging component is fitted with a power law and (b) this component is subtracted leaving the SILC which can be fitted to extract the defect generation rate in the dielectric.

such as metal-organic chemical vapor deposition (MOCVD).[15] When a defect forms in the oxide, it can then use these boundaries as conductive "stepping stones" to other defects and depending on the length of the grain boundaries, this will drastically reduce the density of defects necessary to break the layer. In this case, the length of the grain boundaries traverses almost the entire film from anode to cathode, reducing the number of defects required to form a breakdown path from ~20 to just 2 and exhibiting the progressive degradation characteristics of an ultra thin layer.

Unless the material can be grown in a manner that minimizes grain boundaries this property will act as a fundamental barrier to the incorporation of MgO dielectric layers to CMOS processes.
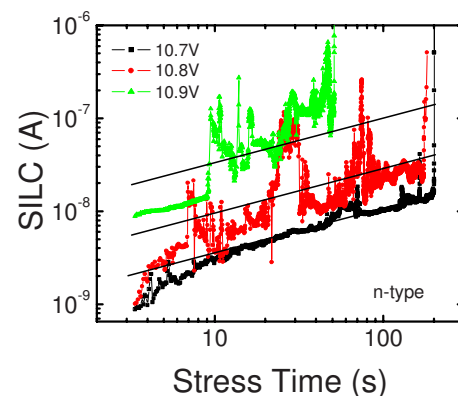

FIG. 6. (Color online) The fitted SILC components for an *n*-type device shows a defect generation rate of ~0.5 independent of voltage

IV. CONCLUSIONS

The TDDB characteristics of thin MgO layers were studied. The distributions for both nMOS and pMOS devices showed very low Weibull slopes characteristic of a 1–2 nm layer of conventional high-*k* material. The *I-t* traces also showed progressive breakdown and not the expected catastrophic hard breakdown. Analysis of the *I-t* traces showed a SILC generation rate of ~0.5 which pointed to very few defects being required to cause breakdown.

The reason why so few defects are required was attributed to the films' columnar grain morphology in which the grain boundaries serve as high-leakage paths linking the stress induced defects and triggering breakdown at a very low defect density. This property of MgO independent of growth method suggests that it is not suitable as a single material high-*k* dielectric for use in CMOS processes.

ACKNOWLEDGMENTS

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