

**EXAMINATION OF SOLDER BUMP REFLOW
PROCESS AND COPPER METALLISATION PROCESS
INDUCED STRESS DISTRIBUTION IN SILICON
SUBSTRATES USING SYNCHROTRON X-RAY
TOPOGRAPHY, MICRO-RAMAN SPECTROSCOPY
AND FINITE ELEMENT MODELLING**

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I hereby certify that this material, which I now submit for assessment on the programme of study leading to the award of Doctor of Philosophy is entirely my own work and has not been taken from the work of others save and to the extent that such work has been cited and acknowledged within the text of my work.

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ABSTRACT

Due to the fact that semiconductor devices have decreased significantly in geometry and increased enormously in electronic design complication, flip-chip packaging technology was launched to increase input/output (I/O) count, improve electrical performance, reduce packaging size, and to be cost effective. The Intel®Pentium®III microprocessor uses the popular ball grid array (BGA) packaging technique. The ball grid array (BGA) is one of the most common flip-chip packaging techniques used for microprocessor applications. However, mechanical stresses induced by the flip-chip process are a major concern for the reliability of such devices.

In addition, Copper (Cu) is becoming the interconnect metal of choice and is rapidly replacing Aluminium alloys (Al/Cu) in the Integrated Circuit (IC) industry. However, mechanical reliability issues, such as those related to thermal strain are also a major concern.

The aim of this thesis is to employ the application of white beam synchrotron x-ray topography (WBSXRT), micro-Raman spectroscopy (MRS) and Finite Element Modeling (FEM) to investigate the spatial extent of strain fields imposed on the underlying silicon substrate for microelectronic packaging of Intel®Pentium®III microprocessors due to the lead-tin solder bump process for BGA packaging, and to evaluate and compare stress distributions in Si wafers due to the electroless Cu interconnect process with varying geometrical line width in IC processing and compare with the sputtered Cu interconnect technique.

In the case of the lead-tin solder bump process, large area and section back-reflection SXRT images were taken before and after a simulation of the reflow process at 350°C in atmosphere. The effects of strain imposed by the overlying bump structures in these x-ray topographs have been observed principally via orientational contrast. The estimated magnitudes of stress, $|\tau_{xy}|$, imposed on the underlying silicon were

calculated to be of the order of 100 MPa. A simulation of the orientational contrast at the edge of bump was performed based on the kinematical theory of x-ray diffraction. The degree of lattice distortion is well fitted to the topographs of the *post*-reflow sample. The spatial strain in the underlying silicon was relieved dramatically after the lead bumps were removed from the wafer, which confirms that the solder bump formation is indeed a major source of strain in the underlying Si.

Micro-Raman Spectroscopy (MRS) is used to confirm the strain fields in the Si due to the reflow process. For *pre*-reflowed samples, an approximate uniaxial compressive stress (σ_{xx}) of 200 MPa is developed near the edge of the under bump metallisation (UBM). However, a tensile stress (σ_{xx}) up to ~300 MPa is found for *post*-reflowed samples.

Two-dimensional (2-D) plane strain Finite Element Modelling (FEM) has also been performed. The magnitudes and spatial distribution of the stresses after the reflow process are in good agreement with the SXRT and MRS results.

In case of the Cu metallization, 100 nm of Ti is used as a barrier layer and 20 nm of sputtered Cu is used as a seed layer. Electroless and sputtered Cu were subsequently deposited on patterned Si wafers with 4, 6, 8, 10, 20, 40, 60 and 100 μm line widths using a lift-off patterning and single damascene pattern.

The presence of distinct orientational contrast observed in section topographs suggests that the strain fields in the Si substrate reach values as high as ca. 100 MPa nears the metal edge. The stress magnitudes in the underlying Si as a function of individual line widths were measured using MRS. Compressive stresses of ~100 MPa were found in the Si wafer near the line edges when the width is less than 10 μm . The stresses changed to tensile with a magnitude of the order of 100 MPa at metal widths of 10-60 μm and decreased to ~50 MPa for 100 μm widths. The FEM analysis confirmed this tendency.

Large area back-reflection WBSXRT revealed that strain fields in the Si due to the Cu metallisation were relieved when the sample was heated to 100°C. Subsequently, the stress increases again when the sample was heated up to 400°C.

When the samples are returned to room temperature, the MRS data confirms that the strain in the Si near the metal edges become more compressive than in the unannealed case. X-ray diffraction (XRD) data confirms the generation of new material phases after the heat treatment.

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- A1: Investigation of Mechanical Stresses in Underlying Silicon due to Lead-Tin Solder Bumps via Synchrotron X-Ray Topography and Finite Element Analysis, MRS Spring Meeting, Mat. Res. Soc. Symp. Proc. Vol. 682E, N5.7, 2001.
- A2: Evaluation of Mechanical Stresses in Silicon Substrates due to Lead-Tin Solder Bumps via Synchrotron X-Ray Topography and Finite Element Modeling, Microelectronic Engineering, Vol. 65, 2003, pp. 209-221.

- A3: Examination of Mechanical Stresses in Silicon Substrates due to Lead-Tin Solder Bumps via Micro-Raman Spectroscopy and Finite Element Modelling, Will be published in Semiconductor Science and Technology.
- A4: White Beam Synchrotron X-Ray Topography Studies of Pb/Sn Ball Grid Array Induced Strain in Si Substrate, Hamburger Synchrotronstrahlungslabor HASYLAB am Deutschen Elektronen-Synchrotron DESY, User Meeting, 2000, http://www-hasylab.desy.de/science/annual_reports/2000_report/.
- A5: White Beam Synchrotron X-Ray Topography Studies of Copper interconnect in IC processing Induced Strain in Si Substrate, Hamburger Synchrotronstrahlungslabor HASYLAB am Deutschen Elektronen-Synchrotron DESY, User Meeting, 2001, http://www-hasylab.desy.de/science/annual_reports/2001_report/.
- A6: Mapping of Mechanical Stresses in Silicon Substrates due to Lead-Tin Solder Bump Reflow Process via Synchrotron X-Ray Topography and Finite Element Modeling, will be published in Journal of Applied Physics: D.
- A7: Estimation of Mechanical Stresses in Silicon Substrate due to Lead-Tin Solder Bumps via Synchrotron X-Ray Topography, Micro-Raman Spectroscopy and Finite Element Modeling, waiting for review in IEEE Transactions in Electronic Devices.

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List of Abbreviations

m_0	electron's rest mass
c	velocity of light
λ	x-ray radiation wavelength
θ_B	Bragg angle
\mathbf{k}	wavevector
\mathbf{k}_0	wavevector outside the crystal in the direction of incident beam
\mathbf{k}_H	wavevector outside the crystal in the direction of diffracted beam
\mathbf{K}_0	wavevector inside the crystal in the direction of incident beam
\mathbf{K}_H	wavevector inside the crystal in the direction of diffracted beam
χ	electric susceptibility
\mathbf{S}	Poynting vector
μ_0	linear absorption coefficient
$\Delta\phi$	divergence of the incident x-ray beam
$\Delta\theta_B$	effective misorientation
t_p	penetration depth
\mathbf{g}	the diffraction vector
\mathbf{H}_i	unit vector normal to the film edge and point away from film edge
σ_i	normal stresses in i direction
τ_{ij}	shear stress
ε_i	normal strain
γ_{ij}	shear strain
E	Young's modulus
ν	Poisson's ratio
G	shear modulus of elasticity
ω	scattering frequency
\mathbf{P}	polarisation of radiation
\mathbf{R}_j	Raman tensor of phonon j
\mathbf{e}_0 and \mathbf{e}_s	polarisation vectors of incident and scattered lights, respectively
CCD	charge-coupled device

CID	charge-injection device
PCB	printed circuit board
FCOB	flip-chip on board
KGD	known good die
KGB	known good board
SMT	surface mount technology
BGA	ball grid array
FBGA	flip-chip ball grid array
FPGA	flip-chip pin grid array
FCSP	flip-chip scale packaging
CTE	coefficient of thermal expansion
UBM	under bump metallisation
BLM	ball limited metallurgy
E3	evaporated, extended eutectic
C4	controlled collapse chip connection
SXRT	synchrotron x-ray topography
MRS	micro-Raman spectroscopy
XRD	x-ray diffraction
FEM	finite element modelling
BRT	back-reflection topography
BRST	back-reflection section topography
LAT	large area transmission topography
ST	section transmission topography
TEM	transmission electron microscopy
ILD	interlevel dielectric
EM	electromigration
CVD	chemical vapour deposition
PVD	physical vapour deposition
CMP	chemical.mechanical planarisation
RIE	reactive ion etching
ECD	electrochemical deposition
AFM	atomic force microscopy

CHAPTER 1 INTRODUCTION

1.1 Background

As microelectronics device features become smaller and smaller with an increase in complexity, functionality and higher levels of performance, the intricacy of metal interconnect and semiconductor-packaging technology grows proportionally. With an enormous number of functions integrated on a silicon chip, manufacturers face novel and increasingly challenging electrical interconnect issues. To accommodate the use of the die efficiently, each level of electrical interconnects between the die and from the die to the package must also keep pace with these revolutionary devices. At present, submicron feature sizes at the die level are driving the package size down significantly. The idea of attaching the semiconductor die directly to the substrate (Printed Circuit Board, PCB) by introducing the flip-chip technology, which simply turns the chip upside down so that its termination can be connected directly to the pads on the substrate [1], has been in existence for some time. With this technique the IC package is omitted, saving cost, space and weight. The concepts were advanced by IBM [2] and AT&T more than 30 years ago as they developed flip-chip and beam leaded die respectively. Originally, it was used in mainframe computers, the military, and specialist applications, but more recently in mobile phones, smart cards, disc drives and automotive electronics. However, there are number of issues that prevent flip-chip technology from becoming dominant. Firstly, a concern regarding the long-term reliability issues and, secondly, mechanical stress. The deposition of Under Bump Metallisation (UBM) and solder bump followed by solder reflow process at high temperature, has lead to a high mechanical stress induced in the underlying silicon, as a result of the differences in Coefficient of Thermal Expansion (CTE) of those materials. These factors, coupled with the lack of standardisation (i.e. commitment to fixed bump pattern footprint and matching substrates) have prevented this technology from proliferating.

The solder-bumped flip chip was introduced by IBM in the early 1960s, becoming the logical foundation of the IBM System/360 computer line. The so-called C4

(controlled-collapse chip connection) technology utilizes solder bumps deposited on wettable metal terminals on the chip and a matching footprint of solder wettable terminals on the substrate. The solder-bumped flip chip is aligned to the substrate, and all solder joints are made simultaneously by reflowing the solder [5]. The solder materials IBM used are usually the 5wt% Sn / 95wt% Pb solder, which has solidus and liquidus temperatures of 308°C and 312°C, respectively. Alternatively, IBM also employed 3wt% Sn / 97wt% Pb solder, which has solidus and liquidus temperatures of 314°C and 320°C, respectively. During the reflow process, the surface tension of the molten solders controls the height of the joint flip-chip connection and supports the weight of the chip. In addition, the chip will self-align to the substrate; this leads to a very high-yield manufacturing process [5].

However, the advantages offered by the flip-chip technology are such that industry is pushed to further develop and refine this technique. The increasing demands for cheaper, smaller, and higher performance of electronic products have made flip-chip a package of choice. The difference between flip-chip and other direct chip attach techniques, such as wire bonded chip on board, is that flip-chip packages offer an option to move from peripheral terminations to area array terminations. As a result, the number of I/O counts increase significantly with the same die area. It is estimated that [6] 40% of the semiconductor industry costs are in packaging and substantial cost savings can be achieved by switching to an unpackaged die.

As flip-chip awareness increases and the support infrastructure comes to maturity, the undoubted size, weight and performance benefits of the “ultimate packageless package” could well make this a dominant technology [1].

Worldwide consolidated efforts between academia and industry are directed to overcome the difficulties associated with the flip-chip technology. Issues arising from the mismatch of the Coefficient of Thermal Expansion (CTE) between silicon die, UBM, and solder bumps has led to a high mechanical stress induced in the silicon.

Recent advances in electronics have blurred the divide between chip manufacture and assembly. As the drive towards greater integration continues and the precision of tracking, alignment and placement improves, the idea of omitting the IC package and mounting the chip directly on the board becomes quite feasible, thus making the issue of product reliability paramount.

Since the 1960s, the use of semiconductor devices increased significantly as a result of improvements in terms of miniaturization (more devices packed on the die), better performance (higher speed), higher functionality in the chip and low effective costs. This is partly a result of the improvements in materials processing such as device insulators and metals. Basically, the material, which is selected to be the metal interconnect, should have low resistivity and a low temperature coefficient of resistance. In addition, the metal should be easy to deposit on a planar surface with a high deposition rate, be easy to etch and planarize, be oxidation and corrosion resistant, (i.e. low chemical reactivity), be mechanically stable, (i.e. low stress and high stress migration resistance), possess a high melting point for high electromigration resistance, be compatible with encompassing materials, be an environmentally safe material during processing and use, and be reliable and cheap. To achieve faster devices, reduction in resistance (R) and Capacitance (C) of the metal interconnect is inevitable. IC interconnect manufacturing technology had been dominated by the use of Aluminium (Al) until 1999. However, the continuity in size reduction of the devices has led to a fundamental discrepancy between device and metal interconnect. Therefore, a new metallisation, which has lower resistance than Aluminium, has to be used. Copper has been seen as an ideal metal to replace Aluminium according to its physical properties. The new era of interconnect manufacturing technology is the use of Copper as a metal interconnect. Although copper metallization is now well positioned to take over as the main on-chip conductor for integrated circuits (ICs), issues such as thermal stress cannot be ruled out. Thermal stresses in copper are larger than for traditional Al, Ag or Au based metallization schemes, because of the greater differential in Young's Modulus (E) between Cu and the Si substrate or deposited dielectrics. Thus there is a concern for enhanced stress related failures in Cu-based metallization [13]-[14]. To date, few if

any studies have been carried out on the build-up of such stresses at device operating temperatures or at accelerated (high temperature) conditions.

To study the stress in underlying silicon due to IC processing, three important techniques, synchrotron x-ray topography (SXRT), micro-Raman spectroscopy (MRS), and finite element modelling (FEM), were employed. Synchrotron x-ray topography (SXRT) was used for visualisation of strains imposed on silicon wafers due to fabrication of Cu-based lines and the flip-chip reflow process. Micro-Raman spectroscopy was employed to confirm the strains in the underlying Si. FEM modelling was carried out to compare with those results and to improve understanding of these structures.

SXRT is a *non-contact, non-destructive* characterization tool able to track an individual wafer from virgin substrate to completed device or circuit, providing a comprehensive 3-dimensional stress/strain and/or dislocation map due to each fabrication level. It is a straightforward technique in which an intense, highly collimated beam of x-rays generated by synchrotron-accelerated charged particles is directed at a crystalline sample in a simple set-up, i.e. Laue or Bragg configurations. All kinds of defects or imperfections such as precipitates, inclusions, dislocations, oxide/overlayer edges and epitaxial layers can be observed in the single crystal materials. Geometrical resolution is governed by the incident beam local divergence on the sample and, to date, usually lies in the micron range.

Micro-Raman spectroscopy is a vibrational techniques, involving the scattering of electromagnetic radiation by optical phonons in solids and molecular vibrations. The scattering of light by the solid interactions can be categorised as elastic (Rayleigh scattering) and inelastic (Raman scattering). The former scattering is observed when the scattered light is of the same frequency as the incident light, whereas the inelastic scattering is obtained at a different frequency, and produces what is termed a Raman spectrum. In this report, only inelastic scattering is emphasized.

1.2 Objectives of this project

The aim of this project is to evaluate the stress/strain imposed on Si substrates due to flip-chip reflow process and due to Cu metallization in IC processing. To examine these issues, synchrotron x-ray topography (SXRT) and micro-Raman spectroscopy (MRS) were employed. Both results were compared to the finite element modelling (FEM) in order to understand the behaviour of the materials due to the elevated temperature. Finally, x-ray diffraction (XRD) was used to examine the material compounds which could be related to the major sources of strain in the Si wafer due to these processes.

The objectives of the study of the flip-chip reflow process are divided into three main categories as follows:

- (a) To study the stress distribution in the silicon substrate due to C4 metal etching times, four different samples which were etched for 10, 15, 25 and 35 minutes as sample wafer numbers 511, 509, 424 and 445, respectively, were prepared by Intel Ireland. This sample category was observed using SXRT only.
- (b) To study the stress distribution in the silicon substrate due to the reflow process, the *Pre*-reflow process samples from (a) were examined, and subsequently were reflowed using a simulated process at 350°C in atmosphere and are thus defined to be *post*-reflowed process samples.
- (c) To study the major source of strain distribution in the silicon substrate, the Pb/Sn bumps on both the *Pre*- and *post*-reflowed process samples were removed and investigated using SXRT and MRS.

The objectives of the study of Cu metallisation are divided into three categories:

- (a) To examine electroless Cu metallisation induced strain distributions in Si wafers in IC processing and to relate the strain fields to the curvature of the lattice planes based on the work of Meieran and Blech [15].

- (b) To compare the strain fields in Si substrates caused by electroless and sputtered Cu metallisation for both lift-off and single damascene patterns at *Pre*- and *Post*-metallisation steps using SXRT and MRS.
- (c) To study the influence of elevated temperatures, i.e. 100, 200, 300 and 400 °C, respectively, on the electroless and sputtered Cu metallisations for both lift-off and damascene patterns at *Pre*- and *Post*- metallisation steps using SXRT.
- (d) To study the influence of Cu line widths on the stress distributions in Si and to correlate with MRS and FEM.

1.3 Outline of this thesis

The order of this thesis is as follows:

Chapter 1 is an introduction to the project. Chapter 2 describes the theory of white beam synchrotron x-ray topography. Chapter 3 explains the finite element modelling. Chapter 4 illustrates the theory of micro-Raman spectroscopy to study stress in semiconductor materials. In Chapter 5 the evaluation of stresses imposed on Si substrates due to the flip-chip reflow process is given including experimental details, and results and discussions. Chapter 6 explains the experimental details, sample details and results and discussions for the Cu metallisation problem. Finally, a summary and conclusion is given in Chapter 7.

CHAPTER 2 SYNCHROTRON X-RAY TOPOGRAPHY

2.1 Synchrotron X-Ray Topography (SXRT)

In the 1930's, the first X-ray topograph was reported as a map of the scattered diffracted beam across a crystal position, an explanation for which was based on the theory of x-ray diffraction for a variation of the diffracted intensity as a function of position in a crystal [15]. However, the experiments were slow and the topographs were unable to resolve crystal dislocations clearly due to poor spatial resolution and the overlap of Laue spots (the array of spots formed by the diffracted beams on a recording film). To improve the quality of the x-ray topograph, the x-ray beam must be large and the distance between the sample and the x-ray source must be significantly long. The examination of this spatial resolution will be given later in this chapter. Therefore, x-ray topography with a conventional x-ray generator was not popular as a characterisation technique for single crystals. In 1974, T. Tuomi et al. [12] announced the application of x-ray topography with synchrotron radiation as the x-ray source, commonly called Synchrotron X-Ray Topography (SXRT). The experiment can be performed in only a few minutes with a high quality result. Since then, SXRT has become a popular standard characterisation technique for highly perfect crystals [15]. Two main components of the synchrotron x-ray topographic technique are described in this chapter.

2.1.1 Synchrotron Radiation (SR)

Synchrotron radiation is the electromagnetic radiation which is emitted when high-energy charged particles are accelerated in the magnetic fields of storage rings. These synchrotrons are powerful radiation sources and provide useful beams with high density, broad spectral range from the infrared through the x-ray range, collimation, polarisation, pulsed-time structure and partial coherence [17]. Compared with a conventional x-ray tube, the synchrotron radiation can produce more than ten orders of magnitude higher brightness (photons/s/unit solid angle/unit

source area/unit bandwidth) and five orders of magnitude higher flux (photons/s/mrad/unit bandwidth) as illustrated in Figure 2-1.

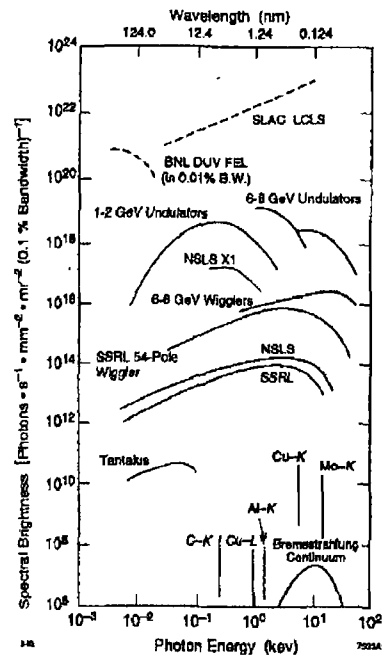


Figure 2-1 Spectral brightness from various radiation sources [18].

In Figure 2-1, it is noted that the x-ray beams with a brightness lower than 10^8 photons/s/mm²/mrad²/ 0.1%Bandwidth such as C-K, Cu-L, Al-K, etc. are generated from a conventional x-ray tube or, e.g., a Cu-K_α rotating anode x-ray tube. Figure 2-1 also shows the brightness figures for various synchrotron sources, which generate x-rays in different energy ranges, such as the NSLS (The National Synchrotron Light Source at Brookhaven National Laboratory) and the SSRL (Stanford Synchrotron Radiation Laboratory). Even though synchrotron radiation sources provide excellent radiation, some experiments need higher brightness and higher power, etc. A new light source, called the Free Electron Laser (FEL) has been invented and is under consideration as a means of meeting these requirements. The dashed lines “SLAC LCLS” (Linear Coherent Light Source) is a multi-institutional proposal for a single-pass x-ray Free Electron Laser, operating in the 1-15 Å wavelength region, using electron beams from the SLAC linac, (Stanford Linear Accelerator Centre) at energies up to 15 GeV [33]). Similarly, “BNL DUV FEL” (Deep-Ultra-Violet FEL at

Brookhaven National Laboratory) also represent future examples of the brightness potential of FELs.

Nowadays, scientists use synchrotrons as radiation sources at more than 30 rings all over the world. Examples of synchrotron radiation sources and energies are illustrated in Table 2-1.

Table 2-1 Synchrotron Radiation Sources [18].

Location	Ring	Energy (GeV)
Brazil		
Campinas	LNLS-2	2.0
China (ROC-Taiwan)		
Hsinchu	SRRC	1.3
England		
Daresbury	Sinbad	0.6
	Diamond	3.0
France		
Grenoble	ESRF	6
Orsay	SuperACO	0.8
	SOLEIL	2.15
Germany		
Dortmund	DELTA	1.5
Berlin	BESSY II	1.5-2
Hamburg	HASYLAB	4.45
Japan		
Hiroshima	HISOR	1.5
Ichihara	Nanohana	2.5
Kashiwa	ISSP	2.0
Nishi Harima	Spring-8	8
Tsukuba	NIJI IV	0.5

2.1.1.1 Synchrotron Radiation Components

A schematic of a general synchrotron system is shown in Figure 2-2 [32]. In brief, electrons or positrons are accelerated to a few tens of MeV by a linear accelerator and then increased to an energy of 2-10 GeV using a booster. These high-energy electrons/positrons are injected into a storage ring. In the storage ring, the electrons

or positrons, travelling with nearly the speed of light in ultra-high vacuum, emit synchrotron radiation. Dipole bending magnets maintain the orbital position of the electron/positron beam in this polygon storage ring, while quadrupole magnets forming a complex 'lattice' of magnets collimate the electron beam [15], [32]. Finally, the x-ray beam is carried out to the experiment hall by passing from the ring vacuum system through a beryllium window.

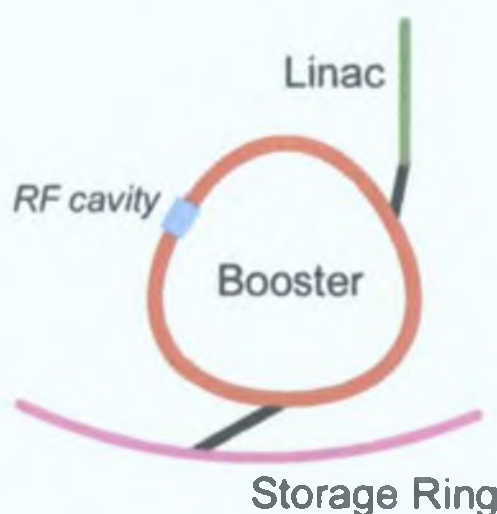


Figure 2-2 The general synchrotron source system [32].

The details of each component used in a SR source are explained as follows [17]:

(a) Injection systems

To accelerate new free electrons/positrons to the operation energy of the storage ring (E_0) with an average lifetime (τ_0), and to inject them into the storage ring, an injection system is required at the front end of the synchrotron source. The injector can be composed of a single accelerator such as a linear accelerator (linac) or a series of several accelerators, for example, a pre-injector, a main accelerator and an accumulator before the beams are delivered to the storage ring. The components of the injection system employed depend on the maximum energy and the experiments using this light source. A typical injection system used to deliver the beam to the storage ring is composed of five stages: Stage 1, an electron gun to generate free electrons; Stage 2, a first accelerator where the free electrons are bunched into a

quasi-continuous charged particle beam and accelerated to relativistic velocities ($E \gg m_0 c^2$ where m_0 = the electron's rest mass and c = the velocity of light); Stage 3, an accelerator at the final energy wherein the charged particles travel with speed $v \cong c$; Stage 4, an extraction system consisting of fast switching magnets and special bending magnets and a transfer line to the storage ring; and finally Stage 5, a system for injection into the storage ring.

(b) The storage ring

After the electrons are pre-accelerated and conveyed from the injectors, the electron bunches are delivered to the storage ring. In this ring, electrons orbit inside a high vacuum polygon-shape chamber, encircled by dipole bending magnets and they are collimated by a lattice of focusing magnets. The lattice is a series of magnetic lenses, which focus the electrons orbiting in the ring to produce an appropriate x-ray beam dimension. Therefore, the lattice controls the lifetime, the transverse size and the divergence of the beam. The lattice is the most vital part in the SR system because it decides the brightness of the beam, the beam lifetime, the emittance of the electron beam and the size and cost of the accelerator.

2.1.1.2 Emission Patterns

When synchrotron radiation is emitted from the storage ring, the quantity of emitted energy is large and relativistic effects cause the radiated pattern to form into a sharp forward cone with an opening angle ($mc^2/E = \gamma^{-1}$) as depicted in Figure 2-3 [18]. This implies that at higher radiated energy, the opening angle is smaller.

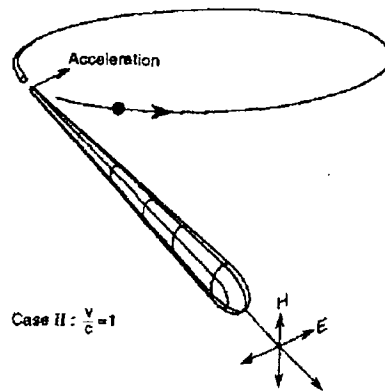
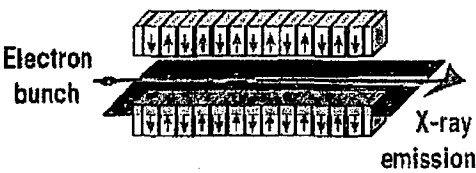


Figure 2-3 Emission pattern of the radiation when the electron/positron speed approaches the speed of light [18].

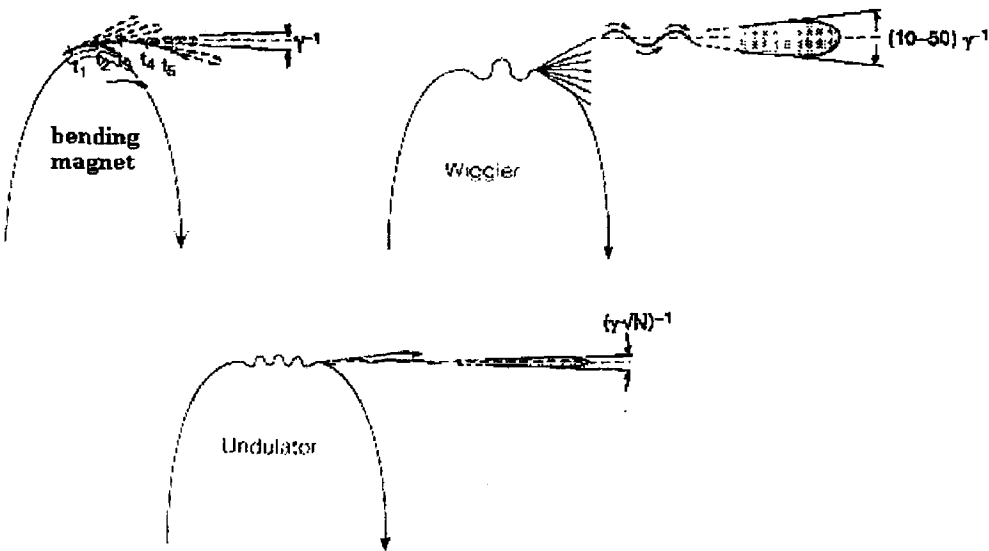
When the relativistic beam of electrons/positrons passes through a bending magnet, this sharp cone is well focussed with a small vertical opening angle, producing a continuous polychromatic beam (white beam). The flux and brightness of the emitted radiation can be enhanced by using either a wiggler magnet or an undulator magnet system, consisting of alternating polarity magnetic poles (see Figure 2-4 (a)). The radiation patterns for these wiggler and undulator insertion devices is shown in Figure 2-4 (b).

If the magnet bends the electron beam through a large angle compared to γ^{-1} (a large magnitude of oscillation), a broadband continuous radiation with high photon energy is produced. This is called a wiggler spectrum. The wiggler magnet can be placed in a straight section of a storage ring as the wiggler magnet is designed for removal of any deflections. The flux and brightness of the wiggler radiation increases by a factor approximately equal to the number of poles [18]. However, if an undulator magnet arrangement is inserted in the system, the beam is forced to bend by the order of γ^{-1} , and the radiation intensity for the consequent undulator spectrum is dramatically enhanced. Note that undulator magnet is similar to the wiggler as illustrated in Fig. 2-4(a). However, with the angle of bending of the undulator is of the order of γ^{-1} , the small divergence emission pattern of synchrotron radiation is not significantly enhanced. Hence, the intrinsic brightness of the radiation is maintained in both vertical and horizontal planes. The undulator spectrum is a pencil-shaped

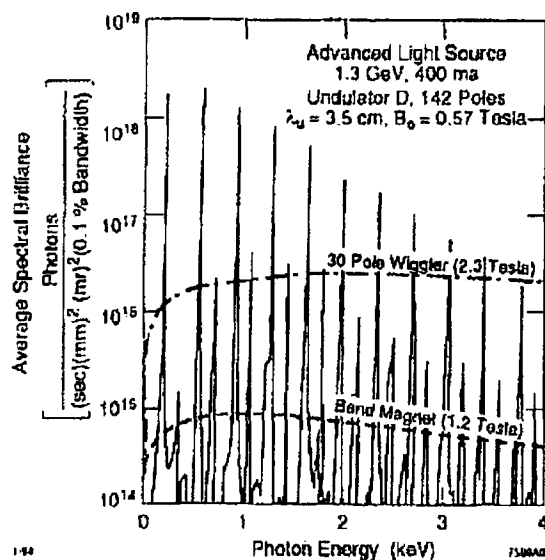
beam of photons peaking in narrow energy bands. The three emission patterns are illustrated in Figure 2-4 (c) [18].



(a)



(b)



(c)

Figure 2-4 (a) The alternating magnetic pole system used to generate wiggler and undulator radiation [32], (b) Radiation patterns of bending magnet (white beam), wiggler and undulator [18], and (c) Emission spectra of bending magnet (white beam), wiggler and undulator [18].

2.1.1.3 Synchrotron radiation: Advantages for X-Ray Topography

The advantages of synchrotron radiation over a conventional x-ray source for x-ray topography are [15]:

- Intensity of synchrotron radiation significantly reduces the exposure time during the experiment.
- Continuous spectrum in the range of $0.1 - 2.5 \text{ \AA}$ allows one to optimise geometry, absorption conditions and strain sensitivity.
- Collimated beam allows topographic experimental stations a long distance away from the generator due to their inherently low divergence. Therefore, a large area beam can impinge on the sample and large areas could be examined on the topographic film without performing scanning techniques.
- High degree of x-ray polarisation can provide topographs with high signal/noise ratio and high penetration depth in the specimen. However, this depends on the

selection of polarisation of the incident plane, either σ -polarisation, (electric vector of the x-ray wave is perpendicular to the scattering plane) or π -polarisation, (the electric vector is parallel to the scattering plane).

2.2 X-ray topography

Berg (1931) performed the first x-ray topography on a large sodium chloride crystal before and after plastic deformation. In 1945, Barrett refined Bragg's reflection technique (Bragg case). Barth and Horsemann (1958) applied Bragg's reflection technique to transmission (Laue case). In 1959, Lang introduced the projection and section topographic techniques. Later, Tuomi (1974) developed synchrotron x-ray topography providing high resolution, less experimental time and a simple set-up for sample characterisation. Since then, the methodical and instrumental developments of x-ray topography have improved significantly [34]. The experimental set-ups for these techniques will be explained briefly later in this section.

2.2.1 Theories

X-ray topographic or X-ray diffraction topographic methods are based on the diffraction of x-rays from the lattice planes (hkl) in a single crystal [34]. This technique can be used to observe strain and/or dislocations in the crystal by recording the different diffracted intensities from perfect and imperfect regions of the crystal [35].

The basis of x-ray diffraction is described in terms of Bragg's law. Generally, diffraction occurs in a crystal as shown in Figure 2-5.

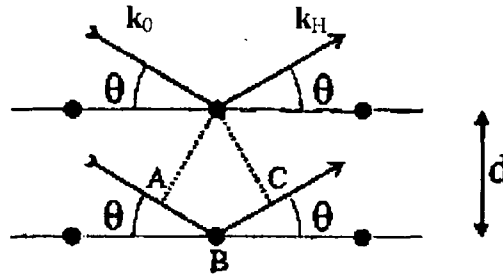


Figure 2-5 X-ray diffraction for rectangular grid case [42].

A section of the crystal in Fig. 2-5 above shows that the atoms comprise of a set of parallel planes where d is the interplanar spacing of the reflecting planes and \mathbf{k}_0 and \mathbf{k}_H are the wavevectors in the directions of the incident and diffracted beams, respectively, and $|\mathbf{k}_0| = |\mathbf{k}_H| = 1/\lambda$. It is assumed that the x-ray beams are perfectly parallel with a wavelength λ . During diffraction, the incident beams make an angle of θ_B to this crystal where θ_B is called the Bragg angle. The path difference for waves scattered by atoms from an adjacent (hkl) lattice plane with spacing d is given by

$$(AB + BC) = d \sin \theta + d \sin \theta = 2d \sin \theta \quad \text{Eq. 2- 1}$$

In addition, the scattering can be composed of overlapping rays; thus the condition for constructive interference is given by

$$n\lambda = 2d \sin \theta_B \quad \text{Eq. 2- 2}$$

where λ is the x-ray radiation wavelength, and n is the order of reflection. This relation was derived by W.L. Bragg and is known as Bragg's law [37].

Two geometrical facts obtain in this diffraction technique: (1) the angle between the diffracted beam and the incident beam is always $2\theta_B$ and (2) the incident beam and the diffracted beam are always co-planar [37].

In order to explain the changes of intensity between imperfect and defected regions in x-ray topographs, the theories of x-ray diffraction in solids are employed, i.e. kinematical and dynamical theories.

2.2.2 Kinematical theory

It is assumed that the amplitude of the x-ray beam does not change for all diffracting centres of the crystal [38]. This assumption is based on a negligible amount of energy being transferred to the diffracted beam; hence, re-diffraction effects are ignored in the approximation [15]. However, this theory is accurate only when the scattering is very weak or the crystal sample is very thin. When the crystal is thick, the dynamical theory comes into effect, since the kinematical assumption is unsatisfactory due to the extinction effect [15]. The most important parameter to explain in the kinematical theory is the structure factor, F_{hkl} ($|F_{hkl}|$ is the amplitude ratio of the wave scattered by the atoms of a unit cell to the amplitudes of the wave scattered by one electron). The structure factor for the hkl reflection is given by [16]

$$F_{hkl} = \sum_i f_i \exp\{-2\pi i(\mathbf{k} \cdot \mathbf{r})\} \text{ or}$$

$$F_{hkl} = \sum_i f_i \exp\{-2\pi i(hu + kv + lw)\} \quad \text{Eq. 2- 3}$$

where \mathbf{k} is the wavevector scattered from two points in the unit cell which are separated by a vector \mathbf{r} , f_i is the atomic scattering factor of atoms of type i with a fractional coordinate (uvw) which is defined from the origin of the unit cell to the atom of type i . The f_i is normally derived in terms of the scattering of an individual free electron. Thus, the intensity I scattered by an electron with an angle $2\theta_B$ relative to the incident intensity I_0 is

$$\frac{I}{I_0} = \frac{C^2 r_e^2}{R^2} \quad \text{Eq. 2- 4}$$

where R = the distance from the observation point to the particle, r_e = the classical electron radius in cgs unit and C = polarisation factors, i.e. $C = 1$ for σ -polarisation and $C = \cos 2\theta_B$ for π -polarisation. The atomic scattering factor can be written by

$$f_i = \int_{space} \rho(r) \exp(2\pi i \mathbf{Q} \cdot \mathbf{r}) dV \quad \text{Eq. 2-5}$$

where $\rho(r)dV$ is the probability that an electron lies in a volume element dV of the atom at a radial distance r from the nucleus. From Figure 2-6, the scattering vector $\mathbf{Q} = \mathbf{k}_H - \mathbf{k}_0$ where \mathbf{k}_0 = the incident beam vector, \mathbf{k}_H = the scattering beam vector.

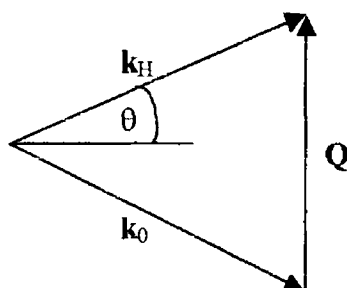


Figure 2-6 The vector relationship between the incident vector \mathbf{k}_0 , the scattered beam vector \mathbf{k}_H and the scattering vector \mathbf{Q} [15].

The diffracted intensity from a thin crystal can be examined [15] by

$$J = \sum_i \exp(2\pi i \mathbf{r}_i \cdot \mathbf{Q}) \quad \text{Eq. 2-6}$$

where J = amplitude of the wave due to the interference of waves scattered from all the unit cells in the crystal. Thus, the overall scattering amplitude, $A = F_{hkl}J$ and the intensity $I = A^2$.

It must be emphasised that the diffraction can occur only when the Bragg law is satisfied. Therefore, it can be written that $Q = 1/d_{hkl}$ where d_{hkl} is the spacing of a plane with Miller indices hkl , and the structure factor is not zero. If $|\mathbf{h}| = 1/d_{hkl}$, thus $\mathbf{Q} = \mathbf{h}$, where \mathbf{h} is the reciprocal lattice vector of the crystal.

2.2.3 Dynamical theory

The dynamical theory evolved in order to solve for errors in the assumptions of the kinematical theory, which cannot be used for thick and highly absorbing crystals, especially those crystals employed in the semiconductor industry. The diffracted

intensity of x-rays as a function of thickness becomes non-linear for those crystals. The assumption of the dynamical theory is that the re-diffraction phenomena can occur from the same reflecting planes, providing they are at the correct angle as illustrated in Figure 2-7 [15]. The energy is spread throughout the crystal thickness in a triangular area known as the Borrmann fan.

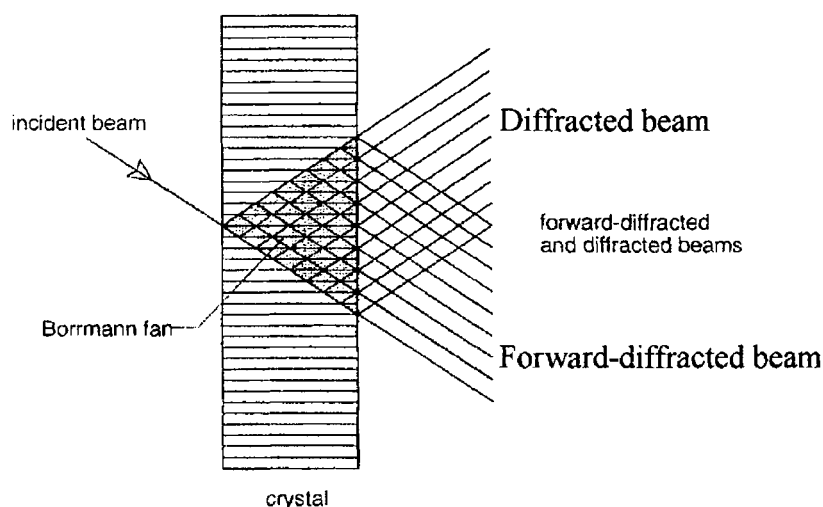


Figure 2-7 The diffraction and re-diffraction of an X-ray beam from a set of reflecting planes. The triangle bounded by the incident beam and diffracted beam from the entry surface is called the Borrmann fan [41].

- **Fundamental equations of Plane-wave Dynamical Theory**

A brief survey of the dynamical theory is given here. It is noted that a full discussion is rather complex and there are many papers with more complete details such as that of Batterman and Cole [39]. In order to describe the diffraction theory, the crystal lattice is described in terms of the reciprocal lattice. The position of the reciprocal lattice indicates the orientation and reciprocal of the d spacing of the set of direct lattice planes.

(a) Von Laue's Assumption

The basic dynamical theory, founded by von Laue considers for the propagation of the electromagnetic wave that the electric negative and positive charges are

distributed in a continuous way throughout the volume of the crystal [34]. The interaction of the electromagnetic wave with charged particles is an electric interaction and a magnetic interaction. However, in a classical treatment of the dynamical theory, it is assumed that the magnetic interaction is weak and can be neglected. In addition, the strength of the electric interaction (r_e) is defined by [34]

$$r_e = \frac{e^2}{(4\pi\epsilon_0 mc^2)} \quad \text{Eq. 2- 7}$$

where r_e is 2.817938×10^{-15} m is the classical radius of the electron, e is the electric charge of the particle, m is its mass and ϵ_0 is the dielectric constant of vacuum. If the medium is polarised under the influence of the electromagnetic field and behaves as a perfect dielectric, the coherent part of the electric interaction of the electromagnetic wave with the electron density $\rho(\mathbf{r})$ can be given in terms of the electric susceptibility $\chi(\mathbf{r})$ as [34]

$$\chi(\mathbf{r}) = -\frac{e^2 \rho(\mathbf{r})}{4\pi^2 \epsilon_0 v^2 m} = -r_e \lambda^2 \rho(\mathbf{r}) / \pi \quad \text{Eq. 2- 8}$$

where v is the frequency of the electromagnetic wave.

(b) *Maxwell's Equations*

The basic diffraction theory founded by Von Laue is built on solutions to Maxwell's equations in a medium with a periodic complex dielectric constant. The material relationship of the medium and the electro-magnetic field can be written as [34]

$$\begin{aligned} \mathbf{D} &= \epsilon \mathbf{E} = \epsilon_0 \mathbf{E} + \mathbf{P} \\ \mathbf{B} &= \mu \mathbf{H} \end{aligned} \quad \text{Eq. 2- 9}$$

where \mathbf{E} is the electric field, \mathbf{B} is the magnetic induction, \mathbf{H} is the magnetic field, \mathbf{D} is the electric flux density or the electric displacement, μ is the magnetic permeability and in the case of weak magnetic interaction $= \mu_0$, the magnetic permeability of vacuum, ϵ is dielectric constant [34], and \mathbf{P} is a polarisation [39].

In the absence of local electric charge and of a local current density, Maxwell's equations can be given as [15]:

$$\begin{aligned}\nabla \times \mathbf{E} &= -\frac{\partial \mathbf{B}}{\partial t} = -\mu_0 \frac{\partial \mathbf{H}}{\partial t} \\ \nabla \times \mathbf{H} &= \frac{\partial \mathbf{D}}{\partial t} = \varepsilon_0 \frac{\partial (\kappa \mathbf{E})}{\partial t}\end{aligned}\tag{Eq. 2- 10}$$

$$\nabla \cdot \mathbf{D} = 0$$

$$\nabla \cdot \mathbf{B} = 0$$

where κ is the dielectric constant. It is noted that the electric conductivity (σ) is zero and the magnetic permeability is unity at x-ray frequencies.

In a vacuum, $\mathbf{E} = \mathbf{D}/\varepsilon_0$, and $\nabla \cdot \mathbf{E} = 0$. From the relation $\varepsilon_0 \mu_0 = 1/c^2$ where c is the velocity of light, the propagation of the electromagnetic wave in vacuum obtained by eliminating \mathbf{H} between the first two relations of Maxwell's equations can be written as [34]

$$\nabla^2 \mathbf{E} = \frac{1}{c^2} \frac{\partial^2 \mathbf{E}}{\partial t^2}\tag{Eq. 2- 11}$$

In the case of a plane wave,

$$\mathbf{E} = \mathbf{E}_0 \exp 2\pi i(\nu - \mathbf{k} \cdot \mathbf{r})\tag{Eq. 2- 12}$$

where ν is the frequency and \mathbf{k} is the wavenumber $= 1/\lambda = \nu/c$.

In a material, $\bar{\mathbf{E}} = \bar{\mathbf{D}}/\varepsilon$, where $\varepsilon = \varepsilon_0(1+\chi)$ varies with the space coordinates. Hence, $\bar{\nabla} \cdot \mathbf{E} \neq 0$ [34]. Considering the scattering without changing frequency and $\chi \ll 1$, the electric displacement can be written as [34]

$$\mathbf{D}(\mathbf{r}) = \exp 2\pi i \nu \mathbf{r}\tag{Eq. 2- 13}$$

Therefore, the electric field is [34]

$$\mathbf{E} = \frac{\mathbf{D}}{\varepsilon_0(1+\chi)} \approx \frac{\mathbf{D}}{\varepsilon_0}(1-\chi)\tag{Eq. 2- 14}$$

Using Eq. 2-14 and removing \mathbf{H} , the equation of propagation of an electromagnetic wave in the crystalline medium can be given as

$$\nabla \mathbf{D} + \bar{\nabla} \times (\bar{\nabla} \times \chi \mathbf{D}) + 4\pi^2 k^2 \mathbf{D} = 0 \quad \text{Eq. 2- 15}$$

(c) Fourier Expansion of the Dielectric Susceptibility

In a crystalline medium, the electric susceptibility is a triply periodic function of the space coordinates. The Fourier series of the electric susceptibility can be written as [34]

$$\chi(\mathbf{r}) = \sum_{\mathbf{h}} \chi_{\mathbf{h}} \exp (-2\pi i \mathbf{h} \cdot \mathbf{r}) \quad \text{Eq. 2- 16}$$

where the reciprocal lattice of the unit cell $\mathbf{h} = h\mathbf{b}_1 + k\mathbf{b}_2 + l\mathbf{b}_3$ where h, k and l are the Miller indices of the reflection ($|\mathbf{h}|$ = the reciprocal d spacing), and $\mathbf{b}_1, \mathbf{b}_2$ and \mathbf{b}_3 are the reciprocal lattice vectors defining the unit cell in reciprocal space, and the coefficient of the Fourier expansion of the electric susceptibility ($\chi_{\mathbf{h}}$) can be derived in terms of the structure factor, i.e.

$$\chi_{\mathbf{h}} = -\frac{r_e \lambda^2}{\pi V} F_{\mathbf{h}} \quad \text{Eq. 2- 17}$$

where V = the unit cell volume, r_e = the classical electron radius = $e^2 / 4\pi\epsilon_0 mc^2 = 2.818 \times 10^{-15}$ m and $F_{\mathbf{h}}$ is the structure factor, which is given by [34]

$$F_{\mathbf{h}} = \sum_j (f_j + f_j' + f_j'') \exp[-M_j - 2\pi i \mathbf{h} \cdot \mathbf{r}_j] = |F_{\mathbf{h}}| \exp i\phi_{\mathbf{h}} \quad \text{Eq. 2- 18}$$

where f_j is the atomic structure factor of atoms j , f_j' and f_j'' are the dispersion corrections and $\exp(-M_j)$ is the Debye-Waller factor. In general, the $\chi_{\mathbf{h}} = 10^{-5} - 10^{-7}$ depending on the wavelength and the structure factor.

In the case of an absorbing crystal, the absorption is considered in the imaginary part of the refraction index and of the wavevector. Thus, the electric susceptibility is given as [34]

$$\chi = \chi_r + i\chi_i \quad \text{Eq. 2- 19}$$

where χ , χ_r and χ_i are a triply periodic and can be expanded in a Fourier series as

$$\begin{aligned} \chi_r &= \sum_{\mathbf{h}} \chi_{r\mathbf{h}} \exp(2\pi i \mathbf{h} \cdot \mathbf{r}); \quad \text{with} \quad \chi_{r\mathbf{h}} = -r_e \lambda^2 F_{r\mathbf{h}} / (\pi V) \\ \chi_i &= \sum_{\mathbf{h}} \chi_{i\mathbf{h}} \exp(2\pi i \mathbf{h} \cdot \mathbf{r}); \quad \text{with} \quad \chi_{i\mathbf{h}} = -r_e \lambda^2 F_{i\mathbf{h}} / (\pi V) \end{aligned} \quad \text{Eq. 2- 20}$$

$$\begin{aligned} F_{r\mathbf{h}} &= \sum_j (f_j + f'_j) \exp[-M_j - 2\pi i \mathbf{h} \cdot \mathbf{r}_j] = |F_{r\mathbf{h}}| \exp i\varphi_{r\mathbf{h}} \\ \text{where} \quad F_{i\mathbf{h}} &= \sum_j (f_j + f'_j) \exp[-M_j - 2\pi i \mathbf{h} \cdot \mathbf{r}_j] = |F_{i\mathbf{h}}| \exp i\varphi_{i\mathbf{h}} \end{aligned}$$

The linear absorption coefficient is

$$\mu_0 = -2\pi k \chi_{i0} = 2r_e \lambda F_{i0} / V \quad \text{Eq. 2- 21}$$

(d) Wavefields

Ewald announced the word “wavefield” in 1917 and it proved to be one of the most basic concepts for the dynamical theory [34]. From the equation of propagation of an electromagnetic wave in a crystalline medium (Eq. 2-15), the wave that exists in a crystal with the periodicity of the lattice can be written

$$\mathbf{D} = \exp(-2\pi i \mathbf{K}_0 \cdot \mathbf{r}) \sum_{\mathbf{h}} \mathbf{D}_{\mathbf{h}} \exp(-2\pi i \mathbf{h} \cdot \mathbf{r}) \quad \text{Eq. 2- 22}$$

This equation is also written as

$$\mathbf{D} = \sum_{\mathbf{h}} \mathbf{D}_{\mathbf{h}} \exp(-2\pi i \mathbf{K}_{\mathbf{h}} \cdot \mathbf{r}) \quad \text{Eq. 2- 23}$$

$$\text{and } \mathbf{K}_{\mathbf{h}} = \mathbf{K}_0 - \mathbf{h} \quad \text{Eq. 2- 24}$$

where \mathbf{K}_0 and $\mathbf{K}_{\mathbf{h}}$ are the wavevectors inside the crystal in the directions of the incident and diffracted beams, respectively, and $|\mathbf{K}_0| = |\mathbf{K}_{\mathbf{h}}| = 1/\lambda$. The sum in Eq. 2-23 is a wavefield or Ewald wave [34].

The relationship of the wavevectors in a wavefield and the reciprocal lattice can be explained in terms of the geometry of a boundary condition at the entrance surface in Figure 2-8. The wavevector $\mathbf{K}_0 = \mathbf{OP}$ and $\mathbf{K}_h = \mathbf{HP}$, the common extremity P of the two wavevectors is called the tiepoint by Ewald to emphasise that the two waves are closely linked together to form a wavefield; note that \mathbf{n} is normal to the entrance surface [35].

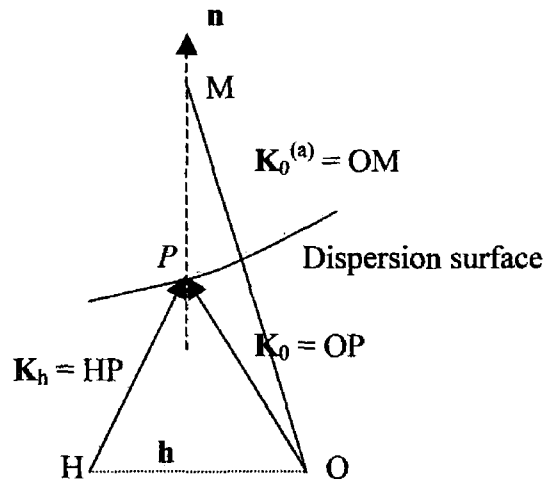


Figure 2-8 Boundary condition for wavevectors at the entrance surface[34].

For an absorbing crystal, the wavevectors must include the imaginary part given as

$$\begin{aligned}\mathbf{K}_0 &= \mathbf{K}_{0r} + i\mathbf{K}_{0i} \\ \mathbf{K}_h &= \mathbf{K}_{hr} + i\mathbf{K}_{hi}\end{aligned}\tag{Eq. 2- 25}$$

From Eq. 2-24, all wavevectors have the same imaginary part, $\mathbf{K}_{0i} = \mathbf{K}_{hi}$ and thus suffer the same absorption.

From Fig. 2-8, in a semi-infinite medium where the waves are produced with vacuum or air by an incident plane wave with wavevector $\mathbf{K}_0^{(a)}$, \mathbf{K}_0 is determined by the boundary conditions which are satisfied when the difference between the wavevectors is parallel to the normal to the entrance surface. Hence, it can be written that

$$\mathbf{K}_0 - \mathbf{K}_0^{(a)} = \mathbf{OP} - \mathbf{OM} = \overline{\mathbf{MP}} \cdot \mathbf{n}\tag{Eq. 2- 26}$$

where \mathbf{n} is the unit vector normal to the crystal entrance surface [34].

The relationship between the amplitude of the waves in the wavefield given in Eq. 2-23 and the wavevector \mathbf{h} is given as [34]

$$\mathbf{D}_{hj} = \frac{\mathbf{K}_{hj}^2}{\mathbf{K}_{hj}^2 - \mathbf{k}^2} \sum_{h'} \chi_{h-h'} \mathbf{D}_{h'\{h\}j} \quad \text{Eq. 2-27}$$

where \mathbf{h}' is reciprocal lattice vector, $\chi_{h-h'}$ is the Fourier coefficient of the dielectric susceptibility associated with reciprocal-lattice vector $\mathbf{h}-\mathbf{h}'$, $\mathbf{D}_{h'\{h\}j}$ is the projection of $\mathbf{D}_{h'j}$ on a plane normal to \mathbf{K}_{hj} and the sum is overall reciprocal-lattice vectors \mathbf{h}' . The term labelled “a” in Eq. 2-27 is called the resonance factor by Ewald [34] and the term labelled “b” in Eq. 2-27 is called the effect of polarisation [34]. These wavevectors correspond to reciprocal lattice points, which lie close to the Ewald sphere.

- **Dispersion surface**

Equation 2-27 is a basic equation of dynamical theory. The solution of this equation is related to the locus of the tiepoints of all the wavefields which may propagate in the crystal with a given frequency [34].

To understand the wave propagation inside the crystal, the geometrical diffraction can be drawn in terms of direct space (Fig. 2-9 (a)) and reciprocal space (Fig. 2-9 (b)).

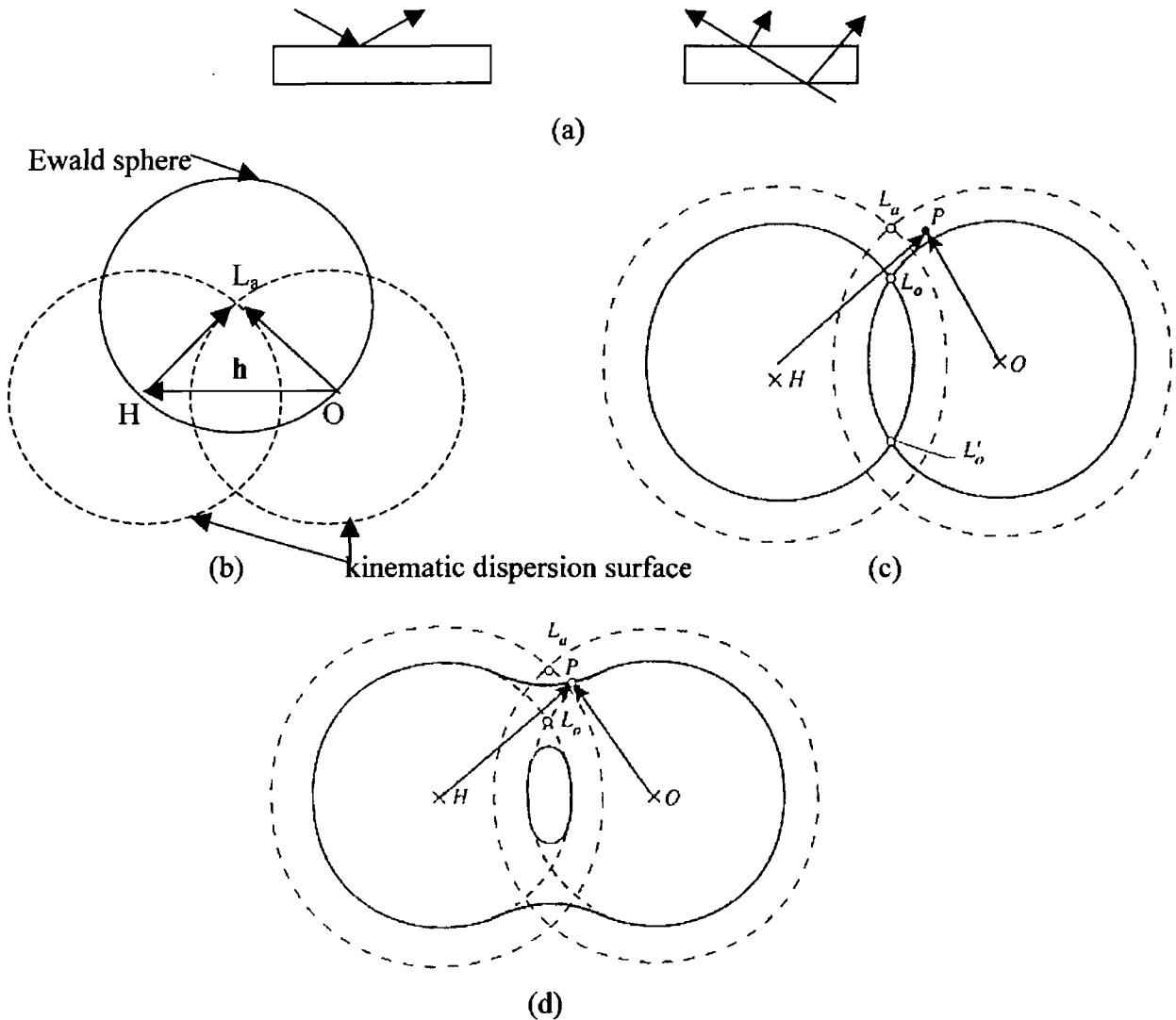


Figure 2-9 Diffraction according to the geometrical theory

- (a) Direct space, Bragg geometry (left) and Laue geometry (right);
- (b) Reciprocal space; $\overline{OH} = \mathbf{h}$: reciprocal lattice vector, L_a = Laue point; $\overline{OL_a} =$ incident wave ($\overline{OL_a} = k$) and $\overline{HL_a} =$ reflected wave ($\overline{HL_a} = k$);
- (c) Influence of the refraction index where L_o = Lorentz point, $\overline{OL_o} = \overline{HL_o} = nk$, OP = refracted wave and HP = reflected

wave and L_0' = Lorentz point corresponding to the reciprocal lattice vector $\mathbf{HO} = -\mathbf{h}$;

- (d) Interaction of the refracted (OP) and reflected (HP) waves. The solid line is called the dispersion surface and P is the tiepoint [35].

For a perfect and infinite crystal, the reflection can be represented by a single point, called a Laue point (L_a) [35]. This point is the centre of the Ewald sphere [37], which is the intersection of two spheres, centred at the reciprocal nodes \mathbf{O} and \mathbf{H} , with radius k , where $k = 1/\lambda$ (Fig. 2-9 (b)). Considering the propagation of the wave in matter, the refraction index, n , must be taken into account. In this case, the point represents the intersection of two spheres with the same centre of radius nk , where n is the refraction index of the crystal, and is called the Lorentz point, L_o (Fig. 2-9(c)). The wave propagating inside the crystal in the incident direction is called the refracted wave [35]. It is assumed that for any position of the crystal within the reflection domain, the refracted wave of the refracted wave, $\mathbf{K}_o = \mathbf{OP}$ and the reflected wave, $\mathbf{K}_H = \mathbf{HP}$ [34], and this position P must lie on a connecting surface between the two spheres, called the *tiepoint* (Fig. 2-9 (d)). The connecting surface, which has two sheets, is called the *dispersion surface* as shown in Fig 2-9 (d). Close to the Lorentz point, these two spheres are replaced by their tangential planes and their interaction is replaced by two straight lines. Thus, the dispersion surface can be represented in terms of a hyperbola whose asymptotes are T_o and T_h as illustrated in Figure 2-10 [34].

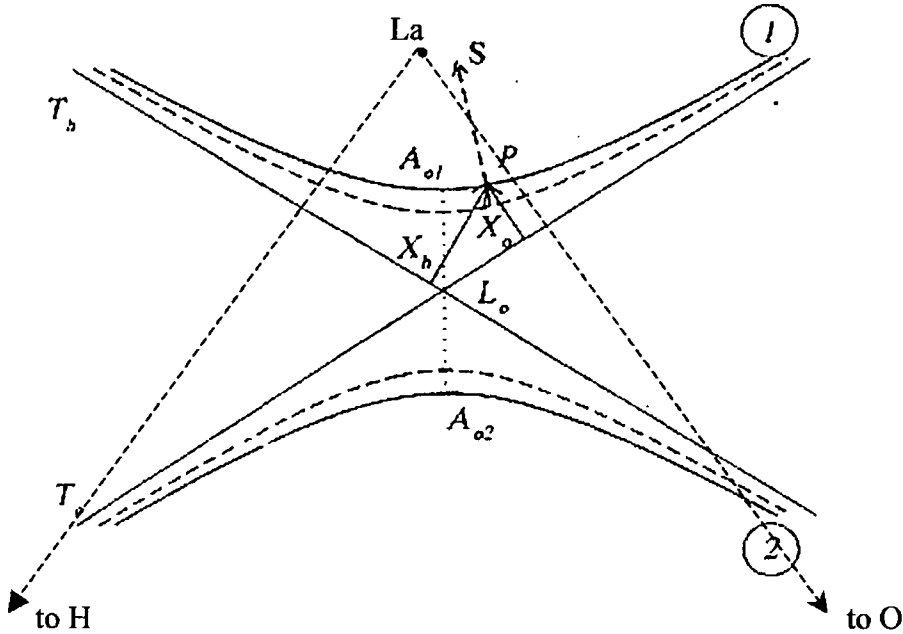


Figure 2-10 Intersection of the dispersion surface with the plane of incidence. Full hyperbola: polarization normal to the plane of incidence ($c=1$). Dashed hyperbola: polarization parallel to the plane of incidence ($c=\cos 2\theta_B$). S = Poynting vector and P = tiepoint of a Bloch wave or wavefield [34].

This dispersion surface is very important for an explanation of diffraction in terms of the dynamical theory. It is noted that the effects of the dynamical theory occur near the intersection of the circles O and H at the L_0 point. The solution of this surface can be found from the fundamental equation of dynamical theory in Eq. 2-27. In the two beam case, if the resonance terms are very large and there exist two nodes simultaneously on the Ewald sphere, Eq. 2-27 can be written as [35]

$$D_0 = \frac{k^2}{K_0^2 - k^2} [\chi_0 D_0 + \chi_h D_h],$$

$$D_h = \frac{k^2}{K_h^2 - k^2} [\chi_h D_0 + \chi_0 D_h]$$

Eq. 2- 28

where $\chi_{\bar{h}}$ is the Fourier coefficient of the polarisability associated with the $\bar{h} \bar{k} \bar{l}$ reflection. In a semi-infinite crystal, the notation labelled "0" is the refracted wave or forward diffracted wave and the other one is the reflected wave. It is noted that when the crystal is rocked through the reflection domain and the tiepoint P moves along the dispersion surface, there is no discontinuity in the properties of the refracted wave.

To solve these above equations, the determinants are set to be zero. The secular equation of the relationship between the lengths $|K_0|$ and $|K_h|$ of the wavevectors of the field which gives the relation of the loci of the tiepoint P and the dispersion surface can be obtained as [35]

$$\begin{aligned} \{K_0^2 - k^2(1 + \chi_0)\}D_0 + k^2C_{\chi_h}D_h &= 0 \\ -k^2C_{\chi_h}D_0 + \{K_h^2 - k^2(1 + \chi_0)\}D_h &= 0 \end{aligned} \quad \text{Eq. 2-29}$$

with

$$\begin{aligned} X_0 &= \frac{K_0^2 - k^2}{2k^2} - \frac{k\chi_0}{2}, \\ X_h &= \frac{K_h^2 - k^2}{2k^2} - \frac{k\chi_0}{2}, \end{aligned} \quad \text{Eq. 2-30}$$

where C = polarisation factor; $C = 1$ for σ -polarisation and $C = \cos(2\theta_B)$ for π -polarisation.

It is noted that the approximation in Eq. 2-29 and 2-30 is based on the classical treatment. They are correct only when the Ewald sphere can be replaced by its tangential plane, whereas they cannot be used when the Bragg angle is $\sim \pi/2$. Since

$K_h \approx k$ and $K_0 \approx k$, $\frac{K_h^2 - k^2}{2k^2} \approx (K_h - k)$, thus Eq. 2-30 can be written as

$$\begin{aligned} X_0 &\approx K_0 - k(1 + \frac{\chi_0}{2}) \approx K_0 - nk, \\ X_h &\approx K_h - k(1 + \frac{\chi_0}{2}) \approx K_h - nk \end{aligned} \quad \text{Eq. 2- 31}$$

where $n \approx (1 + \frac{\chi_0}{2})$. In the case of an absorbing crystal, K_0, K_H, X_0, X_H are complex. Subsequently, the dispersion surface is also a complex surface [35].

Substituting Eq. 2-31 into Eq. 2-29 gives

$$\begin{aligned} 2X_0D_0 - kC_{\chi_H}D_h &= 0 \\ -kC_{\chi_H}D_0 + 2X_hD_h &= 0 \end{aligned} \quad \text{Eq. 2- 32}$$

The secular equation, which is the equation of the dispersion surface, is

$$X_0X_h = k^2C^2\chi_h\chi_{\bar{h}}/4 \quad \text{Eq. 2- 33}$$

Hence, Eq. 2-33 is the equation of a hyperbola whose asymptotes are T_0 and T_h (Fig. 2-10). The angle between asymptotes T_0 and T_h is $2\theta_B$. The branch of the hyperbola, which lies on the same side as the Laue point is called Branch 1 and the other, is called Branch 2, lying on the same side as centres **O** and **H**. Therefore, X_0 and X_h are positive when the tiepoint **P** lies on branch 1 and negative when it lies on branch 2.

From Fig. 2-10, A_{01} and A_{02} are defined as the vertices of the hyperbola and the length ($\overline{A_{02}A_{01}}$) can be given from Eq. 2-33 as [35]

$$\overline{A_{02}A_{01}} = |C| \sqrt{\chi_h\chi_{\bar{h}}} / \cos \theta = |C| r_e \lambda \sqrt{F_h F_{\bar{h}}} / (\pi V \cos \theta) \quad \text{Eq. 2- 34}$$

The ratio (ξ) of the amplitude of the refracted and reflected waves in the wavefield can be given by means of Eq. 2-32 i.e.

$$\xi = \frac{D_h}{D_0} = \frac{2X_0}{kC\chi_h}$$

$$\xi^2 = \frac{\chi_h}{\chi_h} \frac{X_0}{X_h}$$

Eq. 2- 35

From Fig. 2-10, the hyperbola has two branches, i.e. 1 and 2 for each direction of polarisation. The coordinates of the tiepoint, X_0 and X_h are positive for Branch 1 and negative for Branch 2.

In the Laue case, the phase of the amplitudes (Ψ) is thus equal to $\pi+\varphi_h$ for Branch 1 (so-called nodes), and to φ_h for Branch 2 (so-called anti-nodes), where φ_h is the phase of the structure factor. The difference of π of these two branches is important in distinguishing the difference in the nodes of standing waves which are related to phenomenon of anomalous absorption, which will be explained later in this chapter [35].

In the Bragg case, Ψ alters continuously from $\pi+\varphi_h$ to φ_h , when the angle of the incident wave is varied from the low angle to the high angle side of the reflection [34].

• Nodes of Standing Waves

In the two beam case, the intensity of the wavefield can be written using Eq. 2-22 and 2-35 as [35]

$$|D|^2 = |D_0|^2 \exp(4\pi\mathbf{K}_0 \cdot \mathbf{r}) [1 + |\xi|^2 + 2C|\xi| \cos 2\pi(\mathbf{h} \cdot \mathbf{r} + \Psi)]$$

Eq. 2- 36

where Ψ is the phase of ξ , ($\xi = |\xi| \exp i\Psi$). Eq. 2-36 exhibits the interference between the two waves as the origin of standing waves. The nodes of the standing wave system lie on the planes such that $\mathbf{h} \cdot \mathbf{r} = \text{constant}$. Their position within the unit cell, therefore, depends on the value of Ψ [34].

• **Propagation Direction of the Wavefields**

The energy flow of an electromagnetic wave propagating through the crystal is in the same direction as the Poynting vector (\mathbf{S}):

$$\mathbf{S} = \mathbf{E} \times \mathbf{H} \quad \text{Eq. 2- 37}$$

The Poynting vector (\mathbf{S}) can be related to the wavefields inside the crystal and can be derived from Fig. 2-11 as [15]

$$\mathbf{S} = |\mathbf{D}_0|^2 \mathbf{s}_0 + |\mathbf{D}_H|^2 \mathbf{s}_H \quad \text{Eq. 2- 38}$$

where the \mathbf{D}_0 and \mathbf{D}_H are the electric displacements of the refracted and reflected waves in the wavefield, respectively, and \mathbf{s}_0 and \mathbf{s}_H are unit vectors of the incident and the reflected directions, respectively. \mathbf{S} is unique in the propagation direction for the two waves in the wavefield.

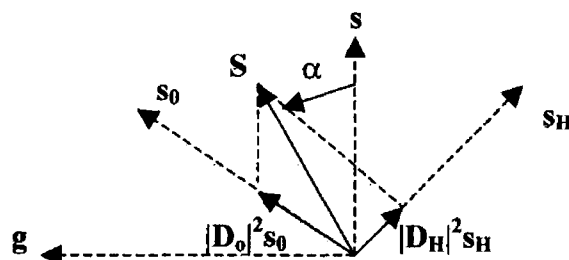


Figure 2-11 Poynting vector, \mathbf{S} , of a wavefield where \mathbf{s}_0 and \mathbf{s}_H are unit vectors in the incident and reflected directions, respectively, \mathbf{s} is a unit vector parallel to the lattice plane, \mathbf{g} is a unit vector parallel to the reciprocal lattice vector and α is an angle between the propagation direction and the lattice planes [35].

In addition, this Poynting vector is normal to the dispersion surface at any tiepoint of the wavefield. An angle α can be related to the amplitude ratio (Eq. 2-16) by [35]

$$\tan \alpha = \frac{1 - |\xi|^2}{1 + |\xi|^2} \tan \theta_B \quad \text{Eq. 2- 39}$$

- **Borrmann Effect or anomalous transmission**

When x-rays pass through a single crystal wedge, an anomalous transmission phenomenon was first observed by Borrmann (1943). To explain the effect of anomalous transmission consider a thick crystal can be seen in Figure 2-12 [39].

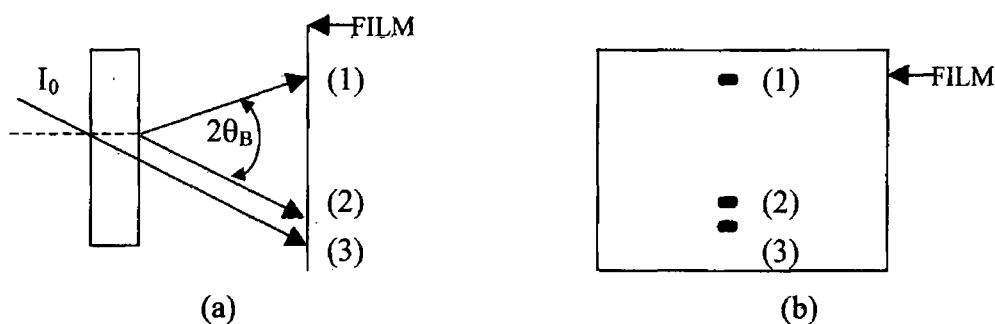


Figure 2-12 Geometry of the beams when anomalous transmission occurs. (a) Ray diagram to describe spots on the film. (b) most of the energy resides in the diffracted beam spot (1) and forward diffracted beam spot (2) [39].

Three spots are shown in the recorded film: Spot (1) is created from the diffracted beam, Spot (2) is generated from the forward-diffracted beam, which has about the same intensity as Spot (1) and the angle between spot (1) and (2) is equal to $2\theta_B$. A weak Spot (3) is in the same direction as the incident beam, which is not produced by the Borrmann effect. It is caused by normal transmission. However, the separation between Spots (2) and (3) is proportional to the sample thickness. The anomalously intense Spots (1) and (2) created from the exit side of the crystal, are caused by an anomalous transmission in the diffraction process. After all, one might expect these spots to be very weak due to high absorption in these thick crystals. However, this is not the case. This phenomenon is commonly called the Borrmann effect. The Borrmann effect has proved to be very useful in the x-ray topography technique for crystals with large $\mu_0 t$ values, where t = the thickness of the crystal and μ_0 = linear absorption coefficient. It is found that this effect is particularly prominent at $\mu_0 t \geq$

10. For a crystal with high $\mu_0 t$, the two branches (Branches 1 and 2) in the dispersion surface are associated with different absorption coefficients, when the diffraction occurs. Thus, the K_0 and K_H wavefields, which travel in opposite directions, set up standing waves in the crystal. Batterman and Cole [39] performed an experiment with CuK_α radiation on a 220 reflection of Ge crystal with $\mu_0 t = 38$. The $\mu_0 t$ factors for the two branches with σ -polarization were calculated to be 74.0 (Branch 1) and 1.9 (Branch 2), respectively. This can be explained in that for Branch 2 waves, the nodes of the standing wave are on the atomic planes, whereas they are between the atomic planes for branch 1 waves as depicted in Figure 2-13 [15]. It is known that photoelectric absorption is caused by an interaction of the wave with the inner K and L electron shells. Therefore, when the node of the standing wave falls between the atomic planes, the photoelectric absorption is high. Therefore, in Fig. 2-12, only one wavefield arrives, i.e. from Branch 2 of the dispersion surface at the exit of the crystal; thereafter generating the images at Spot (1) and (2) by the diffraction process.

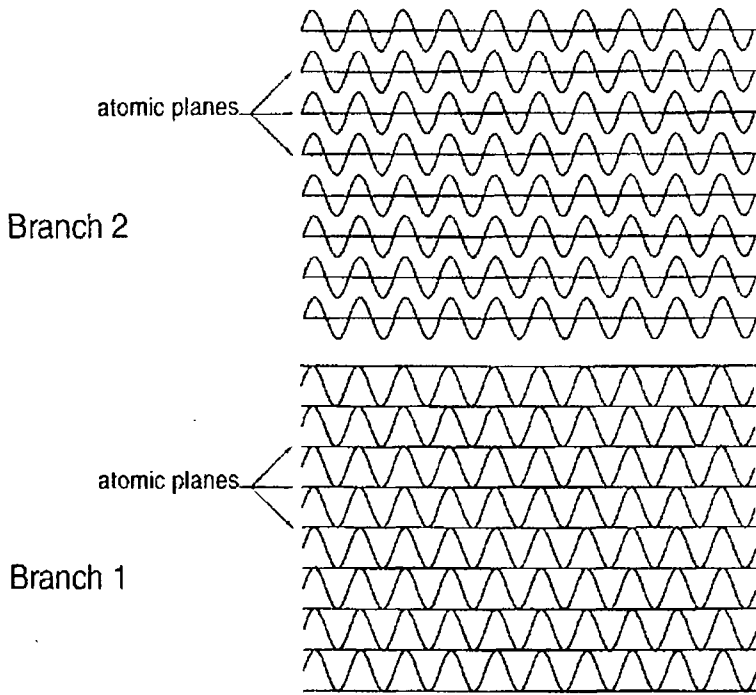


Figure 2-13 Standing waves in anomalous transmission geometry. The nodes of the wavefield from Branch 2 of the dispersion

surface lie on the atomic planes and thus encounter low absorption. Branch 1 wavefields, on the other hand, are heavily absorbed [15].

From this theory, any imperfect part in a Borrmann fan will interrupt the high transmission of x-rays through the sample and will give an extinction contrast in the image, i.e. a loss or extinction of transmission, which will be explained later.

In this transmission (Laue) geometry case, the nodes lie on the planes which are parallel to the lattice planes (Branch 1), the phase ψ is equivalent to π , whereas, for antinodes which lie on the atomic planes (Branch 2), the phase is equal to 0. From this explanation, it is seen that the low intensity Spot (3) is generated from the standing wave, which lies in the lattice plane associated with Branch 1 in the dispersion surface.

- **Contrast Mechanism**

X-Ray (diffraction) Topography (XRT) is a method of mapping the diffracting power as a function of position across the diffracted x-ray beam. Therefore, the imaging contrast depends on two x-ray beams: the incident and the diffracted beam. The contrast in XRT can be divided into two principal mechanisms, called orientational and extinction contrast.

- 1. Orientational contrast**

This contrast occurs when the effective misorientation of the lattice exceeds the divergence of the incident X-ray beam ($\Delta\phi$). A misoriented region (dashed circle in Fig. 2-13) of a crystal diffracts the incident beam with a different Bragg angle with respect to the rest of the crystal. This misorientation may be due to dilatations and rotations of the lattice. Figure 2-14 shows the orientational contrast mechanism for continuous radiation (white beam) [34].

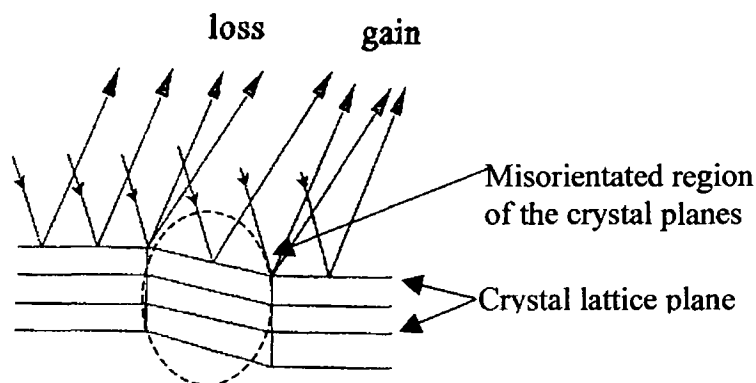


Figure 2-14 The origin of the orientational contrast mechanism for white beam radiation [34].

Fig. 2-14 shows one of the mechanisms for producing the loss and gain of intensity across the misorientated crystal planes. The region producing divergent beams leads to a loss of intensity with respect to the rest of the crystal. However, diffracted intensity occurs in the misoriented areas as the Bragg condition is satisfied due to the presence of a continuum of wavelengths. In addition, the orientational contrast can occur in topographs when the diffracted beam from the misoriented part in the crystal takes a different direction in space compared to the rest of the crystal. This mechanism can be examined in terms of the kinematical theory. The variation in the Bragg angle in the misorientated crystal, when compared the good crystal, is indicated by $\Delta\theta_B$ in Figure 2-15.

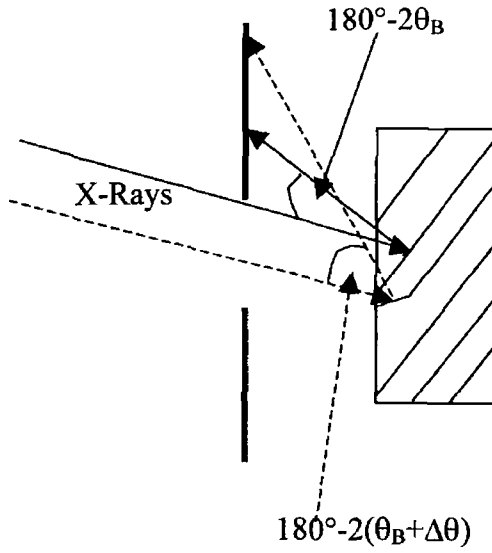


Figure 2-15 The orientational contrast mechanism in cases of severe lattice distortion.

The calculation of the effective misorientation can be described easily in terms of direct space arguments. From Bragg's law, $2d\sin\theta_B = \lambda$, $\Delta\theta_B$ is the total change in Bragg angle (θ_B), which comprises lattice dilatation and the component of the rotation of the lattice planes around the normal to the plane of incidence, i.e. tilt (α) [34]:

$$\Delta\theta_B = \frac{\Delta d}{d} \tan\theta_B + \alpha \quad \text{Eq. 2- 40}$$

where d is the distance between the diffracting planes, and Δd is the dilatation of the planes [46]. In the case of the white beam technique, the dilatation component of the change in Bragg angle $\frac{\Delta d}{d} \tan\theta_B$ cannot be obtained in this calculation since the white beam radiation provides a large number of wavelengths, which give a diffracting wavelength for any dilated planes. Therefore, the misorientation ($\Delta\theta_B$) is equal to the tilt component (α) only

$$\Delta\theta_B = \alpha \quad \text{Eq. 2- 41}$$

This contrast is associated with the distorted part of the lattice around a defect producing a different diffracting power compared to the rest of the crystal [41]. This contrast is explained using the dynamical diffraction theory for thick and highly perfect crystals. Authier classified the extinction contrast into 3 types, which are portrayed in Figure 2-16 [34].

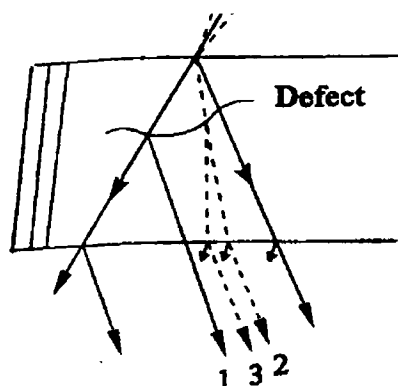


Figure 2-16 Generation of the extinction contrast image where the strain gradient is high. 1 is the direct image, 2 is the dynamical image and 3 is the intermediary image [34].

The first type is called a *direct image* given by the unsatisfied Bragg condition in the perfect crystal. The contrast, which appears from the direct image, is sharp and intense in the low-absorbing crystal. It is found that hkl and \overline{hkl} reflections are identical. The second type is the *dynamical image* arising from changes in intensity in the wavefields propagating through the perfect crystal (see the previous discussion on anomalous transmission). When the strain gradient in the crystal is high, the tiepoint is shifted from one branch of the dispersion surface to the other. This tiepoint jumping is called interbranch scattering [48]. A total collapse of the Borrmann effect is a very good example in this case. It is assumed that the wave incident on the high strain region in the crystal is on Branch 2 of the dispersion surface. Thus, the new wavefield must be on Branch 1, which is highly absorbing. The result is a diminution of the x-ray intensity in the direction of the incident wave. This depletion of intensity is called Borrmann contrast [48]. In contrast, when the strain gradient is low, the tie-point stays in its branch by moving to a different

position on the dispersion surface. This interaction is called tiepoint migration [48]. The wavefield in this case is not decoupled but moves along the dispersion surface. As mentioned above, the Poynting vector (S) is always normal to the dispersion surface, thus the ray paths becomes curved in real space. This leads to a redistribution of the energy between the forward-diffracted beam and the diffracted. Basically, this sort of image results in a forward-diffracted beam image, which differs in contrast, from the diffracted beam image. In the other words, the hkl and \overline{hkl} reflections are not identical, i.e. hkl may show black-white while \overline{hkl} would give white-black images for identical regions of the crystal [48]. The third type of contrast is generated by interference between a current wavefield and a new wavefield formed at the distorted region in the perfect crystal, and is called the *intermediary image* [34]. It is noted that these images (Fig. 2-16) occur in the case of high strain gradient regions.

To interpret the extinction contrast, the dynamical diffraction theory is used in terms of the effective misorientation for a deformed crystal [34]-[35]. In the reciprocal space, if the crystal undergoes a deformation, any point P of a position vector \mathbf{r} is transformed to a point P' of a position vector \mathbf{r}' . The deformation is illustrated in Figure 2-17 [34].

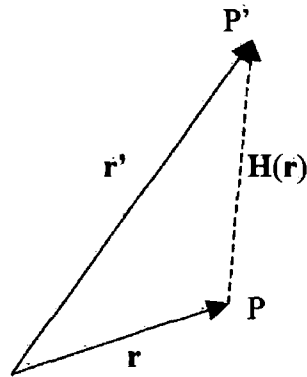


Figure 2-17 Deformation of a crystal, where $\mathbf{H}(\mathbf{r})$ is a deformation vector [34].

The relationship between \mathbf{r} and \mathbf{r}' can be written by

$$\mathbf{r}' = \mathbf{r} + \mathbf{H}(\mathbf{r}) \quad \text{Eq. 2- 42}$$

if the coefficients of the strain tensor ($\frac{\partial h_i}{\partial x_j}$) are small with respect to unity, and the relationship also can be written by

$$\mathbf{r} = \mathbf{r}' - \mathbf{H}(\mathbf{r}) \cong \mathbf{r}' - \mathbf{H}(\mathbf{r}') \quad \text{Eq. 2- 43}$$

Assuming the crystal is perfect and infinite, \mathbf{P} is in direct space and \mathbf{H}' is its reciprocal lattice vector. The equation of a plane of the family of direct lattice planes (hkl) is

$$f \equiv \mathbf{g} \cdot \mathbf{r} = N \quad \text{Eq. 2- 44}$$

The reciprocal-lattice vector \mathbf{g} can be defined in terms of the gradient of f by

$$\mathbf{g} = \vec{\nabla}(f) \quad \text{Eq. 2- 45}$$

Thus, the position vector after deformation, \mathbf{r}' , can be defined using Eq. 2-43 as

$$f' \equiv \mathbf{g} \cdot \mathbf{r}' - \mathbf{g} \cdot \mathbf{H}(\mathbf{r}') = N \quad \text{Eq. 2- 46}$$

This equation is for the lattice plane at the surface, which is transformed by the deformation. The reciprocal lattice vector (\mathbf{g}') of the asymptotically perfect crystal is given by

$$\mathbf{g}' = \vec{\nabla} f' = \mathbf{g} - \vec{\nabla}(\mathbf{g} \cdot \mathbf{H}) \quad \text{Eq. 2- 47}$$

and the local variation of the reciprocal lattice ($\delta\mathbf{g}$) is thus defined by

$$\delta\mathbf{g} = \mathbf{g}' - \mathbf{g} = -\vec{\nabla}(\mathbf{g} \cdot \mathbf{H}) \quad \text{Eq. 2- 48}$$

In the reciprocal space, $\delta\mathbf{g}$ is the projection on the plane of incidence of the local variation which is equal to $\mathbf{H}\mathbf{H}'$ as indicated in Figure 2-18.

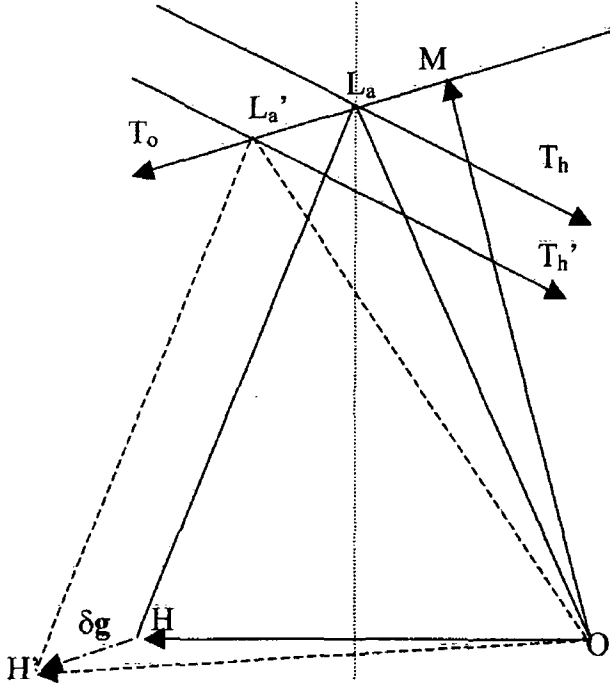


Figure 2-18 Modification of the reciprocal lattice due to the deformation of the crystal, where L_a is Laue point before deformation, $L_{a'}$ is Laue point after deformation, $\delta \mathbf{g}$ is the variation of the reciprocal lattice vector [34].

As mentioned above, the Laue point (L_a) is the intersection of two spheres with centre O and H and of radius $k = 1/\lambda$ and on the reciprocal lattice of OH . The deformed Laue point ($L_{a'}$) lies on the same sphere and on the new reciprocal lattice vector (OH'). If an incident vector, $\mathbf{K}_o^{(a)} = OM$, the effective misorientation can be given by [34]

$$\delta \theta = \Delta \theta' - \Delta \theta = (\overline{L_{a'} M} - \overline{L_a M}) / k \approx \overline{L_a' L_a} / k \quad \text{Eq. 2- 49}$$

in terms of the reciprocal lattice vector, and the effective misorientation can be written as

$$\delta \theta = \frac{\delta \mathbf{g} \cdot \mathbf{s}_h}{k \sin 2\theta} = \frac{-\mathbf{s}_h \cdot \nabla(\mathbf{g} \cdot \mathbf{h})}{k \sin 2\theta} \quad \text{Eq. 2- 50}$$

The effective misorientation in reciprocal space in Eq. 2-50 is a linear combination of components of the strain tensor $\partial u_i / \partial x_j$, where u_i = a displacement vector at any given point i . If the local variation of the reciprocal lattice vector is normal to the reflection direction, $\delta \mathbf{g} \cdot \mathbf{s}_h = 0$. The effective misorientation in Eq. 2-50 is equivalent to that in Eq. 2-40, which is calculated in direct space.

The derivative of the effective misorientation along the incident beam $\partial(\delta\theta)/\partial s_o$ is equivalent to the strain gradient in the deformed crystal. The relationship can be given by [34]

$$\frac{\partial[\delta\theta]}{\partial s_o} = \frac{1}{g \cos \theta_B} \frac{\partial^2(\mathbf{g} \cdot \mathbf{h})}{\partial s_o \partial s_h} \quad \text{Eq. 2- 51}$$

2.2.4 Techniques

Before x-ray topography will be explained, two x-ray sources for the x-ray topographic experiments need to be clarified: white-radiation and monochromatic-radiation sources, since many of the techniques also use monochromatic radiation sources. Consider first the creation of radiation from an x-ray tube consisting of a source of electrons and two metal electrodes. The x-rays are generated when the charged particles, i.e. electrons of sufficient kinetic energy, are significantly decelerated by interacting with the anode field and the x-rays radiate in all directions. Two kinds of characteristic radiation curves are obtained with a mixture of different wavelengths as illustrated in Figure 2-19 [37].

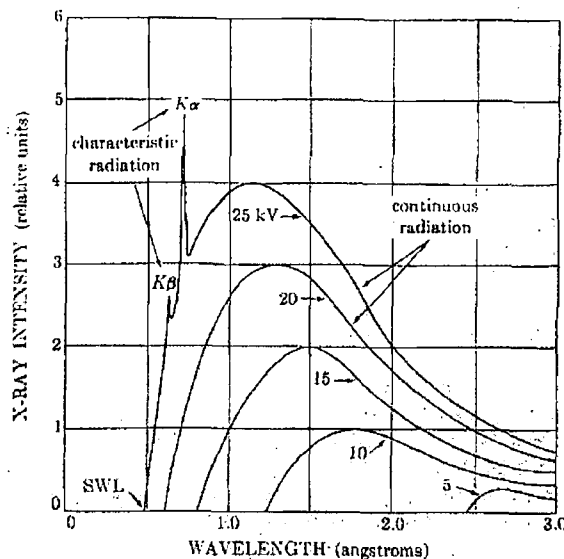


Figure 2-19 X-ray spectrum of a molybdenum anode target as a function of applied voltage for an x-ray tube [37].

The continuous radiation or white beam is a ray of many wavelengths, generated by the rapid deceleration of the electrons under the influence of the anode field. On the other hand, the characteristic radiation displays a sharp intensity at certain wavelengths depending on the anode metal used. This is because an electron with sufficient energy hits the target composed of atoms with electrons in varying quantised energy shells such as K, L, M, etc. For example, the impacting electron could knock the electron out of the K shell, leaving the atom in an excited stage. Then, an outer electron immediately falls into the vacancy in the K shell and emits the energy exchanged in the form of x-ray radiation, which in this case is called K-radiation.

Using a white beam or continuous, radiation source with x-ray topography has the following benefits:

- (a) The sample is placed in front of the white beam path without adjustment;
- (b) Many reflections forming a Laue pattern can be recorded simultaneously on the film. Each spot is itself an x-ray topograph;
- (c) Short exposure times compared to monochromatic radiation sources;

- (d) The ability to observe overall strain distributions in severely distorted samples;
- (e) Simple experimental set-up.

The use of white beam synchrotron radiation for x-ray topography has tremendous advantages, especially when the distance between the x-ray source and sample and the width of the beam at the sample are large. The spatial resolution of the experiment (δ) is related to the radiation source dimension (H), the source-sample distance (L), and the sample-plate distance (D) by [15]

$$\delta = HD/L \quad \text{Eq. 2- 52}$$

The geometrical resolution limit is illustrated in Figure 2-20 [15].

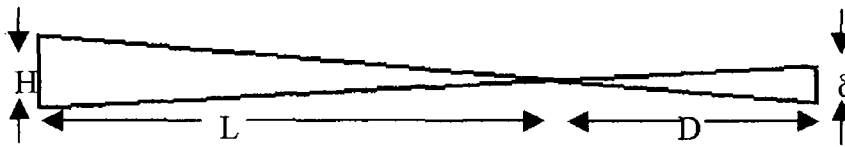


Figure 2-20 The spatial resolution limit set by the projected source height normal to the incident beam [15].

From Eq. 2-21, the synchrotron radiation source is suitable for this technique since it has low divergence and the x-ray source is very far from the sample.

- **Berg-Barrett technique**

Barrett (1945) developed Berg's technique, which is based on the Bragg (reflection) orientation geometry. The set-ups are illustrated in Figure 2-21 [34].

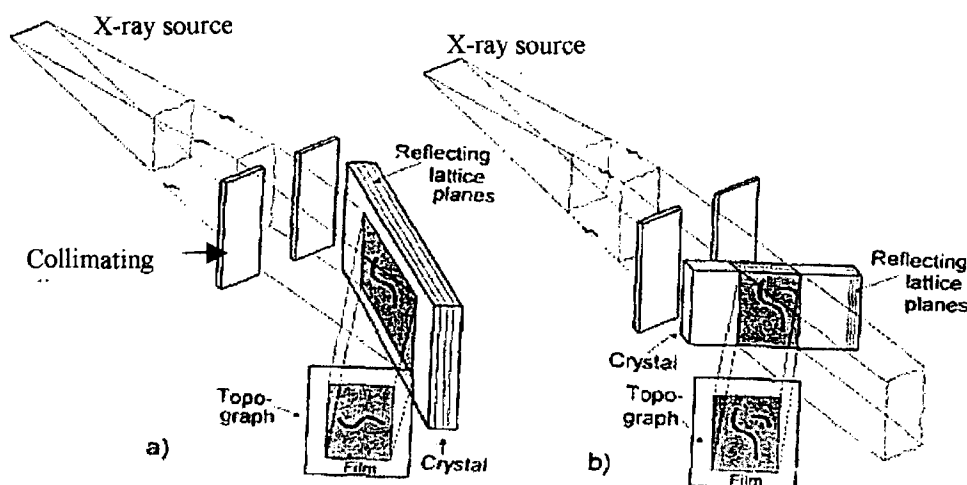


Figure 2-21 Berg-Barrett technique in reflection and transmission with film normal to the diffracted beam [34].

This Berg-Barrett reflection method is one of the simplest techniques. The image is recorded by the diffracted beam on the surface of the crystal. There are many limitations to this technique: (a) the recording film should be perpendicular to the surface of the sample to minimise image distortion [40], and (b) the sample to film distance must be as small as possible to get rid of the effect from vertical beam divergence as explained above in reference to the spatial resolution; therefore this technique is insensitive to orientational contrast which can be observed only when the effective misorientation is larger than the vertical beam divergence, (c) low spatial resolution between the K_{α} -doublet, which simultaneously reflects two nearly overlapping images on the film.

- **Lang topography**

This technique was invented by Lang (1959) and is commonly used for high-resolution transmission x-ray topography [34]. It is very sensitive to both extinction and orientational contrast. Two experimental set-ups are introduced: projection and section topography [15], [34] and [41].

Projection topography is a transmission method providing an image covering large regions of a sample. The experimental set-up is illustrated in Figure 2-22 [15].

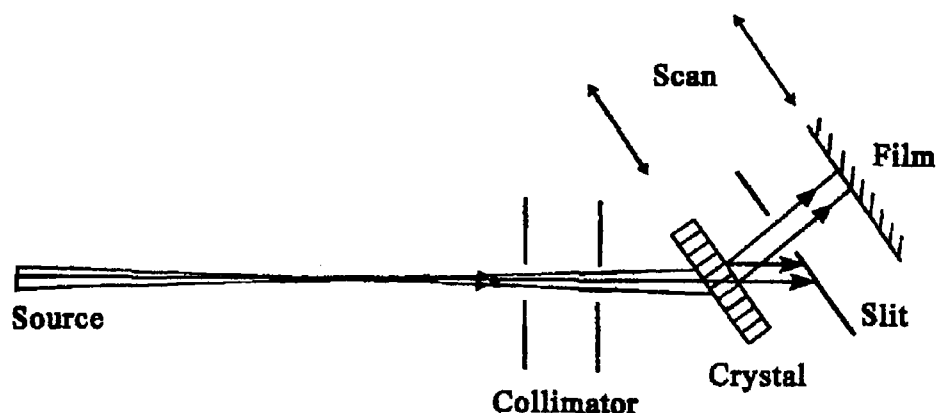


Figure 2-22 The experiment set-up for projection x-ray topography. Sample and film are scanned across the beam. Note that scanning is not employed for the section topography set-up.

Using a goniometer, the film and the sample can be translated together across the x-ray beam. Using this set-up with a conventional x-ray tube source, the beam divergence is small enough to get rid of the simultaneous diffraction of the K_{α} -doublet by blocking the weaker $K_{\alpha 2}$ beam with an appropriately placed slit. This technique can provide an image of the 3-D distribution of defects in the crystal by narrowing the beam to less than the width of the base of the Borrmann fan (the beam width must be less than $t \cdot \sin 2\theta_B$, in which t is the specimen thickness and θ_B is the Bragg angle) [15]. The formation of section topography and its integration to projection topography is illustrated above in Figure 2-22.

- **Synchrotron X-Ray Topography Techniques [42]**

(a) White Beam Large Area Back Reflection Topography (LA-BRT)

In this case, the incoming x-rays are perpendicular to the upper surface of the sample. This Bragg geometry is used to access information in the near surface regions of the probed wafer as illustrated in Figure 2-23.

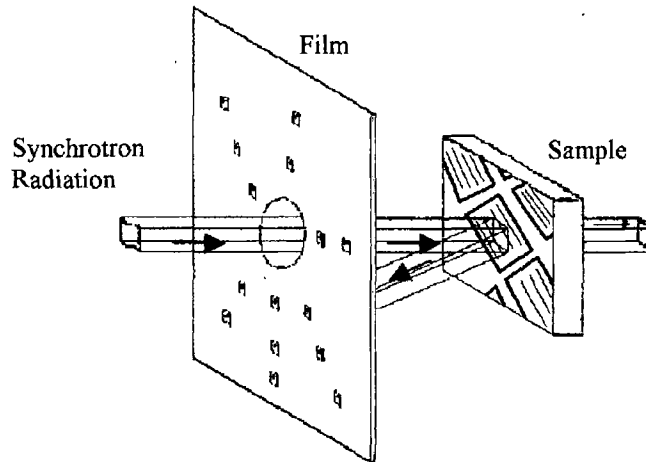


Figure 2-23 Back-reflection Topography.

Depending on the wavelength of the diffracted beam, typical penetration depths can vary from $<1 \mu\text{m}$ to $>1000 \mu\text{m}$ in e.g. silicon. Please note that many reflections, each with a different associated penetration depth, are recorded simultaneously. Penetration depths (t_p) tend to be much smaller in unstrained perfect crystals, where the dynamical theory of diffraction applies. However, for imperfect or strained materials, e.g. GaN, GaAs, SiC, InP or silicon with circuit topography or strained epitaxial layers, conventional kinematical theory applies [42] and

$$t_p = \left[\mu(\lambda) \left(\frac{1}{\sin \phi_i} + \frac{1}{\sin \phi_f} \right) \right]^{-1}$$

where t_p = penetration depth, ϕ_i = incident grazing angle, ϕ_f = exit grazing angle and $\mu(\lambda)$ = wavelength-dependent absorption constant for the material.

(b) White Beam Back Reflection Section Topography (BRST)

The White Beam Back Reflection Section Topography (BRST) technique is essentially similar to LA-BRT, only in this case the incoming beam is collimated into a narrow ribbon by a slit typically 10-15 μm in width. A set of Bragg case section topographs of sample cross-sections is produced as illustrated in Figure 2-24.

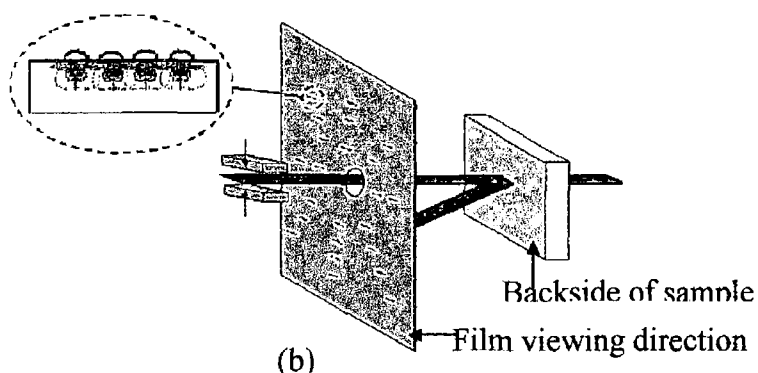


Figure 2-24 Back reflection section topography set-up.

(c) White Beam Large Area Transmission (Laue) Topography (LAT)

The transmission technique can be classified into large area and section transmission methods. In large area transmission, each diffracted beam has a different wavelength due to the d spacing and θ_B value of the crystal planes producing the reflection. Figure 2-25 shows the experimental set-up for the transmission geometry [42].

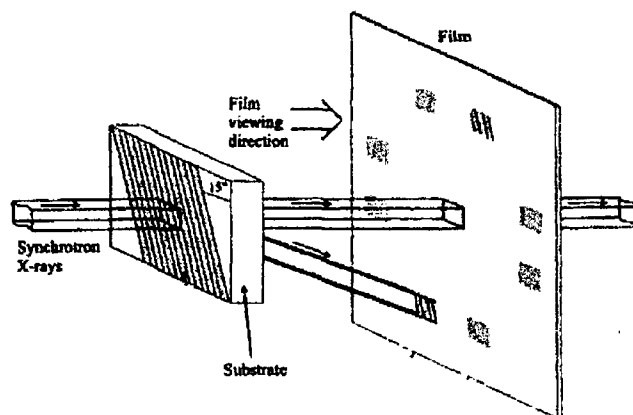


Figure 2-25 Large area transmission geometry for x-ray topography.

(d) White Beam Transmission Section (Laue) Topography (ST)

Similar to back-reflection x-ray topography, the beam is collimated into a ribbon, whose width is typically 10-15 μm and passed into the crystal. The diffracted intensity passing through the crystal is recorded on the photographic plate as illustrated in Figure 2-26 [42].

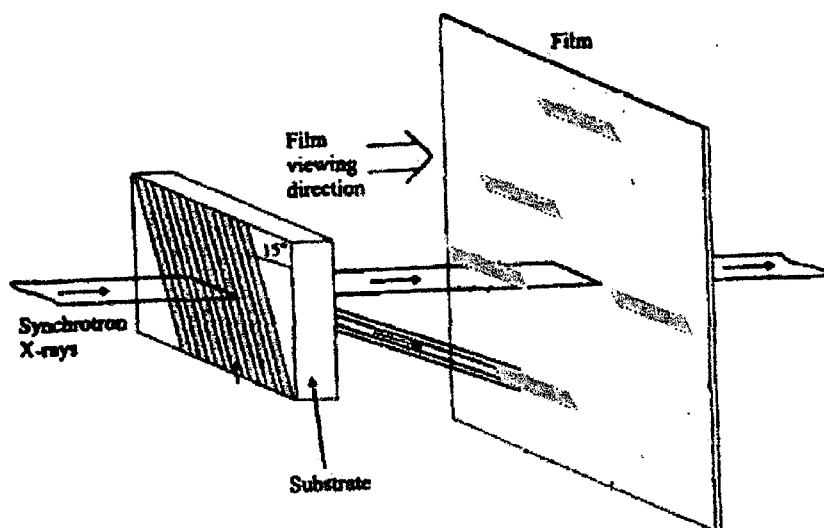


Figure 2-26 Transmission section topography.

2.3 SXRT interpretation of Stress Analysis of IC Processing Steps

Many topographic scientists have studied IC processing-induced stresses in semiconducting single Si crystals using XRT or SXRT. For example, Blech and Meieran [43]-[46], and Schwuttke [47]-[48] have published many papers on this topic, which have proved to be very valuable for this thesis.

Meieran and Blech [43] used the large-area transmission (Laue) or projection technique to investigate strains induced in Si substrates due to oxide and metal thin film deposition. They found that the elastic strain was visible via both extinction contrast and Borrmann (anomalous transmission) effects near film edges. The values

of $\mathbf{g} \cdot \mathbf{H}_i$ were compared to the contrast intensity which were recorded during measurement, where \mathbf{g} = the diffraction vector and \mathbf{H}_i = the unit vector normal to the film edge and pointing away from film edge. The extinction contrast (black/white contrast) in the image is governed by the relationship between the diffraction vector (\mathbf{g}) and the lattice displacement (\mathbf{H}_i) as shown in Figure 2-27. The vector \mathbf{H}_i is normal to the lattice displacement and deviates from the lattice direction in the undisturbed crystal due to an imposed strain field.

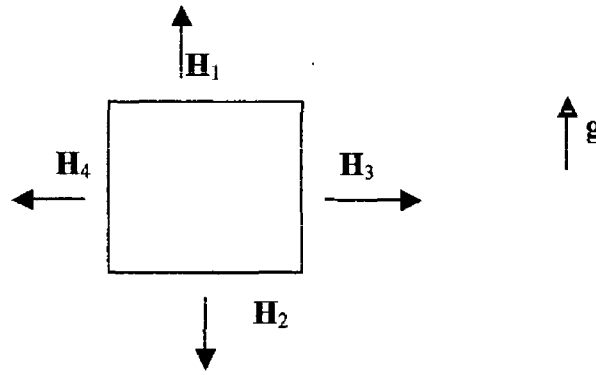


Figure 2-27 The lattice displacement (\mathbf{H}_i) of Si lattice planes, due to a square overlayer. The imposed strain in the Si pushes away from the edges of this overlayer (i.e. Si is in compression) as indicated by the displacement vectors \mathbf{H}_i . For the sake of this discussion, the direction of the diffraction vector, \mathbf{g} , is shown.

For an oxide film on a Si sample, three cases were examined by Meieran and Blech [43]:

- (a) $\mathbf{g} \cdot \mathbf{H} \approx 1$, the vector \mathbf{g} is parallel or nearly parallel to the vector \mathbf{H} (e.g. \mathbf{H}_1). As a result, that region in the diffracting Si is visible with enhanced (i.e. black) intensity.
- (b) $\mathbf{g} \cdot \mathbf{H} \approx 0$, \mathbf{g} is perpendicular or nearly perpendicular to \mathbf{H} (e.g. \mathbf{H}_3 and \mathbf{H}_4), resulting in reduced diffracted intensity or white contrast.
- (c) $\mathbf{g} \cdot \mathbf{H} \approx -1$, \mathbf{g} is anti-parallel or nearly anti-parallel to \mathbf{H} (e.g. \mathbf{H}_2), resulting in a contrast which is intermediate between (a) and (b).

However, these assumptions are reversed when a deposited metal film on Si was investigated. This contrast reversal between the oxide film and metal film can be explained in terms of the force \mathbf{F} at the film edge, which points toward the centre of the lattice curvature. In the case of the oxide film, \mathbf{F}_1 is parallel to \mathbf{H}_1 (film in compression-see Fig. 2-28). Hence the edge wherein $\mathbf{g} \cdot \mathbf{H}_1 > 0$ is a region of positive curvature. This is reversed for film edge \mathbf{H}_2 . In contrast, the metal film is opposite to the oxide film in that now \mathbf{F}_1 is anti-parallel to \mathbf{H}_1 (film in tension), thus this edge, wherein $\mathbf{g} \cdot \mathbf{H}_1 > 0$ produces a lower intensity diffraction, is an area of negative curvature. This picture relating to the black/white contrast is shown in Figure 2-28. However, an alternative and easier explanation is shown in Fig. 2-29 where the Forces (\mathbf{F}_i) are not used, but rather the lattice displacements (\mathbf{H}_i) they induce are studied. For example, in the previous case of the oxide film, forces \mathbf{F}_1 and \mathbf{F}_2 are parallel to \mathbf{H}_1 and \mathbf{H}_2 , respectively. Thus, at the edge of the film, the black contrast appears at the film edge 1 ($\mathbf{g} \cdot \mathbf{H}_1 > 0$) and white contrast is observed at the film edge 2 ($\mathbf{g} \cdot \mathbf{H}_1 < 0$). On the other hand, if \mathbf{F}_1 and \mathbf{F}_2 point inwards from the film edge as for the metal film, \mathbf{H}_1 and \mathbf{H}_2 are also in the same direction as \mathbf{F}_1 and \mathbf{F}_2 , respectively. Therefore, the white contrast is visible at the film edge 1 ($\mathbf{g} \cdot \mathbf{H}_1 < 0$) and the black contrast appears at the film edge 2 ($\mathbf{g} \cdot \mathbf{H}_1 > 0$). This explanation is illustrated in Figure 2-29.

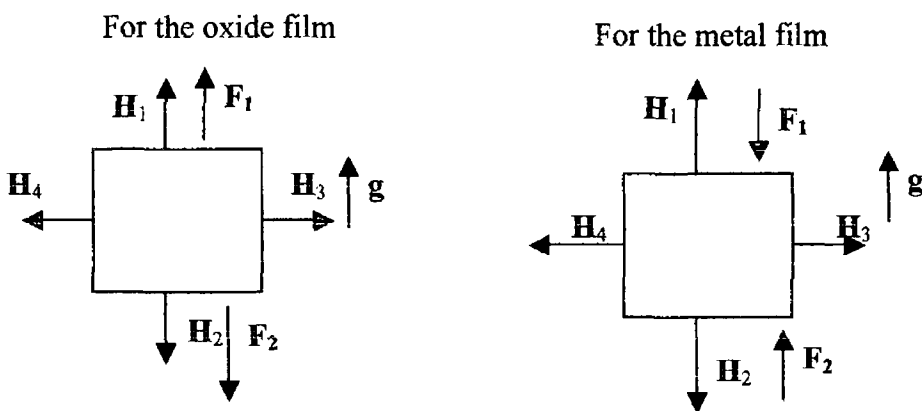


Figure 2-28 The force (\mathbf{F}_i) and $\mathbf{g} \cdot \mathbf{H}_i$ relation of Meieran and Blech [45].

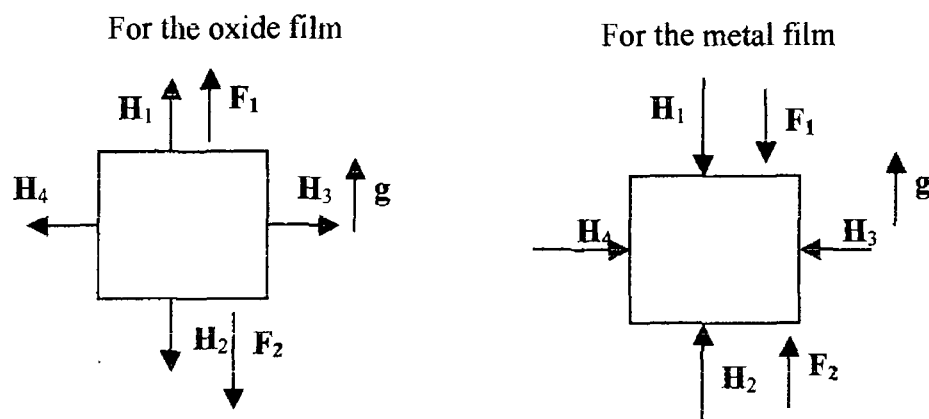


Figure 2-29 An alternative and easier explanation for x-ray topographic contrast around a strained structure.

The relationship between the values of $g \cdot H_i$ and the intensity of the extinction contrast in topographs due to the strain induced in the Si substrate is also described by Schwuttke *et al.* for the case of a metal film on Si [47]-[48]. They found that when $g \cdot S$, where S = the vector of strain gradient, is equal to 1 the Si adjacent to the film edge always shows the strongest x-ray diffracted intensity. When $S = 0$, the Si near the film edge shows a reduced contrast. His assumption is in agreement with the result of Meieran and Blech [14] wherein the force direction F is related to S .

In addition, Meieran and Blech also related the black and white contrast (extinction contrast) of $g \cdot H_i$ to the lattice curvature at the interface of the Si and the metal [14]. It has been mentioned that when the Si near the edges of the metal layer is elastically strained by the metal film, the intensity of the x-rays diffracted from the strained area will be altered when compared to the unstrained area. This phenomenon is called surface extinction contrast, arising where the scattering power around the defect differs from that in the rest of the crystal. It is noted that this phenomenon appears when the crystal is thick and highly perfect. They found that the perfect crystalline regions do not diffract strongly. On the contrary, the defected/strained region produces a black image (enhanced intensity). The image of a strained region in a perfect Si crystal is a dark line on a light background. Two set-ups are used in to analyse this phenomenon as shown in Figure 2-30 below

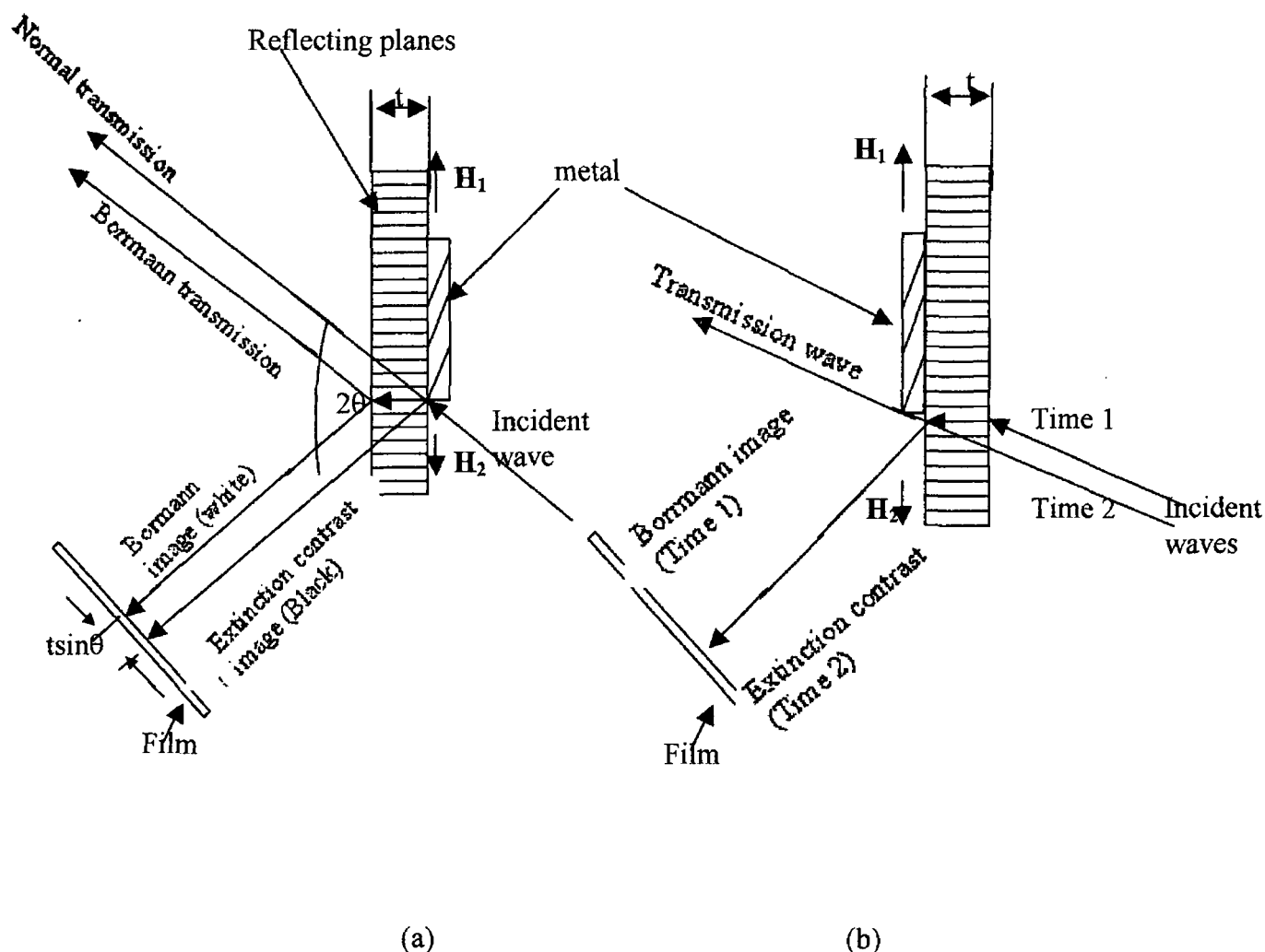


Figure 2-30 Two set-ups for extinction contrast topography [43]: (a) the metal layer faced the x-ray source and (b) the metal layer faced the recorded film.

In fig. 2-30 (a), the incoming beam enters from the metal film side. The strained area near the edge of the metal is observed as a white image beside the black image. As explained above, the black line is caused by the extinction contrast. In addition, the white line is caused by the Borrmann effect or anomalous transmission. Tanner notes that this effect relates to the progression of the (Borrmann) fan of the energy flow within a triangle bounded by the incident and diffracted beams when $\mu t > 1$ (where μ = the linear absorption coefficient and t = the sample thickness) [34]. This

Borrmann effect results in x-ray intensity reaching the exit surface and then being separated into 2 beams, namely the incident beam and diffracted beam. However, the Borrmann fan condition is destroyed/shifted as a result of the distortion of the crystal lattice around defect/strain region. The extinction and Borrmann effects are separated by $t \sin \theta$ as shown in fig. 2-30 (a). However, if the metal film faces toward the film, the Borrmann effect disappears as seen in Fig. 2-30 (b).

This mechanism is related to the change in curvature of the crystal lattice planes. The direction of the Si lattice plane curvature can imply strain fields either tension or compression at the metal/Si interface as illustrated in Figures 2-31 (a) and (b), respectively.

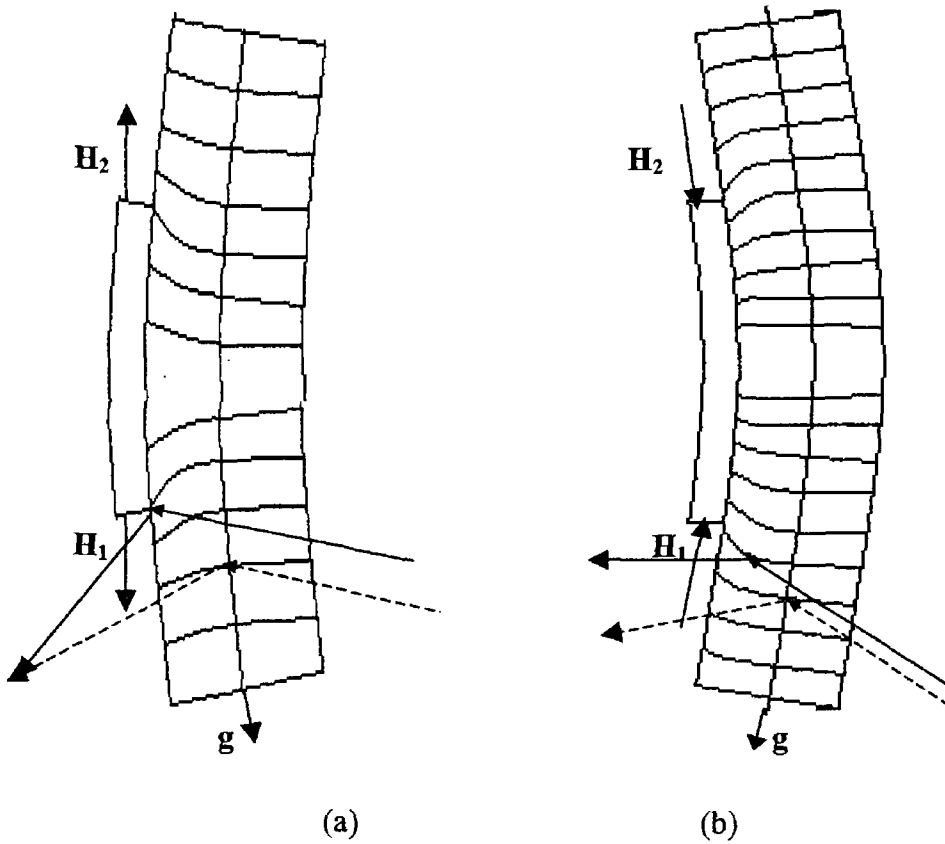


Figure 2-31 Strain directions in Si substrate [14].

In the case of Fig. 2-31 (a), the topograph shows black contrast at the edge 1 and white contrast at the edge 2, i.e. $g \cdot H_1 > 0$ and $g \cdot H_2 < 0$. Therefore, the bowing of the

sample can be drawn as in Fig. 2-31 (a). In this case, the film is in compression and puts the Si in tension at the interface. In Fig. 2-31 (b), the opposite bowing direction can generate the extinction contrast in the reverse directions such that the edge denoted by \mathbf{H}_2 diffracts more strongly than edge \mathbf{H}_1 , i.e. $\mathbf{g} \cdot \mathbf{H}_1 < 0$ and $\mathbf{g} \cdot \mathbf{H}_2 > 0$ as the metal film is on tension and puts Si in compression at the interface.

Chapter 3 Mechanical strain models

3.1 Stress-Strain Relationship

It is easier to explain stress and strain using a basic cubic element as illustrated in Figure 3-1.

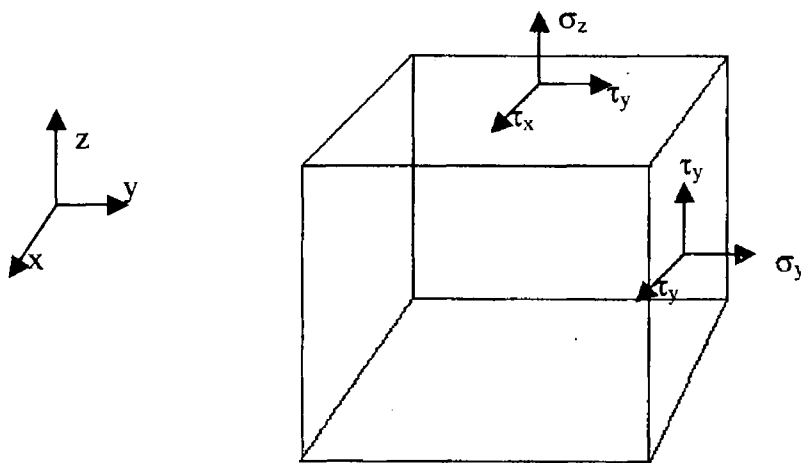


Figure 3-1 The cubic element [50].

A number of symbols are used to define the stresses acting on the six sides of the element: three symbols σ_x , σ_y and σ_z for normal stresses, and six symbols τ_{xy} , τ_{yx} , τ_{xz} , τ_{zx} , τ_{zy} and τ_{yz} for shear stresses. Assuming that $\tau_{xy} = \tau_{yx}$, etc the stress components are composed of 3 normal stresses and 3 shear stresses.

For strain components, the symbols ϵ and γ are used to define normal and shear strains, and u , v and w are the components of the displacement at any given point in the x -, y - and z - directions, respectively. By definition [50]

$$\begin{aligned}\epsilon_x &= \frac{\partial u}{\partial x}, \epsilon_y = \frac{\partial v}{\partial y}, \epsilon_z = \frac{\partial w}{\partial z} \\ \gamma_{xy} &= \frac{\partial u}{\partial y} + \frac{\partial v}{\partial x}, \gamma_{xz} = \frac{\partial u}{\partial z} + \frac{\partial w}{\partial x}, \gamma_{yz} = \frac{\partial v}{\partial z} + \frac{\partial w}{\partial y}\end{aligned}\tag{Eq. 3- 1}$$

It is well-known that the stress-strain relationship can be defined by Hooke's law. If a rectangular sample suffers a normal stress in the x-direction, σ_x , the unit elongation of the sample is given by [50]

$$\varepsilon_x = \frac{\sigma_x}{E} \quad \text{Eq. 3- 2}$$

where E is the modulus of elasticity (Young's modulus) and ε_x is the normal strain in the x-direction. The lateral strain components can be written as

$$\varepsilon_y = -\nu \frac{\sigma_x}{E} \quad \text{and} \quad \varepsilon_z = -\nu \frac{\sigma_x}{E} \quad \text{Eq. 3- 3}$$

where ν is Poisson's ratio.

However, if the sample suffers normal stresses in all directions, i.e. σ_x , σ_y and σ_z simultaneously, and the strain components are produced by each of the three stresses, then the stress-strain relationship [50] is

$$\begin{aligned} \varepsilon_x &= \frac{1}{E} [\sigma_x - \nu(\sigma_y + \sigma_z)] \\ \varepsilon_y &= \frac{1}{E} [\sigma_y - \nu(\sigma_x + \sigma_z)] \\ \varepsilon_z &= \frac{1}{E} [\sigma_z - \nu(\sigma_x + \sigma_y)] \end{aligned} \quad \text{Eq. 3- 4}$$

The relation between shear strain and shear stress is defined by E and ν , that is

$$G = \frac{E}{2(1 + \nu)} \quad \text{Eq. 3- 5}$$

where G is the shear modulus of elasticity. Therefore, $\gamma = \frac{\tau}{G}$ where γ is the shear strain.

3.2 Finite Element Modeling (FEM)

FEM was first applied to problems of stress analysis to calculate a “field quantity” [49] on its displacement field, resulting in a calculation of the peak values or gradients of the field. However, FEM provides only an approximate value, not the solution. Basically, material structures are divided into several elements and each element is reconnected at nodes, which are then used to form a set of simultaneous algebraic equations for entire structures. Figure 3-2 shows a two-dimensional model of a gear tooth element.

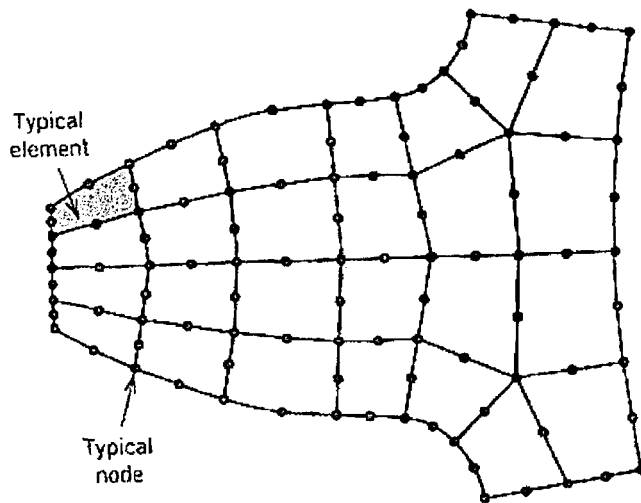


Figure 3-2 Two-dimensional model of a gear tooth. It is noted that all nodes and elements are in the plane of the paper [49].

After the structure is specified the elements and nodes, parameters e.g. loads, material properties, etc., will be identified in a Pre-process step. Thereafter, a Post-processing step will allow us to manipulate the set of equations.

To obtain a correct result, the models must be selected properly for the material structure. The models are categorised into one of a number of models, including the bar and beam model, plane model, shell model etc. For most semiconductor applications, the plane model is most commonly used since the thickness (y) of the thin film is much smaller than its length (x) and width (z) as shown in Figure 3-3.

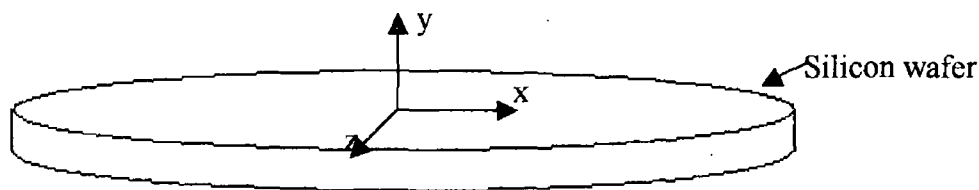


Figure 3-3 The general geometry of the plane model for semiconductor applications.

3.2.1 Plane Stress and Plane Strain

Consider a force which is applied uniformly at the boundary, and which is parallel to the plane of a thin plate as shown in Figure 3-4.

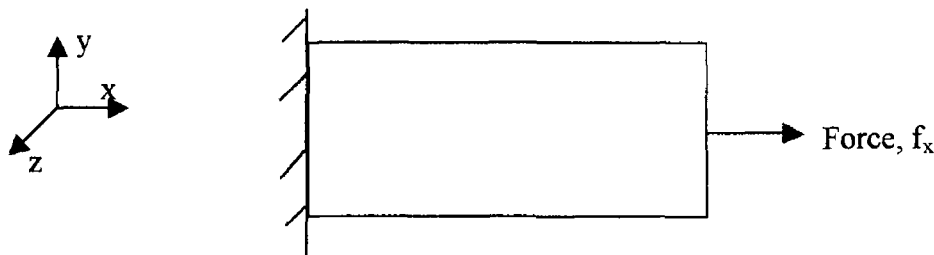


Figure 3-4 The geometry for plane stress and strain analysis.

The stress components σ_z , τ_{xz} and τ_{yz} are zero on both faces of the plate. Hence, it is possible to hypothesise that these components are also zero inside the plate. The stress components of σ_x , σ_y and τ_{xy} are only considered in this circumstance and are independent of z . This is called plane stress.

In contrast, if the dimension of the sample in the z -direction is very large, and if it is assumed that all cross sections are the same, the displacements u and v are functions of x and y and are independent of z . Since the displacement w is zero, it can be written that

$$\begin{aligned}\gamma_{yz} &= \frac{\partial v}{\partial z} + \frac{\partial w}{\partial y} = 0 \\ \gamma_{xz} &= \frac{\partial u}{\partial z} + \frac{\partial w}{\partial x} = 0 \\ \varepsilon_z &= \frac{\partial w}{\partial z} = 0\end{aligned}\tag{Eq. 3-6}$$

From Eq. 3-6, σ_z can be derived in terms of σ_x and σ_y such that

$$\begin{aligned}\sigma_z - \nu(\sigma_x + \sigma_y) &= 0 \\ \sigma_z &= \nu(\sigma_x + \sigma_y)\end{aligned}\tag{Eq. 3-7}$$

At this point the plane stress and plane strain problems can be examined by the determination of σ_x , σ_y and τ_{xy} as a function of x and y only [50].

By using Hooke's law in Eq. 3-6, the relation between stress and strain for the plane model can be given as

$$\begin{aligned}\varepsilon_x &= \frac{1}{E}(\sigma_x - \nu\sigma_y) \\ \varepsilon_y &= \frac{1}{E}(\sigma_y - \nu\sigma_x) \\ \gamma_{xy} &= \frac{1}{G}\tau_{xy} = \frac{2(1+\nu)}{E}\tau_{xy}\end{aligned}\tag{Eq. 3-8}$$

and

$$\begin{aligned}\varepsilon_x &= \frac{1}{E}[(1-\nu^2)\sigma_x - \nu(1+\nu)\sigma_y] \\ \varepsilon_y &= \frac{1}{E}[(1-\nu^2)\sigma_y - \nu(1+\nu)\sigma_x] \\ \gamma_{xy} &= \frac{1}{G}\tau_{xy} = \frac{2(1+\nu)}{E}\tau_{xy}\end{aligned}\tag{Eq. 3-9}$$

Since the elastic problem requires the solution of certain partial differential equations, the numerical method was invented to solve several thousand linear

algebraic equations simultaneously, and is called Finite Element Modelling (FEM) [49].

3.3 Example of Models

There are two examples of FEM in this study, i.e. for flip-chip packaging and copper metallisation.

3.3.1 FEM of flip-chip process induced stress in a silicon substrate

FEM is used commonly in Integrated Circuit (IC) packaging since it is known as an effective method to predict the mechanical situation in multi-component systems with complicated material behaviour, geometry and thermal loading patterns during and after electronic packaging processes. In this project, the mechanical stress induced by solder bump reflow processing has been analysed. However, there are few studies relating directly to this process step. Most studies employed FEM to simulate the mechanical stress after the IC chip was flipped to contact either organic or ceramic substrates with an underfill material rather than solder process itself [51]-[54]. However, the geometry, dimensions and boundary conditions used in these studies have proved to be useful for this project. In addition, several researchers have developed/modified the two-dimensional (2-D) FEM methods in order to improve the accuracy of modelling. As mentioned above, the thickness of typical electronic packaging structures is smaller than the length and the width of the wafer; therefore, 2-D plane strain models are commonly employed for modelling the thermomechanical behaviour.

Madenci *et al.* [51] studied the effect of underfill on the mechanical stress using special FEM techniques. The thermomechanical stress induced between the substrate and die was investigated with and without an underfill material layer. It is believed that the underfill layer can reduce the strain in the solder connections between the die and the substrate, thus enhancing the thermomechanical reliability of

the flip-chip assembly. However, interfacial cracking still remained due to the stress intensification at the interface between the substrate and the solder bump, and the die and the solder bump as shown in Figure 3-5. Therefore, Madenci *et al.* aimed to use FEM to predict the cracks between material interfaces (dark areas in Fig. 3-5) using special techniques for modelling the singular stress behaviour near the material junction based on asymptotic expansions. This technique is called a global/local finite element analysis. This technique is based on the 2-D theory of elasticity and often uses the polar co-ordinate system (r, θ). The technique is outlined in Figure 3-5.

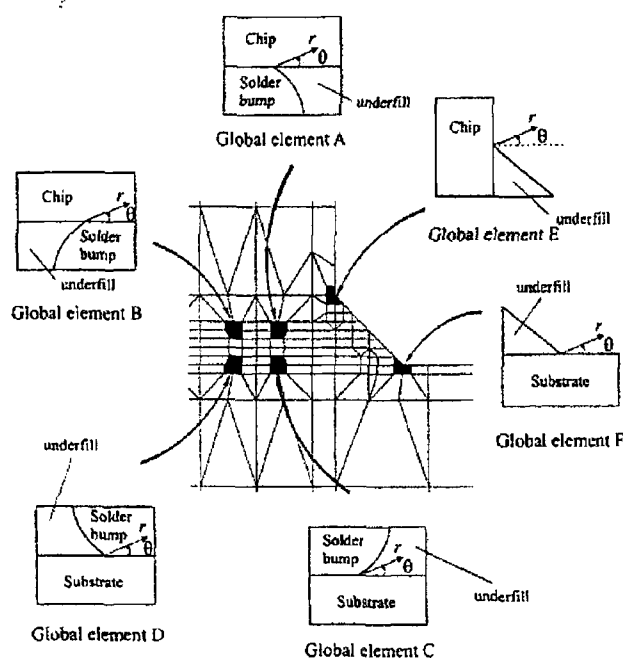


Figure 3-5 Locations of global elements as part of the local finite element representation in the presence of underfill [51].

The effect of the underfill in flip-chip packaging was also investigated by Wang *et al.* [52] using a non-linear FEM method. Geometric and material nonlinearities were considered such as the viscoelastic properties of the underfill and the viscoplastic properties of the solder alloys. The thermal residue stresses induced by different stress-free temperatures for different materials in a flip-chip assembly were simulated using two models: processing and non-processing models. The flip-chip processes consist initially of bonding the silicon chip onto the substrate at temperature T_1 and cooling the chip to room temperature T_2 , and subsequently,

dispensing the underfill material under and around all of the chip at temperature T_2 , and finally cooling the chip to room temperature T_1 . The model assumed that (a) the silicon chip was linearly elastic and temperature independent and (b) the flip-chip solder balls (95PbSn and 63PbSn) were elastic-plastic isotropic materials in an initial stress state. A two-dimensional plane strain model was used with boundary conditions, dimensions and the flip-chip geometry as in Figure 3-6.

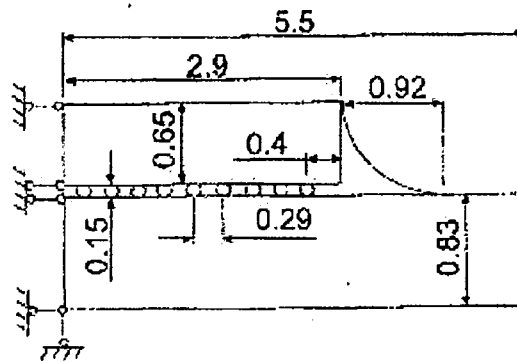


Figure 3-6 The geometry and boundary conditions of flip-chip for the FEM study in [52]. It is noted that the scale is in mm.

In the processing model, the analysis was performed following the temperature step as described above. In contrast, the thermal stress induced by the first step was neglected in the non-processing model. Therefore, T_2 was the stress-free temperature for the whole package. It was found that the stresses and deflections observed from the non-processing model were smaller than those observed in the the processing model due to the elimination of the residual stress from the first step of the flip-chip process.

Yao and Qu [53] analysed flip-chip packaging using 2-D plane stress quadrilateral and 4-node 2-D plane strain elements, and compared these to a 4-node linear tetrahedral element in three-dimensional (3-D) FEM. Figure 3-7 illustrates the geometry, dimensions and boundary conditions used for the flip-chip sample.

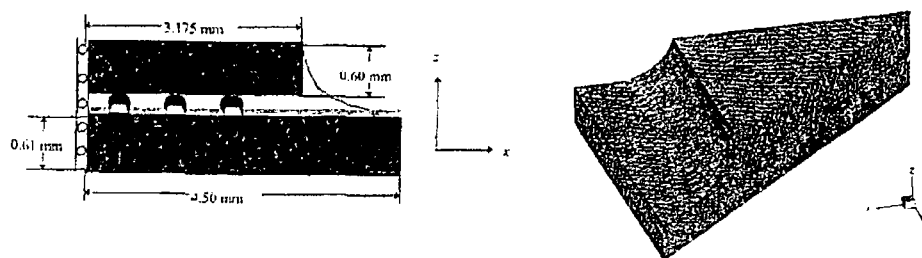


Figure 3-7 Geometry, dimensions and boundary conditions for the 2-D and 3-D FEM study in [53].

It was found that the 2-D result overestimated the stress distribution and the deflection of the flip-chip assembly. However, the 2-D plane stress result was reasonably close to the 3-D estimates, which are known to be the most accurate. This is similar to the work of Variyam *et al.* [54].

3.3.2 FEM of Cu Metallisation Induced Stress in Si Substrate in IC Processing

Most of the simulation papers for thermal stress studies of the copper metallisation in IC interconnect investigated the effect of the thermal stress in copper thin film. However, the results of those papers can be a guideline to understand the behaviour of the copper on Si. For instance, Su *et al.* [59] investigated thermally induced stresses for voiding failure in the Cu interconnects using FEM. This stress generated via the differences in the CTEs between the metal and the passivation material, which can be relieved by the formation of stress-induced voids. The model considered the stresses in terms of anisotropic mechanical properties for copper and for different crystallographic orientations of the grains in the copper interconnect lines. The simulation showed that the highest stress concentration is at the interconnection/ dielectric interface and at the grain boundaries. It was reported that the grain structure of the line approaches and reaches the bamboo structure which has a single grain boundary along the line width for lines narrower than the grain size as the line width decreases as a function of the number of voids and as the ratio of central voids to edge voids decreases.

Nevertheless, the stress analysis of the Cu interconnect is not as complicated as that of the flip-chip process. Many papers have examined the stress in Si due to other thin film materials.

CHAPTER 4 MICRO-RAMAN SPECTROSCOPY

Researchers have been using a variety of techniques to observe material and device behaviour in microelectronics. Vibrational spectroscopic characterization is one of these techniques since the effect of external factors can alter the material vibrational and electronic spectra.

Raman spectroscopy is one of the aforementioned vibrational techniques, involving the scattering of electromagnetic radiation by optical phonons in solids and molecular vibrations [60]. The scattering of light by solid interactions can be categorised as elastic (Rayleigh scattering) and inelastic (Raman scattering). The former is observed when the scattered light is of the same frequency as the incident light, whereas the inelastic scattering is observed at a different frequency, and constitutes what is known as a Raman spectrum [62]. In this report, only inelastic scattering is emphasized.

The inelastic scattering mechanism was postulated by Brillouin (1922) and Smekal (1923) [62]. However, the first experimental inelastic (Raman) scattering was obtained by Raman and Krishnan in 1928 [63]. Subsequently, a laser source was used for Raman spectroscopy by Porto and Wood (1962) [62]. Since then, many research scientists have used Raman spectroscopy in many fields, e.g. chemistry, physics and semiconductor devices.

4.1 The Raman Scattering Mechanism

As mentioned above, Raman scattering results from the interactions of the vibrational and/or rotational motions with electromagnetic radiation. In modern systems, the interaction of the molecular vibrations with the laser excitation produces the Raman spectrum. An idealised scattering experiment is illustrated in Figure 4-1.

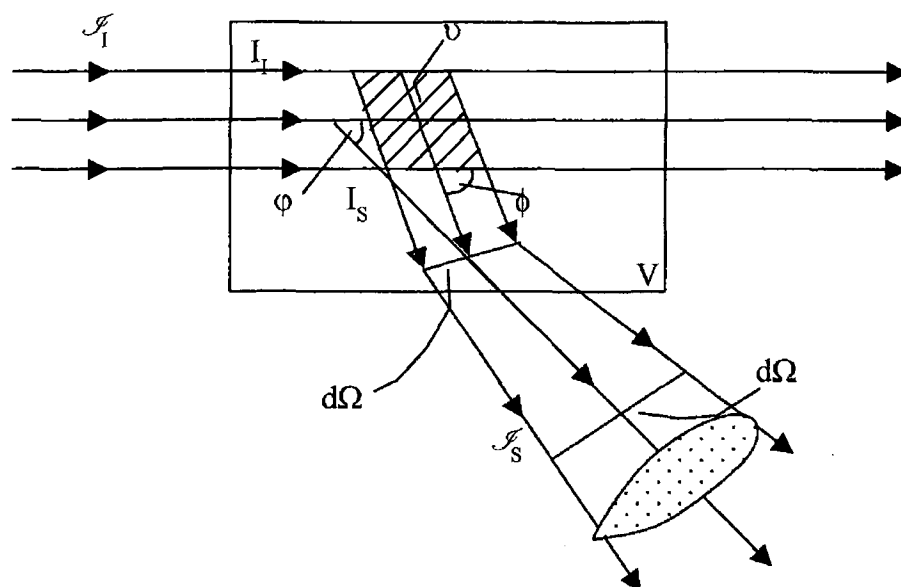


Figure 4-1 Idealised scattering experiment [64].

The incident beam from the laser source passes through a sample with volume V and is scattered in all directions. A detector is set up to investigate the beam scattered at angle ϕ to the incident beam in the sample volume of V . The tolerable range of the detector is limited to a small solid angle $d\Omega$ by the lens. The intensity outside the sample of the incident and scattered beams are labelled \mathcal{J}_I and \mathcal{J}_S , respectively, corresponding to the scattering angle ϕ , and the intensities are I_I and I_S inside the scattering sample [64].

Using the laser as a light source, the laser frequency is regarded as monochromatic with a single angular frequency ω_0 and a magnitude of the propagation vector, k_0 . The interaction of the matter with the electromagnetic radiation, which is produced by a laser in this case, can be analysed in terms of an energy-transfer mechanism [62]. In the scattering mechanism, at least two quanta moving simultaneously must be involved in the light-matter system. Rayleigh scattering takes place when a quantum of light energy is generated at the same time that the incident light is annihilated. Hence, the molecule is unchanged by this process. On the other hand, inelastic scattering occurs when the photon energy is less or more energetic than the

annihilated incident light. Consequently, the scattered light is obtained at a frequency either lower or a higher than that of the incident light, called Stokes and Anti-Stokes Raman scattering, respectively. The scattering spectra of these three mechanisms are depicted in Figure 4-2.

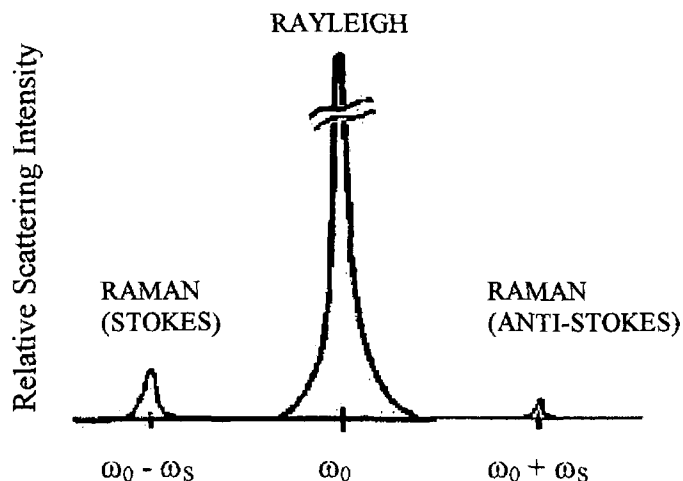


Figure 4-2 Molecular vibrations in the sample at frequency ω_s [62].

From Fig. 4-2, the laser excitation at frequency ω_0 is visible as the relatively strong Rayleigh line and the Raman lines are a result of the inelastic scattering by the molecular vibration of frequencies $\pm\omega_s$. The scattering frequency is defined by a conservation law as [60]

$$\omega = \omega_0 - \omega_s \quad \text{Eq. 4- 1}$$

In Stokes Raman scattering, the scattered photon is associated with an energy gain $\hbar\omega$ by the sample where $\omega = \omega_0 - \omega_s$. On the other hand, the sample loses energy $\hbar\omega$ for each scattered photon in the anti-Stokes Raman scattering where $\omega = \omega_s - \omega_0$.

In addition, the scattering wavevector is given [60] as

$$\mathbf{k} = \mathbf{k}_0 - \mathbf{k}_s \quad \text{Eq. 4- 2}$$

For the inelastic scattering process, the conservation of energy and momentum must be balanced. To consider these conservation laws, the elementary excitations are

denoted by the wavevector \mathbf{q} , called the crystal momentum. In the first-order processes, a single elementary excitation is taken into account; therefore, the scattering wavevector is equal to the excitation wavevector:

$$\mathbf{k} = \mathbf{q} \quad \text{Eq. 4-3}$$

and the conservation of energy is

$$\omega = \omega_{\mathbf{q}} \quad \text{Eq. 4-4}$$

In higher order scattering, the frequency ω is a sum of the frequencies of two or more quanta for which the total wavevector = \mathbf{k} [60], which can be written as

$$\mathbf{k} = \sum_j \mathbf{q}_j \quad \text{Eq. 4-5}$$

In the inelastic scattering process, the magnitude and orientation of the wavevector are examined by the geometry of the experimental set-up. Three standard arrangements for the propagation of the incident and scattered beams can be obtained as illustrated in Figure 4-3.

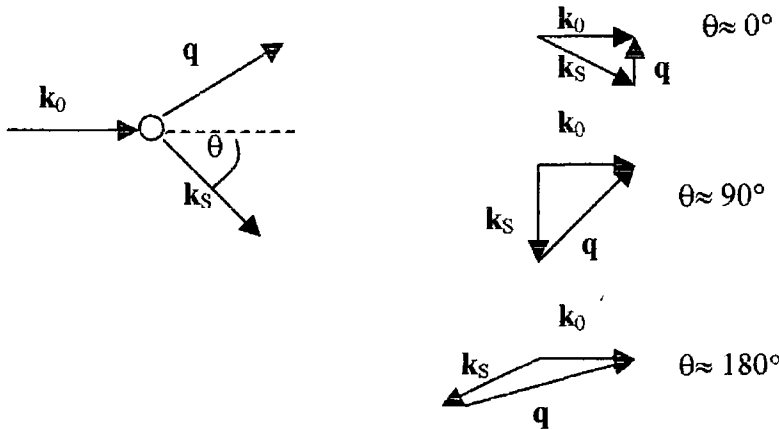


Figure 4-3 The scattering process and their geometries [60] given Eq. 4-2 and Eq. 4-3, $\mathbf{q} = \mathbf{k}_0 - \mathbf{k}_s$.

The smallest wavevector is in the forward geometry ($\theta \approx 0^\circ$) and the magnitude of the scattering wavevector is

$$|\mathbf{k}_{\min}| = [n\omega_0 - n\omega_s]/c \quad \text{Eq. 4-6}$$

and the largest wavevector is in the backscattering geometry ($\theta \approx 180^\circ$), the scattering wavevector being

$$|\mathbf{k}_{\max}| = [n\omega_0 + n\omega_s]/c \quad \text{Eq. 4-7}$$

The most common practice in micro-Raman scattering is to use the largest wavevector, which is in the backscattering geometry.

4.2 Electromagnetic Radiation and Classical Light Scattering

Maxwell's equations, which describe the behaviour of the electric and magnetic fields in space and time, are used in the analysis of the scattering phenomena. It is assumed that a plane-polarised homogeneous medium exists in this case. The electric vector, \mathbf{E} , is parallel to the X axis, and the magnetic vector, \mathbf{H} , is directed along the Y axis. Thus, similar to the Poynting vector discussion in Chapter 2, the direction of the propagation of the wave (Poynting vector, \mathbf{S}) is in the Z direction [62]. The electric field (\mathbf{E}) in the crystal at position \mathbf{r} is given as

$$\mathbf{E}_x = \mathbf{E}_x^0 \exp[-i(\mathbf{k}_0 \cdot \mathbf{r} - \omega_0 t)] \quad \text{Eq. 4-8}$$

where \mathbf{k}_0 is the magnitude of the wavevector, t is time, \mathbf{E}_x is the electric field in the X-direction and \mathbf{E}_x^0 is the amplitude of the wave in the X-direction.

The excitation of the crystal corresponding to the inelastic light scattering is given by a space- and time-dependent amplitude, i.e. the lattice vibration. The vibration amplitude at position \mathbf{r} is given [63] as

$$Q_j = Q_j^0 \exp[\pm i(\mathbf{q}_j \cdot \mathbf{r} - \omega_j t)] \quad \text{Eq. 4-9}$$

where Q_j is the normal coordinate of the vibration, \mathbf{q}_j is the wavevector of the lattice wave at any possible vibration j of the lattice. This quantised lattice vibration is called a normal mode or *phonon*, which can cause a variation in the electrical susceptibility of the crystal and provide for Raman scattering.

When the molecule is polarised by the electric field described by Eq. 4-8 of the laser light with a frequency ω_0 in a crystal with direction \mathbf{k}_0 , a fluctuating electric moment is established in the scattering medium by the simultaneous action of the incident beam and the elementary excitations of the solid, thus creating Stokes and anti-Stokes radiation [60]. The electric moment per unit volume, i.e. polarisation \mathbf{P} , of the electric field (\mathbf{E}) is defined as [62]

$$\mathbf{P} = \varepsilon_0 \chi \mathbf{E} \quad \text{Eq. 4- 10}$$

where χ is the first-order or linear susceptibility tensor of the medium and ε_0 is the permittivity in free space.

Thus, the susceptibility, which may be variable due to the lattice vibration, can be written in terms of these vibrations and expanded in a Taylor series [62] as

$$\chi = \chi_0 + \left(\frac{\partial \chi}{\partial Q_j} \right)_0 Q_j + \left(\frac{\partial^2 \chi}{\partial Q_j \partial Q_k} \right)_0 Q_j Q_k + \dots \quad \text{Eq. 4- 11}$$

It is noted that the higher terms can be neglected for small atomic displacements. Thus, eq. 4-10 can be given as [62]

$$\mathbf{P} = \varepsilon_0 \chi_0 \cdot \mathbf{E}_x^0 \exp[-i(\mathbf{k}_0 \cdot \mathbf{r} - \omega_0 t)] + \varepsilon_0 \mathbf{E}_x^0 \left(\frac{\partial \chi}{\partial Q_j} \right)_0 Q_j^0 \exp[i(\omega_0 \pm \omega_j)t] \exp[-i(\mathbf{k}_0 \pm \mathbf{q}_j) \cdot \mathbf{r}]. \quad \text{Eq. 4- 12}$$

In Eq. 4-12, the first term $\varepsilon_0 \chi_0 \cdot \mathbf{E}_x^0 \exp[-i(\mathbf{k}_0 \cdot \mathbf{r} - \omega_0 t)]$ represents the oscillation of the induced moment at the frequency ω_0 of the incident light, resulting in Rayleigh scattering. The induced moments which are produced at frequencies $\omega_0 - \omega_j$ lead to Stokes and at $\omega_0 + \omega_j$ to Anti-Stokes first-order Raman scatterings, and this scattered light is propagated in the directions $\mathbf{k}_0 - \mathbf{q}_j$ and $\mathbf{k}_0 + \mathbf{q}_j$, respectively [64]. It is noted that at temperatures near zero, the Stokes scattering predominates and the anti-Stokes scattering vanishes [66].

From Eq. 4-12, it is clear that the Raman spectrum is dependent on the orientation of the crystallographic axes with respect to the vibrational direction and polarisation of molecular coordinates, Q_j [65].

To understand the Raman intensity, the polarisation of the Raman scattered light for an atom i at position u from Eq. 4-11 can be written as

$$\chi_{ij}(u) = \chi_{ij}(0) + \sum_f \chi_{ij,f} Q_f \quad \text{Eq. 4- 13}$$

where tensor χ_{ij} is the electronic susceptibility as a function of the frequency ω_0 of the system.

The scattering cross-section σ can be related to the scattered intensity (I_s) and average energy per second from the vibrating dipole or average power (Φ) as

$$\sigma = \frac{\Phi}{I_s} \quad \text{Eq. 4- 14}$$

Thus, the differential cross-section ($d\sigma/d\Omega$) as a solid angle is given as [69]

$$\frac{d\sigma}{d\Omega} = \frac{d\Phi/d\Omega}{I_s} \quad \text{Eq. 4- 15}$$

Alternatively, the differential cross-section can be defined as [69]

$$\frac{d\sigma}{d\Omega} = \frac{\omega_0^4 V^2}{c^4} \left| \sum_{ij} e_{si} \chi_{ij} e_{0j} \right| \quad \text{Eq. 4- 16}$$

where V is the volume of the scattering medium, and e_0 and e_s are unit polarisation vectors for the incident and scattered light, respectively. The susceptibility χ_{ij} depends on the electronic structure of the system, which alters the vibration. The light scattering due to the phonon-induced change in susceptibility is known as Raman scattering.

By substituting the susceptibility χ_{ij} from Eq. 4-13 into Eq. 4-16 and using the quantum theory of the harmonic oscillator for the thermal average a Raman differential cross-section was given by Placzek [69] as

$$\frac{d\sigma}{d\Omega d\omega} = \frac{\hbar V^2}{2c^4} \sum_f \frac{(\omega_0 - \omega_f)^4}{\omega_f} \{n_f + 1\} \delta(\omega - \omega_f) + n_f \delta(\omega + \omega_f) \left\{ \sum_{ij} e_{Si} \chi_{ij,f} e_{0j} \right\}^2 \quad \text{Eq. 4-17}$$

where ω_f = the Raman shift

$n_f = [\exp(\hbar\omega_f/k_B T) - 1]^{-1}$ = Bose-Einstein phonon occupation probability
for mode f

term $[(n_f + 1)\delta(\omega - \omega_f)]$ represents Stoke scattering (phonon generation)

term $[n_f \delta(\omega + \omega_f)]$ represents anti-Stokes scattering (phonon annihilation)

term $(\omega_0 - \omega_f)^4 = \omega_s^4$ = the scattering frequency term.

Eq. 4-17 is correct when $\omega_f \ll \omega_0 \ll E_g(\text{dir})/\hbar$, where $E_g(\text{dir})$ is the semiconductor direct bandgap.

In the case of a three-fold degenerate zone-centre for optical phonons in diamond and zincblende semiconductors, the electronic susceptibility χ_{ij} can be defined as [69]

$$\chi_{ij,f} \equiv \frac{1}{v_c} \sqrt{\frac{1}{\mu N}} R_{ij,f} \quad \text{Eq. 4-18}$$

where v_c = the volume of the unit cell for diamond $v_c = a^3/4$, where a is the lattice constant,

$R_{ij,f}$ = the Raman tensor which is a volume-independent quantity,

μ = the reduced mass of the unit cell,

N = the number of scattering particles in volume v_c .

Placzek [69] introduced a Raman cross-section per unit volume ($dS/d\Omega d\omega$) term defined as a scattering efficiency. Therefore, Eq. 4-17 can be re-written as [69]

$$\frac{dS}{d\Omega d\omega} = \frac{\hbar}{2\mu\nu_c c^4} \sum_{k=x,y,z} \frac{\omega_s^4}{\omega_f} \{n_f + 1\} \delta(\omega - \omega_f) + n_f \delta(\omega + \omega_f) \times \left| \sum_j e_{si} R_{ij} e_{0j} \right|^2$$

Eq. 4- 19

where $k = x, y, z$ is labelled as one of the three degenerate modes.

According to Placzek's semi-classical dispersion theory [65], the intensity of the scattered light is given as

$$I_s = C \sum_j |e_0 \cdot \mathbf{R}_j \cdot e_s|^2 \quad \text{Eq. 4- 20}$$

where C is a constant, e_0 and e_s are the polarisation vectors of the incident and scattered light, respectively, and \mathbf{R}_j is the Raman tensor of phonon j which is obtained from spatial symmetry of the crystal, characterised by the point group comprising of the rotations and reflections, which leave the crystal invariant.

To analyse the Raman spectrum, the number of Raman active modes must be identified by the crystal structure, i.e. the space group and the nature of the irreducible representations (Γ) of the zero-centre phonons ($q \approx 0$) in the unit cell, which is appropriate to the excitation of the scattering light. For example, silicon crystallises in the diamond structure with space group O_h . There are eight equivalent atoms in the unit cell (non-primitive).

Silicon has three Raman tensors in the crystal system where $x = [100]$, $y = [010]$ and $z = [001]$ given by

$$R_x = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & d \\ 0 & d & 0 \end{pmatrix}, R_y = \begin{pmatrix} 0 & 0 & d \\ 0 & 0 & 0 \\ d & 0 & 0 \end{pmatrix} \quad \text{and} \quad R_z = \begin{pmatrix} 0 & d & 0 \\ d & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} \quad \text{Eq. 4- 21}$$

where d indicates the non-zero component in the matrix position ij .

From Eq. 4-21, the Raman tensors correspond to phonon eigenvectors along the x-, y- and z- axes, respectively [69]. Hence, it also can be written for a polarisation along a given h-direction as [69]

$$R_h = \sum_{\lambda=x,y,z} v_{\lambda,h} R_{\lambda} \quad \text{Eq. 4-22}$$

where $v_{\lambda,h}$ is the λ^{th} component of a unit vector (eigenvector) in the h-direction.

Eq. 4-22 is applied in the case of polar semiconductors, for which the three zone centre modes are split into two transverse optic modes (TO) and one single longitudinal (LO) mode. If no strain is present, these three peaks have the same frequency. However, due to the polarisation rule in Eq. 4-22, only the LO peak is visible when measuring in backscattering mode along the (001) surface of Si and only one of the TO peaks is obtained when observing in backscattering along the (110) and ($\bar{1}10$) surfaces of the Si [71]. Details will be given later in the next section.

4.3 Raman Scattering in Semiconductors

Micro-Raman spectroscopy has been used to characterise semiconductor materials since their electronic and vibrational properties are reproducible. The characterisation can be performed without contacting or damaging the sample, which is very useful for microelectronic devices. The Raman technique can be used to examine crystalline orientation, doping level, stress, etc. in the semiconductor device. In this study, micro-Raman spectroscopy was employed to evaluate the flip-chip solder bump and the copper metallisation induced stress in Si substrates in IC processing. Table 4.2 is an outline of the electronic and vibrational properties of cubic semiconductors at room temperature.

Table 4- 1 The structural, electronic and vibrational properties of some cubic semiconductors at room temperature [69]

Material	Lattice parameter (Å)	Indirect gap (eV)	Direct gap (eV)	ω_{LO} (cm ⁻¹)	ω_{TO} (cm ⁻¹)
Diamond	3.56683	5.4	6.5	1332	
Si	3.43086	1.12	4.25	521	
Ge	5.65	0.66	0.81	303	
GaAs	5.6534	-	1.429	292	269

Note: Table 4-1 illustrates the frequencies of longitudinal (ω_{LO}) and transverse (ω_{TO}) optic phonons at $q \cong 0$.

In this study, micro-Raman spectroscopy was used particularly for stress gradient measurements in semiconductor devices. Thus, the characterisation of the stress using micro-Raman spectroscopy is emphasised below.

4.4 Stress Measurement using Micro-Raman Spectroscopy

It is well known that stress generated in the crystal can change the equilibrium position of the atoms. The phonon frequencies associated with the distorted crystal can be calculated from the force constants of the crystal between the perfect and distorted parts. In the case of small strains, it is assumed that the difference of the force constant ($\Delta\Phi$) and strains is linear, and the frequencies of the three optical modes ($k = 0$) can be solved by [70]

$$\sum_{\beta} K_{\alpha\beta} \eta_{\beta} = \omega^2 \eta_{\alpha}, \quad \alpha, \beta = 1-3 \tag{Eq. 4- 23}$$

where η_{α} are Cartesian coordinates of the eigenvectors, ω is the Raman modes' frequency in the presence of the stress, and $K_{\alpha\beta}$ are elements of the force constant tensor which can be related to the strain tensor by

$$K_{\alpha\beta} = K_{\alpha\beta}^0 + \sum_{\nu\delta} \varepsilon_{\nu\delta} K_{\nu\delta\alpha\beta}^{(\varepsilon)}, \quad K_{\alpha\beta}^0 = \omega_0^2 \delta_{\alpha\beta} \tag{Eq. 4- 24}$$

where ω_0 is the Raman frequency of the unstrained crystal, $\varepsilon_{\nu\nu}$ are elements of the strain tensor ε , and $\delta_{\alpha\beta}$ is the Kronecker delta function. For Silicon, the symmetrical tensor $K^{(\varepsilon)}$ has only three independent elements:

$$\begin{aligned} K_{1111}^{(\varepsilon)} &= K_{2222}^{(\varepsilon)} = K_{3333}^{(\varepsilon)} = p, \\ K_{1122}^{(\varepsilon)} &= K_{1133}^{(\varepsilon)} = K_{2233}^{(\varepsilon)} = q, \\ K_{1212}^{(\varepsilon)} &= K_{1313}^{(\varepsilon)} = K_{2323}^{(\varepsilon)} = r. \end{aligned} \quad \text{Eq. 4-25}$$

where p , q and r are constants, the so-called phonon deformation potentials, and ε_{ij} are the strain tensor components.

Combining Eq. 4-23 – 4-25, the secular equation, which is defined in terms of the reference axis system, where $x = [1\ 0\ 0]$, $y = [0\ 1\ 0]$ and $z = [0\ 0\ 1]$ is formed [65].

$$\begin{vmatrix} p\varepsilon_{11} + q(\varepsilon_{22} + \varepsilon_{33}) - \lambda & 2r\varepsilon_{12} & 2r\varepsilon_{13} \\ 2r\varepsilon_{12} & p\varepsilon_{22} + q(\varepsilon_{33} + \varepsilon_{11}) - \lambda & 2r\varepsilon_{23} \\ 2r\varepsilon_{13} & 2r\varepsilon_{23} & p\varepsilon_{33} + q(\varepsilon_{11} + \varepsilon_{22}) - \lambda \end{vmatrix} = 0 \quad \text{Eq. 4-26}$$

The eigenvalues λ_j in Eq. 4-26 can be related to the difference between the Raman frequency of each mode in the presence of stress (ω_j) ($j = 1,2,3$) and the absence of stress (ω_{j0}) that $\lambda_j = \omega_j^2 - \omega_{j0}^2$ or $\Delta\omega_j = \omega_j - \omega_{j0} \approx \lambda_j / 2\omega_{j0}$. The polarisation direction of each mode in the presence of stress is defined by the secular equation and its eigenvectors. The Raman frequency of each of the three modes as a function of the strain can also be solved using the above secular equation (Eq. 4-26).

However, microelectronics structures are typically oriented along a $[1\ 1\ 0]$ axis on the $(0\ 0\ 1)$ surface of the silicon wafer, where $x' = [1\ 1\ 0]$, $y' = [\bar{1}\ 1\ 0]$ and $z' = [0\ 0\ 1]$, the so-called sample axes system. The direction of the sample axes system is shown in Figure 4-4.

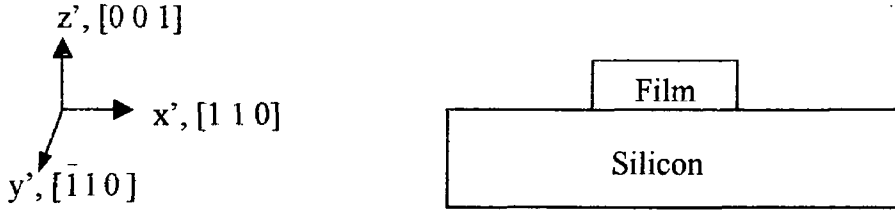


Figure 4-4 The direction of the sample along the cross section of the sample. It is noted that σ_{11}' is the uniaxial stress along the x' -axis.

To find the secular equation for a sample axes system, the elements of the force constant tensors in Eq. 4-24 can be written as [70]

$$K'_{\alpha\beta} = K'_{\alpha\beta}{}^0 + \sum_{\nu\omega} \epsilon'_{\nu\omega} K'_{\nu\omega\alpha\beta}^{(\epsilon)}, \quad K'_{\alpha\beta}{}^0 = \omega_0^2 \delta_{\alpha\beta} \quad \text{Eq. 4-27}$$

By rotating the tensor $K^{(\epsilon)}$ into the sample system, the results are [70]

$$\begin{aligned} K'_{1111}^{(\epsilon)} &= K'_{2222}^{(\epsilon)} = p', & K'_{3333}^{(\epsilon)} &= p, \\ K'_{1122}^{(\epsilon)} &= q', & K'_{1133}^{(\epsilon)} &= K'_{2233}^{(\epsilon)} = q, \\ K'_{1212}^{(\epsilon)} &= \frac{p-q}{2} + r, & K'_{1313}^{(\epsilon)} &= K'_{2323}^{(\epsilon)} = r. \end{aligned} \quad \text{Eq. 4-28}$$

$$\text{where } p' = \frac{p+q}{2} + r, \quad q' = \frac{p+q}{2} - r \quad \text{Eq. 4-29}$$

Thus, the secular equation in the sample axes system is given by [70]

$$\begin{vmatrix} p'\epsilon'_{11} + q'\epsilon'_{22} + q\epsilon'_{33} - \lambda & (p-q)\epsilon'_{12} & 2r\epsilon'_{13} \\ (p-q)\epsilon'_{12} & p'\epsilon'_{22} + q\epsilon'_{33} + q'\epsilon'_{11} - \lambda & 2r\epsilon'_{23} \\ 2r\epsilon'_{13} & 2r\epsilon'_{23} & p\epsilon'_{33} + q(\epsilon'_{11} + \epsilon'_{22}) - \lambda \end{vmatrix} = 0$$

Eq. 4-30

To solve the Raman shift-stress relationship from the secular equation, two stress models are considered: uniaxial stress and plane stress.

4.4.1 Uniaxial Stress Model

Firstly, the uniaxial stress model is given. It is assumed that only $\sigma'_{11} \neq 0$ [70]. The solution is divided into the reference and sample axes systems.

(a) *Solution in the Reference System*

In the absence of stress, the Raman tensors and corresponding polarisation vectors for the three optical modes of Si are

$$\begin{aligned} TO_1 \rightarrow R_1 &= \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & d \\ 0 & d & 0 \end{pmatrix}, \\ TO_2 \rightarrow R_2 &= \begin{pmatrix} 0 & 0 & d \\ 0 & 0 & 0 \\ d & 0 & 0 \end{pmatrix}, \text{ and} \\ LO \rightarrow R_3 &= \begin{pmatrix} 0 & d & 0 \\ d & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} \end{aligned} \quad \text{Eq. 4- 31}$$

$$v_1 = (1 \ 0 \ 0), v_2 = (0 \ 1 \ 0) \text{ and } v_3 = (0 \ 0 \ 1) \quad \text{Eq. 4- 32}$$

In the presence of stress, the secular equation in Eq. 4-26 has to be solved. De Wolf and her co-workers have a very good explanation in Ref. 10. The summaries of the Raman shift and stress relationships are given in this report. It must be remembered that the secular equation in Eq. 4-26 is in the reference axes system where x or 1=[1 0 0], y or 2=[0 1 0] and z or 3=[0 0 1].

From Hooke's law in the sample axes system,

$$\begin{aligned}
 \epsilon'_{11} &= \left(\frac{S_{11} + S_{12}}{2} + \frac{S_{44}}{4} \right) \sigma'_{11}, \\
 \epsilon'_{22} &= \left(\frac{S_{11} + S_{12}}{2} - \frac{S_{44}}{4} \right) \sigma'_{11}, \\
 \epsilon'_{33} &= S_{12} \sigma'_{11}, \\
 \epsilon'_{12} &= \epsilon'_{23} = \epsilon'_{13} = 0
 \end{aligned}
 \tag{Eq. 4- 33}$$

where the S_{ij} are the elements of the compliance tensor \mathbf{S} in the reference axes system. Subsequently, the strain tensor is rotated into the reference axes system. Hence,

$$\begin{aligned}
 \epsilon_{11} &= \epsilon_{22} = \frac{\epsilon'_{11} + \epsilon'_{22}}{2}, \\
 \epsilon_{33} &= \epsilon'_{33}, \\
 \epsilon_{12} &= \frac{\epsilon'_{11} - \epsilon'_{22}}{2}, \\
 \epsilon_{23} &= \epsilon_{13} = 0.
 \end{aligned}
 \tag{Eq. 4- 34}$$

Substituting these strain tensors (Eq. 4-34) into the secular equation (Eq. 4-26), the eigenvalues in the reference axes system can be obtained as

$$\begin{aligned}
 \lambda_1 &= p' \epsilon'_{11} + q' \epsilon'_{22} + q \epsilon'_{33}, \\
 \lambda_2 &= q' \epsilon'_{11} + p' \epsilon'_{22} + q \epsilon'_{33}, \\
 \lambda_3 &= q' \epsilon'_{11} + q' \epsilon'_{22} + p \epsilon'_{33}.
 \end{aligned}
 \tag{Eq. 4- 35}$$

Then, their corresponding eigenvectors are

$$\begin{aligned}
 v_{1_st} &= \frac{1}{\sqrt{2}}(1 \ 1 \ 0), \\
 v_{2_st} &= \frac{1}{\sqrt{2}}(\bar{1} \ 1 \ 0), \\
 v_{3_st} &= (0 \ 0 \ 1),
 \end{aligned}
 \tag{Eq. 4- 36}$$

where the subscript “st” indicates that the eigenvectors in Eq. 4-36 are in the presence of stress. From the Raman tensor in the absence of stress in Eq. 4-31,

$R_h = \sum_{\lambda=x,y,z} v_{\lambda,h} R_\lambda$. The Raman tensor from the eigenvector in Eq. 4-36 can be calculated from

$$R_{i_st} = \sum_{k=x,y,z} R_k \frac{\partial v_{\lambda}}{\partial v_{i_st}} \quad \text{Eq. 4-37}$$

Thus, the results are

$$R_{1_st} = \frac{1}{\sqrt{2}} \begin{pmatrix} 0 & 0 & d \\ 0 & 0 & d \\ d & d & 0 \end{pmatrix}, \quad R_{2_st} = \frac{1}{\sqrt{2}} \begin{pmatrix} 0 & 0 & d \\ 0 & 0 & -d \\ d & -d & 0 \end{pmatrix}, \quad \text{and} \quad R_{3_st} = \begin{pmatrix} 0 & d & 0 \\ d & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} \quad \text{Eq. 4-38}$$

From the backscattering configuration, if light is scattered along the z-axis or (0 0 1) surface, only the z-polarised phonon (R_{3_st}) or the LO peak can be observed [65]. This is seen from Eq. 4-20.

Thus, the Raman shift-stress relationship can be written as

$$\begin{aligned} \Delta\omega_3 &= [q(S_{11} + S_{12}) + pS_{12}] \sigma'_{11} / 2\omega_0 \\ &= -1.93 \times 10^{-9} \sigma'_{11} \end{aligned} \quad \text{Eq. 4-39}$$

where $S_{11} = 7.68 \times 10^{-2} \text{ Pa}^{-1}$, $S_{12} = -2.14 \times 10^{-12} \text{ Pa}^{-1}$, $S_{44} = 12.7 \times 10^{-12} \text{ Pa}^{-1}$, $p = -1.43\omega_0^2$, $q = -1.89\omega_0^2$ and $r = -0.59\omega_0^2$ [65].

If the scattering occurs along the (110) or x- axis, only the x-polarised phonon (R_{1_st}) or the TO peak is visible. Similar to the x-axis case, if the scattering takes place along the ($\bar{1}$ 10) or y- axis, only the y-polarised phonon (R_{2_st}) or TO peak is visible.

Therefore, the eigenvalues of λ_1 and λ_2 are activated and the Raman shift-stress relationship can be written as

$$\begin{aligned}\Delta\omega_{1,2} &= \frac{1}{2}[p(S_{11} + S_{12}) + q(S_{11} + 3S_{12}) \pm rS_{44}]\sigma'_{11} / 2\omega_0 \\ &= -2.675 \times 10^{-9} \sigma'_{11}\end{aligned}$$

(b) Solution in the sample axes system

The Raman tensors in the sample axes system obtained by a tensor rotation are given by [70]

$$R'_1 = \frac{1}{\sqrt{2}} \begin{pmatrix} 0 & 0 & d \\ 0 & 0 & d \\ d & d & 0 \end{pmatrix}, \quad R'_2 = \frac{1}{\sqrt{2}} \begin{pmatrix} 0 & 0 & d \\ 0 & 0 & -d \\ d & -d & 0 \end{pmatrix}, \quad \text{and} \quad R'_3 = \begin{pmatrix} 0 & d & 0 \\ d & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} \quad \text{Eq. 4-40}$$

The Raman tensors in Eq. 4-40 are the same as those in Eq. 4-38. Thus, their eigenvalues and eigenvectors are also the same as illustrated in Eqs. 4-35 and 4-36. For backscattering along the z' -axis, only the peak of R'_3 is visible. Therefore, the Raman shift-stress relationship is also equivalent to that in Eq. 4-39.

4.4.2 Line Force Model

To evaluate the stress involved in microelectronics applications, the shear stress and the stress in the z' direction cannot be neglected. For the sake of simplicity we assume that the stress can be explained with the edge force model of Hu [72]. The effect of the film on the substrate is described in terms of a line force (F). This force originates at the film edge and acts parallel to the surface of the film as shown in Figure 4-5.

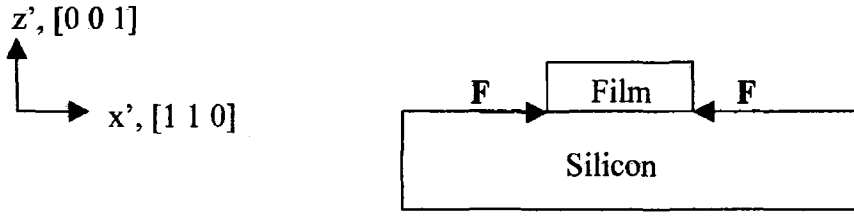


Figure 4-5 The direction coordinates of the sample along its cross section, where F is the force at the edge of the film [70].

The magnitude of the force is $|F| = \sigma_{\text{film}} d_{\text{film}}$, where d_{film} is the thickness of the film and σ_{film} is the stress in the film. For a line with a width w and the plane stress assumption, the stress in the substrate is given by [70]

$$\begin{aligned}\sigma'_{11} = \sigma'_{x'x'} &= -\frac{2F}{\pi} \left(\frac{x'^3}{(x'^2 + z'^2)^2} - \frac{(x'-w)^3}{[(x'-w)^2 + z'^2]^2} \right), \\ \sigma'_{33} = \sigma'_{z'z'} &= -\frac{2F}{\pi} z'^2 \left(\frac{x'}{(x'^2 + z'^2)^2} - \frac{(x'-w)}{[(x'-w)^2 + z'^2]^2} \right), \\ \sigma'_{13} = \tau'_{x'z'} &= -\frac{2F}{\pi} z' \left(\frac{x'^2}{(x'^2 + z'^2)^2} - \frac{(x'-w)^2}{[(x'-w)^2 + z'^2]^2} \right)\end{aligned}\quad \text{Eq. 4- 41}$$

The other components are zero.

(a) Solution in the reference system

The stress components from the edge force model systems are given by [73]

$$\begin{aligned}\sigma_{11} &= \frac{\sigma'_{11}}{2} + \frac{\sigma'_{22}}{2} - \sigma'_{12} = \frac{\sigma'_{11}}{2}, \\ \sigma_{22} &= \frac{\sigma'_{11}}{2} + \frac{\sigma'_{22}}{2} + \sigma'_{12} = \frac{\sigma'_{11}}{2}, \\ \sigma_{33} &= \sigma'_{33}, \\ \sigma_{12} &= \frac{\sigma'_{11}}{2} - \frac{\sigma'_{22}}{2} = \frac{\sigma'_{11}}{2}, \\ \sigma_{23} &= \frac{\sigma'_{23}}{\sqrt{2}} + \frac{\sigma'_{13}}{\sqrt{2}} = \frac{\sigma'_{13}}{\sqrt{2}}, \\ \sigma_{13} &= -\frac{\sigma'_{23}}{\sqrt{2}} + \frac{\sigma'_{13}}{\sqrt{2}} = \frac{\sigma'_{13}}{\sqrt{2}}\end{aligned}\quad \text{Eq. 4- 42}$$

Similar to the uniaxial model, the strain tensor elements in the reference system need to be calculated using Hooke's law resulting in [70]

$$\begin{aligned}
 \epsilon'_{11} &= \left(\frac{S_{11} + S_{12}}{2} + \frac{S_{44}}{4} \right) \sigma'_{11} + S_{12} \sigma'_{33}, \\
 \epsilon'_{22} &= \left(\frac{S_{11} + S_{12}}{2} - \frac{S_{44}}{4} \right) \sigma'_{11} + S_{12} \sigma'_{33}, \\
 \epsilon'_{33} &= S_{12} \sigma'_{11} + S_{11} \sigma'_{33}, \\
 \epsilon'_{12} &= \epsilon'_{23} = 0, \\
 \epsilon'_{13} &= \frac{S_{44}}{2} \sigma'_{13}
 \end{aligned}
 \tag{Eq. 4- 43}$$

Rotating to the crystal axes system gives

$$\begin{aligned}
 \epsilon_{11} &= \epsilon_{22} = \frac{\epsilon'_{11} + \epsilon'_{22}}{2}, \\
 \epsilon_{12} &= \frac{\epsilon'_{11} - \epsilon'_{22}}{2}, \\
 \epsilon_{33} &= \epsilon'_{33}, \\
 \epsilon_{13} &= \epsilon_{23} = \frac{1}{\sqrt{2}} \epsilon'_{13}
 \end{aligned}
 \tag{Eq. 4- 44}$$

and the secular equation (Eq. 4-26) can be written as [70]

$$\begin{vmatrix}
 p\epsilon_{11} + q(\epsilon_{11} + \epsilon_{33}) - \lambda & 2r\epsilon_{12} & 2r\epsilon_{13} \\
 2r\epsilon_{12} & p\epsilon_{22} + q(\epsilon_{33} + \epsilon_{11}) - \lambda & 2r\epsilon_{13} \\
 2r\epsilon_{13} & 2r\epsilon_{13} & p\epsilon_{33} + q(\epsilon_{11} + \epsilon_{22}) - \lambda
 \end{vmatrix} = 0
 \tag{Eq. 4- 45}$$

From Eq. 4-45, none of the elements of the secular matrix become zero. Therefore, three different eigenvalues and corresponding eigenvectors can be given. From the eigenvalues λ_1 , λ_2 and λ_3 , which are similar to the uniaxial stress in Eq. 4-35, the rotation must be made to be compatible with the sample axes system. Thus, the solution will be the same as in the sample system, which will be given in (b) below.

(b) Solution in the sample system

Using the strain components in Eq. 4-43, the eigenvalues and eigenvectors become

$$\begin{vmatrix} p'\varepsilon'_{11}+q'\varepsilon'_{22}+q\varepsilon'_{33}-\lambda & 0 & 2r\varepsilon'_{13} \\ 0 & p'\varepsilon'_{22}+q\varepsilon'_{33}+q'\varepsilon'_{11}-\lambda & 0 \\ 2r\varepsilon'_{13} & 0 & p\varepsilon'_{33}+q(\varepsilon'_{11}+\varepsilon'_{22})-\lambda \end{vmatrix} = 0$$

Eq. 4- 46

From Eq. 4-46, the eigenvalue of λ'_2 can be obtained from

$$q'\varepsilon'_{11}+p'\varepsilon'_{22}+q\varepsilon'_{33}-\lambda = 0 \quad \text{Eq. 4- 47}$$

Substituting Eq. 4-47 into Eq. 4-46, the eigenvalue can be written as [70]

$$\lambda'_2 = (p+q)[(S_{11}+S_{12})\frac{\sigma'_{11}}{2}+S_{12}\sigma'_{33}] + q(S_{12}\sigma'_{11}+S_{11}\sigma'_{33}) - \frac{r}{2}S_{44}\sigma'_{11} \quad \text{Eq. 4- 48}$$

The other two eigenvalues are then given by [70]

$$\begin{aligned} \lambda'_1 &= \frac{X+Y+\sqrt{(X-Y)^2+4Z^2}}{2}, \\ \lambda'_3 &= \frac{X+Y-\sqrt{(X-Y)^2+4Z^2}}{2} \end{aligned} \quad \text{Eq. 4- 49}$$

where $X = p'\varepsilon'_{11}+q'\varepsilon'_{22}+q\varepsilon'_{33}$, $Y = p\varepsilon'_{33}+q(\varepsilon'_{11}+\varepsilon'_{22})$, $Z = 2r\varepsilon'_{13}$

and the corresponding eigenvectors, $\nu'_{i_{st}}$, in the sample system are

$$\begin{aligned} \nu'_{1_{st}} &= \frac{1}{\sqrt{Q^2+1}}(Q, 0, 1), \\ \nu'_{2_{st}} &= (0, 1, 0), \\ \nu'_{3_{st}} &= \frac{1}{\sqrt{L^2+1}}(L, 0, 1), \end{aligned} \quad \text{Eq. 4- 50}$$

where $Q = \frac{X-Y+\sqrt{(X-Y)^2+4Z^2}}{2Z}$ and

$$L = \frac{X-Y-\sqrt{(X-Y)^2+4Z^2}}{2Z}$$

From Eq. 4-50 and Eq. 4-21, the Raman tensors in the presence of stress can be written as [70]

$$\begin{aligned}
 R'_{1_st} &= \frac{1}{\sqrt{Q^2+1}} \begin{pmatrix} d & 0 & Qd \\ 0 & -d & 0 \\ Qd & 0 & 0 \end{pmatrix}, \\
 R'_{2_st} &= \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & -d \\ 0 & -d & 0 \end{pmatrix}, \\
 R'_{3_st} &= \frac{1}{\sqrt{L^2+1}} \begin{pmatrix} d & 0 & Ld \\ 0 & -d & 0 \\ Ld & 0 & 0 \end{pmatrix}
 \end{aligned}
 \tag{Eq. 4- 51}$$

In case of absence stress, L becomes infinity and Q becomes zero. Thus, the R'_{i_st} represent the stress-free Raman tensors in the sample system as described in Eq. 4-40. There are two cases for the backscattering configuration, i.e. backscattering along the z' axis and along the y' axis, respectively. When the backscattering is along the z' axis and the polarizations of the incident light and scattered light are parallel to the width of the lines, i.e. $e_0 = (1 \ 1 \ 0)$ and $e_s = (\bar{1} \ \bar{1} \ 0)$, the intensities of the three modes which can be calculated using Eq. 4-20 are given by [70]

$$I'_1 = \frac{d^2}{Q^2+1}, \quad I'_2 = 0 \quad \text{and} \quad I'_3 = \frac{d^2}{L^2+1}
 \tag{Eq. 4- 52}$$

This implies that either I'_1 or I'_3 is visible depending on the Q and L values.

When the backscattering is along the y' axis and the polarizations of the incident light and scattered light are parallel to the z' axis, i.e. $e_0 = (0 \ 0 \ 1)$ and $e_s = (0 \ 0 \ \bar{1})$, $I'_1 = I'_3 = 0$. Only I'_2 can be observed.

4.5 Micro-Raman Spectroscopic Instrumentation

In the early stage of Raman spectroscopy, mercury arcs were used as light sources. In the 1960s, the light source was usually upgraded to a laser, which dramatically developed the performance of the Raman system [64] since the laser provides an intense monochromatic, highly collimated, highly polarised beam of light. It is noted that only the components, which are used in our micro-Raman spectroscopy, are mentioned. Generally, Raman and micro-Raman spectrometers consist of the light source, sample device, dispersion system and detector, which will be described later in this chapter. However, the most important factors for a micro-Raman system are:

- (a) Quality and focusing of the incident light on the sample,
- (b) The collection of the scattered light with a wide angle of collection and minimum aberration,
- (c) Optimised optical coupling of the observed microvolume of the sample to the detector via the spectrograph,
- (d) Efficient filter for stray light due to the diffuse reflection of the excitation radiation,
- (e) High resolution of the detector.

Fundamentally, the experimental set-up of a micro-Raman system is illustrated in Figure 4-6.

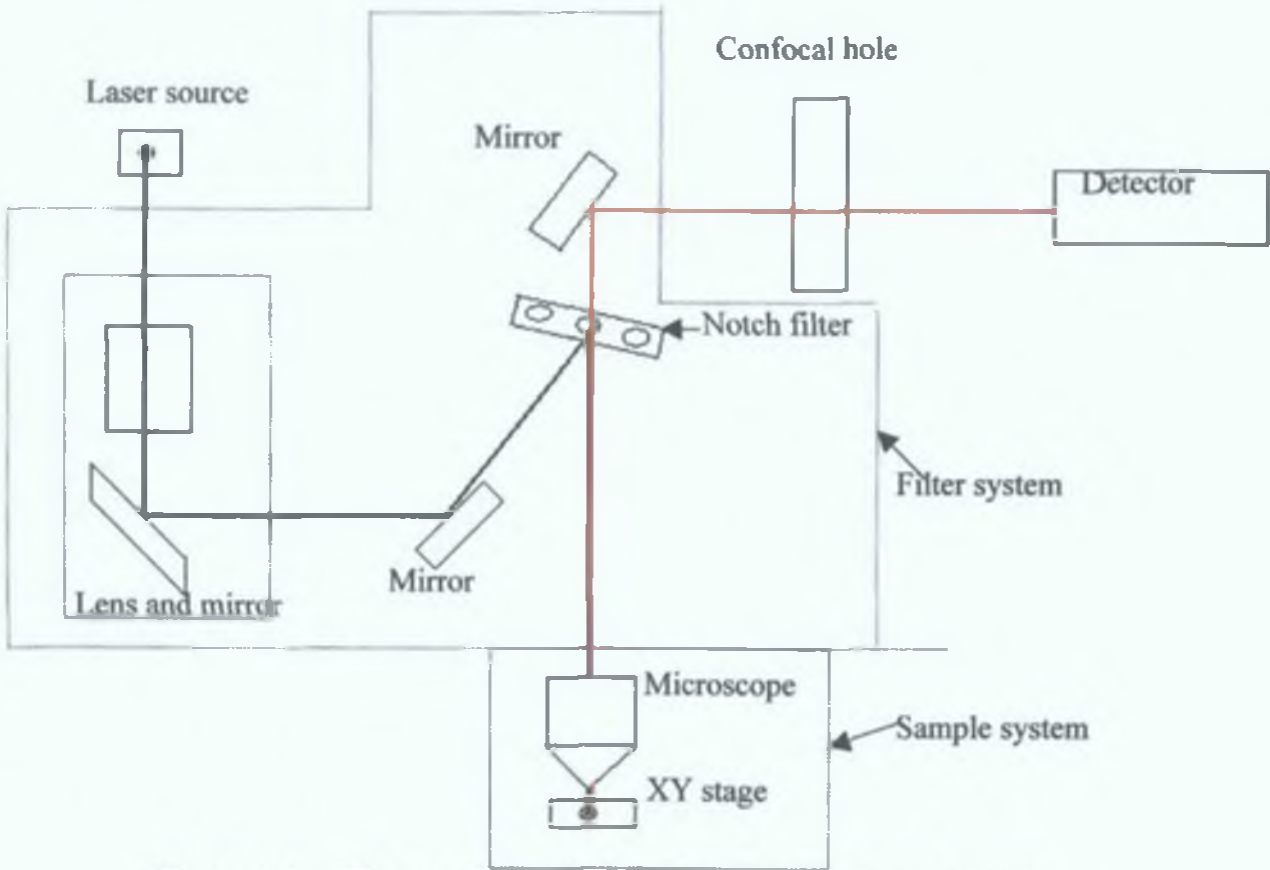


Figure 4-6 The experimental micro-Raman spectroscopy system.

4.5.1 Laser

Figure 4-7 represents an energy-level diagram for a set of atomic energy levels. If an atom is in an excited state 2 at some time, there is a finite probability per unit time, $N_2(t)$, that it will travel to state 1 and emit radiation with a photon energy $h\nu = E_2 - E_1$ where $\nu = \omega/2\pi$.

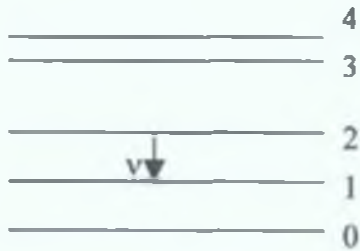


Figure 4-7 Diagram of energy levels for a generic atom [64].

Without the stimulus of external radiation, this process is called spontaneous emission [64], which can be modelled by the following equation

$$-\frac{dN_2(t)}{dt} = A_{21}N_2(t) \quad \text{Eq. 4- 53}$$

where A_{21} is the spontaneous transition rate.

This emission has a finite width and its line-shape function is denoted by $g(\nu)$. If the emission is considered to be a damped harmonic oscillator, $g(\nu)$ is defined by a normalised Lorentzian line-shape function. This line-shape function broadening is important for materials characterisation since it is individual for emitting atoms. For example, the imperfections of the crystal and the lattice environment can affect the emitted frequencies and thus contribute to the line broadening. However, atoms in a gas move with different velocities and the broadening of spectra lines is hence inhomogeneous. The line-shape due to this effect is Gaussian [64].

In this study, a gas laser is used as the excitation source for Raman spectroscopy. An example of a four-level energy diagram of a laser system is depicted in Figure 4-8 [64].

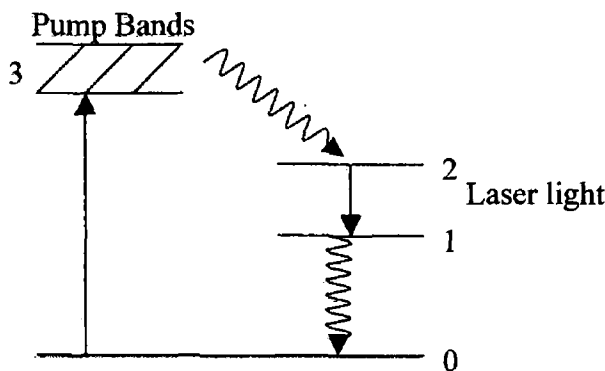


Figure 4-8 A diagram represents a four-level laser system. Level 3 is normally broad for a solid and sharp for a gas [64].

In general, atoms are excited into the pump level, which is level 3 in this schematic (Fig. 4-8). The atoms at this pump level is usually populated via collisions with electrons in an electric discharge. Atoms raised into the upper state of the pump level may be excited to higher level or decay directly to the ground state or decay to level 2. The transition of atoms from level 2 to level 1 creates the laser light.

For the Argon-ion (Ar^+) laser, it produces an intense laser output from the blue (488.0 nm) to the green (514.5 nm). This laser is commonly used in a study of light scattering. The energy levels associated with the operation of this system is illustrated in Figure 4-9 [64].

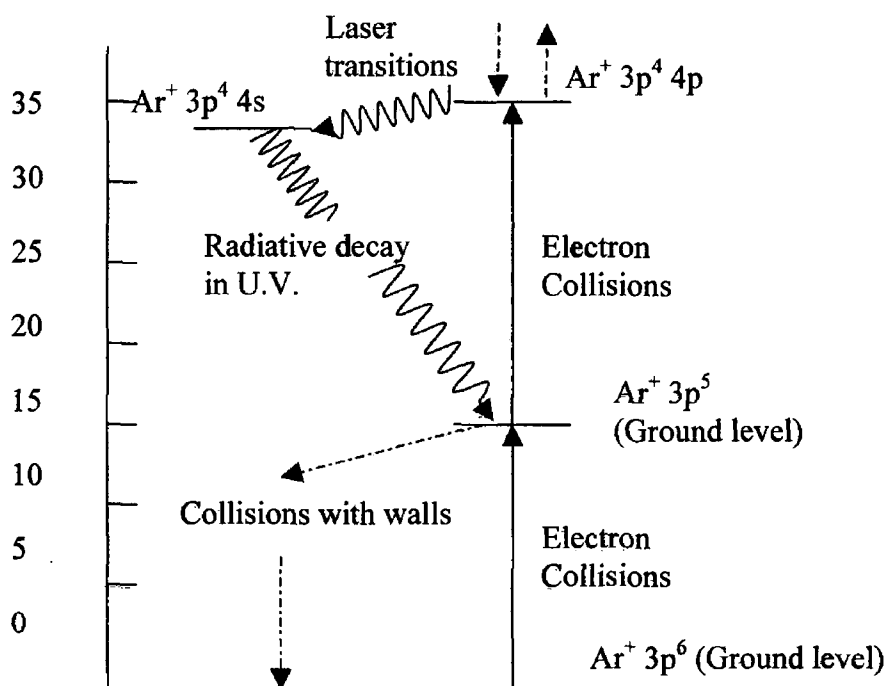


Figure 4-9 Configurations related to laser action in the Ar^+ laser [64].

Table 4-2 indicates some of the transitions and relative intensities of the Ar^+ laser.

Table 4- 2 Examples of transitions and relative intensities for the Ar+ laser lines [64].

Wavelength (nm)	Transition	Relative Intensity
488.0	$4p^2d^0_{5/2} \leftrightarrow 4s^2p_{3/2}$	Strong
496.5	$4p^2d^0_{3/2} \leftrightarrow 4s^2p_{1/2}$	Moderate
514.5	$4p^4d^0_{5/2} \leftrightarrow 4s^2p_{3/2}$	Strong

4.5.2 Sample System

When a laser beam is focused on the sample by an objective with a high numerical aperture, the diameter of the focal region is determined by the diffraction limit and the wavelength of the laser source. Typical micro-Raman spectrometers use single and wide-aperture objective in the 180° or backscattering geometry. In this case, a beamsplitter is necessary to illuminate the sample with the laser beam coaxially, through the objective, and to transmit the backscattered radiation toward the spectrograph. The sample system is illustrated in Figure 4-10.

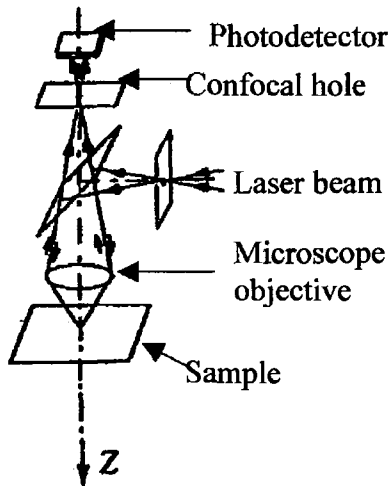


Figure 4-10 The sample system in micro-Raman spectroscopy [62]

Using the microscope objective, the nature of the cone of focused light is determined by the numerical aperture (N.A.), which is given as [62]

$$N.A. = n \sin \theta$$

Eq. 4- 54

where n is the refractive index of the medium between the sample and the lens and θ is the semi-angle of the cone for an axial objective point. Using typical commercial objectives, maximum semi-angles of approx. 72° are achievable yielding a N.A. ≈ 95 in air [62].

4.5.3 Confocal Hole

The objective of the confocal hole is to improve the contrast and the spatial resolution when the point source is focused into the sample. Basically, the confocal configuration is installed in the micro-Raman system both before and after the sample system as shown in Figure 4-11.

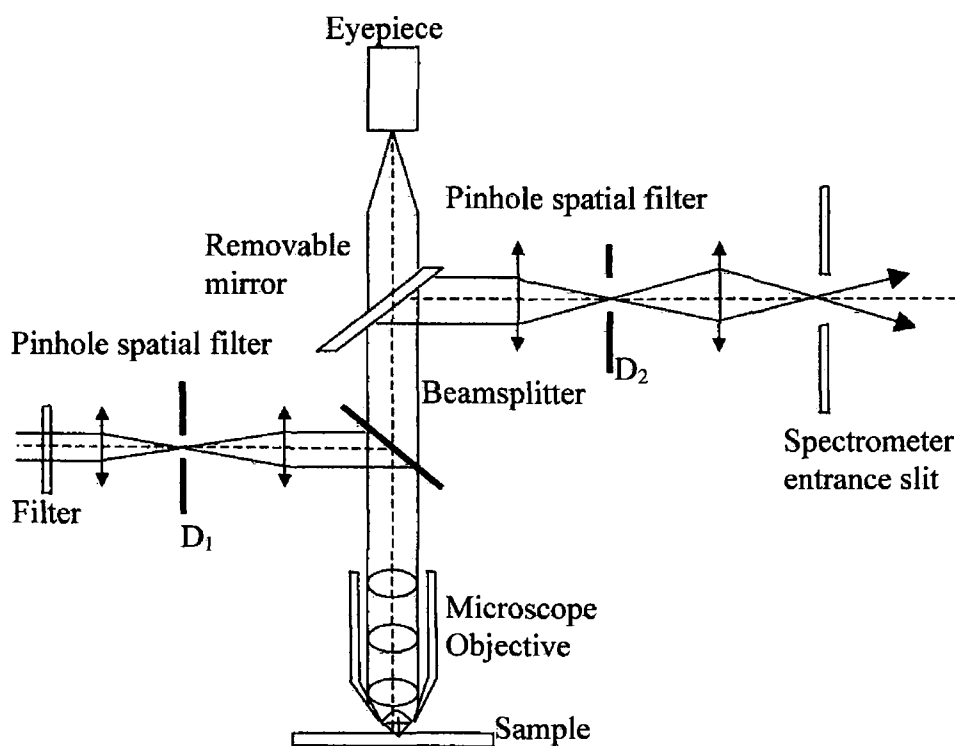


Figure 4-11 Basic diagram of the micro-Raman spectrometer equipped with the confocal diaphragms [62].

Figure 4-11 is a diagram of a commercial micro-Raman spectrometer [62]. Firstly, the laser beam is filtered by a confocal hole D_1 to remove diffraction and speckle noise. Subsequently, the focused and clean source is passed through the sample. The scattered Raman radiation is collected by a wide-aperture objective and focused on a confocal hole D_2 . The focused source and the scattered Raman beam can employ the same sample objective in the backscattering geometry by using the beamsplitter. The confocal hole D_2 is used to get rid of any radiation which does not come from the sample region. Finally, the scattered Raman radiation from the measured region is transmitted to the spectrograph and detector. The spatial filters for both incident and scattered beams are used to eliminate stray light from the out-of-focus regions of the sample. These spatial filters are very useful for the scattered beam in order to attenuate the Rayleigh radiation, which is approx. 10^9 more intense than the weak Raman scattered light.

4.5.4 Filtering system

Several pre-filters are used in commercial micro-Raman systems. These include holographic notch filters, dielectric edge filters and multi-stage spectrometers [67].

- **Holographic Notch Filter**

This notch filter eliminates a narrow band of light, whereas the light outside of the band eradication region can pass through the filter. This kind of filter is created by exposing a photosensitive material to interfering laser beams, which generates a periodic modulation in the refractive index. This modulation can diffract the Rayleigh scattering light, e.g. the laser wavelength λ_0 , away and transmit the adjacent wavelength [67]. The ideal notch filter is illustrated in Figure 4-12 [68].

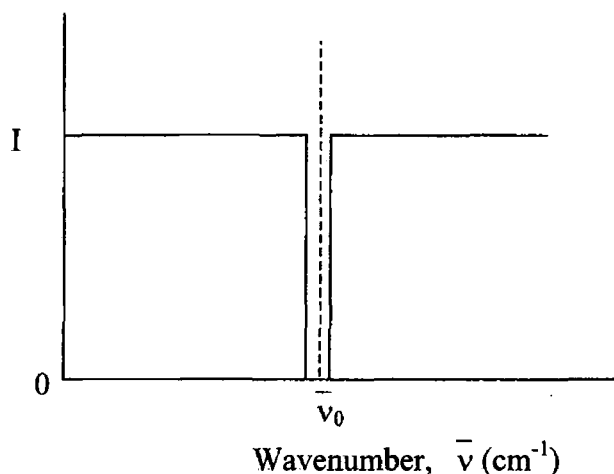


Figure 4-12 The spectral response of an ideal notch filter [68].

- **Pre-monochromator Rayleigh Rejection**

The pre-monochromator is widely employed as an optical pre-filtering system in Raman systems. Usually, a set of monochromators is composed of one grating and two mirrors. A disadvantage of this filter is the low light throughput, i.e. only 30-50% light throughput for a single monochromator [62].

4.5.5 Spectrometer or Spectrograph

The scattered light collected by the objective of a micro-Raman spectrometer is analysed by the spectrometric system. The detected light intensity as a function of the wavenumber is recorded as a spectrum. There are two kinds of spectrographs: dispersive and non-dispersive systems.

For the non-dispersive system, the scattered light is separated into its component frequencies before passing through the spatial filters. An interferometer is an example of this kind of spectrograph [68].

The dispersive system is comprised of a series of monochromatic images. This spectrograph, which scans the grating angle to pass different wavelength regions across a slit, uses a single channel detector. For a high precision Raman system, multi-channel detectors can be employed [67]. The scattered light is dispersed as a function of wavenumber. The results are then displayed in form of a real image of the spectrum [68].

4.5.6 Photoelectric Detectors

A photoelectric detector is utilised for many commercial micro-Raman systems. The photoelectric detector is divided into two types: single- and multi-channel detectors.

- **Single-channel detectors**

Examples of single-channel detectors are photomultiplier tubes (PMTs) and solid-state detectors (semiconductor photodiodes).

In the early stages, photomultiplier tubes were used as micro-Raman detectors. This detector is advantageous for very-low-frequency spectral regions. However, the signal from the scattered light gets weaker with a decrease in the measured size of the sample. In order to obtain a reasonable signal-to-noise ratio for the PMTs, a long exposure must be performed during measurement, which can result in thermal damage or photodegradation [68].

Lately, solid-state detectors such as silicon photodiodes, and germanium and InGaAs photodiodes have been used in a micro-Raman systems. Silicon photodiodes are good for the red and far-red regions. Liquid-nitrogen-cooled germanium and room temperature InGaAs photodiodes are the best near-IR region detectors for a conventional scanning Raman scattering. However, they are very sensitive to cosmic radiation. Hence, the system requires additional filtering [68].

- **Multi-channel detectors**

In recent years, low-noise, multi-channel solid-state detectors have been commonly used as detectors for high-precision micro-Raman system. Three classes of multi-channel solid-state detectors are commonly with Raman systems, i.e. charge-coupled devices (Si, CCD), charge-injection devices (Si CID), and self-scanned, photodiode arrays [68]. Many details of the detectors are outlined in ref. 8.

CHAPTER 5 SOLDER BUMP REFLOW PROCESS

INDUCED STRESS DISTRIBUTION IN SILICON SUBSTRATES

As microelectronic device features become smaller and smaller with an increase in functionality and higher levels of performance, the intricacy of semiconductor packaging technology grows proportionally. The idea of attaching the semiconductor die directly to the substrate (Print Circuit Board, PCB) by introducing flip-chip technology, which simply turns the chip upside down so that its termination can be connected directly to the metal pads on the substrate [1], has been in existence for some time. With this technique the integrated circuit (IC) package is omitted, saving cost, space and weight. The concepts were advanced by IBM [2] and AT&T more than 30 years ago as they developed flip-chip and beam leaded die, respectively. Since then the technology has evolved [3] to encompass a wide variety of materials and techniques for bumping, bonding and underfilling. Originally, it was used in mainframe computers, military and specialist applications, but more recently in mobile phones, smart cards, disc drives and automotive electronics. However, there are a number of issues that prevent FCOB (Flip-chip On Board) technology from becoming prevalent. Firstly, there is a limited availability of tested die with bump terminations (Known Good Die). Additionally, fine-line PCB substrates known as Known Good Board (KGB) [4] and placement/bonding machinery are expensive. These factors, coupled with the deficiency of standardisation (i.e. commitment to a fixed bump pattern footprint and matching substrates) have prevented this technology from expanding. None the less, the packaged IC has a number of advantages, such as IC protection, ease of test, standard footprints and pin-outs, ease of handling, an infrastructure with equipment suited to their assembly, ease of repair and re-work and the ability to compensate for mismatches in coefficients of thermal expansion of the different materials used [1].

However, the advantages offered by flip-chip technology are such that industry is pushed to further develop and refine this technique. The increasing demands for cheaper, smaller, and higher performance of electronic products have made flip-chip

a package of choice. The difference between flip-chip and other direct chip attach techniques, such as wire bonded chip on board, is that flip-chip packages offer an option to move from peripheral terminations to area array terminations. As a result, the number of input/output (I/O) counts increase significantly for the same die area. It is estimated that 40% of the semiconductor industry costs are in packaging and a substantial cost saving can be achieved by switching to an unpackaged die [6]. The small footprint of the die enables manufacturers to place more devices per unit area and the consequent shorter electrical paths reduce parasitic capacitance, cross talk, and inductance, yielding excellent electrical properties and GigaHertz [79] operation frequencies. When the device performance exceeds the 200 MHz range, wire-bonded assemblies, suffer from signal degradation because of cross talk between adjacent wires.

The flip-chip process is compatible with Surface Mount Technology (SMT) and the alignment of die bumps with the corresponding pads on the boards is not so critical (if the pitch size is not too small) due to the self-aligning nature of the solder bumps during the reflow step [7]. Furthermore, flip-chip technology can integrate with SMT technology to produce novel packages i.e. Flip-chip Ball Grid Array (FBGA), Flip-chip Pin Grid Array (FPGA), Flip-chip Chip Scale Packaging (FCSP), etc, which are example of packages used in advanced microprocessors [8].

As flip-chip awareness increases and the support infrastructure comes to maturity, the undoubted size, weight and performance benefits of the “ultimate packageless package” could well make this a dominant technology [1].

Worldwide-consolidated efforts between academia and industry are directed towards overcoming the difficulties associated with the FCOB technology. Issues arise from the mismatch of the Coefficient of Thermal Expansion (CTE) between silicon die, solder bump materials and the PCB.

The use of lead containing solder also triggers environmental concerns that need to be addressed by the manufacturing companies. Legislation to ban lead has also

become a key driver in lead-free soldering. To overcome this problem lead-free materials and polymer adhesives are being examined to replace the use of lead [9].

Many scientists [10] have addressed a number of flip-chip processing issues, though mainly in terms of mechanical integrity such as modelling of joint fatigue failure and underfill delamination [11]. However, the issue of mechanical reliability at wafer level is one of the major concerns for chip manufacturers, which can further affect the electrical performance of flip-chip devices and the production reliability, and these have not been addressed so far.

5.1 Flip-chip Technology

Flip-chip technology is not a novel technology; however it is complex as it involves many process steps and various materials. This section describes the materials and techniques used in flip-chip technology at the wafer level.

5.1.1 Under Bump Metallisation (UBM)

Under Bump Metallisation (UBM), also known as Ball Limited Metallurgy (BLM), is used as an adhesion and barrier layer. It comprises of a series of metal layers to provide adhesion to the Al-alloy bond pads and to prevent an inter-diffusion between the bump metal and Al-alloy bond pads. UBM covers Al-alloy bond pads to avoid corrosion and improve reliability of the flip-chip assembly in both mechanical and electrical integrities [85]. The formation of UBM is necessary before carrying out the solder bumping process.

There are two main processes to form UBM. The first one is an electroplating process and the other one is electroless plating. Both processes are used widely to form the under bump metallisation but electroless plating has an inherent advantage over electroplating in terms of processing cost.

5.1.1.1 *Electroplating UBM*

This process involves a large amount of equipment and materials; therefore, the processing cost is higher than electroless plating. The process begins with wafer cleaning by sputter etching before the deposition of the adhesion/barrier layer and plating base [86]. A layer of metal or metal alloy such as TiW, Cr and Ti is sputtered onto the wafer to form an adhesion/barrier metal layer, followed by another layer of metals (i.e. Ni, Cu and Au) as a plating base. Subsequently, positive photoresist (20-30 μm) is deposited onto the wafer and the plating mask is printed on the photoresist. The photoresist is exposed to form a plating area. A final metal layer (Cu or Ni) is deposited onto the plating area by an electroplating process in an acidic bath [86]. Finally, the remaining photoresist is removed and the plating based metal is etched away. The electroplating (TiW/Au) process is shown in figure 5-1.

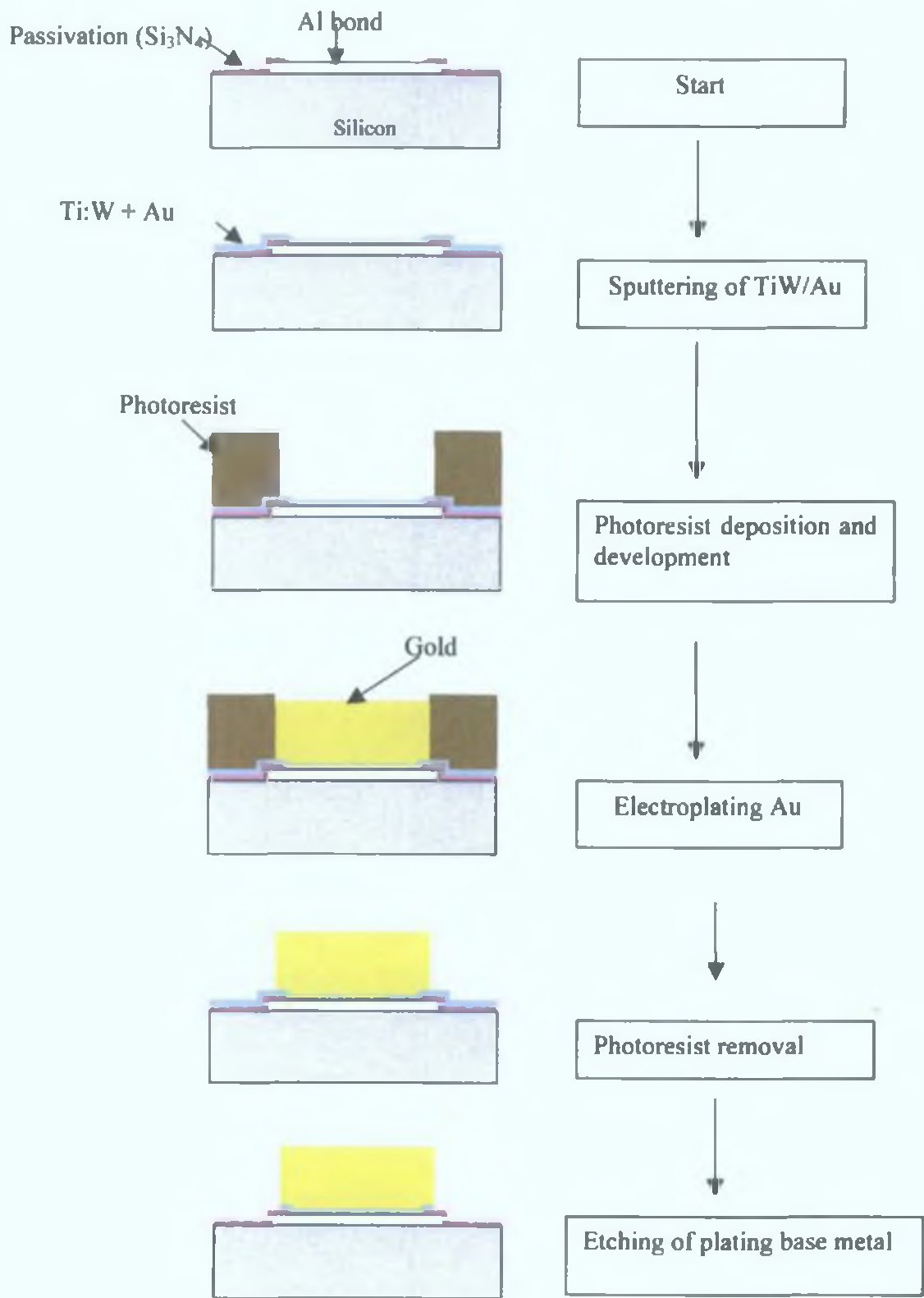


Figure 5-1 Schematic process flow for electroplated gold bumps [86].

5.1.1.2 Electroless UBM

Among the UBM bumping technologies, electroless deposition of Ni bumps is one of the most interesting methods. This is because it possesses several advantages, such as high throughput via parallel processing of wafer batches. It is an economical process with very low investment cost because it is a maskless process and does not require any seed metals, or plating base metals. With this process, the need for traditional high vacuum thin film processing, and the cost of the equipment, and the set-up associated with photolithography and etching can be eliminated. The number of metals, which can be deposited via an electroless plating solution, is limited compared to the electroplating process. Metals such as Copper (Cu), Palladium (Pd), Nickel (Ni), and Silver (Ag) can be used in this process. The most established and most popular process is electroless Nickel/Gold (Ni/Au)[87]. Ni is deposited first onto Al-alloy bond pads and then a thin layer of Gold (Au) is deposited on top to inhibit oxidation. The structure of electroless Ni/Au on Al-alloy bond pads is depicted in Figure 5-2. Ni bumps have proven to be an excellent surface for all types of solder

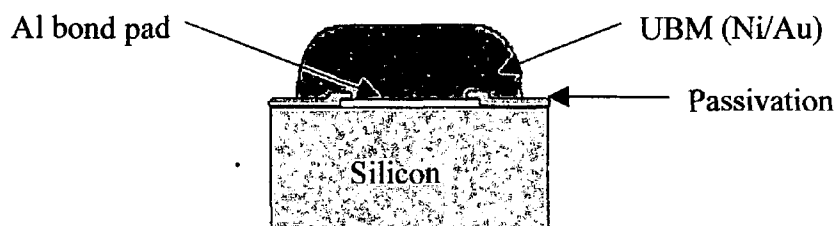


Figure 5-2 Cross section of electroless Ni/Au on Al bond pads.

The electroless Ni/Au bumping can be achieved using standard chemicals available on the market for a simple test structure [90]. Nevertheless, for a sophisticated test structure, the process requires a very precise chemical composition to obtain a good result.

5.1.2 UBM design guidelines

The following are the requirements when using electroless Ni/Au as an Under Bump Metallisation [88]:

- The under bump height must not be larger than half of the pad spacing to prevent short circuits between adjacent pads by overgrowing Ni. Basically, to make it suitable for the solder bumping process, the under bump height should be about 5 μm [88].
- The thickness of Al-alloy bond pads must be at least 1-2 μm in order to have an adequate Al thickness after the cleaning and activation process.
- The passivation layer must not have any defects.
- The spacing between aluminium pads has to be more than 20 μm to avoid short circuits due to overgrowing Ni.
- The UBM must be maintained within the metal bond pads to control stress concentration.
- The UBM must overlap the passivation layer by approximately 10 μm to protect the Al bond pads from corrosion. A schematic of this design is illustrated in Figure 5-3.

It is crucial to follow the design guidelines in order to achieve reliable flip-chip structures.

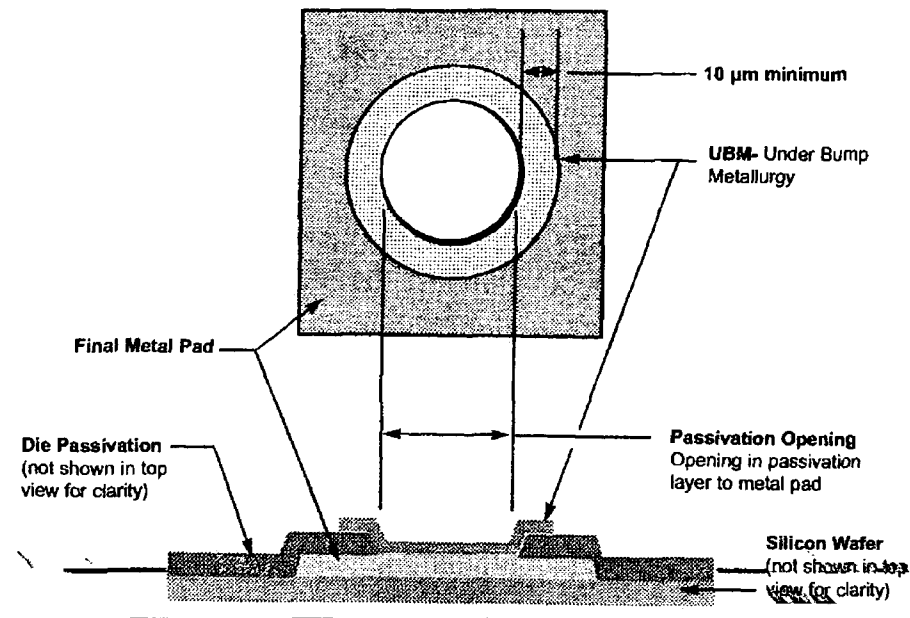


Figure 5-3 Bond pad design and UBM dimension requirement [89].

5.1.3 Solder Bumps

In flip-chip assembly, several interconnect materials such as solder, gold, conductive polymer and anisotropic epoxies are employed. The range of bump materials depends on the required application. For example, in applications that require relatively large heat dissipation, the bump material should be gold. However, the most widely used bump material is solder, as the solder alloys are economical and the bumping process is well established.

The solder bump in flip-chip assemblies provides three main functions [86]:

1. It serves as an electrical connection between the silicon die and the PCB substrate.
2. To some extent, it serves as a path for heat dissipation.
3. It supports the mechanical link between die and substrate.

The mechanical reliability of the solder joint affects substantially the performance of the flip-chip assembly. Solder joint failure can lead to the device open circuit. A required bump height and volume must be achieved to ensure the robustness of the

bump. Before performing solder bumping, Al-alloy bond pads on the silicon die must be treated with a deposited thin layer of Under Bump Metallisation (UBM) because of the unwettability between aluminium pads and solder alloy. The selection of solder composition for solder bumps must take into consideration the melting point of the solder, the bumping process capability, and, most vitally, reliability. The melting temperature of solder alloy determines the maximum reflow profile temperature. Normally, the solder alloy for flip-chip applications is lead-based alloy. The most popular lead-based alloys are lead-tin (Pb/Sn) alloy- either 97%Pb/3%Sn (97PbSn) or 37%Pb/63%Sn (37PbSn). However, in a few years time, the use of lead-based alloy will be prohibited due to environmental considerations and new legislation. Lead-free alloys, therefore, have been developed in recent years. These alloys are based on Indium (In), Tin (Sn), Silver (Ag), and Copper (Cu)[86].

5.1.4 Bumping process

Several bumping technologies are used in industry:

- Evaporation
- Electroplating
- Wire bumping
- Screen printing.

5.1.4.1 Evaporation process

This method provides good uniformity of the solder bumps but it is an expensive process in terms of capital expenditure (materials and equipment) [90]. High lead solder alloy (97PbSn and 95PbSn) is the most commonly used material in the evaporation process (e.g., in the IBM C4 process). The deposition takes place when the solder is evaporated onto the bond pads via the mask opening. The bump size and pitch are dictated by the mask technology.

A process step consisting of an evaporated UBM and solder bump is depicted in Figure 5-4 [90]. From Fig. 5-4, step a is called the *in-situ* sputter clean. This is to

remove oxides or photoresist before the metallization step. In addition, the surface roughness of the passivation is enhanced for better UBM adhesion. In step **b**, the UBM and bump are transferred to the wafer via the evaporation process. The high lead solder, typically 97Pb/Sn or 95Pb/Sn is deposited on top of the UBM as shown in step **c**. The deposit is usually a 100-125 μm high bump where the precise dimensions are determined by the volume of the solder materials. After step **c**, the process can be divided into 2 options, called E3 and C4. Because of the high temperature reflow process associated with this kind of solder material; the solder bump cannot stick well to an organic board. Motorola invented a process, called E3 or “evaporated, extended eutectic”, in which a tin cap is deposited on top of the solder bump, as illustrated in step **e**. Normally, a high lead content for the solder bump is used, which needs a high temperature in the reflow step. However, the organic substrate cannot endure temperatures above 300 °C. This tin cap allows the assembler to heat the structure well below the solder melting point. Thus, after step **e**, the device can be attached to organic boards without using the intermediated eutectic, which has to be added on the board itself. In step **d** (C4 process), the solder bump can be formed as a sphere using the reflow process.

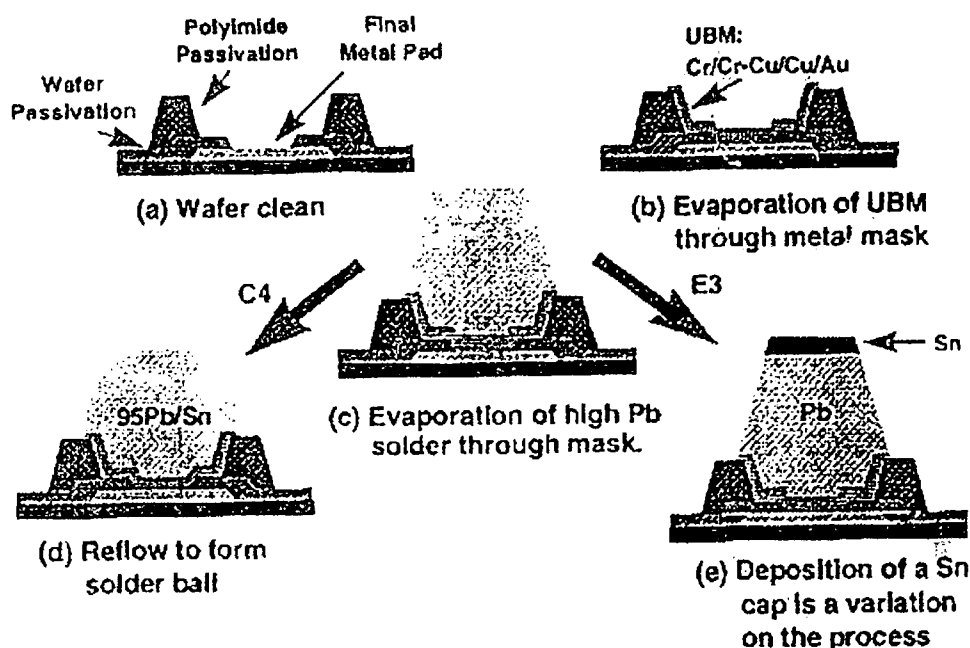


Figure 5-4 Evaporating solder bumping process [90].

5.1.4.2 *Electroplating process*

This process will be described in detail as it was used in the Intel flip-chip samples, which were used in this study. Electroplating is an alternative to the evaporation process, and is considered a cost effective solution for solder bumping process. The process is a modification of the evaporation process and the materials must be compatible with the plating process; in fact, both processes use similar materials such as high lead solder materials [90]. The process involves the deposition of blanket metallisation and photoresist. The photoresist is patterned and developed, so the bump areas are exposed and then subjected to electroplating, which occurs only at exposed areas. The photoresist process determines the bump geometry as well as the pitch size, while the bump height is controlled by the time for which the current is applied. The electroplating solder bumping step is portrayed in Figure 5-5.

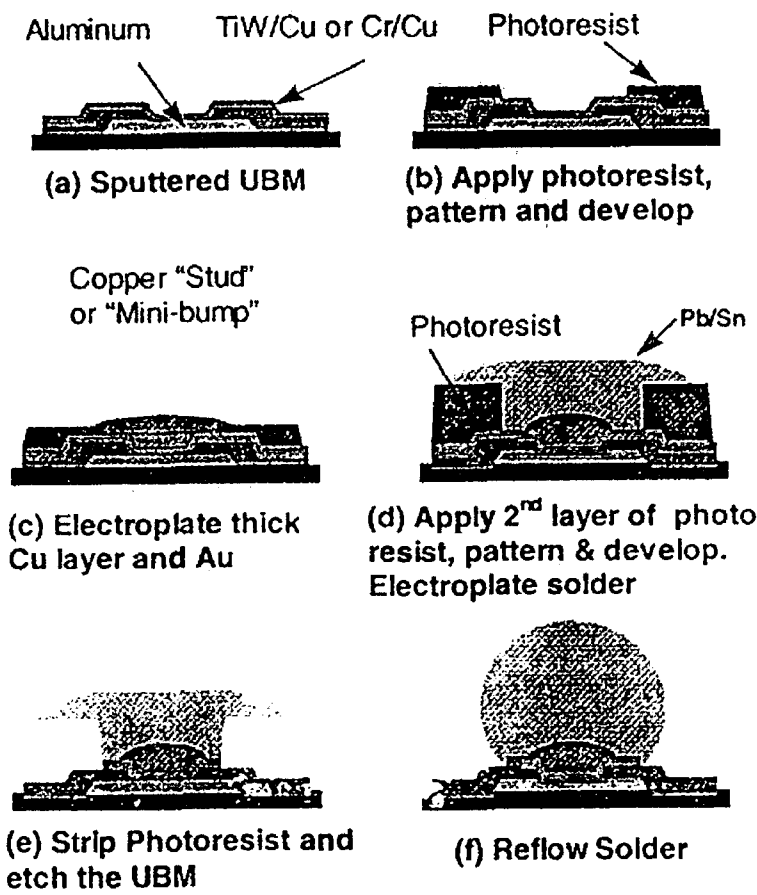


Figure 5-5 Electroplating UBM and solder bumping process [90].

5.1.4.3 Wire bumping process

Solder wire bumping is usually used in low volume applications. A thermosonic bonder is used to attach solder wire bumps directly on Al-alloy bond pads. Hence, a UBM deposition is not necessary. The bump and pitch sizes of the bump are restricted by the wire diameter and alignment capability.

5.1.4.4 Screen printing process

Screen printing or stencil printing is the most cost effective method in solder bumping technologies. Furthermore, the solder bumps formed by this process are very reliable.

This technique is a well-known process as it has been used in Surface Mount (SMT) assembly for quite a long time. In SMT assembly, a solder paste is printed onto a PCB substrate, and the bond pads are located under these solder paste pads. On average, the pitch size on the PCB is more than 400 μm , while the pitch requirement on the wafer is normally less than a 300 μm [91]. This implies a serious challenge for the screen printing process. To enable this technique to print solder paste on the wafer with less than 300 μm pitch, solder paste materials, stencil design, and printing equipment were further developed. Figure 5-6 illustrates the process whereby a solder paste is printed onto a silicon die. The solder paste will transform to solder balls after the solder reflow process (Figure 5-7).

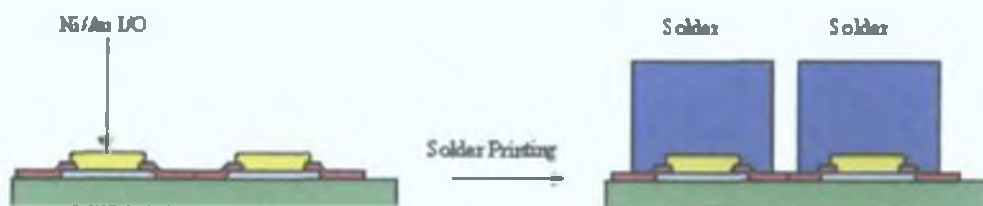


Figure 5-6 Solder paste printed onto silicon die.

The deposition of a sufficient amount of solder paste without solder bridging, missing bumps and mis-alignment must be accomplished in this process.

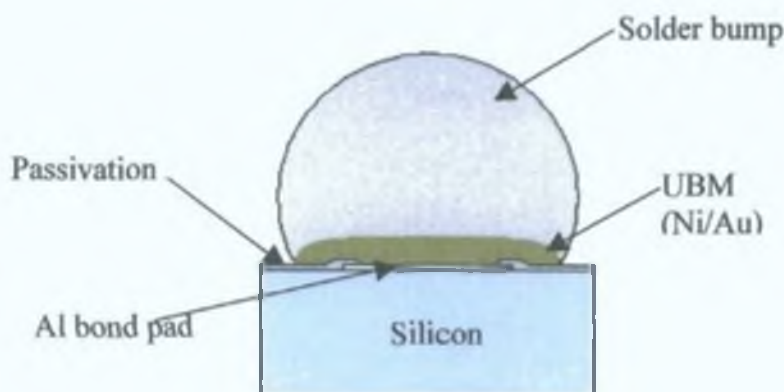


Figure 5-7 Cross section of solder bump after solder reflow process.

5.2 Solder bump Ball Grid Array (BGA) applications for Intel®Pentium®III

The BGA flip-chip technique is used on the Intel®Pentium®III ICs examined in this study. The UBM and solder bump are deposited using a C4 electroplating process. Ti and NiV (2-5 % V content) were used as the UBM layer. In addition, a 97PbSn solder material is employed in this sample. The reflow process is performed at 350 °C in nitrogen atmosphere to prevent oxidation.

5.3 Experimental Details

SXRT and MRS were performed to visualise the residual stress/strain distribution in the silicon substrate, which was induced by the reflow process. The order of magnitude of stresses can be predicted and compared using the FEM method.

5.3.1 Samples

Lead/tin (Pb/Sn) solder bump samples have been provided by Intel Ireland Ltd., Leixlip, Co.Kildare, Dublin, Ireland. The samples consist mainly of silicon substrate

(200 mm diameter and $\sim 700\ \mu\text{m}$ thickness)/ Silicon epilayer/ Aluminium (Al) metal 5/ Nitride passivation/ Polyimide passivation/ Barrier Layer Metal (BLM) which composes of Titanium (Ti) and Nickel/Vanadium (NiV). The Pb/Sn solder bumps were deposited on the BLM layers using an electroplating process or C4 process. The geometry and dimensions are illustrated in Figure 5-8.

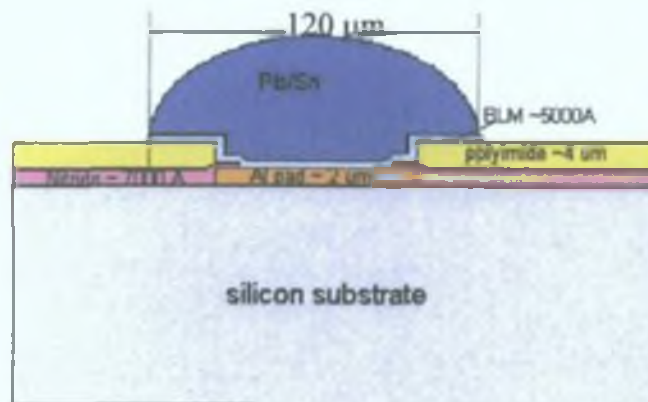


Figure 5-8 Geometry and dimensions of Pb/Sn solder bump sample.

Subsequently, the BLM layers were removed by a C4 etching process. The samples were investigated as *Pre-reflowed* process samples. Afterwards, the samples were reflowed by a reflow process simulation at 350°C in atmosphere and observed as *post-reflow* process samples.

The Pb/Sn samples have been divided into three main categories as follows:

- (d) To study the stress distribution in the silicon substrate due to C4 metal etching times, four different samples which were etched for 10, 15, 25 and 35 minutes as sample wafer numbers 511, 509, 424 and 445, respectively, were prepared by Intel Ireland. This sample category was observed using SXRT only.
- (e) To study the stress distribution in the silicon substrate due to the reflow process, the *Pre-reflow* process samples from (a) were examined, and subsequently were reflowed using a simulated process at 350°C in atmosphere and are thus defined to be *post-reflowed* process samples.

- (f) To study the major source of strain distribution in the silicon substrate, the Pb/Sn bumps on both the *Pre*- and *post*-reflowed process samples were removed and investigated using SXRT and MRS.

5.3.2 Experimental Details of Synchrotron X-Ray Topography

The measurements were performed at HASYLAB-DESY, Hamburg, Germany (Hamburger Synchrotronstrahlungslabor am Deutschen Elektronen-Synchrotron), utilising the continuous spectrum of synchrotron radiation from the DORIS III storage ring bending magnet. The ring operated at a positron energy of 4.45 GeV and at typical currents of 80-150 mA. The aforementioned Bragg or Laue pattern of topographs was recorded on Geola VRP-M films having an emulsion grain size of about 0.05 μm and emulsion thickness of ca. 6-7 μm . The distance from the sample to the film was 50 mm for all samples. The beam size was set to 3 mm x 3 mm for the group (a) experiments and to 1.5 mm x 1.5 mm for the others. The films were developed by immersing in developer for 5 minutes, 2-3 seconds in a stop bath, then fixer for 10 minutes, a 30 minutes water wash and finally drying in a heater for at least 30 minutes. The developer is Kodak D-19 developer, the stop bath is a 2% acetic acid in H_2O solution. The fixer is Kodak No.1 sodium fixer. The topographs have been generated on a system comprising of a microscope with a CCD camera, frame-grabber and appropriate software. Some of the images have been processed using a software package called Visilog[®], in order to improve clarity. The topographs were taken at magnifications of 50X for BRT and 100X for BRST images.

Due to the high absorption of the Pb/Sn bumps, the strain distribution underneath the Pb/Sn bumps could not be detected from the topside of the wafer samples. Therefore, the measurements were performed by permitting the x-ray beam to enter via the backside of the samples. However, the silicon substrate was too thick to access the information underneath the Pb/Sn bumps because the maximum x-ray

energy penetration for, e.g. a $\bar{3}\bar{3}9$ reflection, was only 125 μm (penetration depth, t_p) as shown in Figure 5-9.

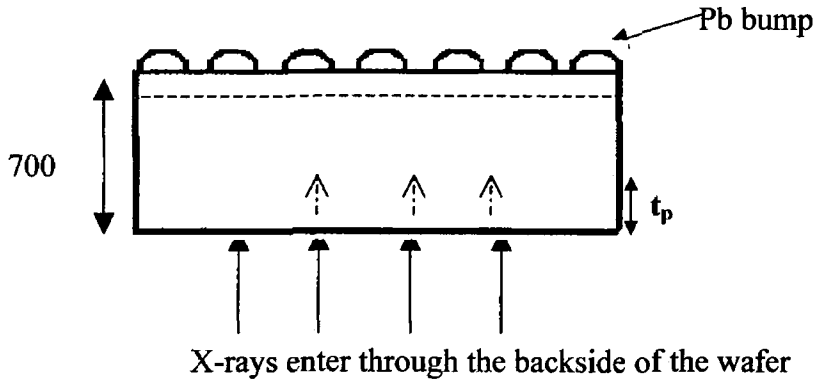


Figure 5-9 An overview of the x-ray topography set-up for the BGA samples.

Hence, the silicon substrate was thinned down to less than 125 μm , excluding the samples from the group (c) category. Since there were no Pb/Sn solder bumps, the measurement of samples without Pb/Sn bumps could be done by entering the x-rays via the topside of wafer. Mechanical polishing was used to decrease the thickness of the Si wafers.

5.3.3 Experimental Details of Finite Element Analysis

Two-dimensional (2-D) plane strain finite element models have been employed in these experiments. The approximate geometry, dimensions and boundary conditions of the *post*-reflowed samples are illustrated in Figure 5-10. The differences between *Pre*- and *post*- reflowed process samples include the geometry of the Pb/Sn bump and the intermetallic materials.

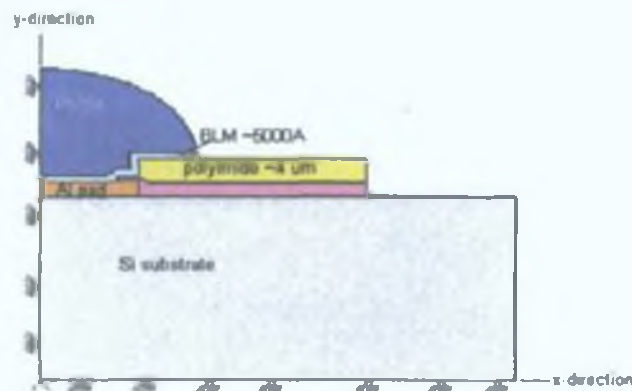


Figure 5-10 Geometry and boundary conditions for the *post-reflowed* sample model.

About 100,000 nodes were used to achieve the simulation. The finite element analyses were carried out using Quickfield® Professional version 4.2 [122]. Eight different materials were considered in these models: Si substrate, Al pad, polyimide passivation, silicon nitride passivation, Ti, NiV, intermetallic layer (Ni_3Sn_4), Pb/Sn solder bump. These materials are assumed to be isotropic and linearly elastic. Their properties are given in Table 5-1.

Table 5-1 Material properties for finite element analysis.

Materials	Young's modulus ($E \times 10^9$) N/m ²	Poisson's ratio (ν)	Coefficient of thermal expansion (α , $\times 10^{-6}$) /°C
Si	112.4	0.28	2.5
Al pad	68.2	0.33	24.0
Polyimide	2.5	0.41	61.3
Silicon nitride	310.0	0.23	3.0
Ti	116.0	0.34	8.9
NiV	204.6	0.312	13.0
Ni ₃ Sn ₄	112.4	0.321	19.2
Pb/Sn solder	18.3	0.30	28.8

Note: The properties of NiV, Ni₃Sn₄ were extrapolated from their pure constituent elements [120]-[121].

5.3.4 Micro-Raman Spectroscopic Experimental Details

A Jobin Yvon LabRam HR micro-Raman spectroscopy system using a 488 nm Ar⁺ laser was used in this study. The system set-up is shown in Figure 5-11.

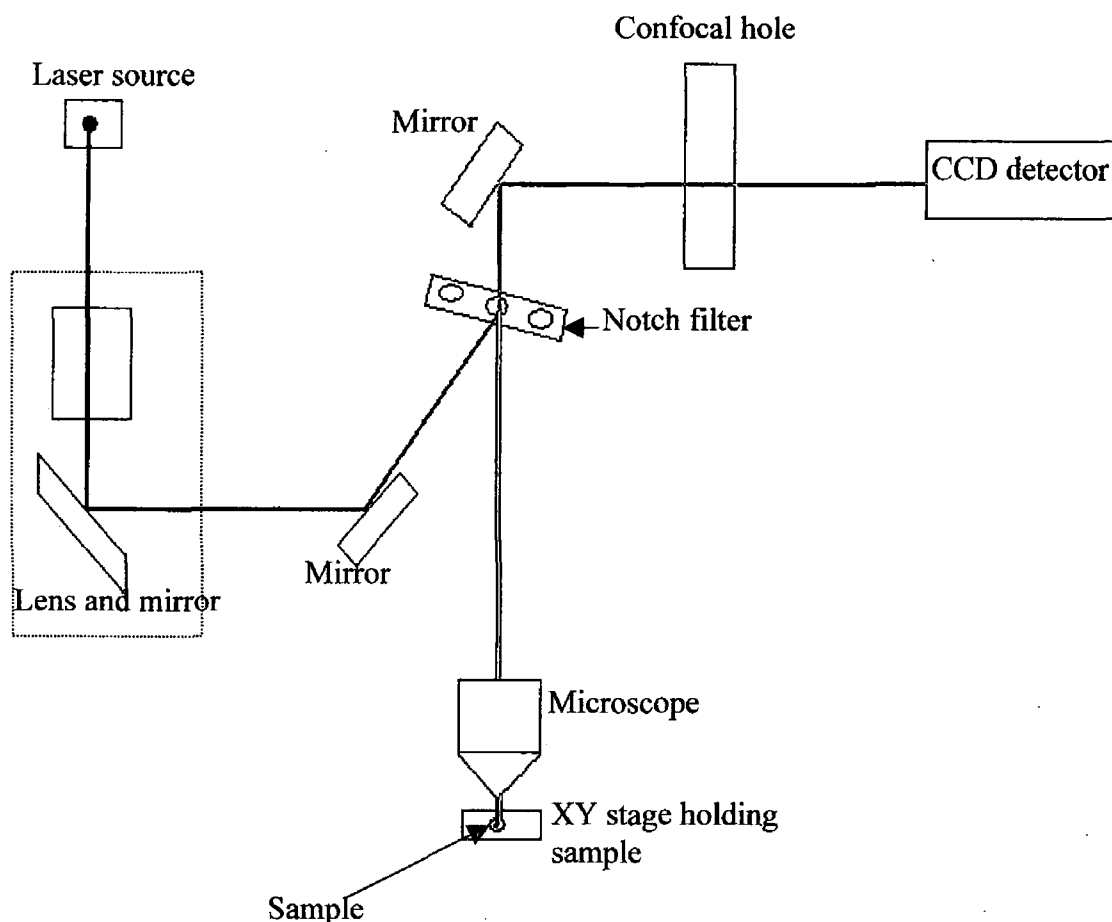


Figure 5-11 The micro-Raman spectroscopy system set-up.

The incident beam is focused through a 100X objective microscope on to the sample. An automatic X-Y stage with a minimum movement of $0.1\ \mu\text{m}$ was used to move the sample during the measurements. The scattered light from the sample was collected in back-scattering mode through the same microscope and passed directly through a notch filter. At this point, the Rayleigh scattering was reflected out and only the Raman beam passed through the notch filter, and subsequently straight through a confocal hole. This scattered beam is carried towards a CCD detector-based spectrometer. The Raman shift is then obtained.

A plasma line at 560 cm^{-1} was used as an internal calibration of the measurements to eliminate environmental and CCD temperature fluctuations during the experiments. A resolution of $\pm 0.05\text{ cm}^{-1}$ is possible for strain-free Si samples using this method. The resolution of this machine as limited by laser drift using the Ar⁺ laser is illustrated in Figure 5-12. This calibration method is described by De Wolf [123].

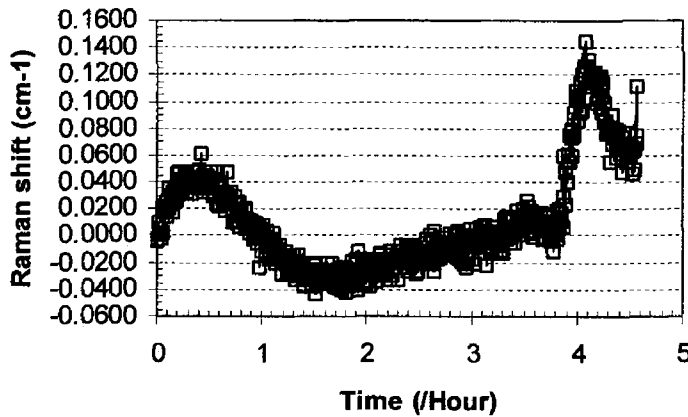


Figure 5-12 The resolution of the micro-Raman system with Ar⁺ laser.

To examine the stresses/strains imposed in the Si substrate due to the reflow process, the samples were cleaved near the middle of the Pb/Sn bumps and investigated in cross-sectional configuration. It must be specified that the Pb/Sn bump takes on a mushroom shape for the *pre*-reflowed process sample. The Pb/Sn bump contacts the BLM layer after the reflow process (*post*-reflowed process sample) and the contact periphery is signified as the edge of the Pb/Sn bump in this study. The micro-Raman data was collected near the interface of the Si and passivation/metal layers. The Raman shift ($\Delta\omega$, cm^{-1}) and the uniaxial stresses (MPa) of the *pre*-reflowed process sample in both X mapping and X-Y mapping modes were performed. The geometry, dimensions and measurement areas of *Pre*- and *post*-reflowed process samples are illustrated in Figures 5-13 and 5-14.

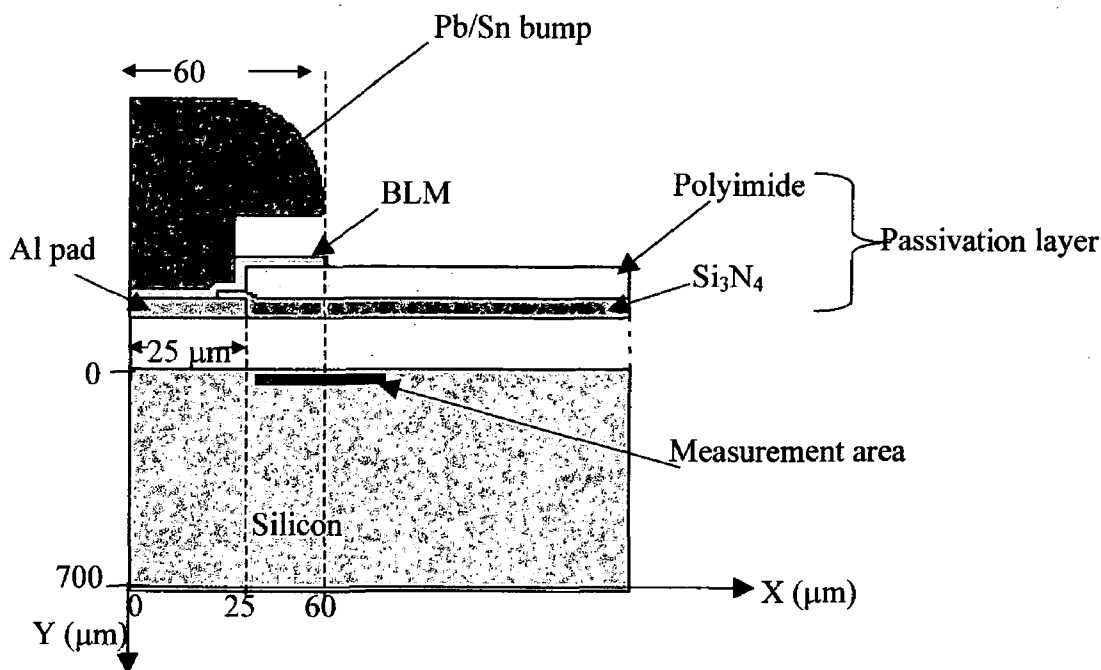


Figure 5-13 Geometry and dimensions of the *pre-reflowed* process sample. Note: the solid area represents the measurement area via X-Y mapping. The positions $X=25\text{ }\mu\text{m}$ and $60\text{ }\mu\text{m}$ are the edges of the metal pad and of the Pb/Sn bump, respectively. The position $Y = 0\text{ }\mu\text{m}$ is the interface between the Si and the metal/passivation layers.

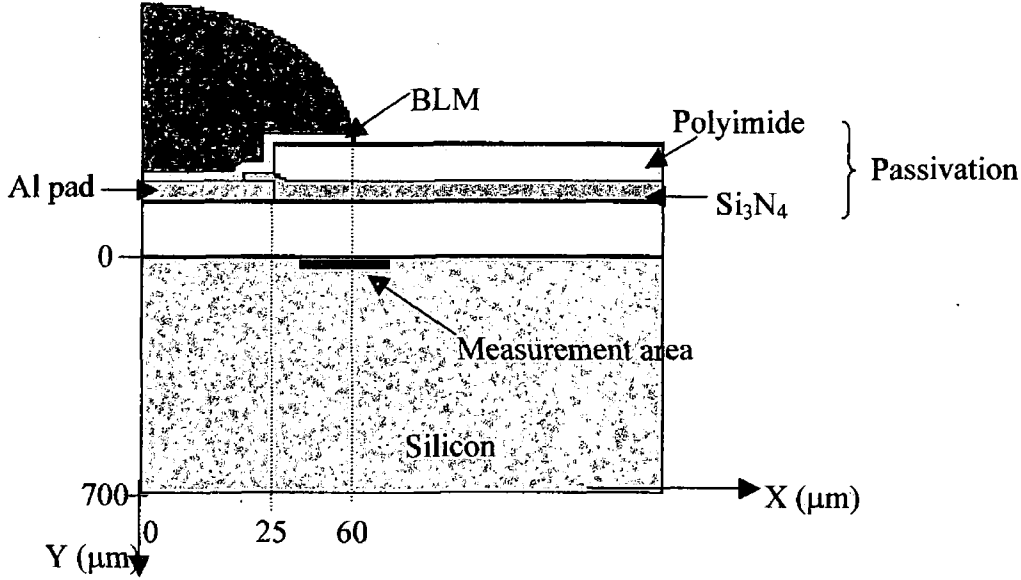


Figure 5-14 The geometry and approximate dimensions of the *post-reflowed* process sample.

The spatial strain distribution in the Si sample can be examined from the measured frequencies of Raman peaks compared with those of a strain-free reference Si sample at 521 cm^{-1} . The relationship between Raman shift and linear strain for the cross-section sample in 0 0 1 direction, derived by De Wolf [123] - [125] and [140] is

$$\sigma_{xx}(\text{MPa}) = -434\Delta\omega(\text{cm}^{-1}) \quad \text{Eq. 5- 1}$$

where σ_{xx} = the uniaxial stress in MPa and $\Delta\omega$ = the Raman shift between the measured Raman peak of strained Si (ω_j) compared with that of strain-free Si (ω_0); $\Delta\omega = \omega_j - \omega_0$, ω_j = the measured frequency of the silicon Raman peak and ω_0 = the frequency of the silicon Raman peak in the stress free state.

5.4 Results and Discussions

This section is separated into 5 parts: (i) SXRT results and discussion, (ii) FEM simulation, (iii) MRS results and discussion, (iv) a simulation of BRST images of *post*-reflowed process sample both for extinction contrast and orientational contrast and (v) XRD results indicating an intermetallic layer between UBM and the Pb/Sn bump for the *post*-reflowed process samples as indicated by sections 5.4.1 to 5.4.5.

5.4.1 SXRT results and discussions

Three main groups of Pb/Sn solder bump samples were examined using SXRT. The results and discussions are described in this chapter.

5.4.1.1 *Stress distribution in Si as a function of various metal (UBM) etching times*

Two UBM etches with etching times of 10 and 35 minutes, defined as wafer numbers 511 and 445, respectively, were performed as described in Chapter 3. The etching process of the UBM layer is one of the important parameter. This step can minimise the stress imposed on the Si substrate due to the residual UBM layer at undesired area. The flowchart of this step is shown in Figure 5-1. Basically, one die is composed of 4 small units as portrayed in Figure 5-15. Two regions of each sample were chosen and examined, and these are shown as positions A and B on any sample die (unit 1-4) in Figure 5-15. All SXRT topographs for both BRT and BRST, were generated by the $\bar{3}\bar{3}9$ reflection harmonic with a penetration depth (t_p) of 125 μm excluding position B of wafer number 511, which was created by the $\bar{2}\bar{2}8$ reflection with a penetration depth of 62.5 μm .

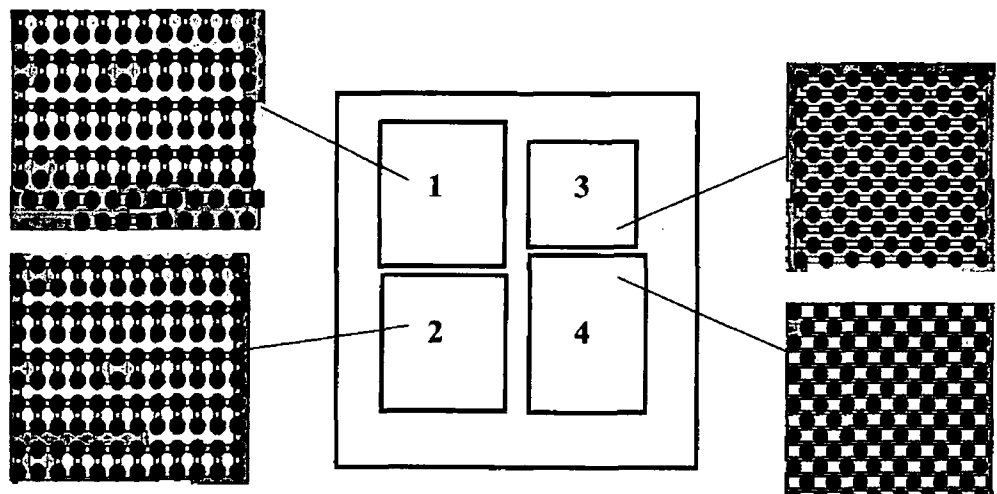


Figure 5-15 Four small units in a die of sample wafer.

Wafer number 445 (etching time = 35 minutes)

The BRT and BRST images of positions A (unit 4) and B (unit 3) illustrated below were generated by the $\bar{3} \bar{3} 9$ reflection harmonic with a penetration depth (t_p) of 125 μm . The sample name and reference number is written beside each topograph.

Position A (unit 4)

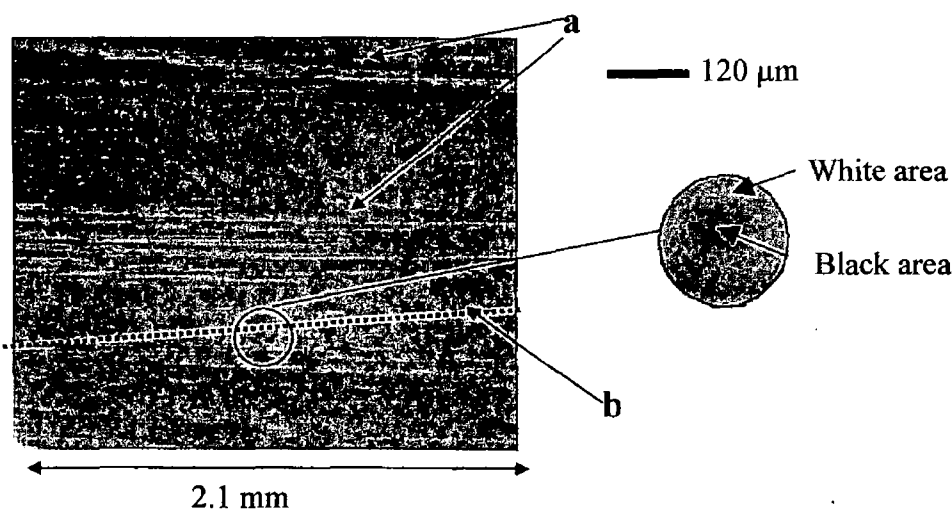


Figure 5-16 $\bar{3} \bar{3} 9$ BRT of sample wafer number 445, 35 minutes etching time, at position A (ref # r25f3-2).

Due to the polishing process, many scratches generated on the backside of the sample were clearly observed (Arrows a) as depicted in Figure 5-16. A dashed line across the image (Arrow b) shows the approximate position of analysis from the back-reflection section topographs, which are portrayed in Figure 5-18 below. From the above image (Figure 5-16), the area highlighted by the dotted circle shows the impact of the strain field in the underlying silicon due to a single lead bump. The magnification of the area illustrates the black and white contrast surrounding the lead bumps due to the strain field. It is noted that the black area represents an increase in recorded intensity. This phenomenon is called the extinction contrast effect [127]-[130] and as mentioned previously it is related to the change in curvature of the crystal lattice planes under the lead bump due to induced strain. For example, the lead bump could produce a strain field, which could resemble one of the two cases shown in Figure 5-17 below:

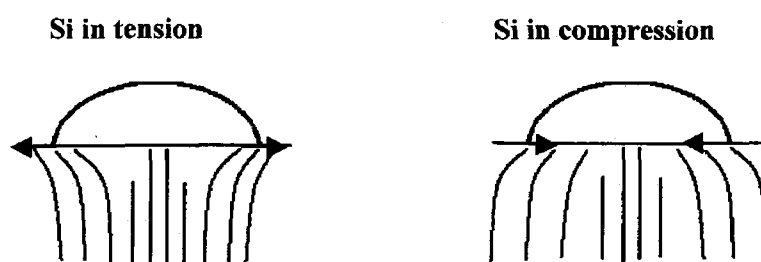


Figure 5-17 The curvature changes in Si lattice planes, which give rise to the extinction contrast effect.

The change in lattice plane curvature, especially near the peripheries of the lead bump will lead to an enhancement or diminution of diffracted intensity in these regions. This phenomenon is observed here. A later and more detailed analysis will elucidate this mechanism more clearly. This black/white contrast is also clearly observed using the BRST technique. The BRST results are depicted in Figure 5-18.

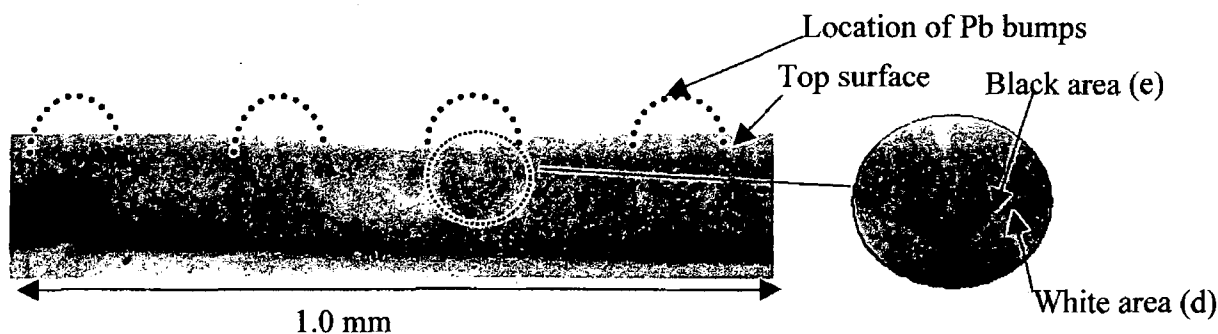


Figure 5-18 $\bar{3}\bar{3}9$ BRST of sample wafer number 445, 35 minutes etching time, at position A (ref # r24f7).

The cross-section of the sample (Figure 5-18) illustrates clearly the aforementioned black and white contrast mechanism (Arrows d and e). It is worthwhile to point out that the metal, BLM and lead alloy materials, which have higher thermal expansion coefficients than silicon (e.g. 28 ppm/C for eutectic Pb/Sn vs. 2.6 ppm/C for silicon), should put the silicon in compression at the interface, thus bowing the silicon lattice planes around the lead bumps. As can be seen, the area around arrow e is the darkest corresponding to the area of greatest compression. In other words, the white contrast beneath arrow e corresponds to an area, which is placed in tension at the interface between these materials. However, this is speculative and a later simulation will be performed to confirm this information. Details of this will follow in Section 5.4.2.

Position B (unit 3)

The images of the second position are also generated by the $\bar{3}\bar{3}9$ reflection, which are shown in Figures 5-19 (a) and (b) below in large area and cross-section modes, respectively.

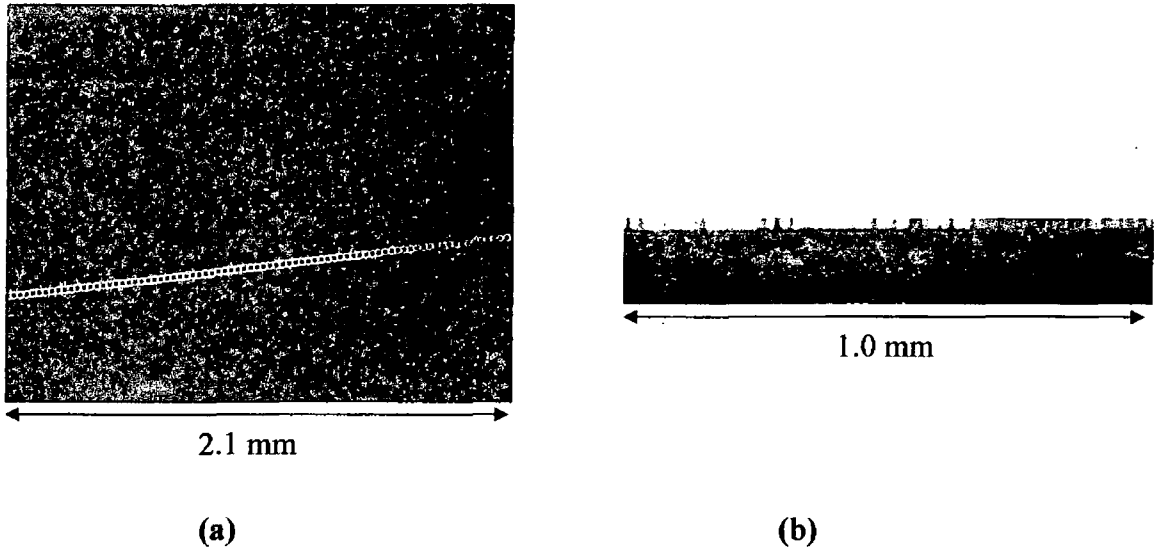


Figure 5-19 $\bar{3}\bar{3}9$ topographs of sample wafer number 445 at position B; (a) BRT (ref# r24f17) and (b) BRST (ref# r24f15-2).

The result at position B confirms the assumption of strain field as explained in position A. In figure 5-19 (b), the image is not as clear-cut as in figure 3-7. However, one can still observe the effect of the bowing of the silicon lattice planes surrounding the lead bump via the black/white contrast change.

Wafer number 511 (etching time = 10 minutes)

The images of sample wafer number 511 were taken from $\bar{3}\bar{3}9$ and $\bar{2}\bar{2}8$ reflections for position A (unit 3) and position B (unit 1), respectively, with t_p of 125 μm and 62.5 μm , respectively.

Position A (unit 3)

Figure 5-20 shows again the black and white contrast corresponding to strain fields in the underlying silicon. However, the delineation of the strain field is not the same as in Wafer 445 (Figure 5-16 and 5-18). From Figure 5-20 (a), it is clearly seen that the strain field is inhomogeneous across the sample i.e. it differs from bump to bump.

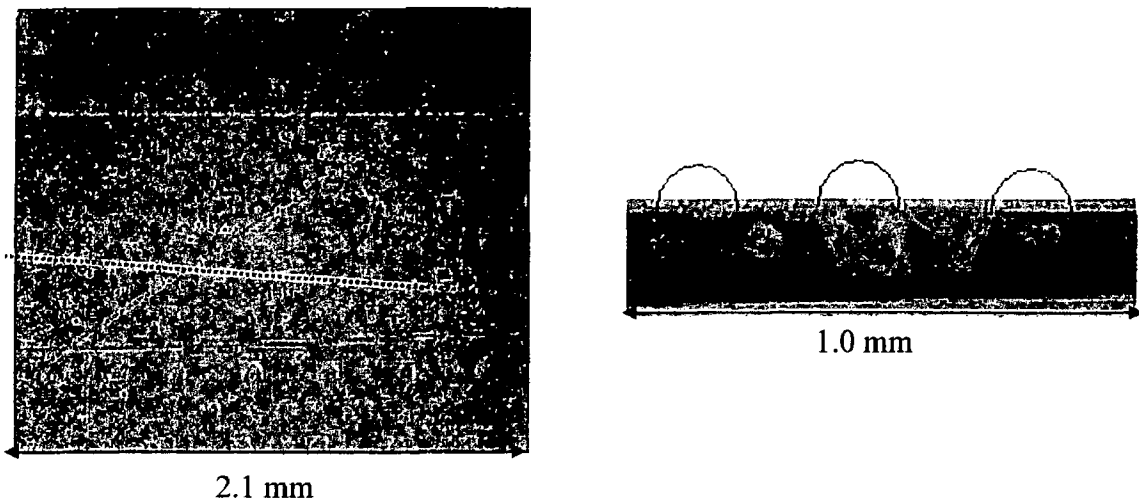


Figure 5-20 $\bar{3}\bar{3}9$ topographs of Pb/Sn solder bump wafer number 511, standard etching time of 10 minutes; (a) BRT (ref# r25f4) and (b) BRST (ref# r24f28).

Position B (unit 1)

The LA-BRT and its corresponding optical microscoph, and BRST topographs generated by $\bar{2}\bar{2}8$ reflections are depicted in Figure 5-21 (a), (b) and (c), respectively. Again, the dashed line across the large area image shows the BRST position

From Figure 5-21(a), an area (Arrow f) displayed a large strain field, whose position is indicated in Figure 5-21(b). The BRST topograph, portrayed in Figure 5-21(c) also shows the large strain field around the arrow f area. The strains appear to be much bigger than those due to the lead bumps.

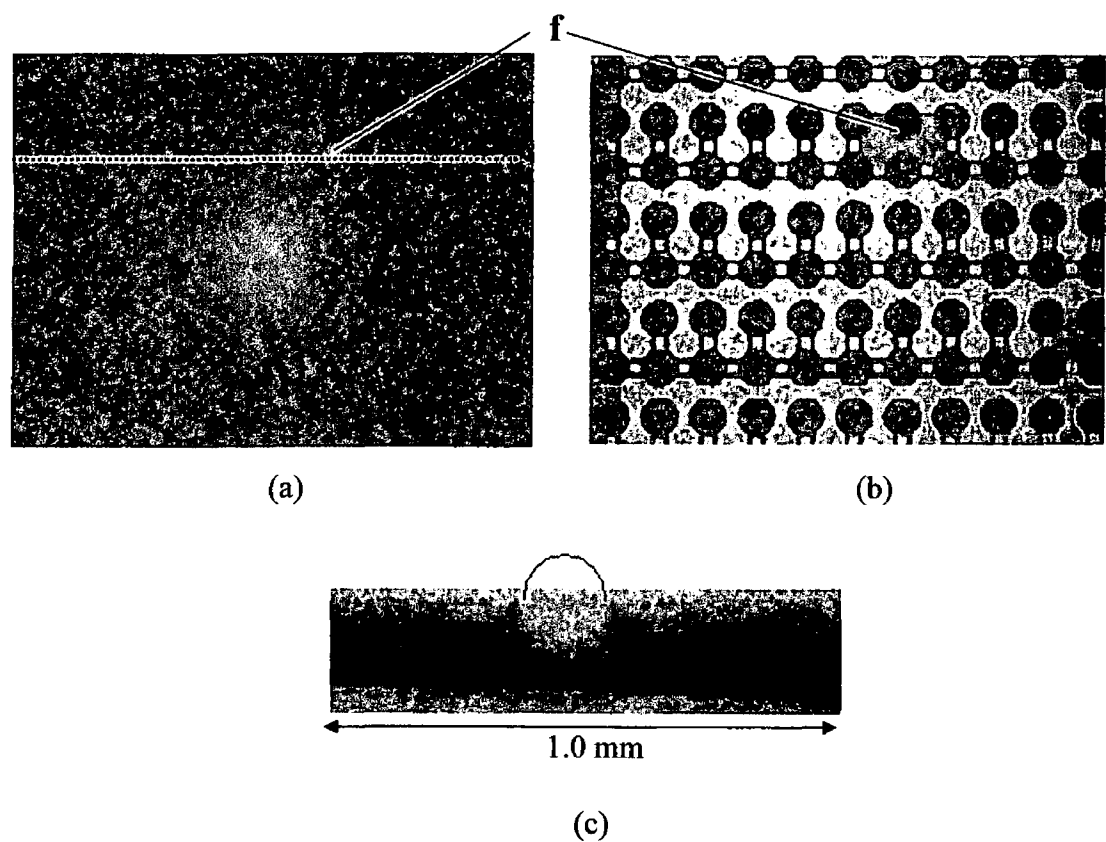


Figure 5-21 $\bar{2}\bar{2}8$ topographs and optical micrograph of sample wafer number 511 at position B (a) BRT (ref# r24f22), (b) its optical micrograph at the same position and (c) BRST (ref# r24f21).

5.4.1.2 Stress distributions in Si due to Pb/Sn solder bump reflow process

As explained in the experimental section, the *Pre*- and *post*- reflowed samples were measured at room temperature before and after simulation of the reflow process at 350°C in atmosphere. Three samples were examined using the SXRT method, i.e. wafer numbers 509, 424 and 445 with UBM etch times of 15, 25 and 35 minutes etching times, respectively.

Wafer number 509 (etching time = 15 minutes)

All topographs were generated from the $\bar{3}\bar{3}9$ reflection harmonic with a penetration depth of 125 μm . The large area and section topographs generated from the $\bar{3}\bar{3}9$ reflection were taken at room temperature for *Pre*- and *post*-reflowed process samples.

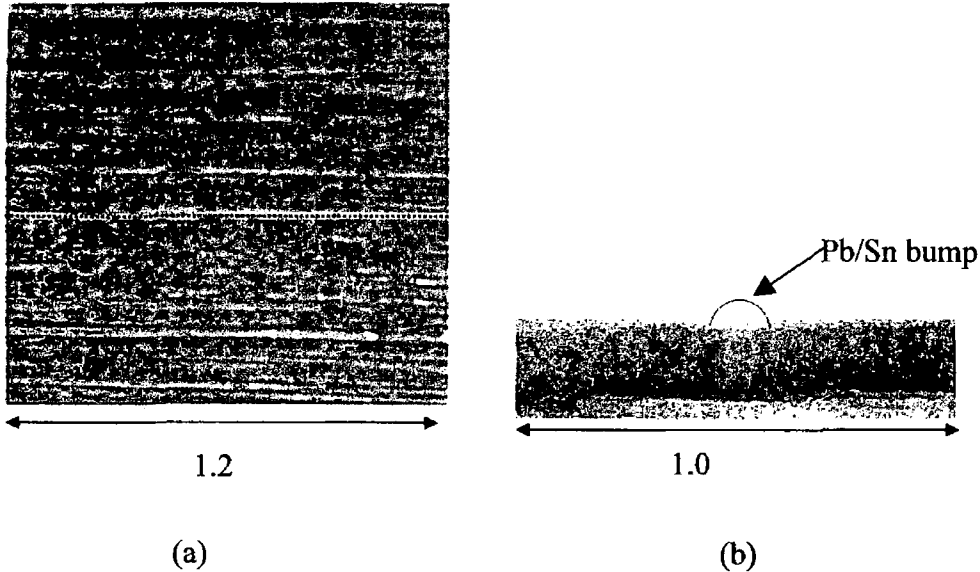


Figure 5-22 Topographs of *Pre*-reflowed sample wafer number 509 (15 minutes etching time): (a) $\bar{3}\bar{3}9$ BRT (ref# r26f205-1) and (b) $\bar{3}\bar{3}9$ BRST (ref# r26f210-1).

The topographs in Figure 5-22 imply lower stresses in the underlying silicon induced by the lead bump process. However, the strain fields are more intense after reflow. Their LA-BRT and BRST images are portrayed in Figure 5-23 (a and b).

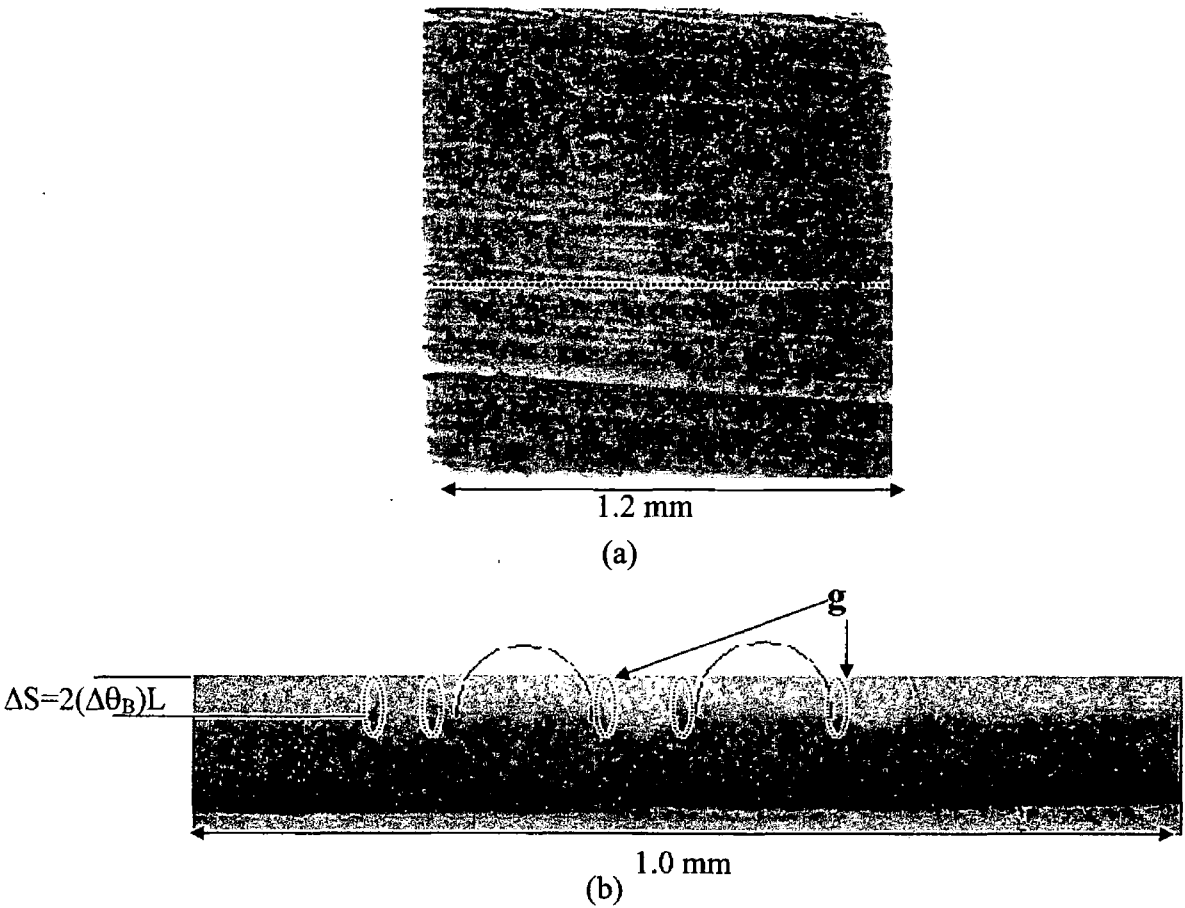


Figure 5-23 (a) $\bar{3}\bar{3}9$ BRT (ref# r26f211) and (b) $\bar{3}\bar{3}9$ BRST (ref# r26f214-1) images of post-reflowed sample number 509.

The strain images, again appearing as a black/white contrast, seem to be larger when the sample was heated. This suggests that the strain fields in the underlying silicon increase after the reflow process. The BRST image above (Figure 5-23 (b)) confirms this observation of Figure 5-23 (a) in that the reflow process induces a higher intensity of strain fields. It is noted that a lifting of the image of strained Si near the Pb edges above the image of the rest of the Si (Arrow g) occurred due to severe stresses being imaged via orientational contrast [131]. The orientational contrast can

be observed if the misorientation exceeds the x-ray beam divergence ($\Delta\phi$)[132] - [133] which in this case is equal to 0.0238 mrad [134]. The images of locally severely strained Si near the peripheries of the Pb/Sn bumps are lifted up in the topography image with respect to the image of the remaining Si matrix due to this orientational contrast effect as shown in Figure 5-24. It is noted that this figure is the same as Fig. 2-15 in the orientational contrast section. The effect of the orientational contrast occurs due to a misorientation of the lattice plane because of severe strain. Thus, the diffracted beam from the misoriented part in the crystal takes a different direction in space compared to the rest of the crystal.

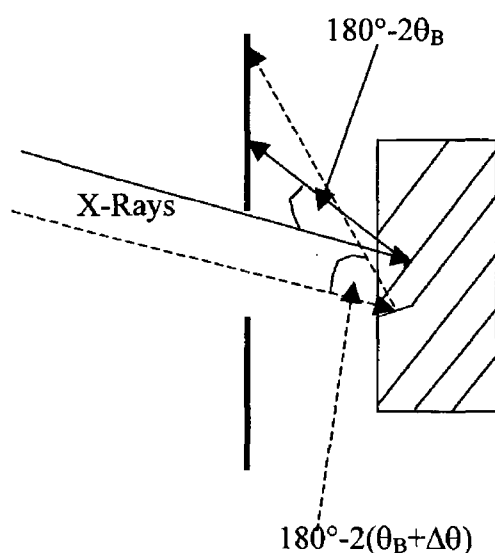


Figure 5-24 The orientational contrast mechanism for the Pb/Sn bump sample.

From Eqs. 2-19 and 2-20, it is found that the misorientation ($\Delta\theta_B$) is equal to the tilt component (α) only, i.e. $\Delta\theta_B \equiv \alpha$, and is related to first order to shear strain (γ_{xy}) as illustrated in Figure 5-25.

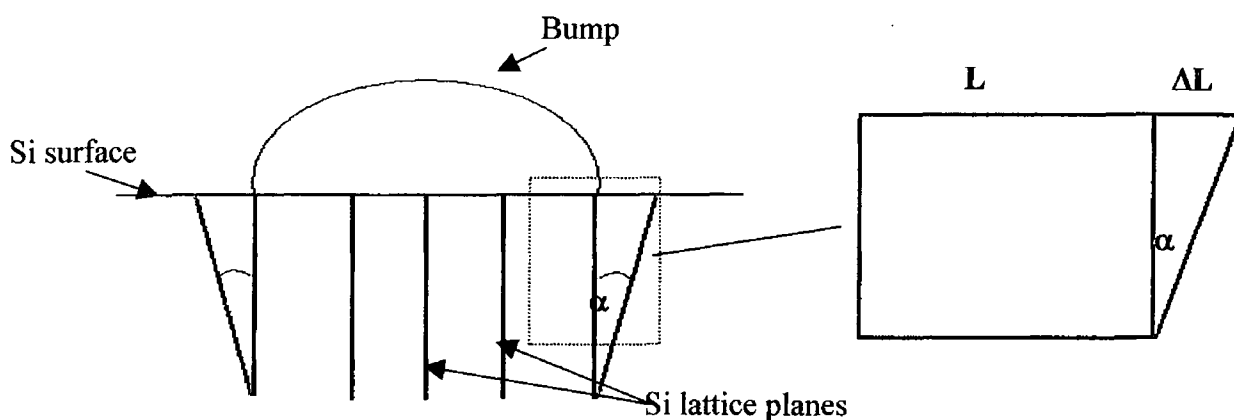


Figure 5-25 Diagram shows the relationship of the misorientational contrast and shear strain.

From Fig. 5-25, L is the lattice plane spacing, T is the sample thickness, ΔL is the distance over which a lattice plane tilts along the surface direction, ΔT is the vertical distance in the sample, over which the planes are tilted and angle α is the tilt angle.

It is assumed that $\Delta L \ll T$ and L , therefore

$$\alpha \ll 1 \quad \text{Eq. 5-2}$$

therefore

$$|\tan \alpha| \cong |\alpha| = \left| \frac{\Delta L}{\Delta T} \right| = |\gamma_{xy}| \quad \text{Eq. 5-3}$$

This gives a quantitative estimate for the magnitude of strain in the underlying silicon via the equations:

$$\Delta S = 2\Delta\theta_B L \quad \text{Eq. 5-4}$$

$$\gamma_{xy} \cong \Delta\theta_B = \frac{\Delta S}{2L} \quad \text{Eq. 5-5}$$

where ΔS is the orientational contrast shift (Arrow g) which can be measured from the topograph.

In this case equation (5-4) yields, $\gamma_{xy} = 6.2 \times 10^{-4} \approx 0.06\%$. The magnitudes of the induced stresses are given by $|\tau_{xy}| = G |\gamma_{xy}|$ where G , the Shear modulus of Si (isotropic) = 162.3 GPa [135]. Thus, the upper limit on the stress magnitudes is of the order of $|\tau_{xy}| \approx 100$ MPa.

Wafer number 424 (etching time = 25 minutes)

The following images were also generated from the $\bar{3}\bar{3}9$ reflection. The BRT image at room temperature is depicted in Figure 5-26.

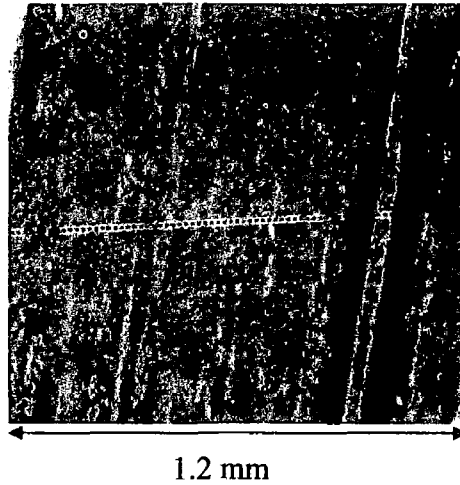


Figure 5-26 $\bar{3}\bar{3}9$ BRT image of *Pre*-reflowed sample wafer number 424 (25 minutes etched, ref# r26f216).

Figure 5-26 indicates that the strains induced by the single lead bump process are more intense and extend for greater diameters than for the 15 minutes etching time, i.e. sample wafer number 509 (Figure 5-22(a)) at room temperature. Finally, the sample was heated to 350 °C. The results are shown in Figure 5-27 (a and b).

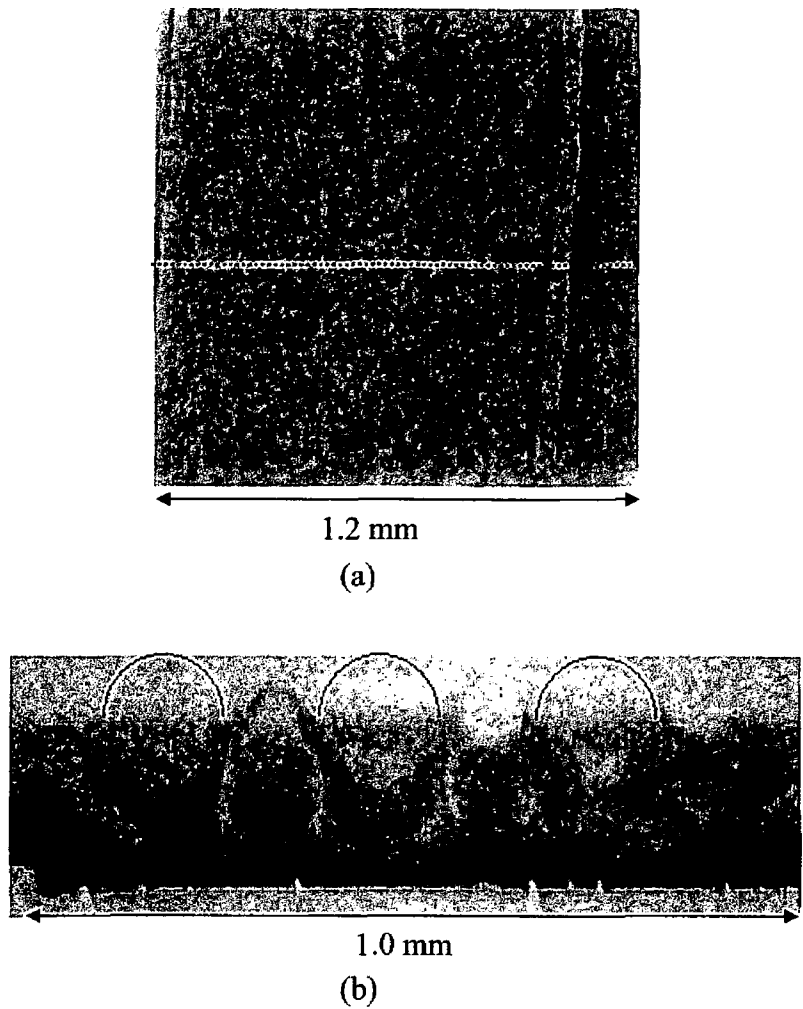


Figure 5-27 $\bar{3}\bar{3}9$ topographs of *post-reflowed* sample wafer number 424 (25 minutes etched); (a) BRT (ref# r26f220) and (b) BRST (ref# r26f221).

Similar to other samples, the black/white contrasts attributable to the Pb/Sn bump imposed strains are expanded to greater diameters when the sample was heated to 350 °C. Again, the severe strains at the edge of the Pb bumps are visible in the BRST (Figure 5-27 (b)) via orientational contrast. In addition, the strain fields in the underlying Si are also observed due to a contribution of extinction and orientational contrast mechanisms. Using Eqs. 5-2 to 5-4, the limits on the strain are $|\gamma_{xy}| = 0.07\%$. Therefore, the maximum magnitudes of stress $|\tau_{xy}| \approx 113.6 \text{ MPa}$.

Wafer number 445 (etching time = 35 minutes)

Figures 5-28 (a - c) show the large area back-reflection topograph, optical micrograph and BRST of the *Pre*-reflowed sample, respectively.

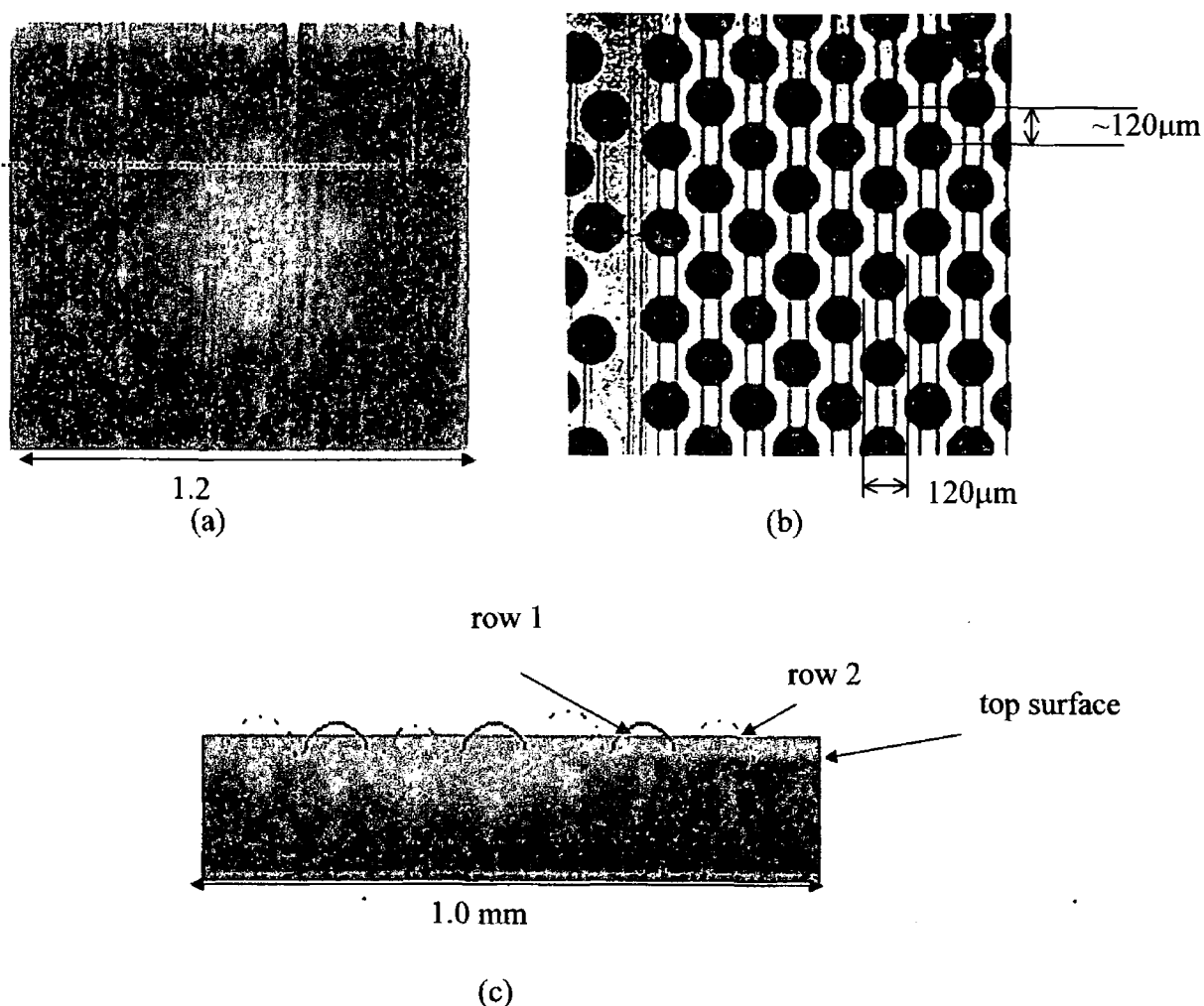


Figure 5-28 Topographs of *Pre*-reflowed sample wafer number 445 (35 minutes etching time); (a) $\bar{3}\bar{3}9$ BRT (ref# r26f3), (b) optical micrograph of similar area and (c) $\bar{3}\bar{3}9$ BRST (ref# r26f10).

The scratches on the backside of the sample, which were generated from the thinning and polishing processes, are clearly observed in the image (Figure 5-28(a)). The optical micrograph of the same area is shown in Figure 5-28(b). A line across the

image locates the approximate position for its corresponding section topograph, which illustrates the strains/stresses due to the single lead bump process (Figure 5-28 (c)). The stresses/strains appear to be smaller than for the other samples because the x-rays passed through the sample between two rows (row 1 and 2) of the lead bump array. The strain fields underneath the lead bumps appear as a black-white contrast, which was explained previously. In addition, the strains from the backside of the sample due to the scratches are observed in this image. The sample was heated to a temperature of 350 °C in atmosphere as a reflow process simulation and cooled down to room temperature. The BRT and BRST images of the *post-reflowed* sample are shown in Figures 5-29 (a and b), respectively.

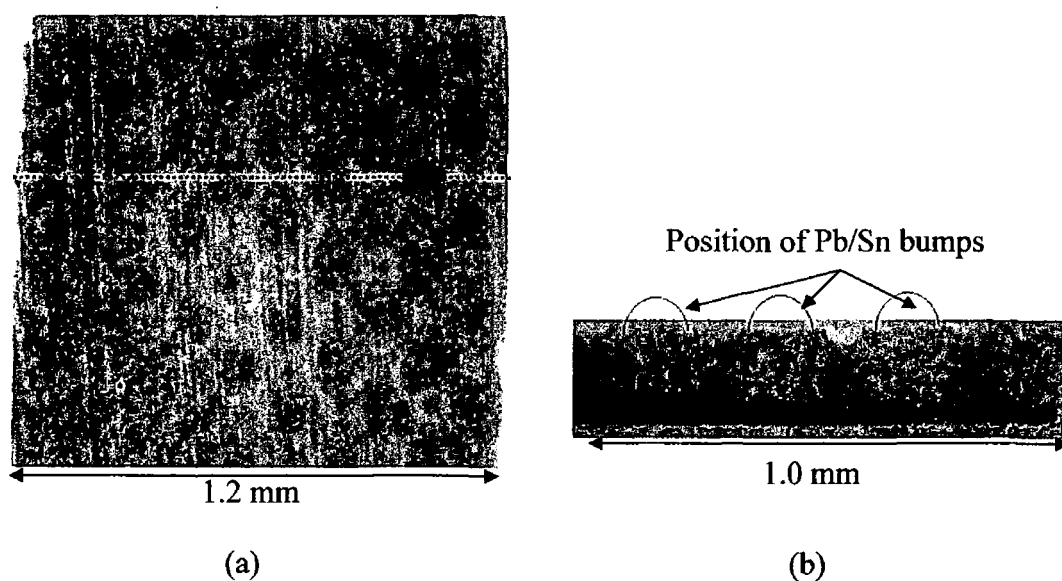


Figure 5-29 Topographs of post-reflowed sample wafer number 445 (35 minutes etching time); (a) $\bar{3}\bar{3}9$ BRT (ref# r26f11) and (b) $\bar{3}\bar{3}9$ BRST (ref# r26f10).

Figure 5-29 shows that the strain fields in the underlying silicon below the lead bumps have again expanded laterally after being heated to 350 °C. This expansion is observed as a greater diameter of the black-white contrast imaged in the underlying silicon due to a single lead bump. From the BRST image (Figure 5-29(b)), it can be seen that the strains are altered dramatically from both the top surface, due to the lead bump process, and from the backside due to scratches after heating to 350°C. It

is noted that the strain fields are visible through to the whole depth of the wafer (~150 μm).

5.4.1.3 *Major source of stress distribution in the silicon substrate*

To confirm that the Pb/Sn reflow process is a major source of stress distribution in the underlying silicon, the Pb/Sn solder bumps were removed from the samples using wet etching.

Wafer number 551 (Pre-reflowed sample, etched back)

Wafer number 551 is an *Pre-reflowed* sample, from which the Pb/Sn solder bumps were removed. Topographs were generated from the $\bar{2}\bar{2}8$ reflection harmonic with a penetration depth (t_p) of 50 μm . The sample name and reference number is written beside each topograph. The circuitry underneath the lead bump was observed in the underlying silicon.

The “normal” circular strain features due to strain imposed by the circular bumps have now disappeared. However, the strain fields attributable to the electrical via structures are still visible (Arrow h). A dashed line across the image is the approximate position for the section topograph in Figure 5-30(c).

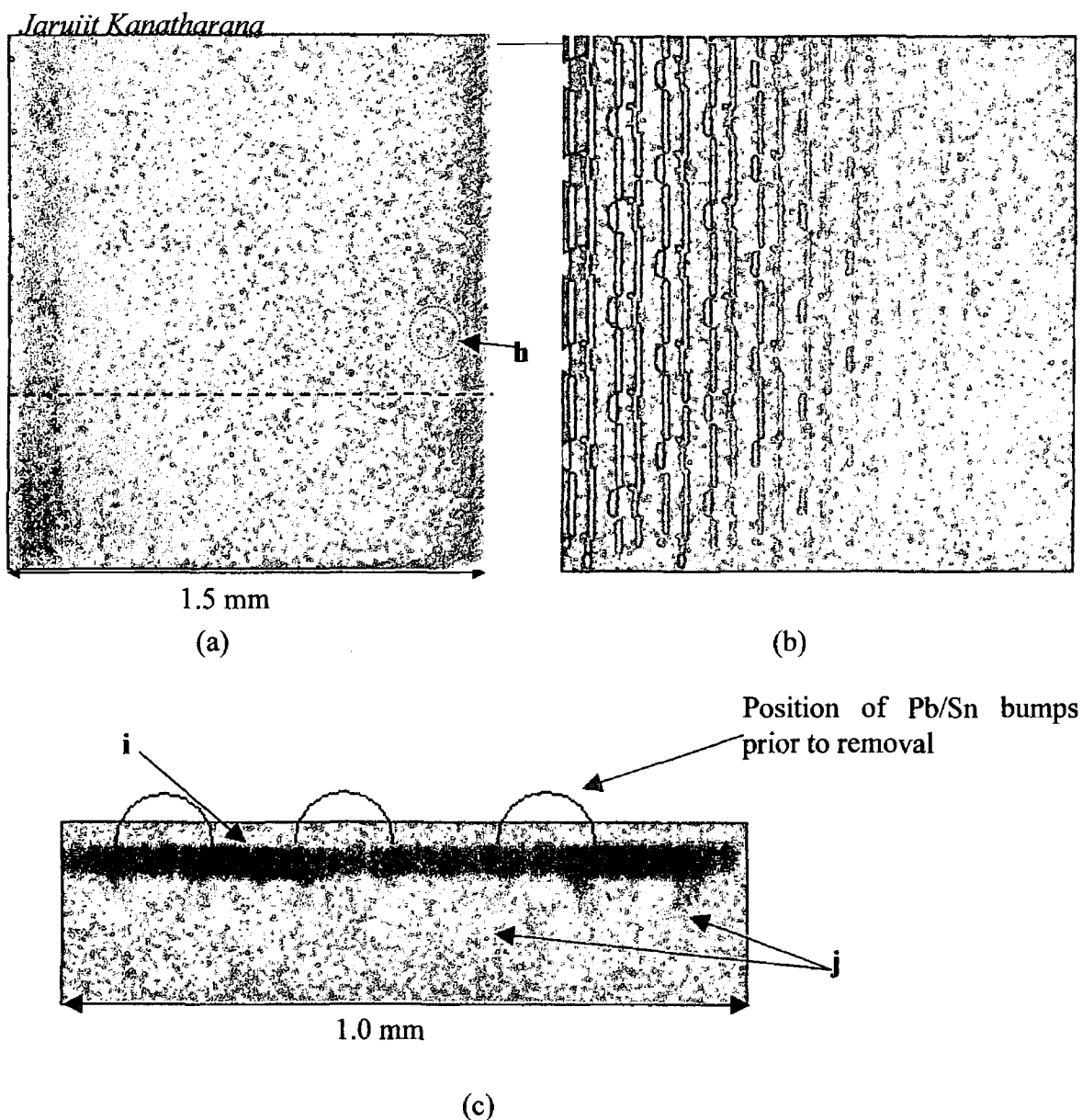


Figure 5-30 (a) $\bar{2}\bar{2}8$ BRT image of *Pre-reflowed* sample number 551, ref# r28f159-2, (b) an optical micrograph of the same area, and (c) $\bar{2}\bar{2}8$ BRST image corresponding to the position of the dashed line, ref# r28f161-2.

Compared to the Pb/Sn *Pre-reflow* sample BRST in Figure 5-24(b), the strain fields in the underlying silicon due to a single lead bump appear to be much relieved. However, the severe stresses/strains from other processes are significant and are still visible in the image. These can be observed as indicated by Arrows j (predominantly between bumps) and by Arrow i (near the surface, e.g. epilayer strain, process layers and metallisation).

Wafer number 225 (post-reflowed sample, etched back)

The Pb/Sn solder bump sample was reflowed at 350°C in nitrogen atmosphere and then etched back in order to confirm that the bumps are the major source of strain in the underlying substrate. The BRT and its optical micrograph, and the BRST images are illustrated in Figures 5-31 (a) – (c).

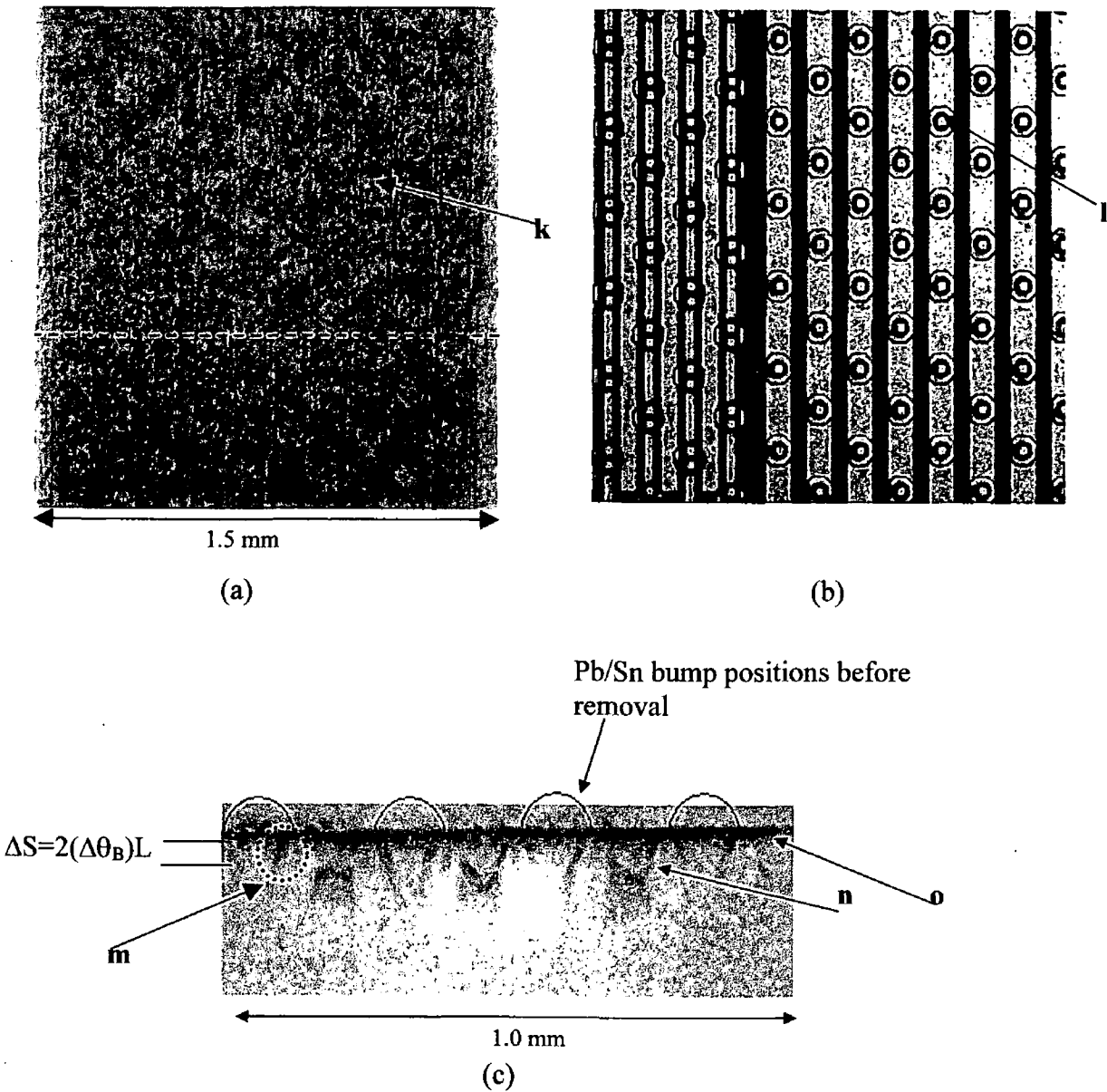


Figure 5-31 (a) $\bar{2}\bar{2}8$ BRT image of *post-reflowed* and etched back sample wafer number 225 (ref# r28f166-3), (b) an optical

micrograph of the same area, and (c) $\bar{2}\bar{2}8$ BRST image (ref# r28f168-2).

In Figure 5-31(a), large circular strained regions in the underlying silicon are still observed. A dashed line represents the approximate position for the section topograph in Figure 5-31(c).

After the Pb/Sn bumps were reflowed and then etched back, the strains in the underlying Si still appear in both of the topographs (Figures 5-31(a) and (c)) and the optical micrograph (Figure 5-31(b)) as Arrows k and l. This correlates well with the position of the bumps and the diffracted x-ray intensity is enhanced at the region near the bump periphery. It is possible that there are new intermetallic layers at the interface of the Pb/Sn bump and the UBM layer in this region. Considering the BRST image (Figure 5-31(c)), the strains distributed in the underlying silicon appear to be much smaller when the Pb bumps were removed, as the orientational contrast related streaks pointing upwards are very short. However, the orientational contrast related images of the misorientated Si now point predominantly downwards into the Si substrate (Arrow m) indicating that the lattice plane tilt has changed sign from the previous case of the Fig. 5-23(b). The maximum shear stress estimated from this orientational contrast is about 100 MPa, which is the same order as the stress value of the *post*-reflowed sample but opposite sign. In addition, other strains are still present and are visible in the image as indicated by Arrow n (predominantly between bumps) and by Arrow o (near the surface, e.g. epilayer strain, process layers and metallisation). These results confirm that the Pb/Sn bumps are the major source of the strain. However, the strains observed here may be generated from the new intermetallic layers, which were mentioned above [136][138]. These layers have to be and will be analysed in order to ascertain the sources of the strain distribution in the underlying silicon due to the Pb/Sn process using XRD (X-Ray Diffraction).

5.4.2 FEM results and discussions

Two types of FEM modeling were initially carried out: (a) examining the strains generated by differences in temperature between the Si substrate and the metallisation and (b) the simpler uniaxial load model of Fig. 5-32. Both models produce similar results. The simpler uniaxial load model is used, due to the complexity of interpreting subtle temperature-related effects on the multilayer metallisation between the Pb/Sn bump and the underlying substrate. While it may be not fully accurate, the uniaxial load model will capture the main features of the BGA-imposed strain fields, in particular locating regions of strain enhancement.

The FEM was performed for the substrates after the Pb/Sn bump was reflowed at 350 °C via a uniaxial loading of 100 MPa at edge G as shown in the Figure 5-32.

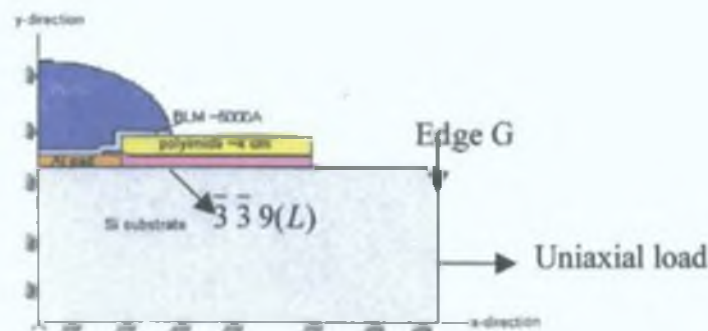


Figure 5-32 The boundary and modelling condition for this study.

The estimated resultant strains ϵ_{xx} , ϵ_{yy} and γ_{xy} are depicted in Figures 5-36 to 5-38. These figures show that significant strain fields in the Si substrate are generated at the edge of the Pb/Sn bump. To compare the strain distributions in Si from the FEM and SXRT data, the strains perpendicular to the $\bar{3}\bar{3}9$ direction (L direction) are simulated as illustrated in Figure 5-33. This figure indicates that the strains build up at the edge of the Pb/Sn bump (at point $x=0$ in the Figure 5-33). In addition, the order of magnitude of the shear strain along the L direction is also similar to the shear strain calculated from the orientational contrast in the SXRT image (Fig. 5-23).

Therefore, it can be confirmed that the shear strain data from FEM corresponds well to the shear strain magnitude obtained from SXRT.

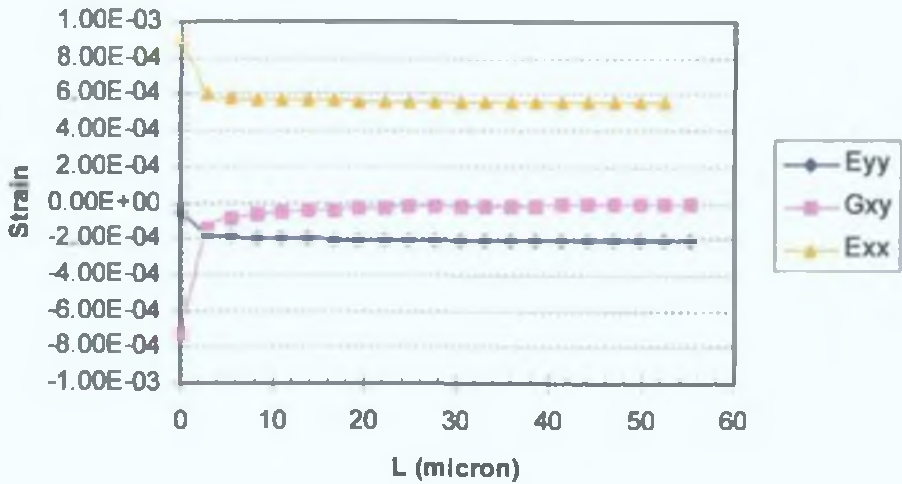


Figure 5-33 Finite element simulation of tensile/compressive strain distribution in Si along the $\bar{3}\bar{3}9$ direction in the *post*-reflowed sample simulated via uniaxial edge loading. $L = 0$ indicates the position of the periphery of the Pb/Sn bump, E_{xx} and E_{yy} = normal strains in x- and y- directions, and G_{xy} = shear strain.

The normal stresses, S_{xx} and S_{yy} , which respond to σ_{xx} and σ_{yy} , near the top surface at the interface between Si and the metal/passivation layers from the middle of the Pb/Sn along the surface are illustrated in Figure 5-34. It is seen that the stress in the Si near the interface is in tension for both σ_{xx} and σ_{yy} . The maximum magnitude of σ_{xx} of about 220 MPa was found near the edge of the Pb/Sn solder bump as indicated by Arrow m.

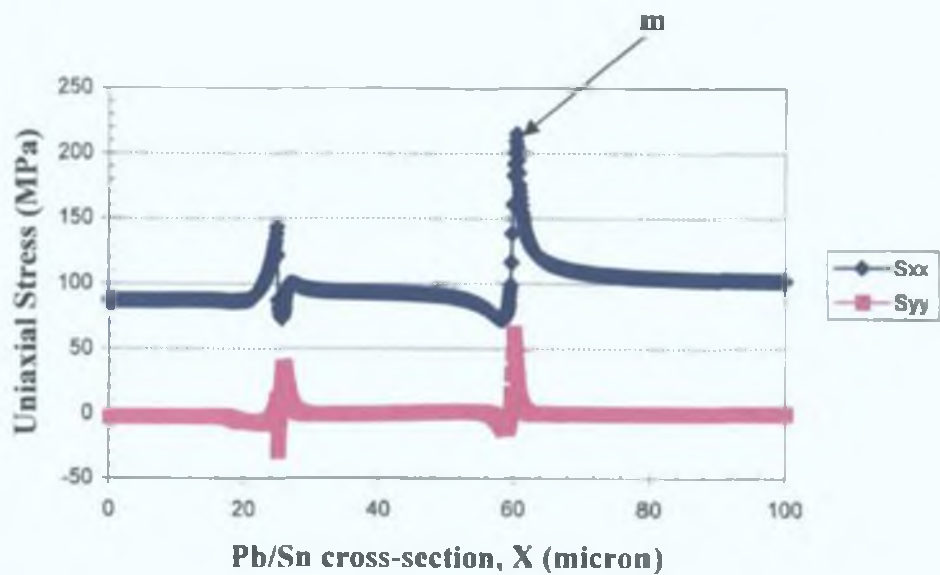


Figure 5-34 The simulated normal stresses (S_{xx} and S_{yy} , or σ_{xx} and σ_{yy}) in the Si wafer due to the Pb/Sn bump reflow process near the interface of the Si and metal/passivation layers due to the Pb/Sn bump reflow process.

In addition, the displacement vectors (\mathbf{H}_i) of the $\bar{3}\bar{3}9$ lattice planes, calculated at each point i in the FEM discretisation within a selected region of the simulated Si, are plotted along the cross-section of the *post*-reflowed sample as illustrated in Figure 5-35 [108]. In order to compare the BRST image of the *post*-reflowed sample (Fig. 5-23(b)) and the FEM results, the geometries and dimensions used in the simulation are overlaid on the corresponding BRST image, as shown in Figure 5-36. In this work, the vector \mathbf{H}_i is normal to the lattice displacement and deviates from the lattice direction due to an imposed strain field. This FEM simulation demonstrates that the Pb/Sn bump is under tension and that it induces compressive stress in the Si directly underneath the central regions of the solder bump and tensile stress near the edge of the bump due to the reflow process. This result is in good agreement with Chen *et al.* [125], which investigated the stress in Si due to one type of Pb/Sn bump using micro-Raman spectroscopic measurement.

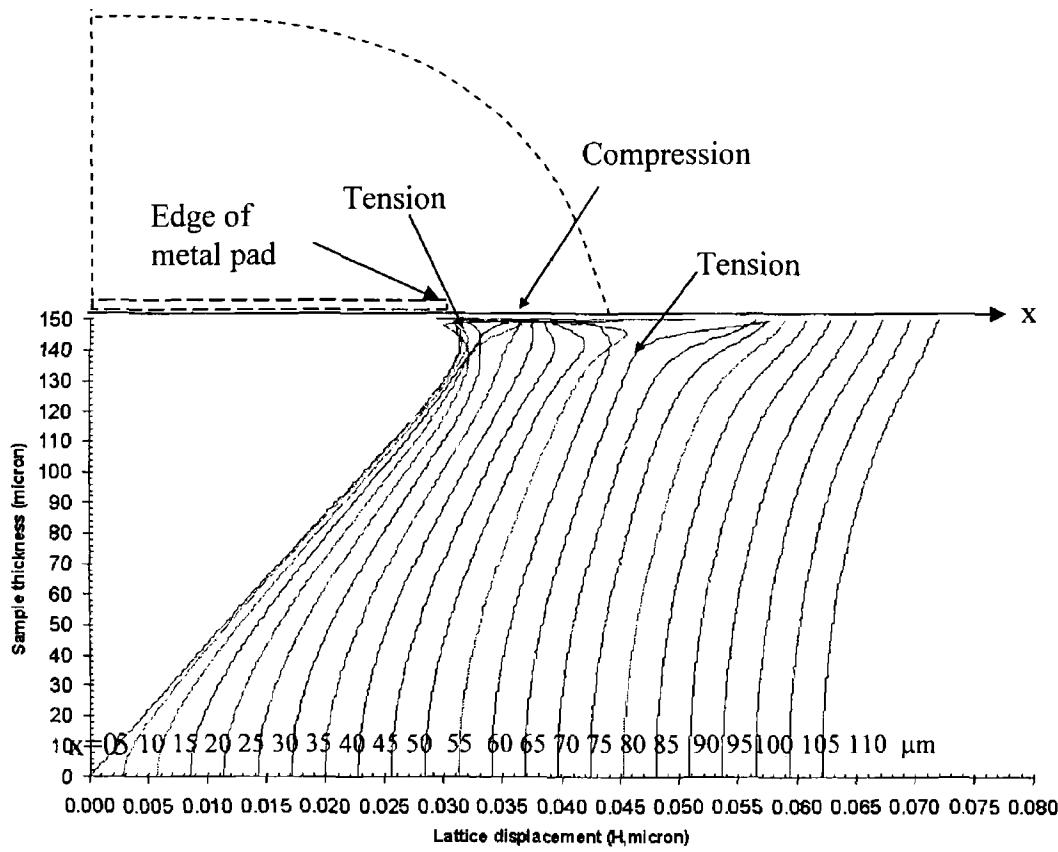


Figure 5-35 The simulated displacement of the $\bar{3}\bar{3}9$ lattice planes calculated for a selected region of the Si under the periphery of the Pb/Sn bump.

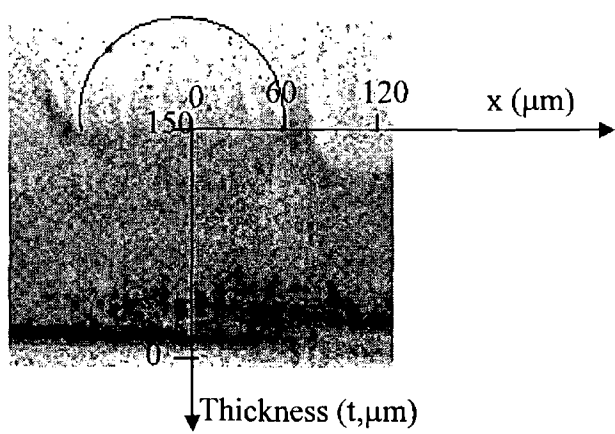


Figure 5-36 An overlay of the dimensions used in the FEM simulation upon the $\bar{3}\bar{3}9$ BRST image of the left hand side Pb/Sn bump of Fig. 5-23(b).

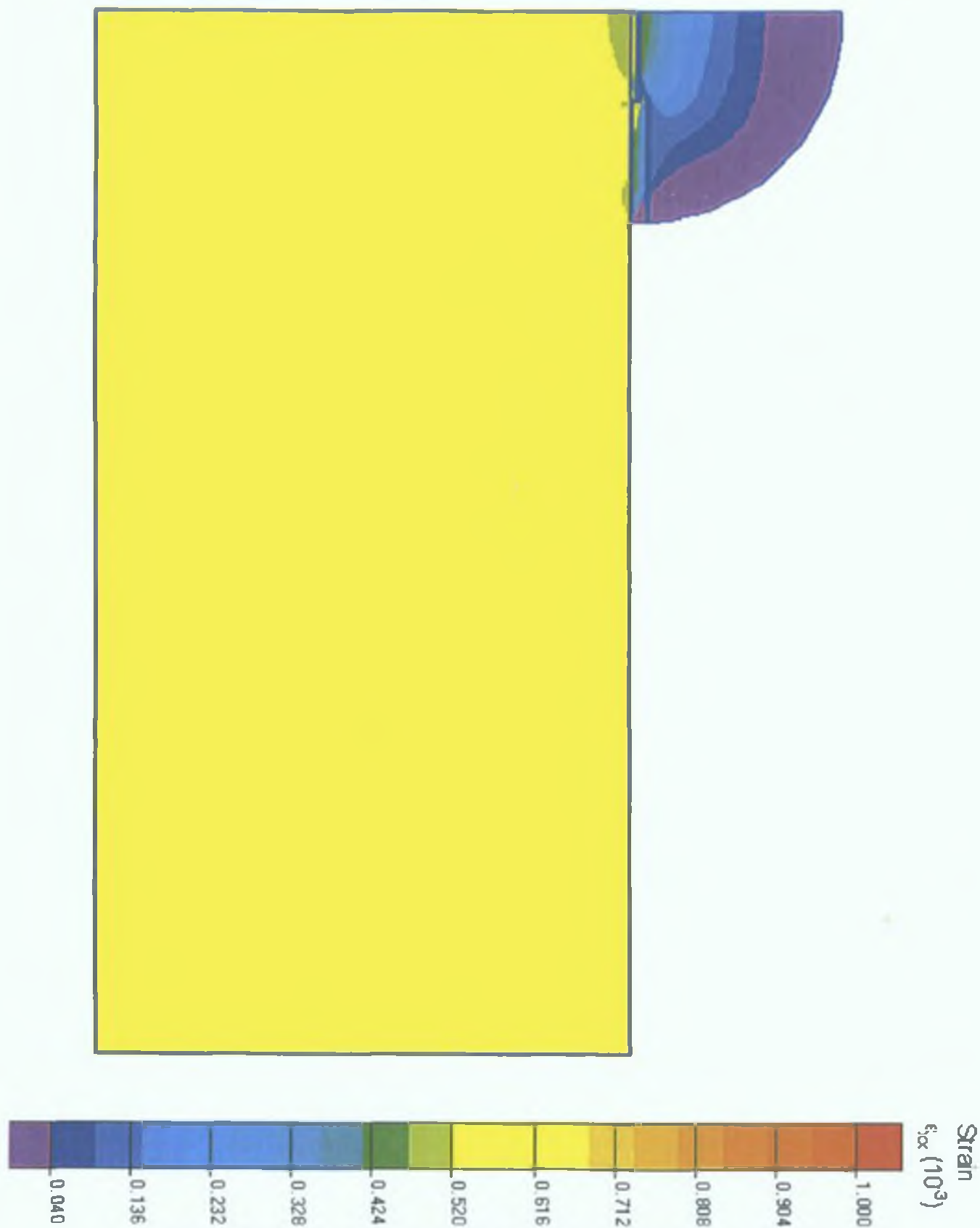


Figure 5-37 The normal strain (ϵ_{xx}) generated by the uniaxial loading model.

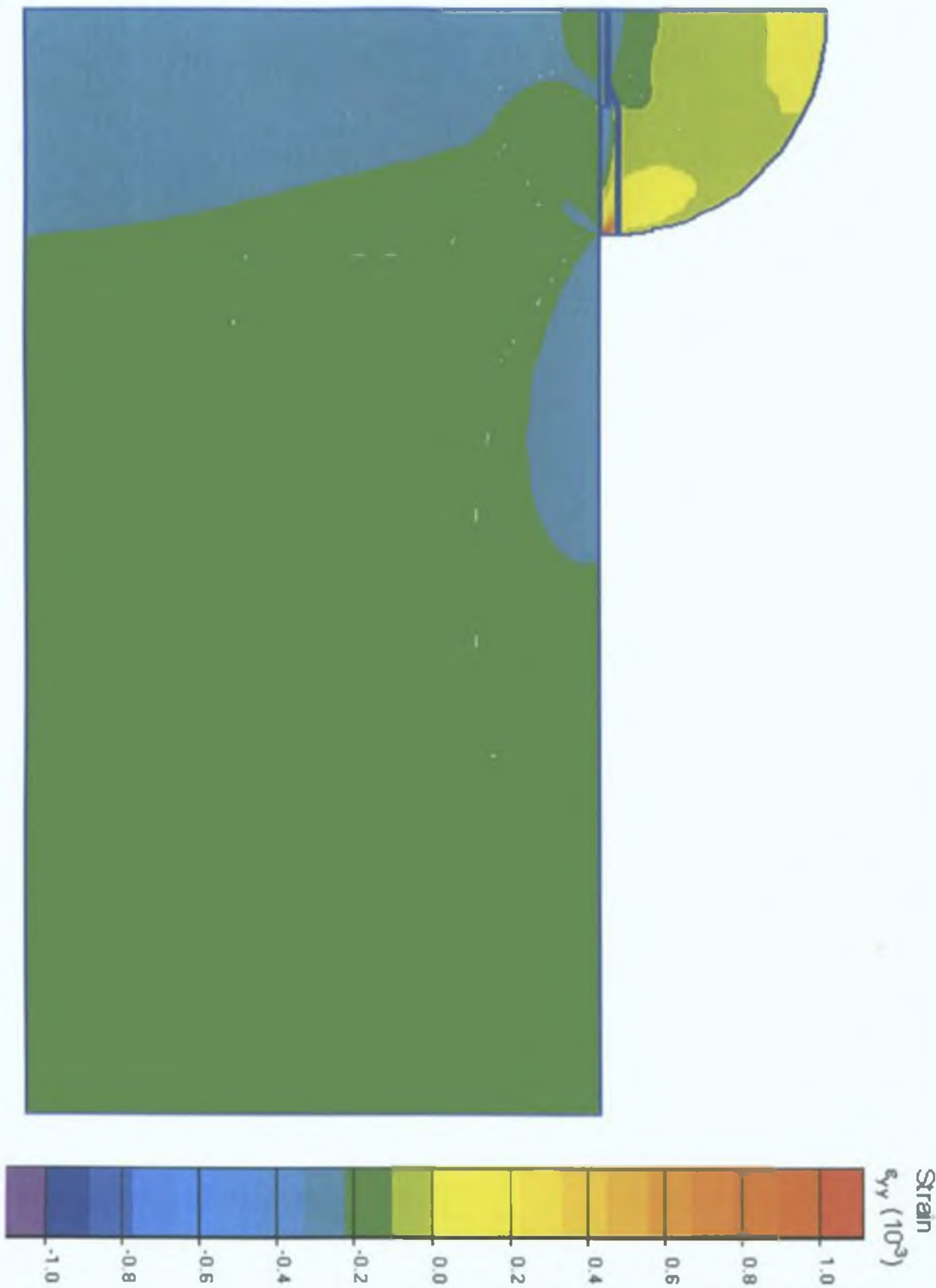


Figure 5-38 The normal strain (ϵ_{yy}) generated by the uniaxial loading model.

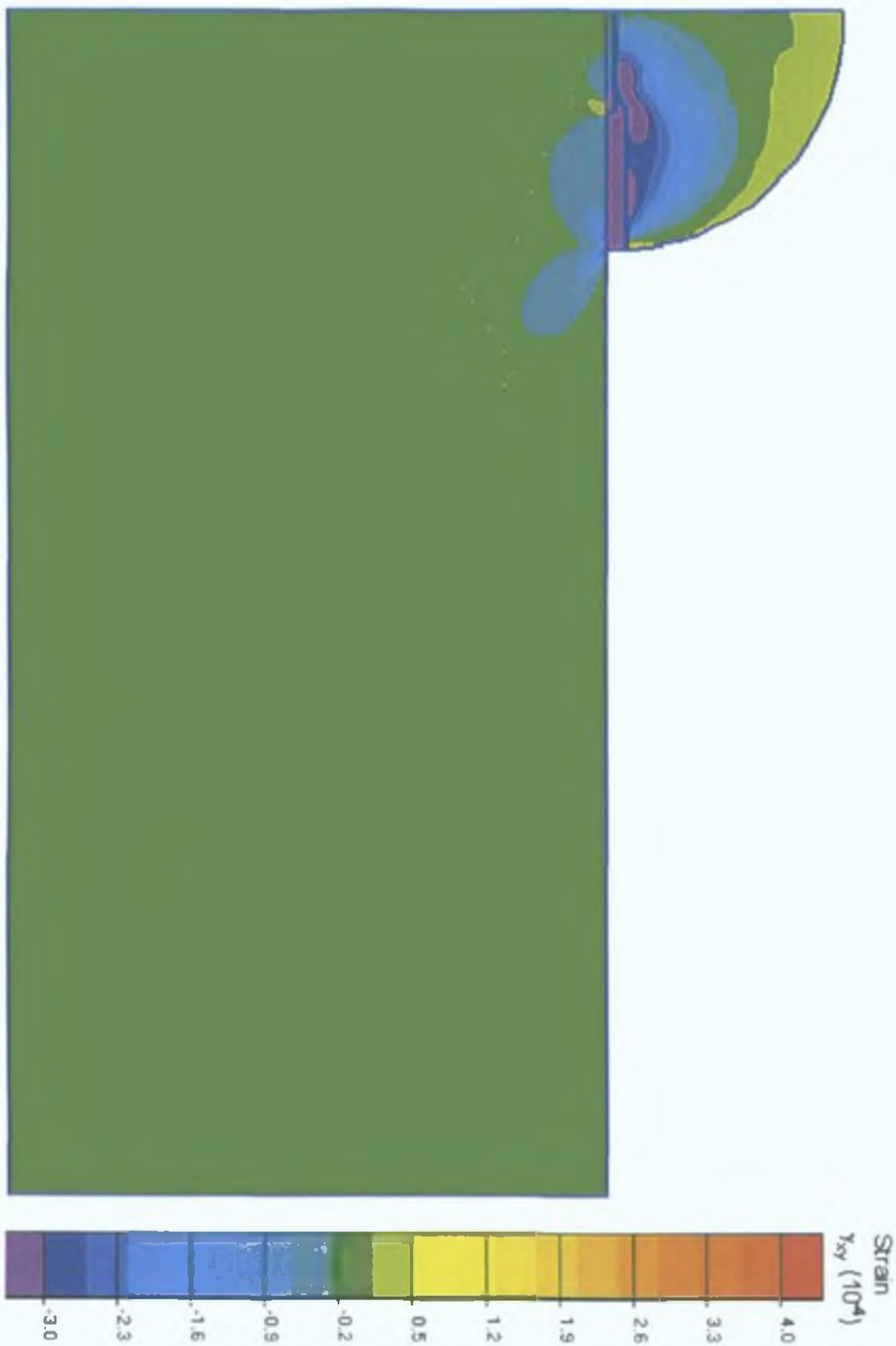


Figure 5-39 The shear strain (ϵ_{xy}) generated by the uniaxial loading model.

This relationship between strain fields obtained from FEM and from SXRT can be analysed by simulations of orientational and extinction contrast images in the SXRT using data from the FEM results.

In the case of the orientational contrast, the comparison can be done by matching the values and position of strains near the edge of the Pb/Sn bump. It is not complicated to compare this contrast. The matching result is portrayed in Figure 5-40.

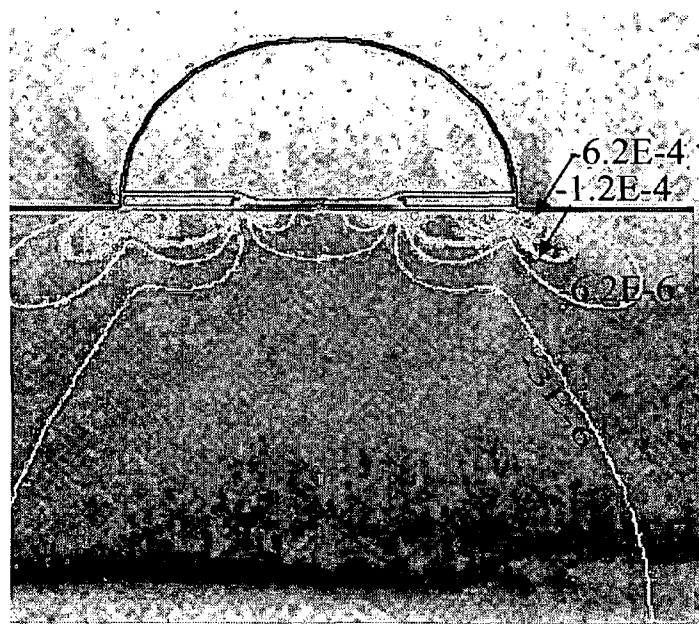


Figure 5-40 The BRST of the *post*-reflowed sample (Fig. 3-23(b)) and shear strain contours calculated using the FEM simulation.

A merged image of the back-reflection topograph and the shear strain simulation shows that the strain fields build up significantly at the periphery of the bump and cause a severe distortion of lattice planes around this edge. Since the values of $\Delta\theta_B$ corresponding to these enhanced values of shear strain, γ_{xy} , easily exceed the FWHM beam divergence; the orientational contrast is visible at the edge of the bump in the BRST image as illustrated in Figure 5-40. It is noted that the values in Figure 5-40 refer to the shear strain (γ_{xy}) contours.

However, in the case of the extinction contrast, the lattice displacements from FEM may be used for several simulation methods in SXRT. The simulated extinction contrast should match the contrast from the SXRT images. This study will be examined in Section 5.4.5 in this chapter.

5.4.3 Micro-Raman Spectroscopy Result and Discussions

As described in the experimental details section, the *Pre*- and *post*-reflowed process samples were cleaved near the middle of the Pb/Sn bumps and the normal stress (σ_{xx}) in the Si substrate was measured on the cleaved side using micro-Raman spectroscopy. The normal stress in MPa and the measured Raman shift (cm^{-1}) of the *Pre*-reflowed process sample for both X and X-Y mapping are shown in Figures 5-41 and 5-42, respectively.

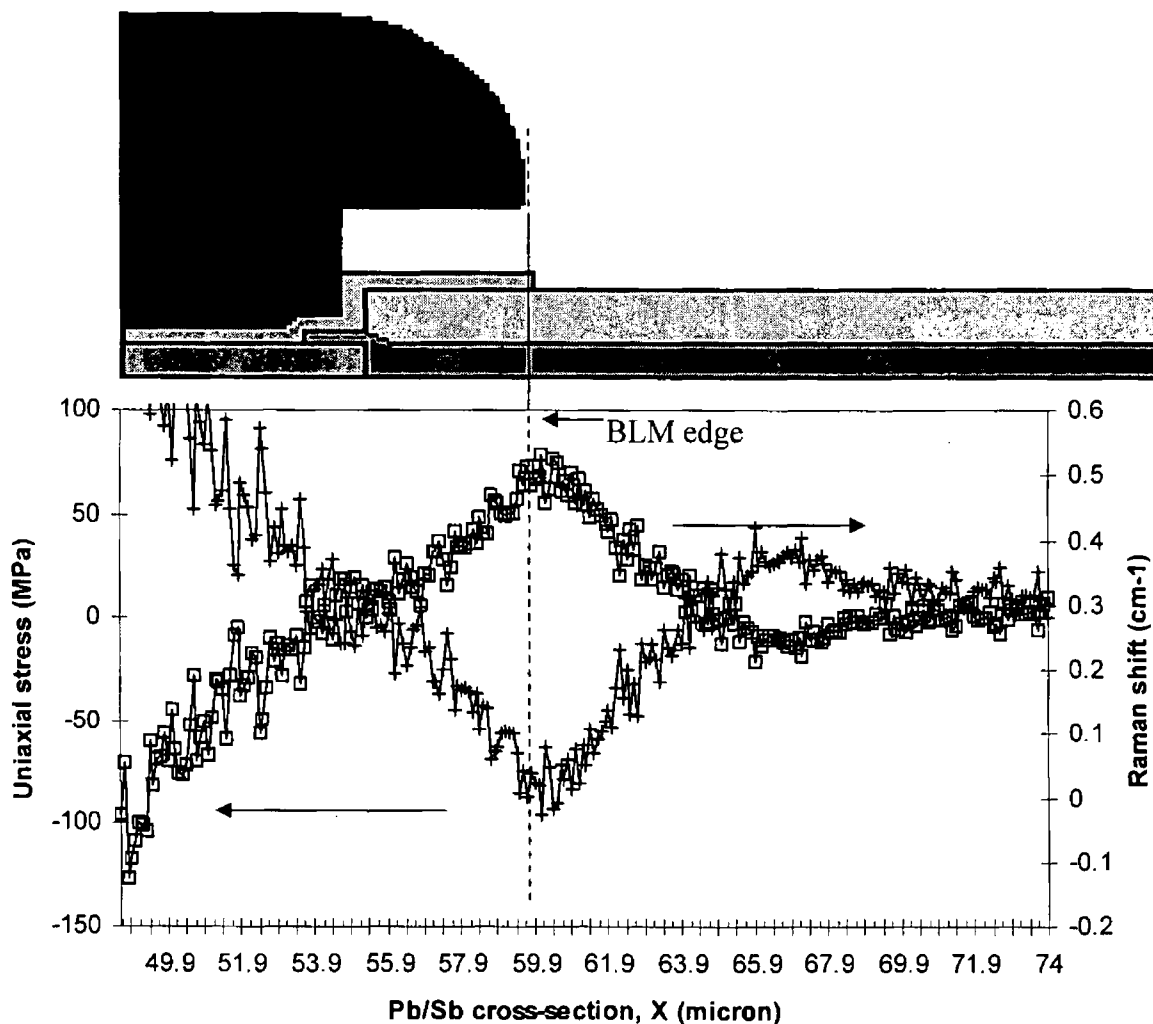


Figure 5-41 The normal stress (σ_{xx}) and the Raman shift (cm^{-1}) of the *Pre*- reflowed process sample (Ref#URS83a1).

In Fig. 5-41, the MRS result shows that the normal stress (σ_{xx}) in the Si substrate due to the Pb/Sn solder bump reflow process is in compression near the interface between the Si and the metal/passivation layers, both underneath and near the edge of the UBM layer. A maximum compressive stress of about 220 MPa was found near the edge of the Pb/Sn bump due to the Pb/Sn, UBM layer and passivation depositions.

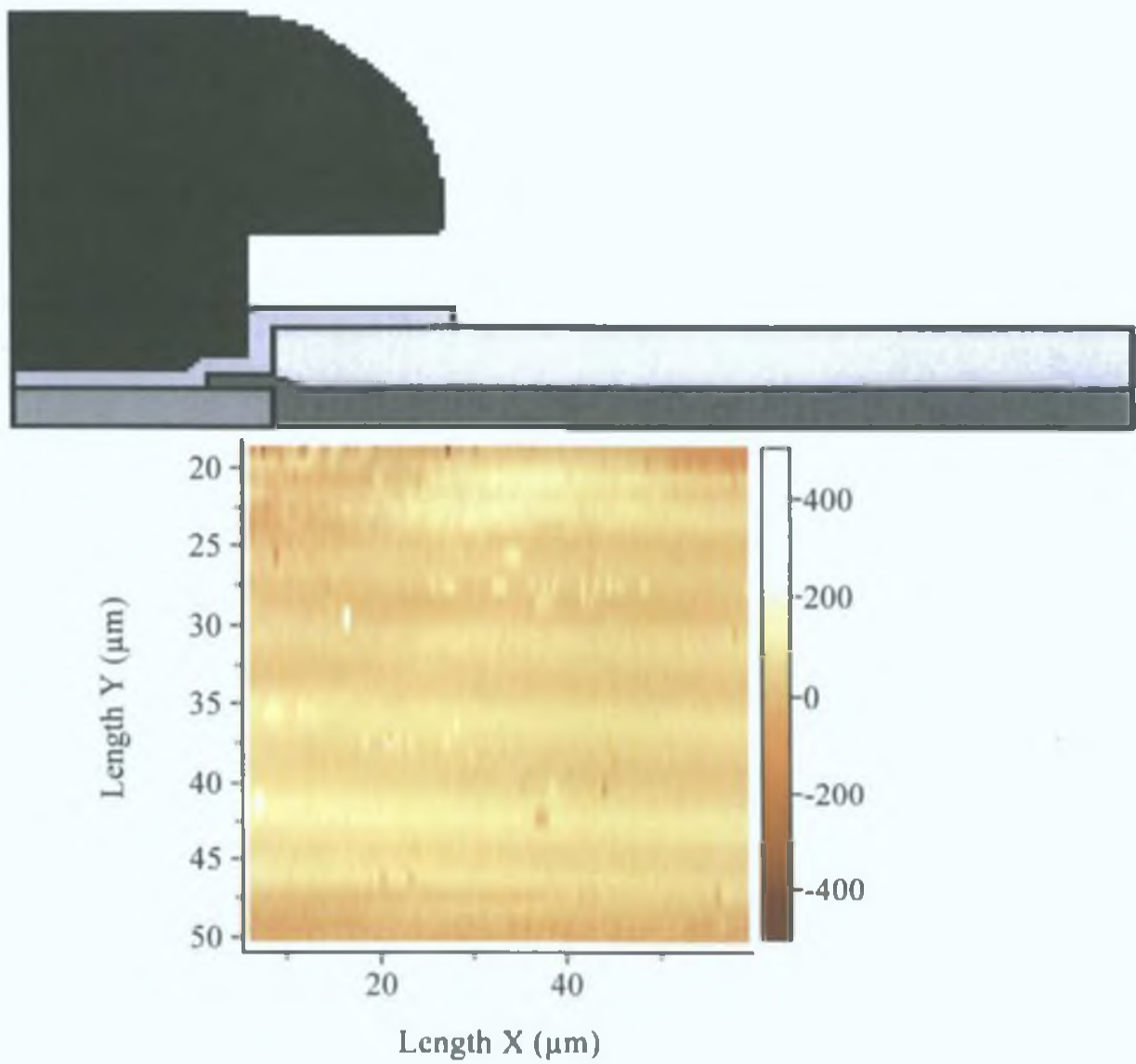


Figure 5-42 The 2-D uniaxial stress of the *Pre*-reflowed process sample. Note that the negative sign and positive sign refer to compressive and tensile stresses, respectively (Ref#URS90b).

For the X-Y mapping (Fig. 5-42), Y is the distance from the interface between the Si and metal/passivation layers down to the backside of wafer. Similar to the line (X) mapping result, the compressive stress builds up in the Si substrate underneath the Pb/Sn bump due to the Pb/Sn bump and the other metal processes. The stresses are reasonably uniform throughout the remainder of the sampled Si.

The X and X-Y Raman mapping data of the *post*-reflowed process sample are illustrated in Figure 5-43 and 5-44, respectively.

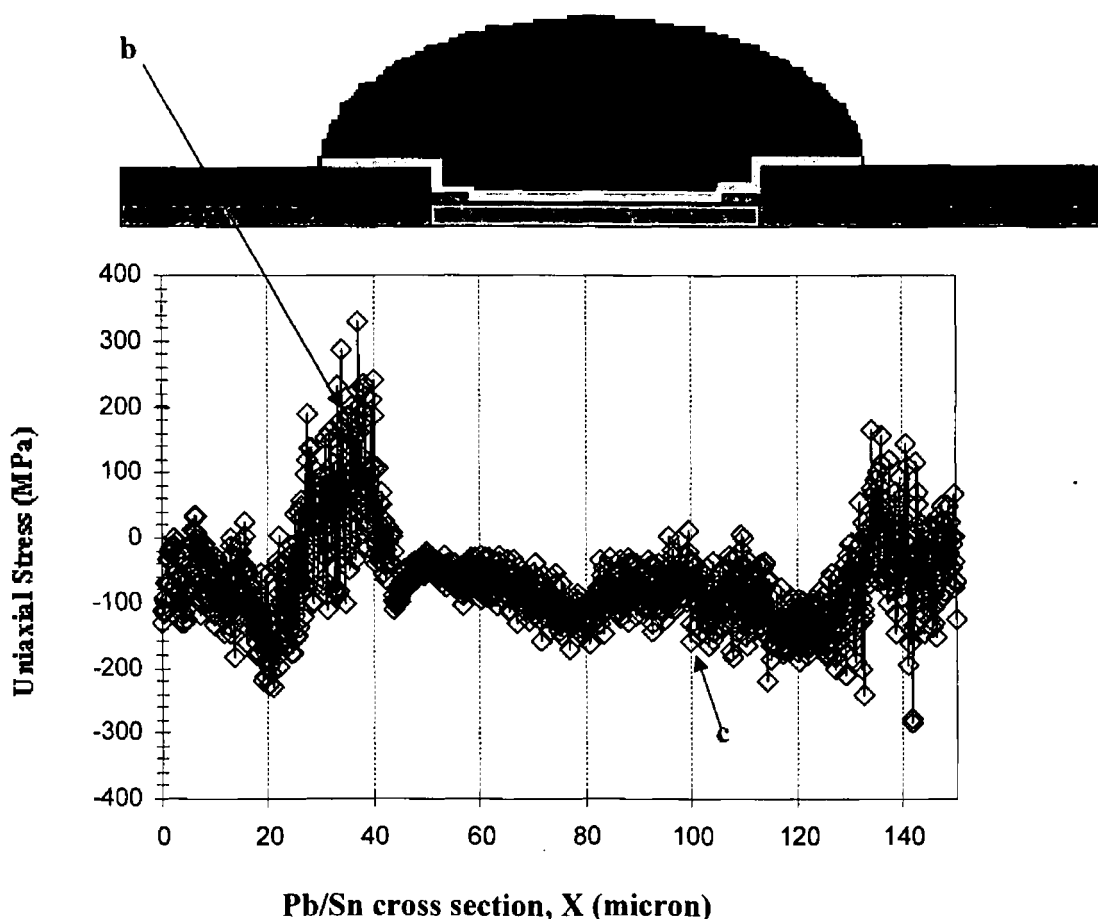


Figure 5-43 The Raman shift and calculated uniaxial stress in the *post*-reflowed process sample along the Pb/Sn bump cross-section (X direction) (Ref#URS81a1).

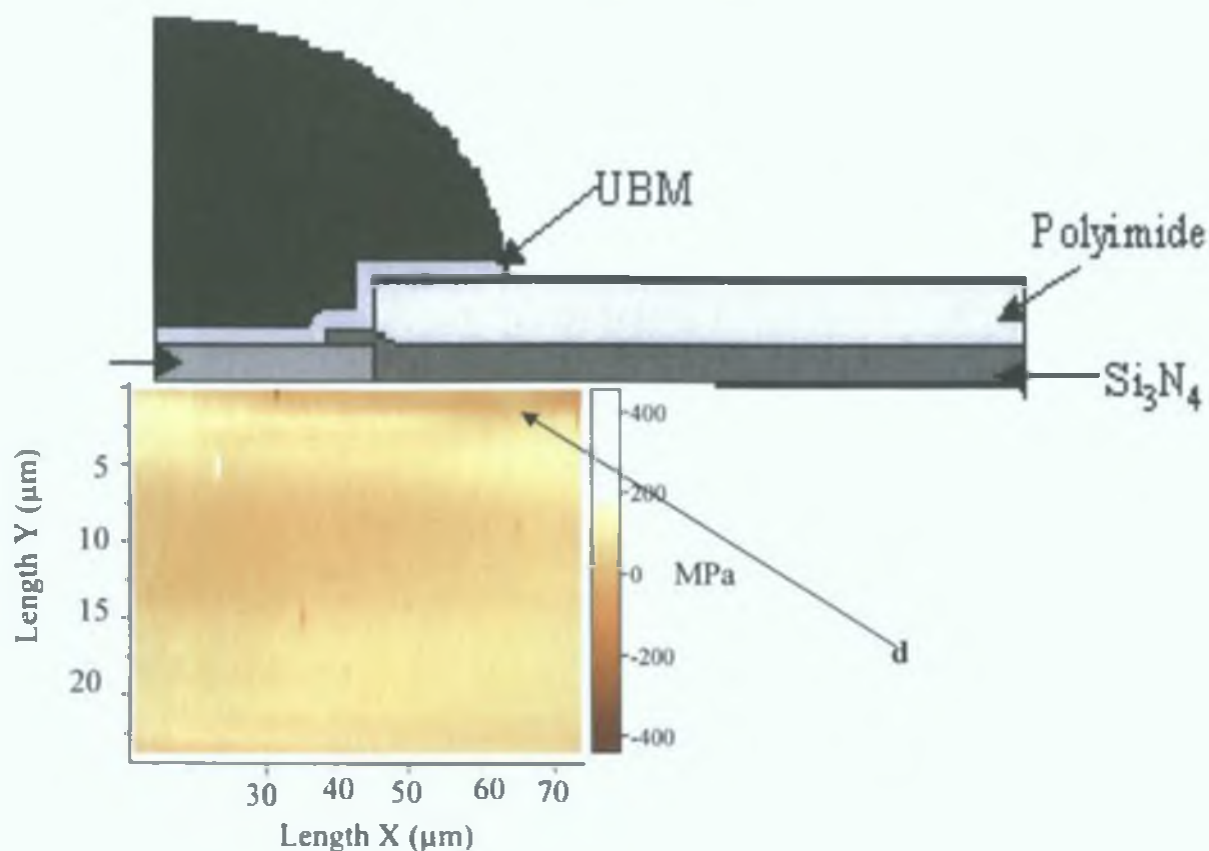


Figure 5-44 The X-Y Raman mapping (2-D) of uniaxial stress in the *post*-reflowed process sample (Ref# URS91a1).

The line (X) mapping result for the *post*-reflowed process sample (Fig. 5-43) shows that the Si at the interface with the metal/passivation layers near the edge of the Pb/Sn bump is in tensile stress with a maximum magnitude of about 250 MPa as indicated by Arrow b. The Si directly underneath the Pb/Sn bump is under compressive stress with a maximum magnitude of ~100 MPa (Arrow c). This correlates well with the X-Y mapping data near the interface of the Si-metal layers

wafer between *Pre*- and *post*-reflowed samples (Fig. 5-41 and 5-43) indicates that the stress in the Si wafer near the edge of the Pb/Sn bump changes from compressive to tensile with a uniaxial stress maximum of 250 MPa. Two explanations for of this occurrence could be (1) the Pb/Sn solder attached to the UBM/passivation layers becomes ball shaped after the reflow process (therefore, the thermal stress due to the CTE mismatch of the Pb/Sn solder, UBM and passivation layers can generate greater stress through the Si wafer near the edge of the Pb/Sn bump), and (2) a new intermetallic layer was generated during the reflow process, which correlates with the SXRT result (this intermetallic can be analysed using TEM/XRD measurement. The TEM result for this intermetallic layer will be described in the next section.

To compare the FEM and MRS results, the FEM data at the Si/metal interface was calculated back to an equivalent Raman shift using Eq. 5-1 and plotted along the X direction as illustrated in Figure 5-45.

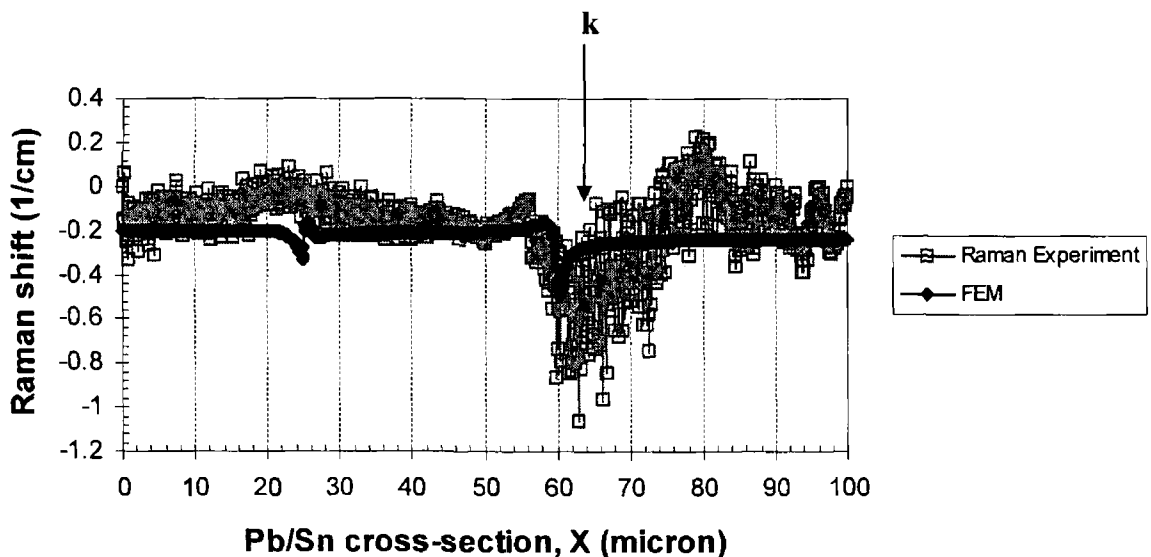


Figure 5-45 Comparison of the Raman shift (cm-1) between the micro-Raman experimental data and FEM data.

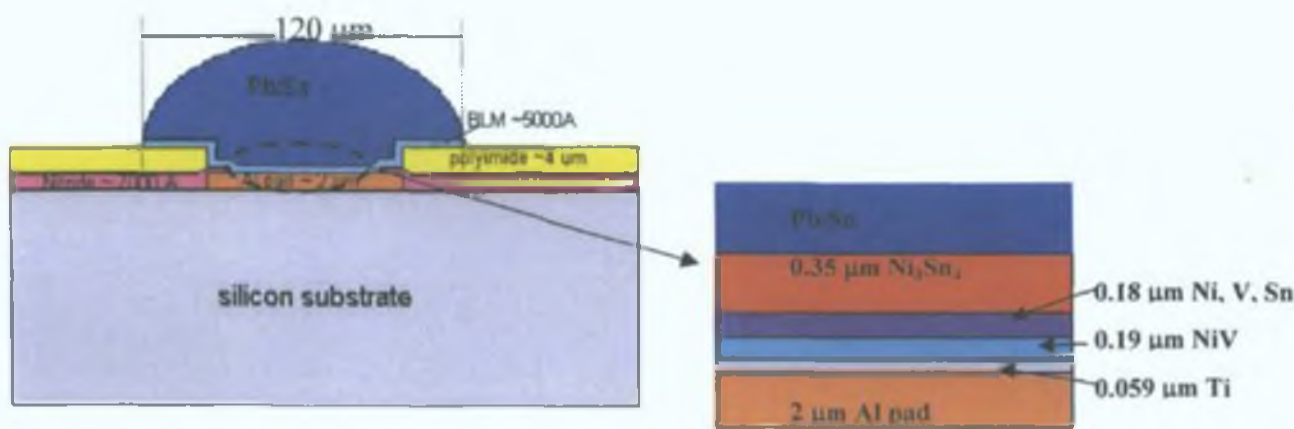
The MRS results and the FEM simulation illustrate that the tensile stress distributions in the Si wafer due to the reflow are of the same order (~ 200 -250 MPa, i.e. Raman shift $\Delta\omega \approx -0.6$) near the edge of Pb/Sn bump near arrow k. There is an

excellent correlation in the shape and distribution of the strain induced Raman shifts near the edge of the metal bump. To date the feature observed at $X \approx 25 \mu\text{m}$ has not been accounted for, but is most likely related to the Al pad/ Si_3N_4 interface.

5.4.4 X-Ray Diffraction (XRD) and Transmission Electron Microscopy (TEM) Intermetallic Analysis

XRD was used to investigate any intermetallic layers, which may be generated during the thermal processing of the flip-chip reflow process. Due to the high absorption of the Pb/Sn solder bump, the x-rays could not enter through the interface area between those metal layers. Therefore, the etched *post*-reflowed process sample (wafer no. 225, *post*-reflowed sample, etched back) was used in this study. SXRT of this wafer was also illustrated earlier wherein we speculated on the generation of a strain field imposed in the Si wafer due to intermetallic layers. The measurement was performed using a Philips X'Pert PRO X-ray diffractometer with a PW3040 generator (mppc) and a PW3050/65 goniometer. However, the XRD result revealed only Ti compounds.

Nevertheless, Intel has investigated the intermetallic layer using Transmission Electron Microscopy (TEM) [139]. It was found that a new intermetallic layer of Ni_3Sn_4 was created during the reflow process. The layer structure of the *post*-reflowed sample analysed by TEM is as follows [139].



5.4.5 An Analysis of BRST of *Post-Reflowed Process Samples*

As mentioned in Chapter 2, the XRT image is generated from two different kinds of contrast mechanisms, i.e. orientational and extinction contrast. A simulation of the BRST for the *post-reflowed process sample* for both contrast mechanisms will be described, in order to determine the major contrast mechanisms in these topographs. A BRST image of the *post-reflowed process sample* (15 minutes etching time) in Fig. 5-23 was chosen to perform the simulation in this study. The image is shown again Fig. 5-46. Again, the orientational contrast is indicated by Arrows **g** in Fig. 5-46. The geometry and dimensions are as in Figure 5-36.

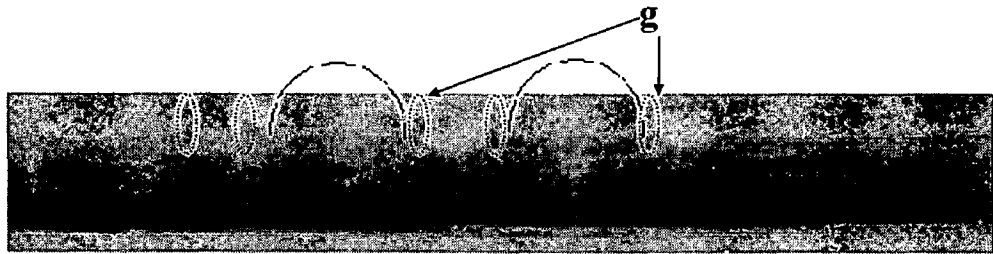


Figure 5-46 BRST image of the *post-reflowed process sample* as a simulating prototype.

5.4.5.1 An Analysis of the extinction contrast

Several scientists have attempted to simulate the extinction contrast of section topographs for both transmission and back-reflection geometries. This study simulates the BRST image using a lattice displacement (\mathbf{H}_i) obtained from the FEM simulation as illustrated earlier in this chapter with several methods suggested as follows;

- a. a plot of $\mathbf{g} \cdot \mathbf{H}$ using the Meieran and Blech methodology [107]
- b. a plot of $\cos(\mathbf{g} \cdot \mathbf{H})$ as per Howard and Schwuttke [113]
- c. a plot of strain gradient in terms of effective misorientation in reciprocal space [98].

To simulate the extinction contrast of the BRST of the *post*-reflowed sample in Fig. 5-46, the impact of a complete bump is considered in this study. Figure 5-47 is taken from the BRST image in Fig. 5-46. All simulated images will be compared to this image.

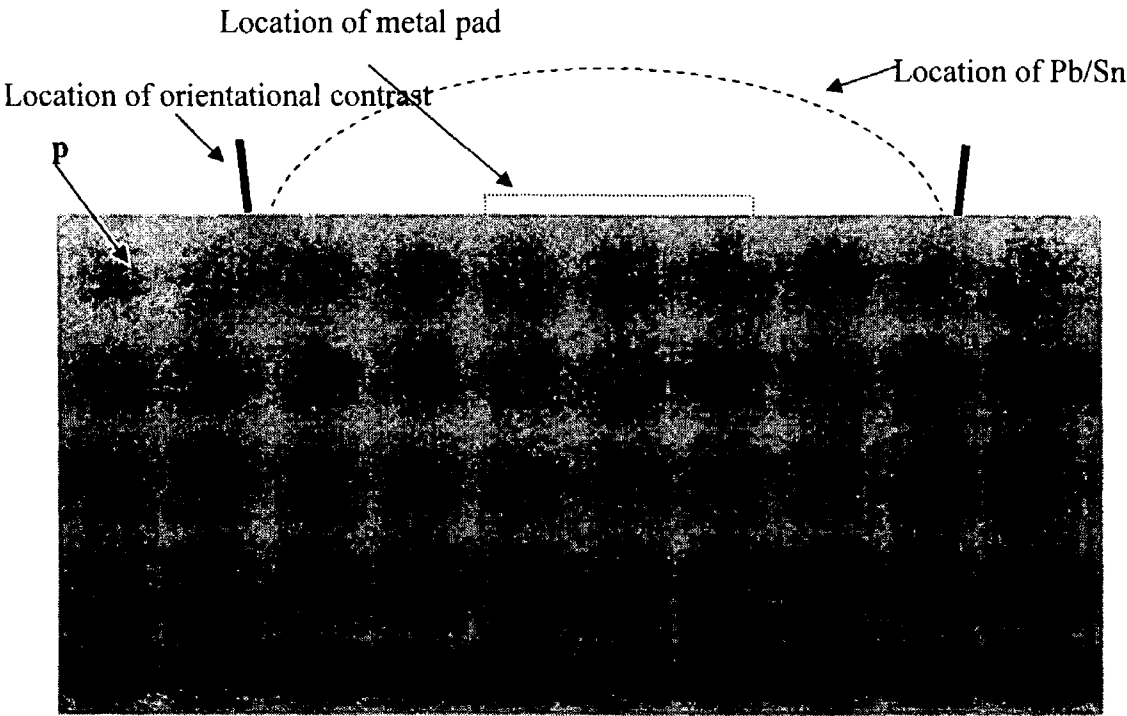


Figure 5-47 A part of the BRST image of the *post*-reflowed process sample (Fig. 5-46).

It is noted that a white region **p** occurs possibly due to the orientational contrast phenomenon, which has been explained earlier in this chapter. It could be possible that the lattice planes in that area are severely distorted leading to the misorientational lifted image region near the edge of the Pb/Sn bump. Therefore, this white contrast from the orientational contrast (Arrows **p**) should not be taken into account during the simulation of the extinction contrast.

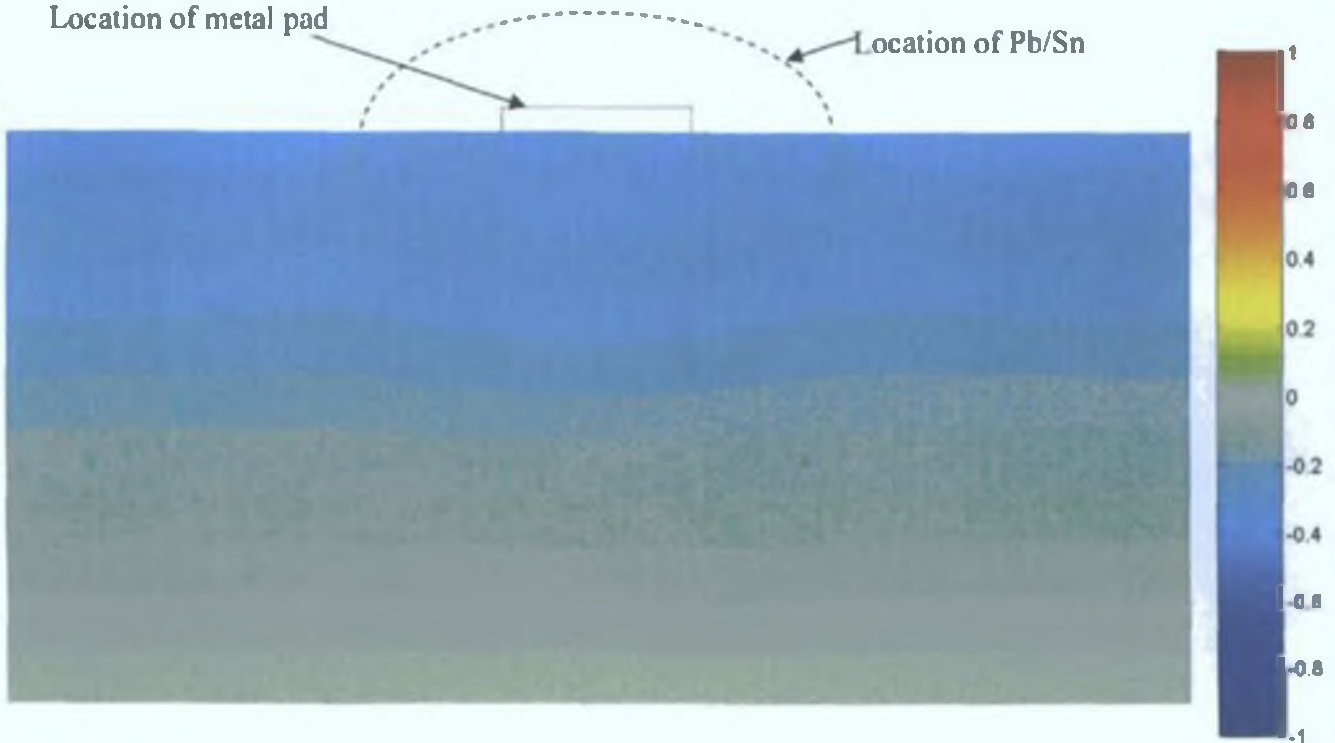
(a) A plot of $\mathbf{g} \cdot \mathbf{H}$ using the Meieran and Blech Method.

Meieran and Blech [107]-[110] showed that the diffracted intensity (I) recorded at a constant $2\theta_B$ can be related to the value of $\mathbf{g} \cdot \mathbf{H}$, where \mathbf{g} = the diffraction vector and \mathbf{H} = the Si lattice distortion. The relationship between the dot product value and the extinction phenomenon was explained in Chapter 2. However, Meieran and Blech used this theory to confirm the relationship only at the edge of metal and oxide lines [108].

In this study, this relationship was extended to simulate the strain gradient in Si due to the Pb/Sn bump reflow process. The relationship between the diffracted intensity and the $\mathbf{g} \cdot \mathbf{H}$ calculation, where \mathbf{g} is the diffraction vector, which is $\bar{3} \bar{3} 9$ in this case, and \mathbf{H} is the lattice displacement, obtained from the FEM simulation at any given point. The matrix of the $\mathbf{g} \cdot \mathbf{H}$ values is plotted in terms of the black and white contrast, which is related to their nominal values, e.g. white contrast appears when $\mathbf{g} \cdot \mathbf{H} < 0$, and black contrast appears when $\mathbf{g} \cdot \mathbf{H} > 0$. However, colour was used in these plots as is clearly seen in this report, i.e. blue represents white contrast and red represents black contrast. A simulation of the $\mathbf{g} \cdot \mathbf{H}$ calculations are illustrated in Figure 5-48(a) and (b).



(a)



(b)

Figure 5-48 The simulation of $g \cdot H$ using the Meieran and Blech model: (a) Black and white contrast, and (b) Blue and red colours represent white and black contrasts, respectively.

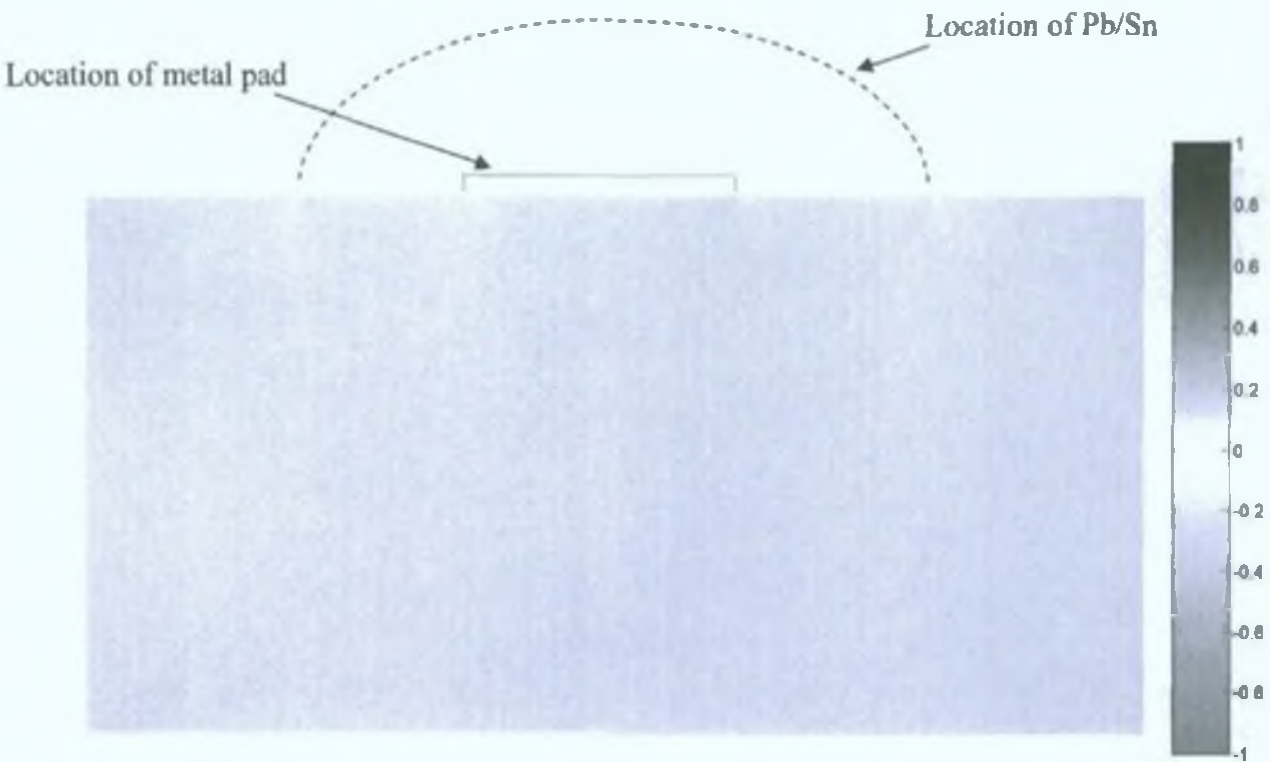
The BRST simulation in Fig. 5-48 shows that the strain fields near the top surface and the two most highly strained regions, i.e. near the Pb/Sn bump edge and the metal pad edge, are observed. The simulation image of the $\mathbf{g} \cdot \mathbf{H}$ calculation (Fig. 5-48) shows that the image intensity near the Pb/Sn bump is quite similar to the BRST image in Fig. 5-47. However, the strain fields due to the metal pad are visible in the simulation image (Fig. 5-48), but could not be observed in the BRST image (Fig. 5-47). This simulation suggests that the extinction contrast, based on the $\mathbf{g} \cdot \mathbf{H}$ calculation, is not a major influence on this BRST image.

(b) A plot of $\cos(\mathbf{g} \cdot \mathbf{H})$ as per Howard and Schwuttke [113]

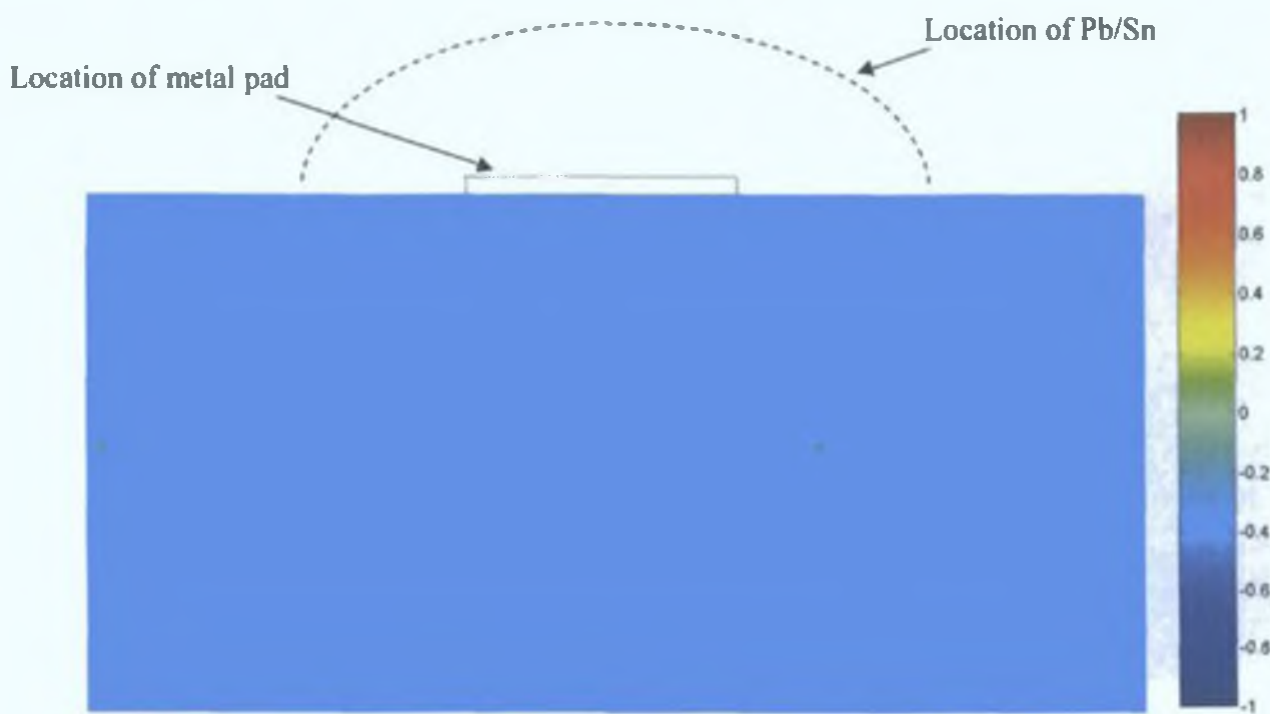
Howard and Schwuttke studied the relationship between strain gradients and the extinction contrast on oxide triangles on Si wafers. A compressive film generates a tensile stress at the substrate/film interface since the thermal coefficient of expansion (CTE, α) of Si is higher than its oxide ($\alpha_{\text{Si}} > \alpha_{\text{SiO}_2}$). In addition, it was discovered that the relative intensity at the oxide edges in the topograph varied with the sign and magnitude of $\cos(\mathbf{g} \cdot \mathbf{H})$. The relationship is illustrated as follows:

- (a) A negative sign implies the existence of a weak contrast region between black and white contrasts, called gray contrast. The maximum of gray is found when $\cos(\mathbf{g} \cdot \mathbf{H}) = -1$,
- (b) A positive sign indicates a strong black contrast. The maximum black contrast is observed when $\cos(\mathbf{g} \cdot \mathbf{H}) = 1$,
- (c) A white contrast is visible in the topograph if $\cos(\mathbf{g} \cdot \mathbf{H}) = 0$.

This relationship was modified for use in the simulation of the BRST image by calculating $\cos(\mathbf{g} \cdot \mathbf{H})$, where \mathbf{g} is $\frac{1}{3} \frac{1}{3} \frac{1}{9}$ in this case and \mathbf{H} is the lattice displacement, obtained from the FEM simulation at any given point. The values of $\cos(\mathbf{g} \cdot \mathbf{H})$ were plotted on a gray scale between white to black colour which is between -1 to 1 of $\cos(\mathbf{g} \cdot \mathbf{H})$. The BRST simulation by the $\cos(\mathbf{g} \cdot \mathbf{H})$ calculation is depicted in Figure 5-49.



(a)



(b)

Figure 5-49 The BRST simulation of the $\cos(\mathbf{g} \cdot \mathbf{H})$ calculation: (a) black and white scale, and (b) colour scale represents the black and white image.

The black-white contrast range is not easily seen in this report. The colour scale is a better representation of the black-white contrast, wherein red and green colours represent black and white contrasts, respectively.

The simulation in Fig 5-49 shows that the strain fields in the Si wafer build up at the Si/metal interface near the edges of the Pb/Sn bump and near the metal pad and the strongest black contrast is introduced in the middle of the Si underneath the Pb/Sn bump. This simulation seems to disagree with the BRST image Fig. 5-47.

(c) A plot of strain gradient in terms of effective misorientation in reciprocal space

This method is a traditional simulation of the section topograph for both BRT and LAT techniques. It is based on the dynamical diffraction theory for a deformed crystal as defined by Authier [98], which was given in Chapter 2. The strain gradient at any given point in the Si is calculated using Eq. 5-5 [98] and is plotted as shown in Figure 5-49.

$$\frac{\partial[\delta\theta(\mathbf{r})]}{\partial\mathbf{s}_0} = \frac{1}{g \cos\theta_B} \frac{\partial^2}{\partial\mathbf{s}_0\partial\mathbf{s}_g} [\mathbf{g} \cdot \mathbf{h}(\mathbf{r})] \quad \text{Eq. 5- 6}$$

where $\delta\theta(\mathbf{r})$ is the effective misorientation, \mathbf{g} is the diffraction vector, which is $\bar{3} \bar{3} 9$ in this case, $\mathbf{h}(\mathbf{r})$ is the lattice displacement which is obtained from the FEM simulation, and \mathbf{s}_0 and \mathbf{s}_h are the directions of the forward diffracted and diffracted beams, respectively.

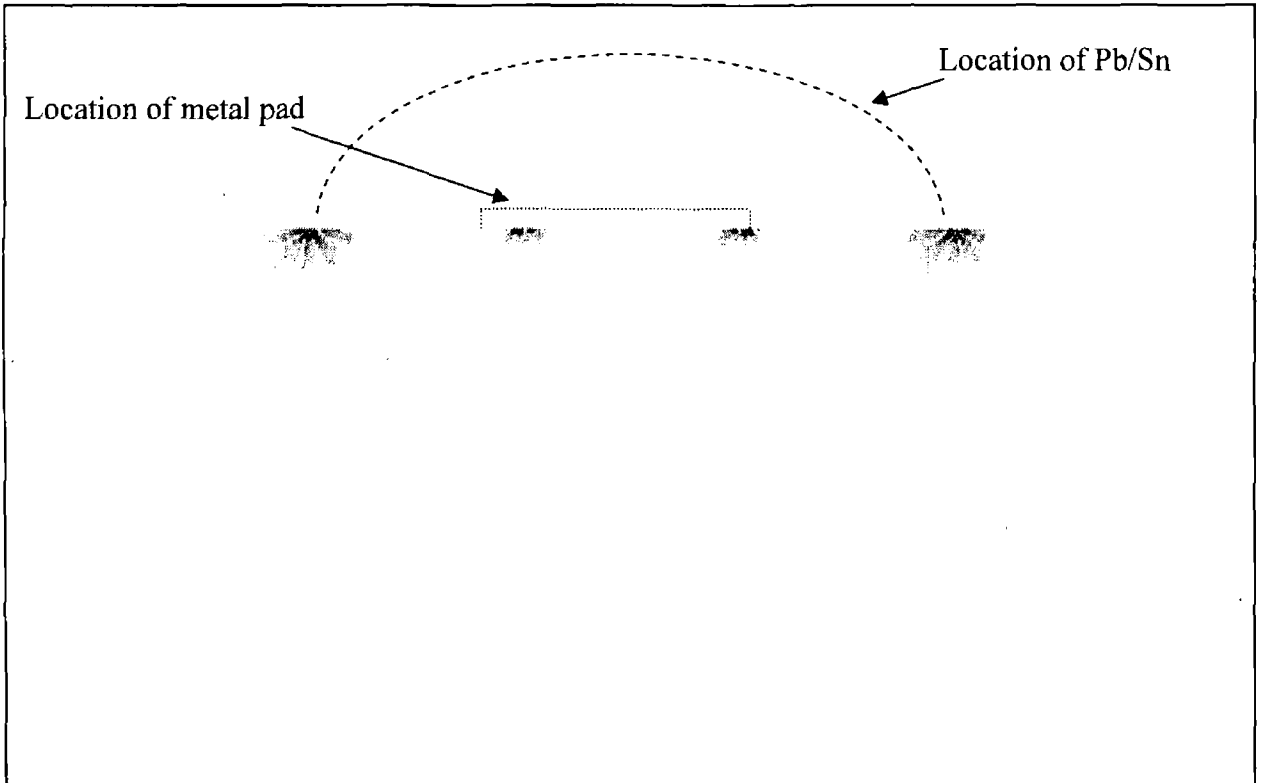


Figure 5-50 The plot of the strain gradients in terms of the effective misorientation in the reciprocal lattice.

Figure 5-50 shows clearly that the simulation of the extinction contrast using the strain gradients calculated with the dynamical diffraction theory disagrees totally with the experimental BRST image.

None of the simulations of the extinction contrast using both kinematical and dynamical diffraction theories is perfectly matched to the experimental BRST image. This implies that the strain gradients in Si due to the reflow process presented in the experimental BRST image do not manifest themselves predominantly via the extinction contrast mechanism.

5.4.5.2 An Analysis of the orientational contrast

To understand the impact of the stress on the Si substrate due to thermal processing, a simulation of the orientational contrast in the back-reflection section topographic image is created. The simulation of the orientational contrast in the BRST of the *post-reflowed* process sample is based on the calculation of Rantamäki [106]. In this case, the kinematical theory is used to correlate the orientational contrast in section topographs with the degree of distortion of the lattice planes. It is assumed that the BRST is influenced by the orientational contrast only. Figure 5-51 shows contours of clear orientational contrast (solid line) in the Si substrate due to the Pb/Sn bump reflow process. The region indicated by Arrow **g** is an orientational contrast region due to severe distortion of the lattice plane.

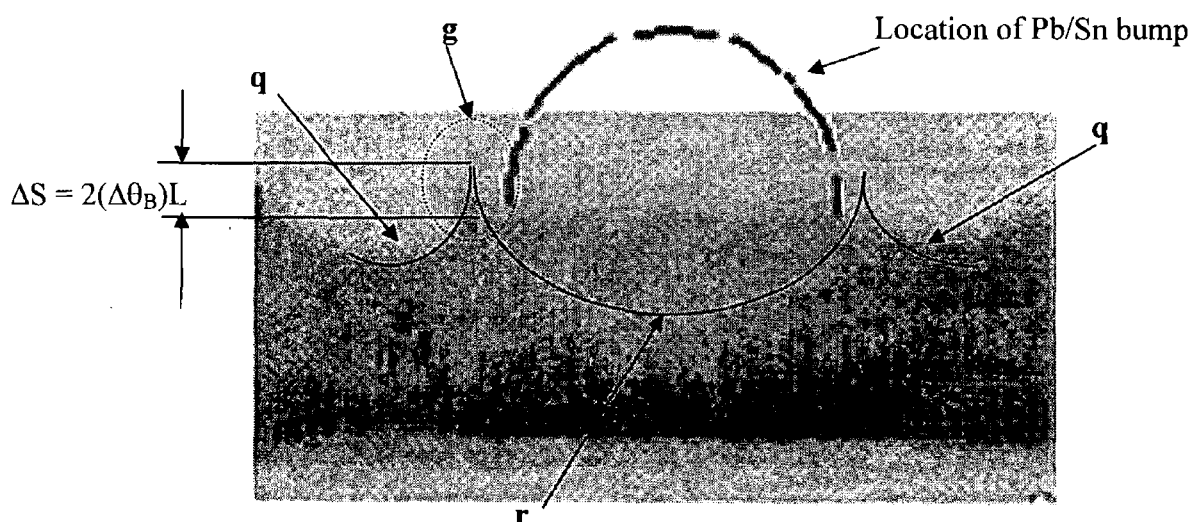


Figure 5-51 The BRST image of the post-reflowed process sample. The lines represent possible contours of clearly identifiable orientational contrast. Arrows **q** and **r** are orientational contrast contours/features outside the Pb/Sn bump and underneath the Pb/Sn bump, respectively.

The simulation of the orientation contrast in this study is based on the dimension of the sample as illustrated in Figure 5-52. T is the sample thickness = $150\text{ }\mu\text{m}$, t_i is the depth from the back surface at which the lattice planes start distorting. x is the coordinate direction from the middle of the Si underneath the Pb/Sn bump and $\Delta\theta(x)$ defines the misorientation of the lattice plane with respect to the (001) plane.

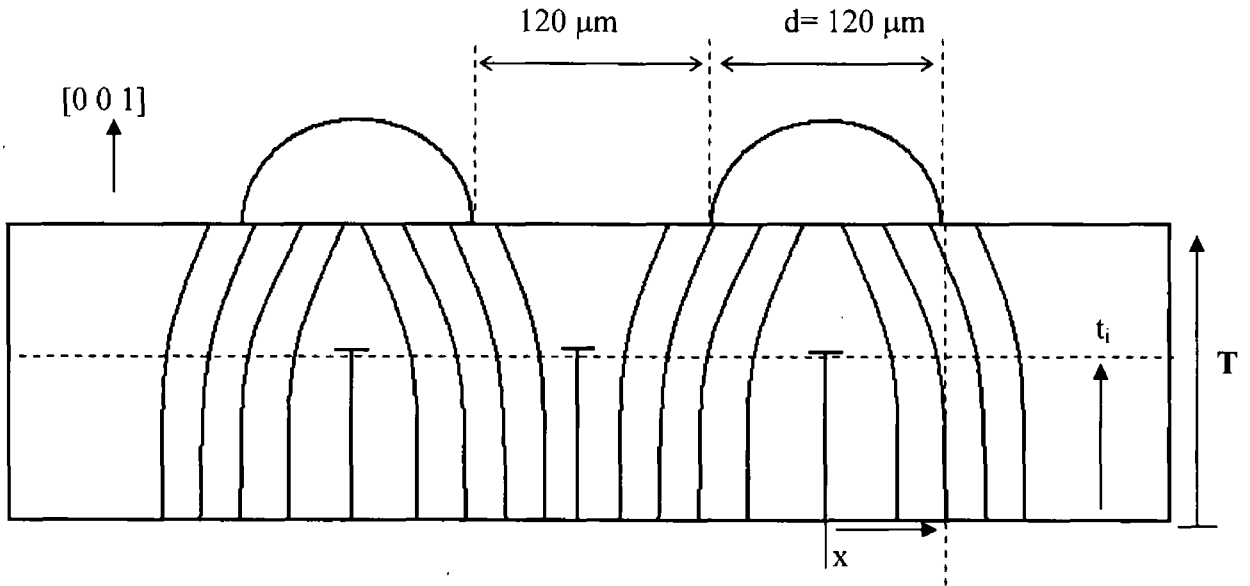


Figure 5-52 The dimensions of the Pb/Sn sample.

In this study, the calculation and simulation method is modified from the theory in [106], which defines each misorientation ($\Delta\theta$) of the (001) plane as a function of its position x via $\Delta\theta(x)$. Therefore, the (001) plane at any given point i is rotated by $\Delta\theta_i$. To simulate the orientational contrast, the direction and orientation are defined as given in Figure 5-53.

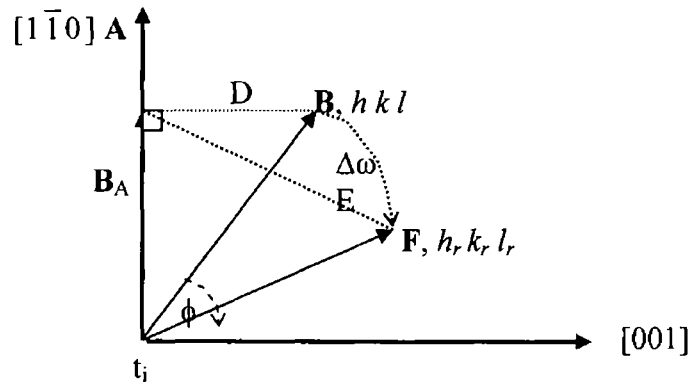


Figure 5-53 The direction and orientation of the lattice plane for the orientational simulation.

It is assumed that A is in the $[1\bar{1}0]$ direction and B is the direction of the normal of the reflecting plane $(h\ k\ l)$, which is the $[\bar{3}\ \bar{3}\ 9]$ direction in this simulation; B_A is a projection of B on A and $\Delta\omega$ is the tilt of the lattice plane around an axis parallel to A . Thus, F is the direction of the distorted lattice plane $(h_r\ k_r\ l_r)$. The misorientation $\Delta\theta(x)$ of the $\bar{3}\ \bar{3}\ 9$ plane with respect to the (001) plane from the BRST of the post-reflowed process sample due to the reflow process is calculated and shown in Equation 5-7.

$$\Delta\theta(x) = \frac{1}{T} \cosh(2|x|) \quad \text{for lattice plane underneath the Pb/Sn bump,}$$

and

Eq. 5- 7

$$\Delta\theta(x) = \frac{1}{T} \cosh 2(d - |x|); |x| = d/2 \quad \text{for the lattice planes outside the Pb/Sn bump.}$$

The simulation of the orientational contrast calculated from Eq. 5-7 is illustrated in Figure 5-54. The image is similar to the main contrast distortion features in the BRST image from the experiment (Fig. 5-51).

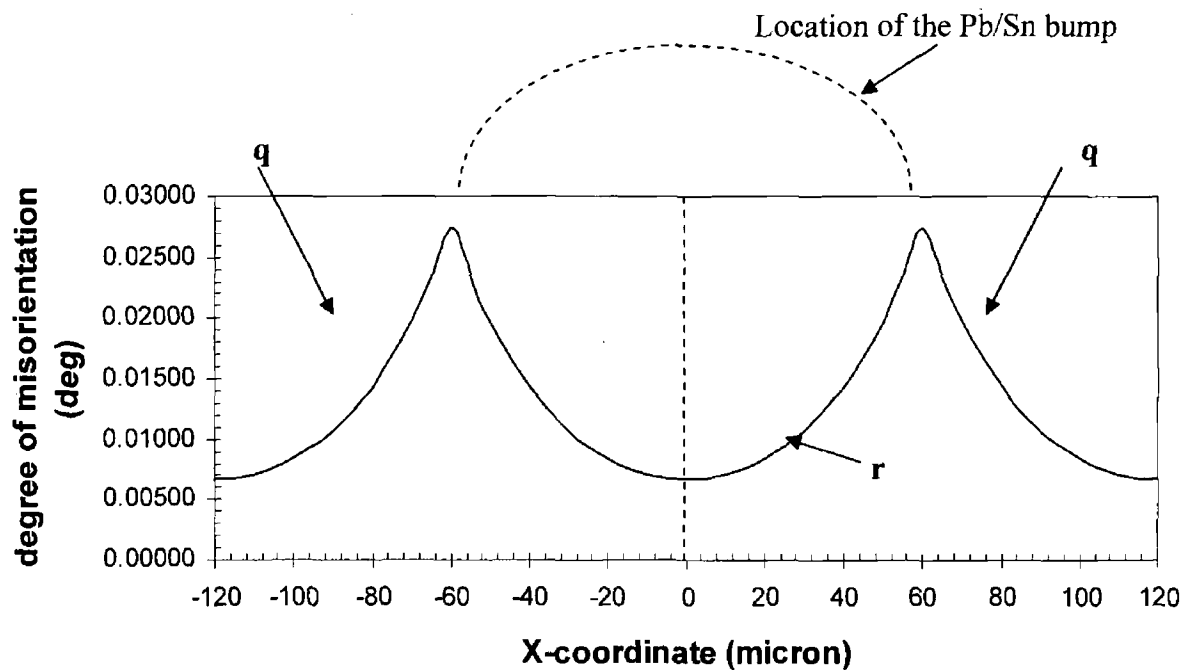


Figure 5-54 The simulation of the principal orientational contrast distortional features in the BRST image of the *post*-reflowed sample.

For the situation examined above, XRD cannot examine the angle of the lattice distortion due to the absorption by the Pb material. However, the lattice displacement can be obtained from the FEM results, which allows one to estimate the expected lattice distortion of the Si ($\bar{3}\bar{3}9$) planes. The degree of misorientation $\Delta\theta(x)$ obtained from the FEM simulation is illustrated in Figure 5-55. The figure shows high lattice distortion in regions close the edge of the metal pad (Arrow s) and the edge of the Pb/Sn bump (Arrow u). However, the misorientation near the metal pad was not visible in the BRST image as mentioned above in this chapter. Therefore, the misorientation near the edge of the Pb/Sn bump is considered as the maximum misorientation.

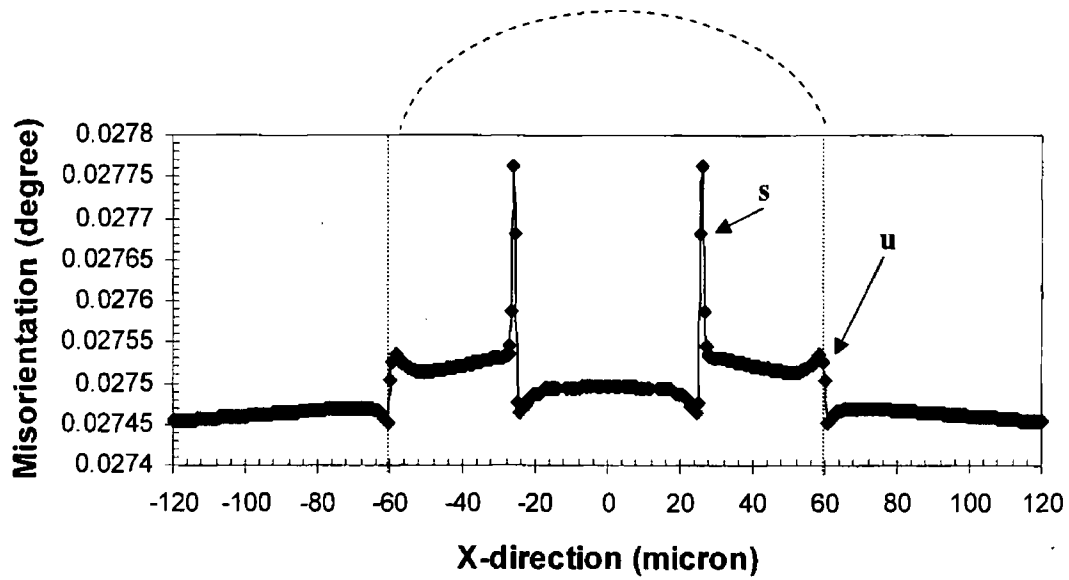


Figure 5-55 A calculation, based on the FEM simulation, of the misorientation $\Delta\theta(x)$ of the $\bar{3}\bar{3}9$ planes in the Si substrate of the *post*-reflowed process sample due to the reflow process.

A plot of the misorientation of the $(\bar{3}\bar{3}9)$ lattice planes to the edge of the Pb/Sn bump is also calculated from the FEM simulations and is depicted in Figure 5-56. The lattice distortion is shown only at the edge of the bump since it gives the maximum degree of misorientation, $\Delta\theta_{\max}$.

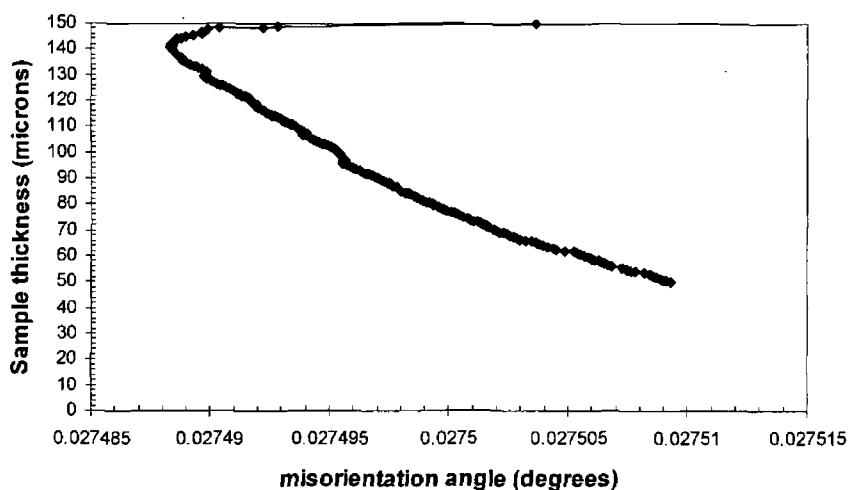


Figure 5-56 The misorientation of the $(\bar{3} \bar{3} 9)$ Si lattice plane at the edge of the Pb/Sn bump ($X = 60 \mu\text{m}$), as a function of depth into the Si, due to the reflow process.

From Fig. 5-56, it appears that the most severe distortion of the lattice planes occurs near the Si/metal layer interface where $T = 140\text{-}150 \mu\text{m}$. This $\Delta\theta_{\text{max}}$ of about 0.027° (0.4 mrad) is larger than the beam divergence ($\approx 0.0238 \text{ mrad}$). Therefore, this is the prime candidate for the upward orientational contrast streak near the edge of the Pb/Sn bump in the experimental BRST image (Fig. 5-51).

5.5 Conclusions

The stress distributions in Si substrates due to the reflow process and UBM etching times were observed using synchrotron x-ray topography. It was found that after the reflow process, the x-ray topographic extinction and orientational contrasts were greater in areal dimension. In addition, a shear stress magnitude of the order of 100 MPa was observed via orientational contrast. These were attributed to the elevated temperatures used in the reflow process. After the removal of the Pb/Sn bumps, the orientational contrast due to the severe strain fields could not be observed in the topographs. This confirmed that the reflow process was one of the major sources of strain fields in the Si substrate. In addition, the shear strains simulated from FEM as well as the uniaxial stress data from MRS show similar results with respect to the SXRT measurements.

It is also found that after the reflow process, when the UBM etching time was increased from 15 to 25 minutes, the stress distributions in the Si substrates were visible via x-ray topography and were of the order of magnitude of 100 MPa. However, for the 30 minutes etching time, no orientational contrast was observed in the BRST image. This suggests that the strain fields in Si substrate are now smaller and this could be due to the residual UBM layer and some passivation layers being etched off the sample.

The XRD measurements were performed on the etched back, *post*-reflowed process sample and the compounds between Ni and Ti were visible. This confirmed that the stress imposed on the Si substrate represented by the orientational contrast in Figure 5-31(c) is generated from the Ni and Ti in UBM layer. TEM revealed that several Ni, Sn and V compounds were found at the UBM/solder bump interface. Ni_3Sn_4 is a major intermetallic phase after the reflow process and this new intermetallic compound could be a major strain source in the Si substrate. Thus, it can be concluded that the major sources of the strain field after the reflow process are the

Pb/Sn material which covered the UBM layer after reflow and the intermetallic materials which are generated during the elevated temperature steps.

MRS result showed that the uniaxial stress (σ_{xx}) changed from compressive stress of 100 MPa to tensile stress of 300 MPa after the reflow process. The σ_{xx} of the FEM data were calculated back to Raman shift and compared to the MRS data. It is found that the FEM result correlates well with the MRS result.

An examination of possible contrast mechanisms was carried out on the BRST images of the *post*-reflowed process sample using both kinematical and dynamical theories to understand the lattice plane behaviour. It is found that the extinction contrast is not a major influence in the BRST image. On the other hand, the simulation of the orientational contrast exhibited that the lattice distortion calculated from the topograph corresponded to that calculated from the FEM result and the simulation could explain the Si lattice plane distortion after the elevated temperature of the flip-chip reflow process.

CHAPTER 6 COPPER METALLIZATION PROCESS

INDUCED STRESS IN SILICON SUBSTRATES USED IN IC PROCESSING

Since the 1960s, the use of semiconductor devices increased significantly as a result of improvements in terms of miniaturization (more devices packed on the die), better performance (higher speed), higher functionality in the chip and low effective costs. This is partly a result of the improvements in materials processing such as device insulators and metals. Basically, the material which is selected to be the metal interconnect should have low resistivity and a low temperature coefficient of resistance. In addition, the metal should be easy to deposit on a planar surface with a high deposition rate, be easy to etch and planarize, be oxidation and corrosion resistant, (i.e. low chemical reactivity), be mechanically stable, (i.e. low stress and high stress migration resistance), possess a high melting point for high electromigration resistance, be compatible with encompassing materials, be environmentally safe material during processing and use, and be reliable and cheap [144].

6.1 Copper Metallisation in IC Processing

Many researchers have studied the metal materials to replace the aluminium (Al) alloy metallisation in IC devices. Copper is poised to take over as the main on-chip metal for many IC applications due to the circuit speed advantage resulting from the higher electrical conductivity of Cu. This can be explained by the so-called RC time delay (resistance (R) and capacitance (C)), which affects charge carrier transport in the device [143]. The RC delay is given by

$$V_{out}(t) = V_{out}(\text{maximum})[1 - \exp(-t / RC)] \quad \text{Eq. 6- 1}$$

where $V_{out}(t)$ is the output voltage of the circuit, t is time. When $t = RC$, $V_{out}(t)$ achieves a value of 63.2 % of the value of the $V_{out}(\text{maximum})$. Thus, the RC delay is

considered as the time when the output voltage is equal to 63.2% of the maximum output voltage. R and C are the effective total resistance of the metal interconnect and the capacitance associated with the interlevel dielectric, respectively.

In a modern IC device, multiple layers of metal lines are used with an insulating layer between the lines. This insulating layer is called the interlevel dielectric (ILD) layer. The ILD layer provides both horizontal and vertical isolation of the metal line in one layer from those in the next line. To estimate the RC time constant, the resistance of the interconnect and the capacitance of the ILD layers are related to the metal dimension. The geometry of both metal line and ILD layer is shown in Figure 6-1.

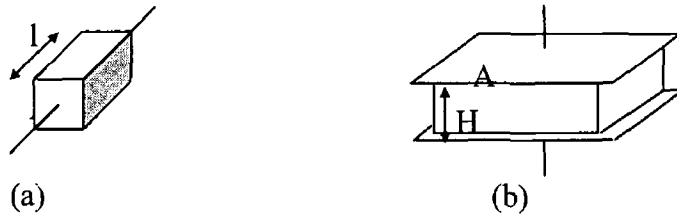


Figure 6-1 (a) conductor and (b) capacitor [143].

From Fig. 6-1, the resistance of the metal layer is

$$R = \frac{\rho l}{A_m} = \frac{\rho l}{wt_m} \quad \text{Eq. 6-2}$$

where ρ is the metal resistivity, l , w and t_m are length, width and thickness of the interconnect, respectively, and A_m is the cross-sectional area [153]. The capacitance of the inter-metallic level dielectric is given by

$$C = \epsilon_{ILD} \epsilon_0 A / H \quad \text{Eq. 6-3}$$

where ϵ_0 is the permittivity of free space = 8.8×10^{-12} N-C/m², ϵ_{ILD} is the dielectric constant of the interlevel dielectric layer (ILD) and H is the spacing between adjacent conducting metal layers.

The electrical resistance (R) of the metal interconnect line and the capacitance (C) between metal lines can be used to estimate the RC time constant for a single metal line. For a multilevel metallisation stack, the layout dimension and electrical representation of the stack are shown in Figure 6-2.

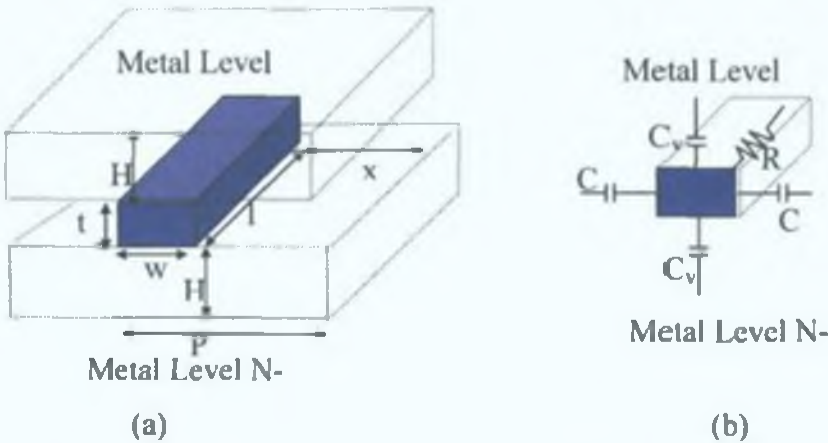


Figure 6-2 (a) dimension and (b) electrical representations of 3 layers of metal in multilevel interconnect device. The metal line in level N is separated from the metal line in level N+1 and N-1 by the ILD with thickness H. It is noted that t = thickness, w = width and l = length of the metal line in level N. P is the metal pitch and the spacing between adjacent lines is x. For the electrical representation, the capacitance of the ILD layer is composed of a lateral capacitance associated with the adjacent lines in the same level and a vertical capacitance associated with the metal lines in levels N+1 and N-1 [143].

The RC time constant from Eq. 6-1 and 6-2 can be given by [143]

$$RC = R(C_v + C_l) = 2\rho\left(\frac{l}{wl}\right)(\epsilon_{ILD}\epsilon_0)\left(\frac{wl}{H} + \frac{ll}{x}\right) \tag{Eq. 6-4}$$

It is assumed that (a) the metal width is equal to the space between the metal line, thus the metal line pitch, $P = 2w$; (b) the metal thickness, t , is equal to the ILD thickness, H . Eq. 6-4 can be reduced to

$$RC = 2\rho\epsilon_{ILD}\epsilon_0\left(\frac{4l^2}{P^2} + \frac{l^2}{t^2}\right) \quad \text{Eq. 6-5}$$

Eq. 6-5 is a vital equation for the estimation of the RC time constant. From Eq. 6-5, one can see that the RC time constant can be reduced by making the line length (l) as short as possible and using a metal with a lower resistivity and an ILD with a lower dielectric constant [143].

Therefore, the effect of metal thickness, metal linewidth and ILD thickness on the metal pitch is a major concern for device performance. Figure 6-3 [181] shows the theoretical advantage of copper over aluminum in an interconnect. Theoretically, a copper and low K dielectric interconnect at 0.1 microns width will offer approximately the same delay as an aluminum and SiO_2 interconnect at the present generation. It is observed that when the metal line width decreases, the RC increases significantly. This is because the increase of the metal resistance is faster than the decrease of capacitance, thereby limiting the effective speed of the device. Therefore, shrinking the Al-alloy interconnect metal in cross section, results in increasing the metal delay and in slower device speed [141].

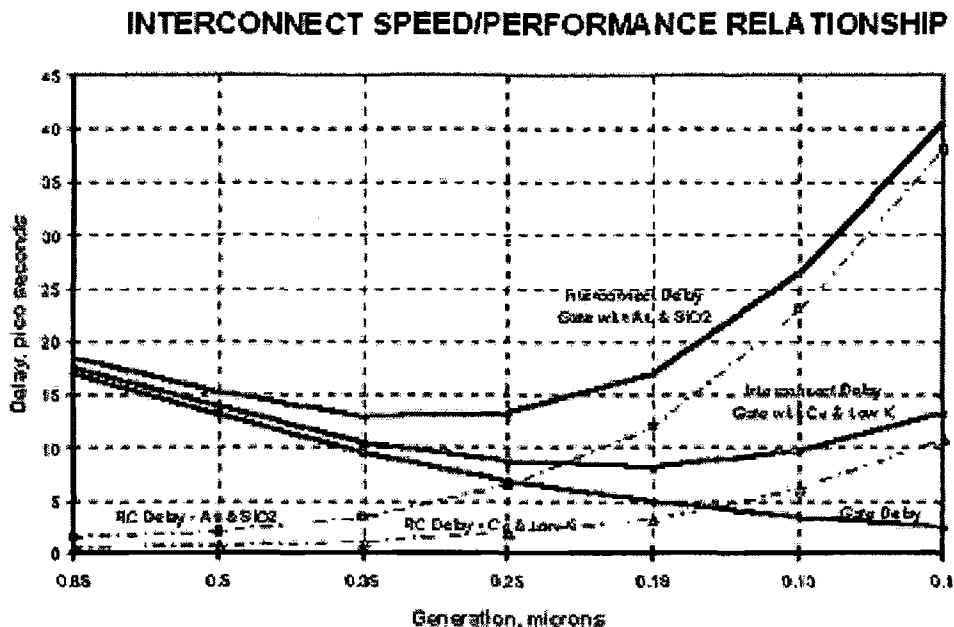


Figure 6-3 RC constant versus linewidth for AlCu and Cu [181].

A comparison of the material properties of Al and Cu is given below:

(a) Resistivity

Copper has the second lowest resistivity of any non-superconductor, the data for which is shown in Table 6-1. Although Silver (Ag) has the lowest resistivity, it has a poor adhesion to common dielectric materials, high diffusion into SiO₂ and high electromigration failure. Thus, Ag is not suitable for IC applications [142]. The next best choice is Cu, whose resistivity is very close to that of Silver (Ag) and it is a cost effective choice. In addition, compared to Al, Cu has about a 37% reduction in resistivity.

Table 6- 1 The resistivity of metals used in electronic applications [141].

Materials	Resistivity @ 18-20 °C in Ohm-cm x 10 ⁻⁶
Al, Pure	2.87
Al, 99.6%	2.83
Au, Pure	2.44
Cu, Pure	1.69-1.77
Ag, 99.98%	1.59-1.63
W	5.6

Since the resistivity of Cu is ~ 40% lower than that of Al and ~50% lower than AlCu (0.5% atomic percent Cu), the speed limit is increased proportionally by changing over from Al to Cu. Therefore, smaller Cu lines can carry the same amount of current, resulting in tighter packing densities, thinner metal layers and fewer metal levels required [152].

In general, σ does not depend on the metal dimension. However, in the case of a continuous thin film, R can depend on temperature, film thickness, crystallinity, defect structure, stress, etc. It is found that the appearance of stress and defects/dislocations in copper metallisation increases the resistivity [144]. Dislocations tend to invoke electron scattering at the surface, resulting in an increase of the metal resistivity. Stress induces a phonon-electron scattering condition in the crystal lattice, which is different from the unstrained lattice and increases the resistivity [145].

(b) Oxidation

Aluminium reacts violently with oxygen and forms Al_2O_3 , which is very stable and adherent to the metal surface. In addition, its oxidation and diffusion rates are very slow. This physical process is called self-limiting oxide growth or self-passivation

[142]. This oxide layer acts as a barrier to the oxidation and also as an effective diffusion barrier for Al itself for mass transport. In contrast, when Cu is oxidized, it forms a mechanically weak oxide with poor adhesion on the metal surface. Thus, the oxide of Cu cannot be used as a protection as is the case for Al_2O_3 . In addition, the Cu diffuses quickly through dielectric layers such as silica glass and polymers, and can easily damage the Si device. It is thus known as a “lifetime killer” [142] and the Cu must be kept away from the Si substrate.

(c) Electromigration performance

Electromigration (EM) is an atomic-scale phenomenon occurring when the conductor is subjected to high current densities at operating conditions. The moving electrons that constitute electrical current collide with the conductor atoms leading to momentum transfer (electron wind effect) and atom movement, and tend to push the ionised atoms in the direction of the electron flow when the atomic diffusion of the conducting material is high leading to mass transport of the atomic flux [143][144].

Fundamentally, EM failure is quantified by the Black equation [144]

$$t_{50} = Aj^{-2} \exp\left(\frac{\Delta H}{kT}\right) \quad \text{Eq. 6- 6}$$

where t_{50} is the EM failure time of the order of 50 percent, A is a constant depending on interconnect material and processing detail, k is Boltzmann’s constant ($k = 1.38 \times 10^{-23} \text{ J/}^\circ\text{K}$), T is the temperature in Kelvin and ΔH is the activation energy for diffusion along the pathway. It has been reported that the Cu is more resistive to electromigration (EM) than Al alloys [142]. This is correlated with the melting point of metals with similar crystal structures, which in the case of both Al and Cu is the Face-Centred Cubic (FCC) structure [142]. Therefore, the activation energy is proportional to the relative absolute melting points, which are 659°C for pure Al and 1082°C for pure Cu, respectively [141]. Many experiments were performed in Ref.2 and Cu was found to have a higher resistance to EM than Al. However, it is reported that the EM time varied widely in the Cu lines. In addition, for narrow lines, the t_{50}

lifetime of Al alloy lines was better than those fabricated with Cu metallisation [142]. The EM performance depends greatly on texture and grain size, and on the direction of current flow. Table 6-2 illustrates the relationship between EM tests and Cu metal grain size [146].

Table 6-2 Relationship between EM performance and Cu metal grain size for chemical vapour deposition (CVD) Cu (200), (111) and electroplated (EP) Cu (111) films [146].

Film types	Barrier Layer	Grain size (μm)	ΔH (eV)	t_{50} (hours) @ 200 °C, 8 MA/cm ²
CVD (200)	Ta, TiN, TiW	0.34	0.81	19
CVD (111)	Ta, TiN, TiW	0.29	0.86	83
EP Cu (111)	Ta	1.05	0.89	278

From Table 6-2, it is seen that EP Cu performs better than the others because of a larger grain size.

(d) Mechanical Strains and Stresses

Mechanical strains and stresses are a major concern in IC processing. They have a large effect on the manufacturing reliability and the properties of devices. Besser [149] compared the mechanical stress obtained in Al and Cu interconnect lines of 0.18 μm logic technology using the x-ray diffraction technique. It was found that the mechanical stresses of dual damascene patterns with inter-level dielectric (ILD) layers were much smaller in the Cu (286 MPa) than Al (411 MPa) because stress-induced voiding may be less prevalent in Cu lines. This result is similar to Kasthurirangan *et al.* [150]. Sullivan [146] mentioned that the stresses in Cu metallisation with a low-k dielectric ILD layer were much smaller than those with

the higher-k silicon dioxide dielectric, primarily because of lower thermal conductivity and lower mechanical strength.

6.1.1 Dual-Damascene Patterning

The Damascene process involves the etching of a trench pattern into a dielectric, the blanket deposition of metallisation and the removal of the excess metal outside the trench by Chemical-Mechanical Planarisation (CMP), leaving only the metal in the dielectric. This was first patented by IBM [144]. Due to the low volatility of the by-products in the reactive ion etching (RIE) of Cu, a Damascene pattern (or in-laid metal) is required. The first reports on the use of copper in microelectronics applications was presented by D.T. Price [144], and is based on a dual-damascene pattern. The process steps for the single and dual damascene processes are shown in Figure 6-4.

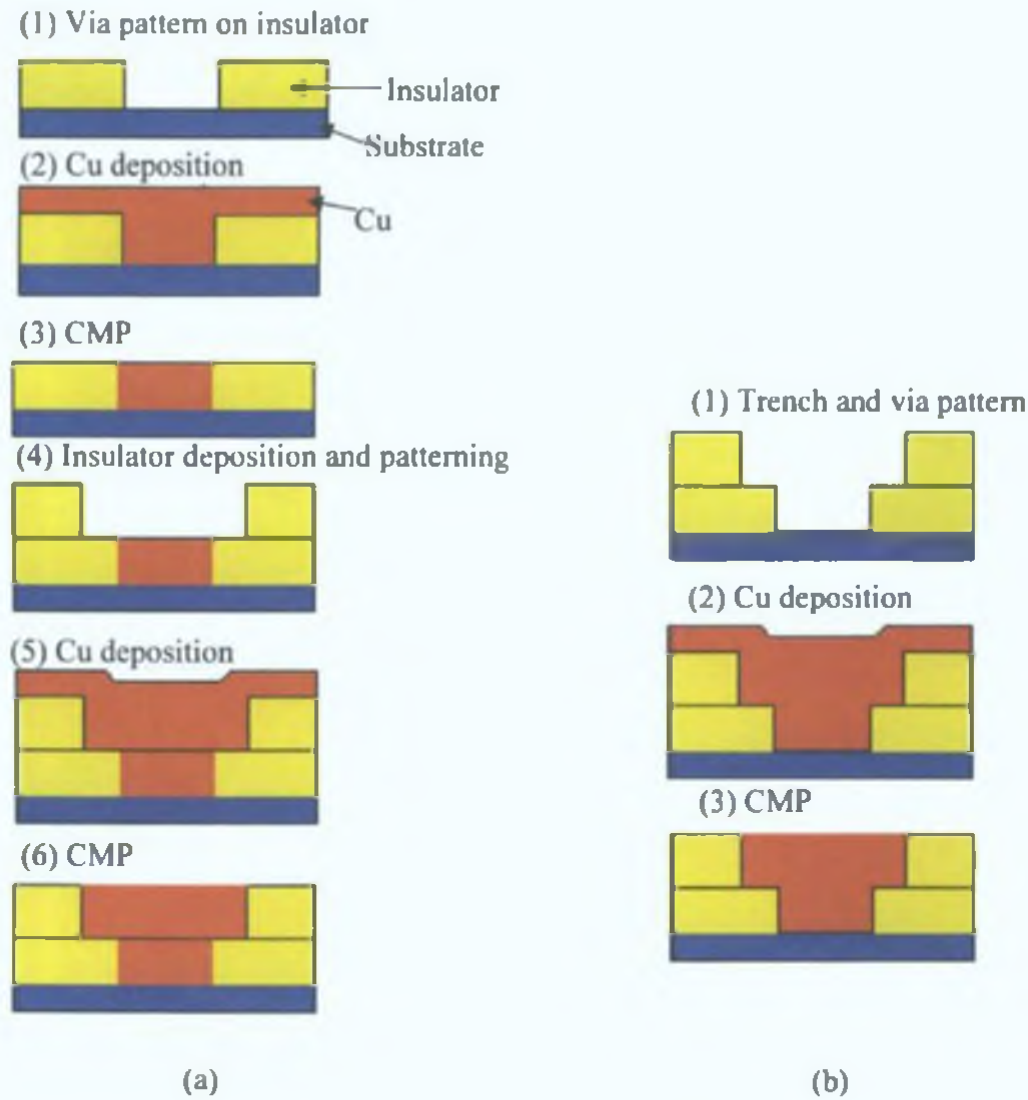


Figure 6-4 (a) Single Damascene and (b) Dual Damascene process outline [144].

In the single damascene process, the via (the linkage hole between the dielectric layer from one metal layer to another filled with a metal conductor) and interconnect ILD etching and chemical-mechanical planarisation (CMP) are performed individually. Thus two separate metal deposition and CMP steps are needed in the process. In the dual damascene process, the vias and interconnect are processed with in-order patterning and are then followed by a metal deposition and CMP. Using this technique, the process is simple and costs are kept low as only one metal deposition

and CMP is required. In addition, it is reported that this technique has less impact on the resolution, linewidth control, alignment tolerance, etc [144]. However, the process had not been carried out in production until Micron Semiconductor, Advanced Micro Devices and SEMATECH showed the possibility and benefit of the dual damascene pattern with Cu interconnect in making production, low Cu contamination, devices [144], [151]. It is noted that the dual-damascene pattern in Fig. 6-4 (b) is based on the use of a silicon oxide dielectric and the deposition of a Cu seed layer is not mentioned. The process steps are slightly modified with a different dielectric layer, i.e. polymer ILD due to a change of the material properties [144].

6.1.2 Copper and barrier layer deposition

Three methods have been used to deposit the Cu, namely Physical Vapour Deposition (PVD), Chemical Vapour Deposition (CVD) and Electrochemical Deposition (ECD). However, since the Cu metallisation samples used for stress characterisation were deposited by PVD and ECD, only these two techniques will be described in this thesis.

6.1.2.1 Physical Vapour Deposition (PVD)

This technique is classified into three methods; (a) evaporation using a filament or an electron gun, (b) DC magnetron, RF magnetron or reactive sputtering, and (c) molecular beam epitaxy (MBE). In this study, Cu is deposited using a planar DC magnetron sputtering method; therefore only sputtering deposition of the Cu will be described here.

The basic principle of all magnetically enhanced sputtering techniques was invented by Penning and further developed by Kay and others [182]. Vossen [182] has summarized this technique as briefly given here. The planar magnetron with either DC or RF sputtering is comprised of a planar cathode with the essential addition of permanent magnets directly behind the cathode. The planar cathode (sputtering

source or target) is parallel to an anode surface, usually grounded, that serves as a substrate holder. A simple geometry for DC magnetron sputtering is a disk-shaped cathode having a toroidal plasma ring facing and parallel to a fixed planar substrate holder. An alternative geometry is a rectangular (or oval) cathode in conjugation with a means whereby the substrates are moved continuously in a direction perpendicular to the cathode width during deposition. The important parts of the planar magnetron sputtering are magnet, insulation, cathode and anode placement.

Magnet arrangements can be varied considerably. The only limitation for the magnet geometry is that at least one closed path where the magnetic field lines are parallel to the cathode surface. The maximum transverse component of magnetic field in front of the target is commonly in the range of 200-500 G. In general, the magnetic field should enter and leave the target to the target face to avoid sputtering from the target edges and maximize the transverse field component.

The insulation or cathode shielding is to separate the chamber wall and the cathode. It is divided into 2 basic designs; (a) the cathode and shielding are totally within the deposition vacuum chamber with power and coolant brought in via vacuum feedthroughs. The advantages of this design are that the cathode can be readily retrofitted to an existing vacuum system and it can be placed to deposit in any direction. The disadvantages are that the system requires vacuum feedthroughs for coolant and high voltage. Slight leakage can cause a failure of the sputtering, (b) the cathode and surrounding electrical insulator form part of the vacuum chamber wall so that high-voltage connections and coolant seals are outside the vacuum chamber. The advantage of not requiring vacuum-to-coolant seals if a cathode backing plate is employed. In contrast, a design of the cathode assembly of the deposition chamber wall is the disadvantage of this design.

The cathode assembly comprises of the source material, typically 3-10 mm thick, bonded to a backing plate. It must have a good thermal conductivity through its thickness. Cathode cooling in the planar magnetron sputtering system is critical due

to the high power dissipation at the cathode. Water is usually used as a coolant to maintain a low cathode temperature.

The auxiliary anode has been stated to be effective in avoiding electron bombardment of the substrate. It was reported that the anode placement is significantly affected to the sputtering performance. The anode must be placed near the regions where the magnetic field enters the cathode.

The planar magnetron sources are commonly operated in argon at a pressure of 1-10 mTorr and at cathode voltage potential of 300-700 V. Thus, current density of 4-60 mA/cm² and power densities of 1-36 W/cm² are found in this condition [182].

Using the sputtering method, the Cu yield (atoms of copper sputtered per argon ion) is among the highest for metals. It is reported that the sputtering yield of Cu is about 2.8 compared to a sputtering yield of 1.2 for Al at a 600 eV argon ion energy [144]. Generally, the Cu interconnect is sputtered at a base pressure of about 5×10^{-7} Torr. With a DC magnetron and argon as a sputter gas, films are obtained with as-deposited resistivities of approx. 2.0 $\mu\Omega$ -cm. This method can deposit high-purity Cu with low-aspect ratios (ratio of height of the line to the width of the line). Three sputtering methods were presented by Rossmagel [147] and Singer [148] for filling trenches and via. These are (a) collimated sputtering in which directional deposition is obtained using a collimator between the target and substrate to filter the sputtering atoms from unaccepted angles; (b) ionised magnetron sputtering by using an internally placed inductively coupled RF antenna to generate the atom ionisation, thus attracting these atoms to a biased substrate; and (c) sputtering on heated substrates to allow reflow of the sputtered atoms along the substrate surface.

During sputtering, the surface of a growing coating is bombarded by ions from adjacent plasma, an independent ion source, sputtered atom, and especially high energy of neutral working gas atoms (as high as several hundred eV). The bombardment from such high energy can result in a macroscopic growth voids and also a number of small voids in the metal film. The presence of voids in a metal film

has lead to a generation of tensile stress, thus resulting in a compressive stress in silicon substrate [183].

However, the stress behaviour of sputtered films is quite complex. It is well known that argon pressure has played an important part on the stress behaviour [184]. The transition from compressive to tensile stress occurred with an increase of argon pressure. The transition of the stress can be explained as follows. At low pressure, there are few collisions within plasma; therefore, sputtered copper atom and reflected argon neutral atoms reach the substrate with high energy. As a result, the atoms in the film are driven closer together by those atoms being implanted and this is believed to generate compressive stress in a film. This mechanism is known as “atomic peening”. At high pressure, the sputtered atoms will have more collisions with atoms in the background gas, thus they reach the substrate with low energy. Without sufficient energy, the peening mechanism cannot take place. Therefore, voids remaining from the nucleation stage of the film growth cannot be filled. These can lead to columnar morphology. It is believed that the film contracts when isolated columnar grains attempt to fill the void between them and form direct grain boundaries. When each columnar grain moves closer to one another, the film attempts to contract on the substrate. However, the film-substrate bond prevents contraction thus causing the film to go into a tensile state [184].

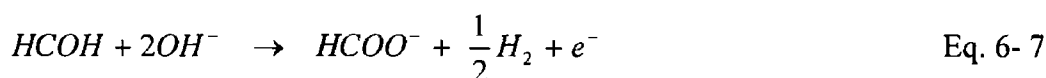
6.1.2.2 Electrochemical Deposition (ECD)

Electrochemical deposition (ECD) for both electroless and electroplating is proving to be very useful and popular for Cu metallisation. It is a simple method, and combines low cost, low processing temperature, high quality deposition, good via/trench filling ability and is reliable in production [144]. The emphasis of this study is on electroless plating of Cu and the induced strains in Si substrates during IC processing (Chapter 1). Therefore, an understanding of the electrochemistry of Cu is necessary. Most chemical and electrochemical stabilities of the metal are explained in terms of the reaction free energy and charge transfer [146]. The explanation for

electroless Cu deposition is divided into electrochemistry, kinetics, and thermodynamics of the reaction.

(a) Electroless Cu electrochemistry

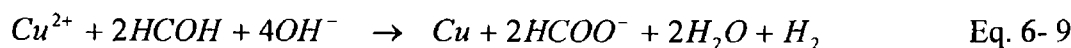
The electroless deposition of Cu can occur simultaneously by two reactions, these being an oxidation reaction of a reducing agent (anodic reaction) or a reduction reaction of the Cu ions on a catalytic surface (cathodic reaction). For deposition to occur the redox potential, E(V), of the reducing agent must be more negative than that for the metal being deposited [154], but not too different since the metal film might be deposited spontaneously in the solution. It has been reported that the reducing agent for electroless Cu deposition in very large scale integration (VLSI) applications can be formaldehyde, di-methylamine borane (DMAB) and glyoxylic acid [154]. The most popular reducing agent is formaldehyde. The anodic reaction of formaldehyde and the redox potential is given by



and E(V) = 0.32-0.12pH. It can be seen that the E(V) of this equation becomes more negative when the pH of the electroless deposition solution is increased. The cathodic reaction and its redox potential are



and E(V) = 0.345, respectively. Therefore, the overall reaction is given by



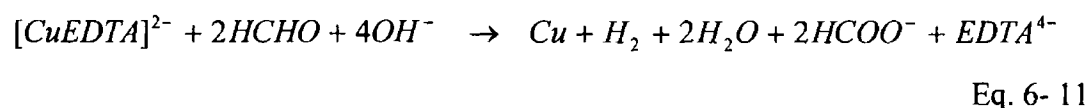
It is also reported that the thermodynamic driving force for the Cu deposition becomes greater as the pH increases [155]. However, at elevated pH values in the Cu solution, the Cu precipitates in the bath. To prevent this phenomenon, a complexant such as ethylenediaminetetraacetic acid (EDTA), malic acid (MAL) or tartrate (Tart) is added to the solution as a complexing agent. The selection and

concentration of the complexing agent must be taken into account because if the metal complex is too strong, there are not sufficient free Cu ions available for the deposition. EDTA is most commonly used in VLSI applications since the complex of EDTA and the Cu ion also reduces the redox potential difference between the anodic and cathodic reactions [154]. The cathodic reaction and the redox potential of the EDTA and Cu ion are given by



and $E(V) \cong -0.216$, respectively.

Therefore, the overall reaction at the catalytic surface is



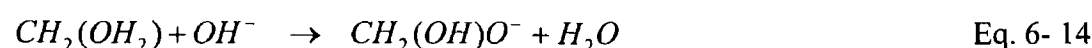
The reactions of formaldehyde in the aqueous solution can be presented in several different forms. Under alkaline conditions, the formaldehyde is almost completely hydrated as a methylene glycol as shown in Eq. 6-12 [155]



This hydrated form is a weak acid and dissociates to a methylene glycol anion as in Eq. 6-13



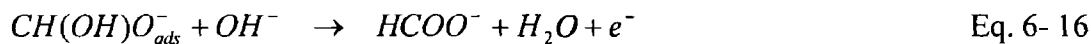
and/or reacts with hydroxide anions, which also generates a methylene glycol anion



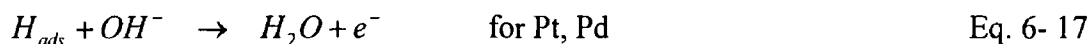
From Eq. 6-13 and 6-14, the methylene glycol anion is found to be the main component in the alkaline formaldehyde solution [154], and this anion plays a vital role in the electrochemical reaction on the catalytic surface such as Copper (Cu), Silver (Ag), Palladium (Pd), Platinum (Pt), Gold (Au), etc. It is noted that the subscript “ads” is defined as the atom or anion being adsorbed on the catalytic surface.



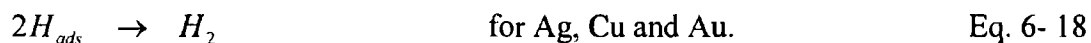
and



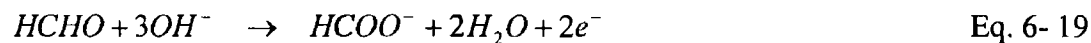
The dehydration of the formaldehyde in Eq. 6-15 is catalysed by the metal (catalytic metal) at which the process takes place. Thus, the reaction of the hydrogen atom on the catalytic surface (H_{ads}) depends on the catalytic metals employed such as



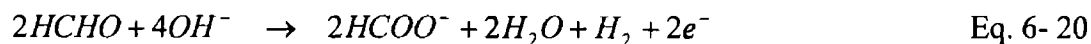
or



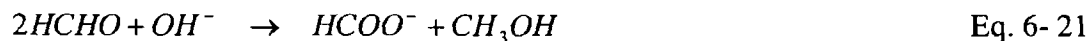
Thus, the overall reaction of the formaldehyde oxidation can be either



or

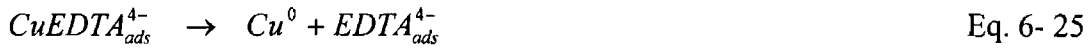


In a highly alkaline solution ($pH > 12$), the formaldehyde dissociates during what is called a Cannizzaro reaction [154]:



The rate of this reaction increases with pH and temperature. When the temperature is higher than 70 °C, the Cannizzaro reaction rate is 3-4 times faster than the normal deposition reaction (Eq. 6-11). Therefore, the integrity of the reaction is limited when the reaction occurs at temperatures higher than 70 °C, resulting in instability of the solution bath. This issue is solved by adding additives to the solution bath, which will be described later in this chapter.

The Cu/EDTA reaction path is given by



The Cu^{2+} can be reduced by the reducing agent to Cu^+ . The reaction is given below:



This reaction is not catalysed, resulting in an uncontrolled reaction and decomposition of the Cu deposition [154].

(b) Electroless Cu deposition kinetics

The overall reaction rate law for Eq. 6-10 can be written by [154]

$$r = K[C_{Cu^{2+}}]^a[C_{HCHO}]^b[C_{OH^-}]^c[C_{EDTA^{4-}}]^d \quad \text{Eq. 6- 27}$$

where K is the observed rate constant at a given temperature and a, b, c and d are the reaction orders for the reactants. $[C_{Cu^{2+}}]$, $[C_{HCHO}]$, $[C_{OH^-}]$ and $[C_{EDTA^{4-}}]$ are the concentrations of the copper ion, formaldehyde, hydroxide ion and complexing agent, respectively [156]. The reaction rate (r) in Eq. 6-27 is a function of temperature, which complies with the Arrhenius equation as

$$r = A \cdot \exp(-\Delta E / RT) \cdot C_{MG^-} \quad \text{Eq. 6- 28}$$

where A is the Arrhenius pre-exponential factor, ΔE is the Arrhenius activation energy, R is the gas constant and C_{MG^-} is the concentration of the methylene glycol anion which is an intermediate form of the formaldehyde. To first order with respect to the methylene glycol anion and to zero order for all other components, an

activation energy of 60.9 KJ/mole was estimated [154],[155]. It is noted that the a, b, c and d values are dependent on the condition of the electroless Cu bath. For instance, when $[C_{Cu^{2+}}] = 0.015-0.1$ mol/litre, $[C_{HCHO}] = 0.05-0.5$ mol/litre, $[C_{OH^-}] = 0.07-0.3$ mol/litre and $[C_{EDTA^{4-}}] = 0.03-0.4$ mol/litre and the temperature is 50 °C, the reaction orders of a, b, c, and d are 0.78, 0.13, 0.02, and 0.02, respectively [154],[156].

(c) Additives for Electroless Cu deposition

Additives to the electroless Cu solution can affect (i) the stability of the solution, (ii) kinetics and mechanisms of the metal growth process, (iii) structure and morphology of the metal deposited, and (iv) purity of the metal layer [157]. As mentioned above, Cu deposition is possible in an alkaline solution; therefore common chemicals such as sodium hydroxide (NaOH) and potassium cyanide are added to increase the pH of the solution. However, sodium and potassium ions can accumulate in silicon dioxide, resulting in changes to its electrical properties. It is known that the sodium concentration must be limited to be less than 10^9 cm⁻². Many researchers have found that Tetra-methyl-ammonium-hydroxide (TMAH) is the best alternative for Cu metallisation in VLSI/ULSI technology [154]. A stabilizer is one of the most vital additives to the electroless Cu bath. It is used to prevent the spontaneous decomposition and deposition of the metal film in the solution by controlling the rate of nucleation in the solution and the behaviour of the nucleus, e.g. its dissolution. It is noted that the nucleation of the electroless Cu probably occurs during the reaction of Eq. 6-26. The critical radius of nuclei (r^*) is given by [154]

$$r^* = 2\gamma v / [nF(E_{ME} - E_{RED})] \quad \text{Eq. 6- 29}$$

where γ is the surface tension of the metal-solution interface, v is the molar volume of the metal, n is the number of electrons used in the redox reaction, F is the Faraday constant, and E_{ME} and E_{RED} are the redox potential of the cathodic (metal) and anodic (reducing agent) reactions, respectively. When the metal nuclei formed in the solution are larger than the critical nuclei (r^*), instability and spontaneous

decomposition of the solution are obtained. Eq. 6-29 shows that r^* increases with a decrease in the difference between E_{ME} and E_{RED} , resulting in improving the stability of the solution. As previously noted, the EDTA is added to the solution as a complexing agent to reduce $E_{ME}-E_{RED}$. The Cu(II)-EDTA complex can affect nuclei growth by adsorbing on the catalytic surface and subsequently dissolving in the solution. Thus, the most common stabilizer of 2,2'-dipyridyl can be added to form a complex with Cu(I) and then oxidizing agents such as chromates or hydrogen peroxide can be added to oxidize Cu(I) to Cu(II). However, Masahiro *et al.* reported that the 2,2'-dipyridyl concentration affects the deposition rate as the deposition rate decreased with increasing 2,2'-dipyridyl concentration at a given temperature above 60°C [158].

A ductility promoter can also be added to the solution to diminish the hydrogen gas by-product of the anodic reaction formed in the Cu film. This is due to the fact that the hydrogen atoms adsorbed on the Cu surface can generate voids in the Cu layer and can lead to stress generation in the Cu film [159]. The ductility promoter also acts as a stabilizer similar 2,2'-dipyridyl.

Surfactants are added to the Cu solution to decrease the surface tension of the electroless plating solution and also to eliminate hydrogen bubble detachment. The choices of the surfactants are dependent on the bath conditions, i.e. temperature, pH and ionic strength [154].

Dubin *et al.* [156] summarised the effects of reactants, i.e. Cu(II), HCHO, EDTA, pH, temperature on the Cu deposition rate and resistivity as shown in Table 6-3.

Table 6-3 Electroless Cu deposition rate and resistivity vs. deposition bath factors [156].

Increasing parameters	Deposition rate change	Resistivity change
[CuSO ₄ ·5H ₂ O]	↑↑	⇔
[HCHO]	↑↑	↑↑
[EDTA]	⇔	⇔
pH (12.2-12.8)	(up to 12.6) ↑↑	⇔
pH (>12.8)	Unstable solution	Unstable solution
Temperature	↑↑	↓↓

Note: ↑↑ - increase

↓↓ - decrease

⇔ - no strong effect

In addition, his group found that the optimised recipe for electroless Cu deposition for VLSI/ULSI applications providing a high deposition rate and good quality Cu films is given in Table 6-4.

Table 6-4 The electroless copper deposition solution component [156],[160].

Components	Function	Quantiy (in range)
CuSO ₄ ·5H ₂ O	Provides Cu (II) ions	0.05-0.1 M
2,2'-dipyridyl	Stablizer	0.5-1.0 M
EDTA	Complexing agent	0.1 M
HCHO	Reducing agent	0.01-0.1 M
Triton® x-100	Surfactant	0.5-2%

(d) *Catalytic Surface*

It is known that the Cu does not adhere well to most dielectrics nor to Si [154]. Thus, a catalytic surface, known as a seed layer needs to be deposited before the deposition of the electroless Cu. It is reported that Palladium, Platinum, Al, Palladium Silicide, Platinum Silicide or Tungsten can be employed as seed layers for the electroless Cu deposition [154]. Sputtered or evaporated Cu can also be used as the seed layer. However, the Cu must be specially treated since the Cu oxidises quickly in air. Dubin *et al.* found that Al can be used as a sacrificial layer if Cu is used as the seed layer to protect it from oxidation [156]. This can be achieved by depositing the Cu seed and Al without breaking the vacuum. The Al will be removed automatically in the electroless Cu bath during the electroless Cu deposition [161].

6.1.3 Mechano-Electrochemical Effects

Mechano-electrochemical is defined as a relationship between mechanical effects in the electrochemical deposition [162]. The effect of stress on the electrochemical layer is a major concern in this relationship. In this study, the stresses in Si substrate due to the Copper metallisation for both room and elevated temperatures are studied. During thermal processing, both internal and external stresses can cause the stress measured in the Si. Therefore, both internal and external stresses are described in this thesis to give a general understanding of the overall stress due to the electrochemical deposition. It is known that the preparation of materials and their subsequent treatment e.g. machining, etc., can produce either compressive or tensile internal stresses in the metal deposited by electrochemical, electroless or vacuum sputtering process. The stability of the materials causes the external stress in this case such as the misfit between the crystal lattices of the depositing material and of the substrate.

The electrochemical process induces the stress in the copper layer can be accounted for as follows [159].

6.1.3.1 Creation of stress during electrochemical deposition of materials

Two types of stresses are visible in the electrocrystallisation of thin layers, i.e. macrostress and microstress.

Fundamentally, macrostress can be compressive or tensile. This macrostress can cause the bending of the sample, which is measured using x-ray techniques, micro-Raman techniques, etc.

Microstress is defined as a stress due to the size of the crystal grains, crystalline boundaries or the deformation of the crystal lattice [159].

Popereka reported that the stress induced during the deposition is not related to its chemical nature or crystal structure [159]. In addition, it seems that the sign of the stress in the layer is related to the melting point of the metal. Metals with low melting points tend to create the compressive stress, whereas the high melting point metals seem to develop a tensile stress within. Examples of the different metals with the possible stress types are shown in Table 6-5 [159].

Table 6- 5 Types of stress generated in the different metals [159].

Metal	Melting point (°C)	Sign of stress	Mode of changing the sign
In	156	-	Unknown
Sb	630.5	±	Changing current density, temperature, additives
Ag	961	±	Same as above
Cu	1083	±	Same as above
Pd	1552	+	Unknown
Rh	1990	+	Unknown

Note: positive and negative signs represent tensile and compressive stresses, respectively.

In addition, several studies [159], [164]-[165] have shown that the generation and quantity of the stress during the electrochemical metallisation can be affected by the type of substrate, composition of the plating solution, pH, layer thickness, deposition temperature and additives. Therefore, the generation of stress due to the electrochemical metallisation is complicated and dependent on many factors.

6.1.3.2 Effect of Hydrogen on the Electrochemical Copper Metallisation

Hydrogen is well known as a co-deposited with the metal. Nakahara and Okinaka [165] showed that the effect of the hydrogen from formaldehyde in the electroless copper metallisation results in poor mechanical properties of the electroless copper layer. Using autocatalytic reduction of the formaldehyde in the alkaline solution of a copper complex, the hydrogen gas could be produced from the splitting of a C-H bond in the formaldehyde molecule and subsequently combines with copper as copper hydride (CuH) at the copper surface. In addition, the hydrogen gas can also exist in the copper layer as a leading to voids and compressive stresses.

Although a stabilizer is added to the copper solution bath to eliminate the hydrogen bubbles from the bath, there is also a chance that the hydrogen will be captured in the layer especially at high deposition rates.

6.2 Experimental details

The sample preparation used in this study is described in this chapter including the experimental details of SXRT, MRS and FEM.

6.2.1 Sample Details

The electroless and sputtered Cu metallisation were deposited on lift-off and single damascene patterns as illustrated in Figure 6-5 and 6-6, respectively. The process steps are shown below:

Batch 1: Lift-off pattern

0. Bare $\langle 100 \rangle$ Si
1. Photolithography
2. Barrier layer (Ti) 100 nm
3. Cu seed layer 20 nm
4. Cu Metallisation 300 nm
 - 4a. Electroless Cu
 - 4b. Sputtered Cu
5. Lift-off

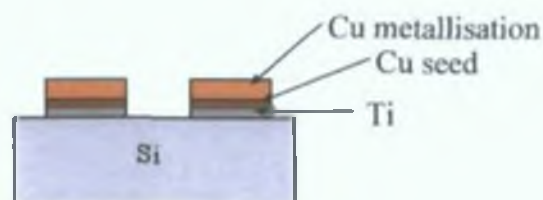


Figure 6-5 The lift-off pattern process.

Batch 2: Damascene pattern

0. Bare $\langle 100 \rangle$ Si
1. Oxidation $0.78\ \mu\text{m}$
2. Photolithography
3. RIE Etch of $0.67\ \mu\text{m}$ SiO_2 layer
4. Barrier layer (Ti) $100\ \text{nm}$
5. Cu seed layer
6. Cu layer $300\ \text{nm}$
 - 6a. Electroless Cu
 - 6b. Sputtered Cu
7. CMP
 - 7a. Electroless Cu
 - 7b. Sputtered Cu

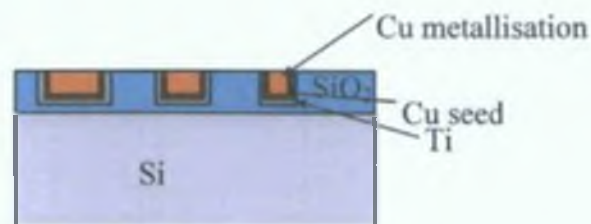


Figure 6-6 The damascene pattern process.

In one set of samples, ten lines of $100, 60, 40, 20, 10, 8, 6, 4, 2$ and $1\ \mu\text{m}$ geometrical width were deposited. The electroless Cu metallisation samples were deposited based on the recipe from Shacham-Diamand [154] and conditions were optimised for our seed layer and Si samples as given in Table 6-6. (001) surface orientation p-doped Si wafers were used in this experiment. The $100 \pm 10\ \text{nm}$ thick Ti barrier layer was deposited using a DC magnetron sputtering method. An Argon carrier gas pressure of $3.5 \times 10^{-3}\ \text{mbar}$ with a DC power of $350\ \text{V} \times 0.8\ \text{A}$ (320 Watts) were used for the Ti deposition. Without breaking the vacuum, a $20\ \text{nm}$ Cu seed layer was deposited on the samples. This sputtering process step was performed at Queen's University, Belfast (QUB).

Table 6- 6 Electroless copper deposition solution components.

Component	Function	Quantity (g/l)
CuSO₄ · 5H₂O	Supplies copper ion	4
HCOH	Reducing agent	5
EDTA	Ligand	14
2,2'-dipyridyl	Stabiliser	0.1
Triton X-100	Wetting agent or surfactant	0.1
NaOH	pH Adjustment	

For the electroless Cu deposition, sodium hydroxide (NaOH) is used to adjust the pH level of the solution to 12.3 - 12.7. The temperature is adjusted to a range of 75-80 °C. The deposition rate is approx. 40 nm/min.

The sputtered Cu samples were produced at QUB using a DC magnetron sputtering system with a power of 550 V x 1 A (550 Watts), power density of 7 W/cm² and a chamber-based pressure of 2 x 10⁻⁶ mbar at room temperature. An Argon carrier gas pressure of 3.5 x 10⁻³ mbar was used.

For the damascene pattern, the chemical-mechanical panarization was performed using a chemical slurry of 2 wt % Al₂O₃ (0.3 µm particle size), 5 vol. % NH₄OH mixed with H₂O and 0.125 wt % BTA (Benzotriazole). The chemical slurry flow rate ≈ 140 ml/min. The rotation of the polishing pad is 60 rpm. A Suba IV/IC1000 stacked polishing pad was used with 1.2065 x 10⁴ Pa of pressure on the wafer. The total polishing time to the centre of the wafer is about 40 minutes.

In order to study the influence of the electroless Cu metallisation on the lattice curvature, 300 nm of the electroless Cu metallisation was deposited on 30 nm gold/ 20 nm chromium on a Si wafer. In this case, patterned chromium was deposited as an adhesive layer. This was followed by the gold, which acts as a catalytic surface for the electroless deposition. The chromium and gold layers were patterned by

lifting off the excess metal in acetone for 10 minutes. The photoresist is then patterned again to protect the silicon substrate. Finally, the sample was immersed in an electroless copper solution bath with a deposit rate of 41.7 ± 3.1 nm/min.

6.2.2 Synchrotron X-Ray Topographic Measurements for Cu Metallisation

The measurements were performed at HASYLAB-DESY, Hamburg, Germany (Hamburger Synchrotronstrahlungslabor am Deutschen Elektronen-Synchrotron), utilising the continuous spectrum of synchrotron radiation from the DORIS III storage ring bending magnet. The ring operated at a positron energy of 4.436 GeV and at typical currents of 80-150 mA. The aforementioned Laue or Bragg pattern of topographs was recorded on Geola holographic high-resolution VRP-M films. The distance from the sample to the film was 50 mm for all samples. The beam size was set to 1.5 mm x 2 mm. The samples were set parallel to the film for the back reflection case and at an angle of 18° with respect to the sample normal for the transmission case. At the beamline, all samples were examined at room temperature, 100, 200, 300 and 400 °C for both back-reflection and transmission geometries.

The films were developed by immersing in developer for 5 minutes, 2-3 seconds in a stop bath, then fixer for 10 minutes, a 30 minutes water wash and finally drying in a heater for at least 30 minutes. The developer is Kodak D-19 developer; the stop bath is a 2% acetic acid in H₂O solution. The fixer is Kodak No.1 sodium fixer. The topographs have been generated in a system comprising of a microscope with a CCD camera, frame-grabber and appropriate software. Some of the images have been processed using a software package called Visilog[®], in order to improve clarity in the laboratory. The topographs were taken at magnifications of 50X for BRT and LAT and 100X for BRST and ST.

The measurements are divided into three categories in accordance with the objectives of the study:

- To examine the electroless Cu metallisation induced strain distributions in Si wafers in IC processing and to relate the strain fields with the curvature of the lattice planes. In this study, the 300 nm electroless Cu metallisation/ 30 nm Au/ 20 nm Cr on Si wafer system was used in SXRT for both back-reflection and transmission techniques.
- To compare the stress distributions in Si substrates; therefore, the measurements are separated into 2 steps of 2 patterns each as follows:
 - (a) *Pre-Cu* metallisation: The *Pre-Cu* metallisation sample is defined by step 4 (lift-off of Cu seed layer on Ti and Si wafer for the lift-off pattern) and by step 5 (for Cu seed layer deposition with the damascene pattern).
 - (b) *Post-Cu* metallisation: The *Post-Cu* metallisation sample is defined by step 5 (a) and (b) (electroless Cu for the lift-off pattern) and by step 7 (a) and (b) (CMP for damascene pattern).
- To compare the influence of line widths on the electroless Cu metallisation, the lift-off pattern, consisting of 500 nm electroless Cu metallisation on the 20 nm Cu seed layer/ 100 nm Ti barrier layer and Si wafer, was employed in this study since the lines were uniformly and well deposited.

6.2.3 Finite Element Modelling for electroless Cu metallisation

This technique is used to compare the influence of line widths on the electroless Cu metallisation on the lift-off pattern and to compare with the SXRT and MRS results. As in the case of Pb/Sn bump modelling, two-dimensional (2-D) plane strain finite element models have been employed in these experiments. The geometry, dimensions and boundary conditions of the *post*-Cu Metallisation samples are illustrated in Figure 6-7. The metallisation with line widths of 0.1, 0.5, 1.0, 2.0, 5.0, 10, 20, 40, 60 and 100 μm were simulated using FEM; therefore the dimension X in Fig. 6-7 is the half-width of the line, which is 0.05, 0.25, 0.5, 1.0, 2.5, 5.0, 10.0, 20.0, 30.0 or 50.0 μm for line widths of 0.1, 0.5, 1.0, 2.0, 5.0, 10, 20, 40, 60 and 100 μm , respectively.

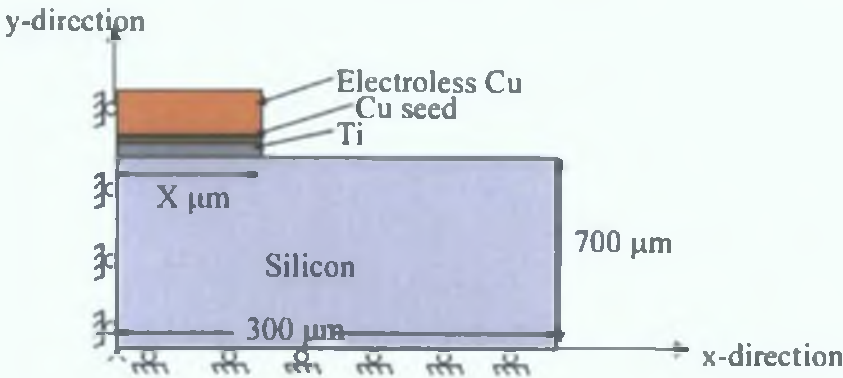


Figure 6-7 Typical geometry and boundary conditions for the *post*-Cu metallisation sample model.

About 100,000 nodes were used to achieve the simulation. The finite element analyses were carried out using Quickfield® Professional version 4.2 [166]. The materials considered in these models are the Si substrate, the Ti barrier layer and Cu. These materials are assumed to be isotropic and linearly elastic. Their properties are given in Table 6-7.

Table 6- 7 Materials properties for finite element analysis [167].

Materials	Young's modulus (E x10 ⁹) N/m ²	Poisson's ratio (ν)	Coefficient of thermal expansion (α, x 10 ⁻⁶) /°C
Si	112.4	0.28	2.5
Ti	116.0	0.34	8.9
Cu	123.0	0.33	17.0

6.2.4 Micro-Raman Spectroscopic measurement for Cu metallisation

This technique was used to examine the stress in the Si due to the Cu metallisation processing. The incident beam is focused through the 100X microscope objective on the sample. An automatic X-Y stage with a minimum movement of 0.1 μm was used to move the sample during the measurements. A plasma line at 560 cm⁻¹ was used as an internal calibration of the measurements to eliminate environmental and CCD temperature fluctuations during the experiments. The spatial strain distribution in the Si sample can be examined from the measured frequencies of Raman peaks compared with those of a strain-free reference Si sample at 521 cm⁻¹. The relationship between Raman shift and linear strain was derived by De Wolf [168] and is given by

$$\sigma_{xx} (MPa) = -434\Delta\omega(cm^{-1}) \qquad \text{Eq. 6- 30}$$

where σ_{xx} = the uniaxial stress in MPa and $\Delta\omega$ = the Raman shift between the measured Raman peak of strained Si (ω_j) compared with that of strain-free Si (ω_0); $\Delta\omega = \omega_j - \omega_0$, ω_j = the measured frequency of the silicon Raman peak and ω_0 = the frequency of the silicon Raman in the stress free state.

In this study, the experiments were performed by pointing the laser along the Z direction and measuring the strains along the X direction. The geometry of the lines is shown in Figure 6-8.

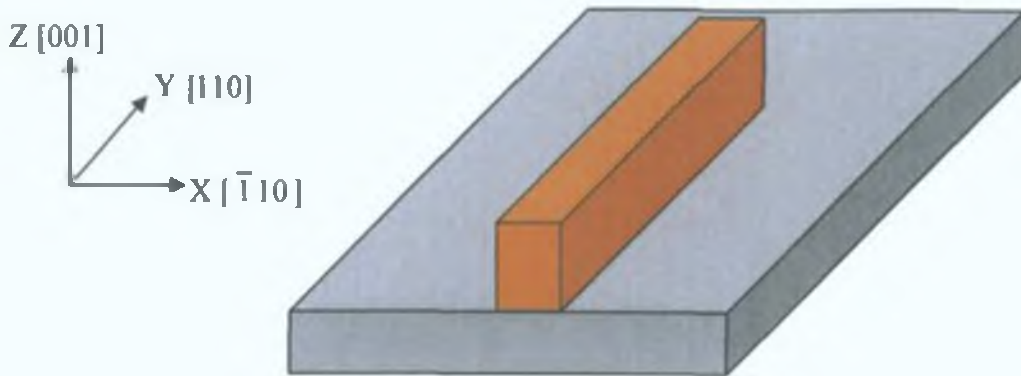


Figure 6-8 The geometry and orientation of the Cu lines for MRS measurement.

The objectives for using this technique are described as follows:

- To compare the stress distributions in Si substrates; therefore, the measurements are separated into 2 steps of 2 patterns each as follows:
 - (a) *Pre-Cu* metallisation: The *Pre-Cu* metallisation sample is defined by step 4 (lift-off of Cu seed layer on Ti and Si wafer for the lift-off pattern).
 - (b) *Post-Cu* metallisation: The *Post-Cu* metallisation sample is defined by step 5 (a) and (b) (electroless Cu for the lift-off pattern) and by step 7 (a) and (b) (CMP for the damascene pattern).
- To compare the influence of line widths on the electroless Cu metallisation; the lift-off pattern, consisting of 500 nm electroless Cu metallisation on a 20 nm Cu seed layer/ 100 nm Ti barrier layer and the Si wafer, was employed in this study since the lines were uniformly and well deposited.

6.3 Results and Discussion for Cu metallisation

This section is separated into 3 main parts, SXRT, FEM and MRS results. As mentioned in Chapter 1, the objectives of this study are as follows

- To examine electroless Cu metallisation induced strain distributions in Si wafers in IC processing and to relate the strain fields with the curvature of the lattice planes based on the work of Meieran and Blech [169].
- To compare the strain fields in Si substrates caused by electroless and sputtered Cu metallisations for both lift-off and single damascene patterns at *Pre-* and *Post-* metallisation steps using SXRT and MRS.
- To study the influence of elevated temperatures, i.e. 100, 200, 300 and 400 °C, respectively, on the electroless and sputtered Cu metallisations for both lift-off and damascene patterns at *Pre-* and *Post-* metallisation steps using SXRT.
- To study the influence of Cu line widths on the stress distributions in Si and to correlate with MRS and FEM.
- To study the influence of the annealing step on the *Post*-metallisation using MRS.

6.3.1 Synchrotron X-Ray Topographic results

SXRT was used to examine the strain fields in Si substrates due to the Cu metallisation process. The first result is the study of the behaviour of the Si lattice planes based on the work of Meieran and Blech [169]. Two electroless Cu samples were measured. The second result is the evaluation of the stress distributions in Si substrates with two different metallisation techniques, i.e. electroless and sputtering techniques, by measuring the impact of *Pre-* and *Post-* metallisation steps for two different patterns (lift-off and damascene). The third result is the study of the stress behaviour in Si wafers due to the annealing process of the Cu metallisation for both

electroless and sputtered samples. Finally, the fourth result is the study of the influence of Cu line width on the strain fields in the Si substrates.

6.3.1.1 Electroless Cu metallisation and lattice curvature.

To study the lattice curvature with electroless Cu metallisation, samples were examined using the LAT technique. The electroless Cu on Si sample (Cu thickness of ~300 nm) was investigated in order to analyse the extinction contrast mechanism, which can give more information about the lattice curvature of the samples. The copper lines are parallel to $[\bar{1}30]$. The sample direction is shown in Figure 6-9.

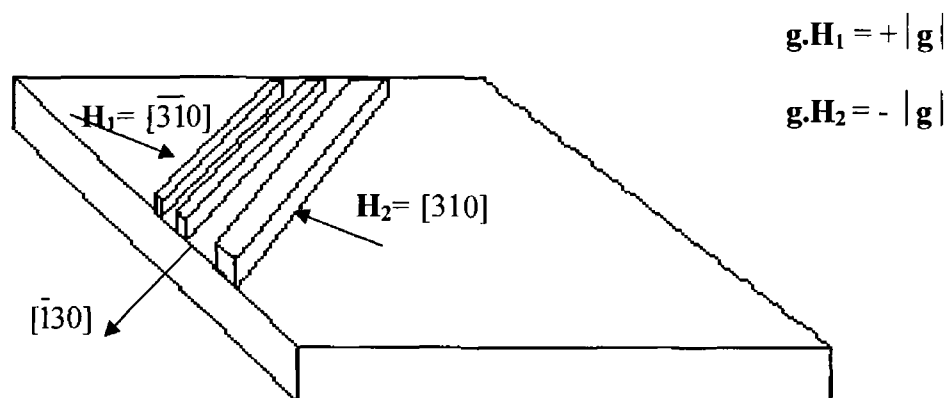


Figure 6-9 Direction of the electroless Cu metallisation.

As mentioned in Chapter 2, the values of $\mathbf{g} \cdot \mathbf{H}_i$ were compared to the contrast intensity which were recorded during measurement, where \mathbf{g} = the diffraction vector and \mathbf{H}_i = the unit vector normal to the film edge and points away from film edge. The extinction contrast (black/white contrast) in the image is governed by the relationship between the diffraction vector (\mathbf{g}) and the lattice displacement (\mathbf{H}_i) as shown in Figure 2-26 (Chapter 2). The vector \mathbf{H}_i is normal to the lattice displacement and deviates from the lattice direction in the undisturbed crystal due to an imposed strain field. In the case of the metal film on the Si substrate, the vector \mathbf{H}_i is pointed inwards to the metal edge as explained in Chapter 2.

In the experiment, the metal surface faced the film. The result of the LAT generated from the $\bar{3} \bar{1} 0$ reflection is illustrated in Figure 6-10.

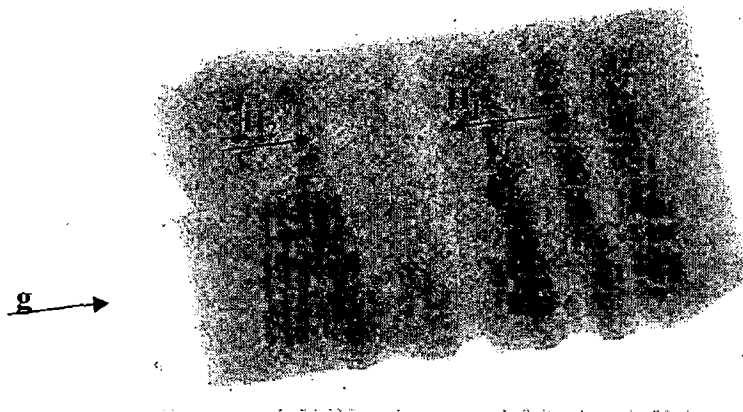


Figure 6-10 The LAT image from 300 nm electroless Cu/ 30 nm Au/ 20 nm Cr/ Si, $\mathbf{g} = [\bar{3} \bar{1} 0]$.

Figure 6-10 shows that the edge of copper with the \mathbf{H}_2 direction ($\mathbf{g} \cdot \mathbf{H}_2 = +|\mathbf{g}|$ or \mathbf{H}_2 parallel to \mathbf{g}) diffracted more intensely than the copper edge with the \mathbf{H}_1 direction ($\mathbf{g} \cdot \mathbf{H}_1 = -|\mathbf{g}|$ or \mathbf{H}_1 anti-parallel to \mathbf{g}). Hence, it is possible that the dark contrast at edge \mathbf{H}_2 is generated because the Borrmann effect cannot be seen as it is overwhelmed by the increase in intensity due to the extinction contrast image. On the other hand, the white contrast at the edge \mathbf{H}_1 is possibly due to the Borrmann effect as the main contributor, since the extinction contrast image is small (\mathbf{g} anti-parallel to \mathbf{H}_1). This assumption is in good agreement with that of Blech and Meieran for metal deposition on a Si substrate [169]. In addition, Blech and Meieran mentioned that when the black contrast is on the \mathbf{H}_2 edge and white contrast is on the \mathbf{H}_1 edge, the strains generated by the metallisation induced bowing of the sample as shown in Figures 6-11 and 6-12.

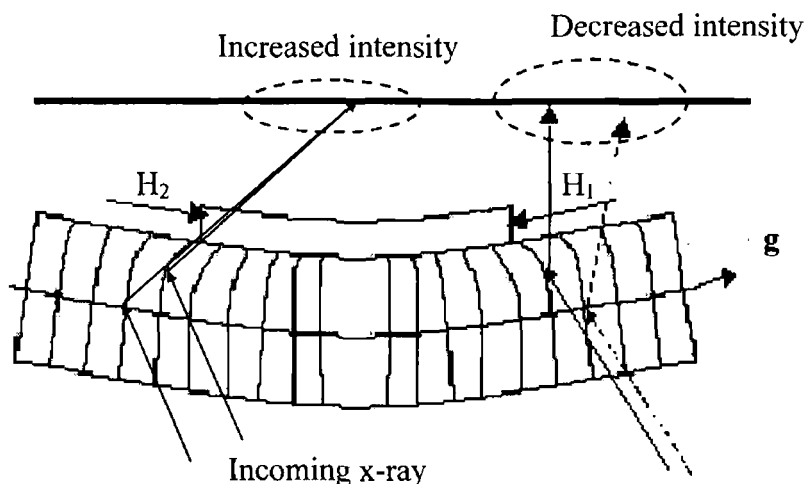


Figure 6-11 Strain in silicon wafer cross section.

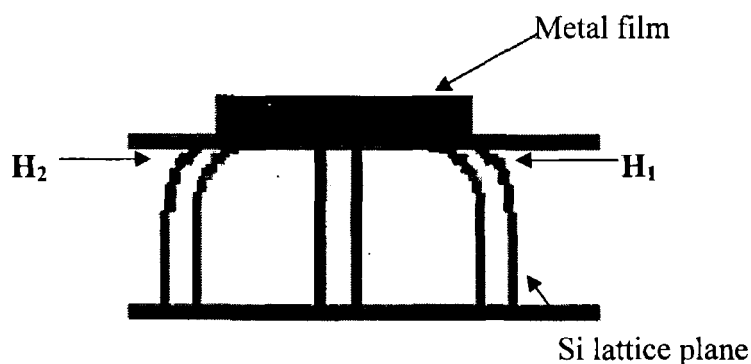


Figure 6-12 Metal places the Si in compression warping the lattice planes near the metal edges as shown. H_1 and H_2 point along the direction of distortion of the Si lattice as shown [169].

In this case, it suggests that the metal is in tension and the silicon is in compression at the interface. This corresponds to coefficients of thermal expansion (CTE) in the metals, which are higher than that of Si ($\text{Cu} \approx 17.7 \text{ ppm}/^\circ\text{C}$, $\text{Au} \approx 14.4 \text{ ppm}/^\circ\text{C}$, $\text{Cr} \approx 6.2 \text{ ppm}/^\circ\text{C}$, and $\text{Si} \approx 2.5 \text{ ppm}/^\circ\text{C}$).

To examine the lattice curvature with different barrier and seed layers, the measurement was performed again on 500 nm electroless Cu/ 20 nm Cu seed/ 100 nm Ti on Si using the LA-BRT technique. The metal line was patterned along the $[110]$ direction. The orientation of the metal lines is shown in Figure 6-13.

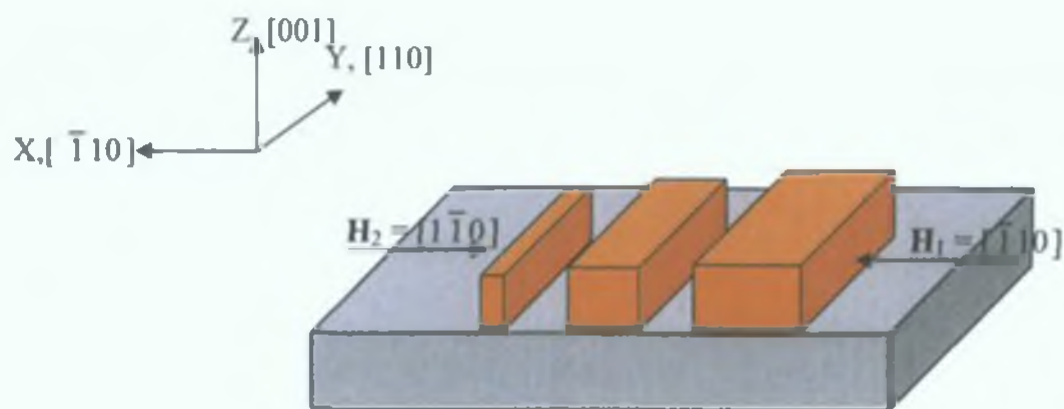


Figure 6-13 The orientation of the Cu metal lines on the Si sample (S#100).

From Figure 6-13, the metal edge vector H_1 is in the $\bar{1}10$ direction and the opposite metal edge, H_2 is in the $1\bar{1}0$ direction. Its LA-BRT images are taken from $\bar{2}28$ and $2\bar{2}8$ reflections as illustrated in Figure 6-14 and 6-15, respectively.

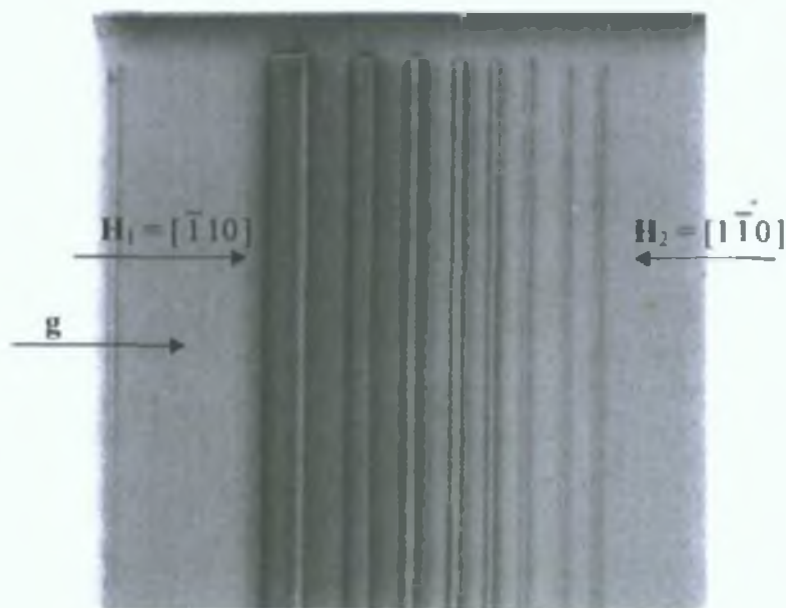


Figure 6-14 LA-BRT image of the Cu metallisation sample taken from $\bar{2}28$ reflection (Ref#R30F328-10).

Figure 6-14 shows that the edge of copper with the \mathbf{H}_1 direction ($\mathbf{g} \cdot \mathbf{H}_1 = +|\mathbf{g}|$ or \mathbf{H}_1 parallel to \mathbf{g}) diffracted more intensely than the copper edge with the \mathbf{H}_2 direction ($\mathbf{g} \cdot \mathbf{H}_2 = -|\mathbf{g}|$ or \mathbf{H}_2 anti-parallel to \mathbf{g}). A similar result is found in topographs taken from the $2\bar{2}8$ reflection as depicted in Figure 6-15 below.

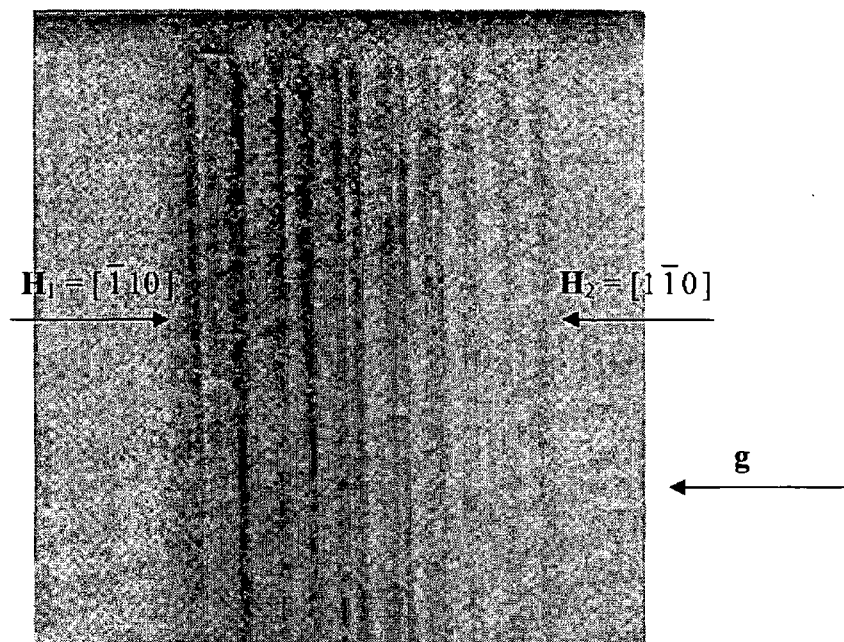


Figure 6-15 LA-BRT image of the Cu metallisation sample taken from $2\bar{2}8$ reflection (Ref#R30F328-11).

Both images ($\bar{2}28$ and $2\bar{2}8$ reflections) in Fig. 6-14 and 6-15 are consistent with the result of the previous sample shown in Fig. 6-10 in that the direction of \mathbf{H}_i at any given point are towards the metal. This clearly suggests that the Cu metal is in tension and places the silicon in compression at the interface. This result will be examined using micro-Raman spectroscopy and will be discussed in Section 6.3.3.

6.3.1.2 A comparison of Electroless and Sputtered Cu metallisation

The following topographs are from the *Pre-* and *Post-* Cu metallisation lift-off and damascene steps for both electroless and sputtered Cu metallisation. The results are divided into two sections; batch 1: lift-off pattern and batch 2: damascene pattern,

using back reflection and transmission topographs. All topographs are generated by the $\bar{2} \bar{2} 8$ harmonic reflection and the $1 1 1$ reflection for back-reflection and transmission techniques, respectively. Silicon samples were cut from wafers, grown in the $[001]$ direction. The copper line pattern was deposited on the silicon substrate parallel to the $\langle 110 \rangle$ directions.

BATCH 1: LIFT-OFF PATTERN

The images are separated into back-reflection topographs (LA-BRT and BRST) and transmission (LAT and ST) topographs and follow each step within the process.

BRT and BRST images

All topographs of the samples were generated by the $\bar{2} \bar{2} 8$ harmonic reflection with a penetration depth (t_p) of $65.7 \mu\text{m}$. Each set of metallisation lines is comprised of 6, 8, 10, 20, 60 and $100 \mu\text{m}$ wide structures. Only metal lines with 20 and $100 \mu\text{m}$ widths are considered in these discussions.

Step 2. Barrier Layer (Ti) 100 nm only---wafer no. B1, 2a

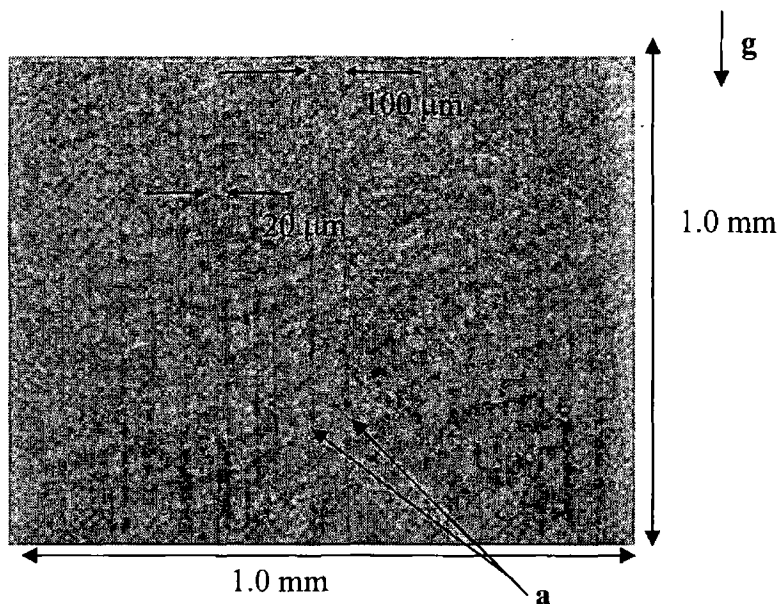


Figure 6-16 LA-BRT image of 100 nm thick Ti on Si wafer prior to Cu metallisation (B1, 2a: ref#R30F67-1).

Figure 6-16 taken from the $\bar{2} \bar{2} 8$ topograph illustrates dark lines in the region of the Ti line edges (Arrows **a**). These dark lines are created by stresses imposed in the Si substrate due to the Ti deposition and are observed as a black and white contrast or the extinction contrast effect which was explained in Chapter 2. The stresses are particularly large at the metallisation edges. The black and white contrast is greatest along the discontinuity generated at the edge of the Ti lines. The cross-section image is shown in Figure 6-17 below. The strain fields are observed clearly in this BRST image as a black contrast at the edge of the lines. It implies that large strains build up at the edges of the Ti lines (Arrows **b**).

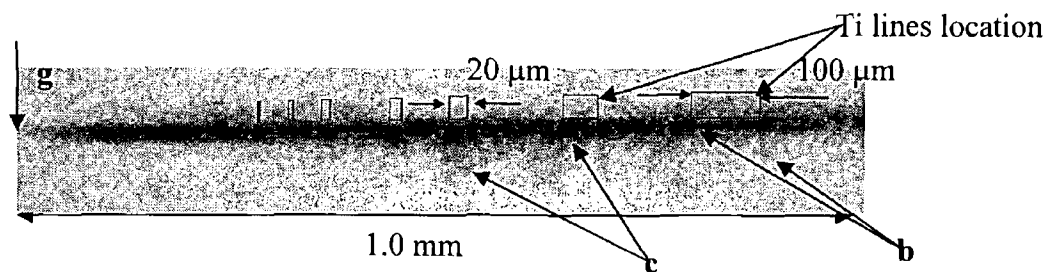


Figure 6-17 BRST image of 100 nm thick Ti lines on Si wafer (B1,2a: ref#R30F70-1).

Fig. 6-17 also shows that there is a significant strain near the middle of the lines as indicated by Arrow **c**. This occurrence is confirmed by FEM simulations of Copper metallisation on Si, which will be described later. The Cu seed layer was deposited on the Ti layer. The BRT and BRST topographs for these are shown below.

Step 4. Lift -off (20 nm Cu seed layer/ 100 nm Ti)---wafer no. D4P3d

The Cu seed layer was deposited on the Ti/Si sample and then the lift-off process was performed to remove the photoresist. The impact of the step is illustrated in Figure 6-18 and 6-19 for BRT and BRST images, respectively. The black and white contrast observed is darker in this process step, which is most likely due to greater strain fields being imposed on the Si substrate.

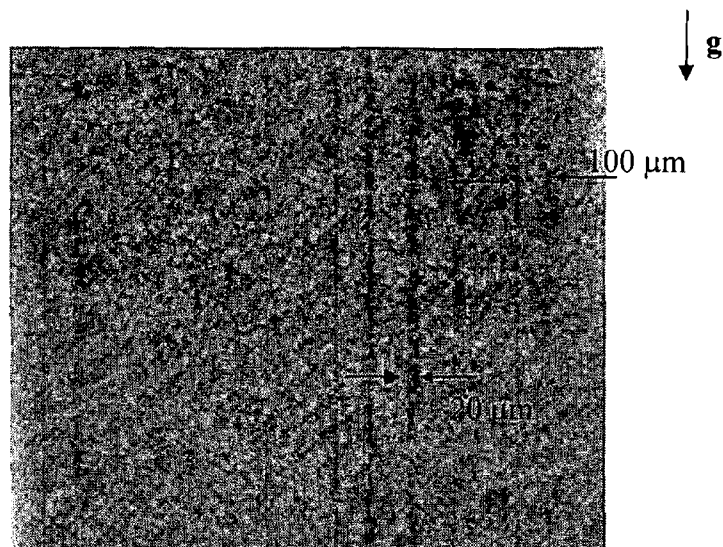


Figure 6-18 LA-BRT of 20 nm Cu seed layer/ 100 nm Ti lines on Si wafer (wfr.D4P3d: ref#R30F354-2).

The BRST (Fig. 6-19) corresponds to the LA-BRT image of Figure 6-18. The strain fields at the edge of the lines are clearer in this image compared with the BRST in Fig.6-9. However, the magnitude of the strains cannot be estimated in these images. Therefore, the values will be extracted later using micro-Raman spectroscopy.

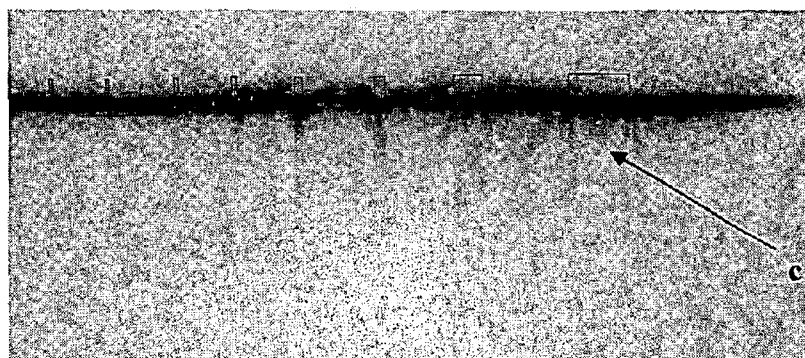


Figure 6-19 BRST image of 20 nm Cu seed layer/100 nm Ti lines on Si wafer (wfr.D4P3d:ref#R30F358-4).

Again, the stresses near the middle of the lines are also visible (Arrows c). Subsequent to the deposition of the thin Cu seed layer, the full Cu metallisation was

then deposited using the electroless deposition method. The method and conditions are explained in the earlier section on electroless Cu deposition.

*Step 5a. Cu metallisation (300 nm electroless Cu/ 20 nm Cu seed layer/ 100 nm Ti)--
-wafer no. D4P3D1 (s#99)*

Non-uniform strain fields imposed on the Si substrate are visible in the BRT image (Figure 6-20) below. It is possible that some delamination occurred after the Cu metallisation. However, topographic images suggest that the strain is much lower in the Si when the electroless Cu layer is deposited. This result will be examined using micro-Raman spectroscopy in section 6.3.3.

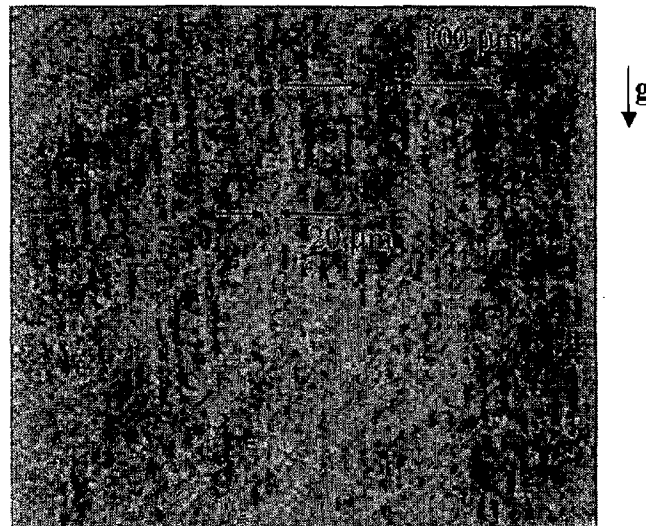


Figure 6-20 LA-BRT image of 300 nm electroless Cu/20 nm Cu seed/ 100 nm Ti lines on Si wafer (wfr.D4P3d1: ref#R30F315-2).

The BRST image (Fig. 6-21) also suggests lower strain at the line edges in this reflection ($\bar{2} \bar{2} 8$), when compared with the previous examples.

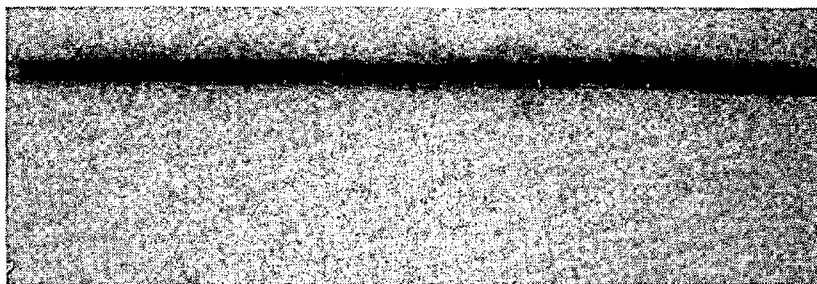


Figure 6-21 BRST image of 300 nm electroless Cu/20 nm Cu seed/ 100 nm Ti lines on Si wafer (wfr.D4P3d1: ref#R30F318-3).

Step 5b. Cu metallisation (300 nm Sputtered Cu/ 20 nm Cu seed layer/ 100 nm Ti)--- wafer no. B1, 4F

The black/white contrast is manifestly observed in both BRT and BRST images of 300nm Cu metallisation by the sputtering process as depicted in Figures 6-22 and 6-23, respectively.

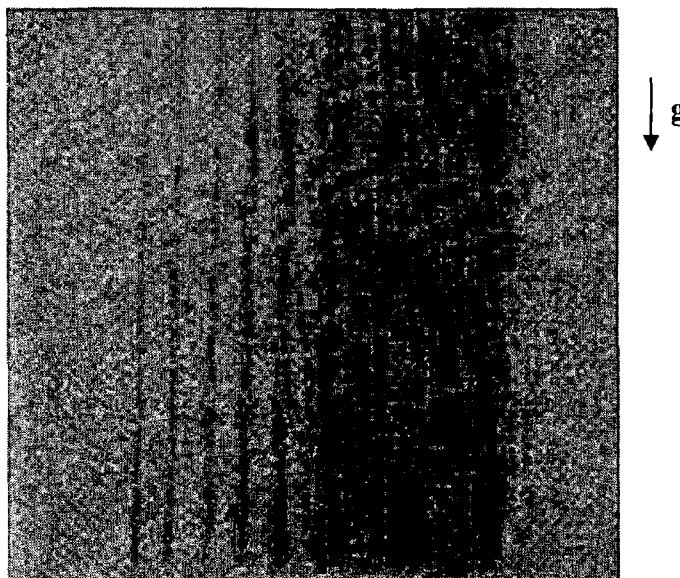


Figure 6-22 LA-BRT image of 300 nm sputtered Cu/ 20 nm Cu seed Cu/ 100 nm Ti on Si wafer (wfr. B1, 4F: ref# R30f352-1).

Using the sputtering technique, the strain field (Fig. 6-22), which is related to the black/white contrast appears to be greater, compared to the electroless Cu at the same

thickness (Fig. 6-20). The BRST image (Fig. 6-23) again shows that the greatest strains appear near the edge of the lines.

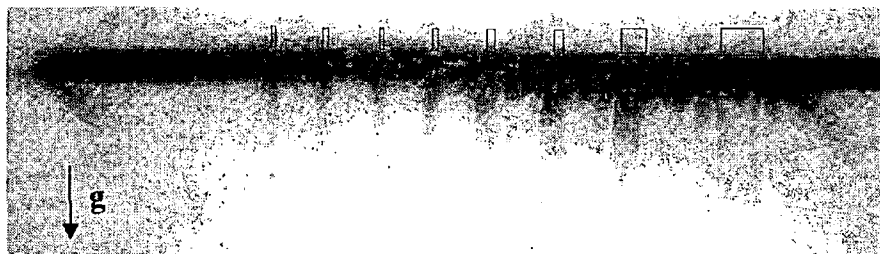


Figure 6-23 BRST image of 300 nm sputtered Cu/ 20 nm Cu seed Cu/ 100 nm Ti on Si wafer (wfr. B1, 4F: ref# R30f353-6).

However, the source of the different strain fields attributable to the sputtering and electroless copper metallisation will be analysed later in this chapter, i.e. section 6.3.3.

LAT and ST images

All LAT and ST images are taken from 111 reflections. During the experiment, the metal lines were set at the exit of the beam. The same samples and positions were used for BRT and BRST. The sample was turned 180° and tilted 18° to perform the LAT and ST experiments. The x-rays entered via the backside of the sample. The set-up is briefly described in Chapter 2. The results are shown below

Step 4. Lift-off (20 nm Cu seed layer/ 100 nm Ti)---wafer no. D4P3d

Figure 6-24 and 6-25 show the LAT and ST of the sample with a Cu seed layer on Ti and Si after the lift-off process. A similar black-white contrast is observed in this geometry.

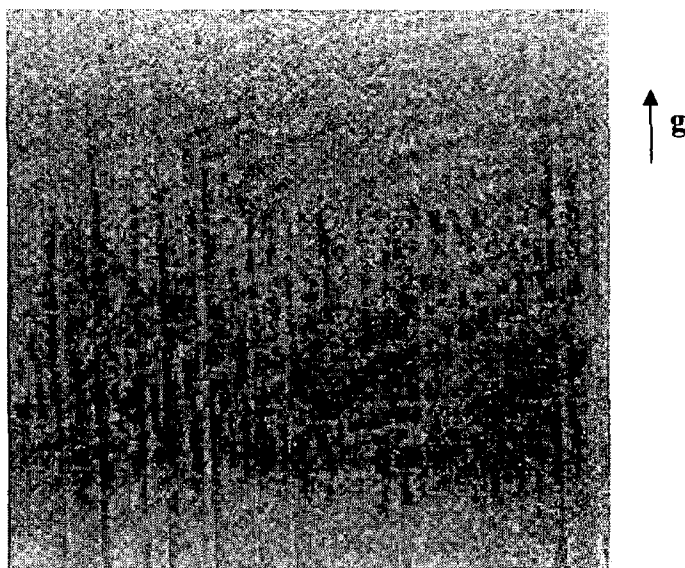


Figure 6-24 LAT image of 20 nm seed Cu/ 100 nm Ti on Si wafer (wfr.D4P3d: ref# R30F359-1)

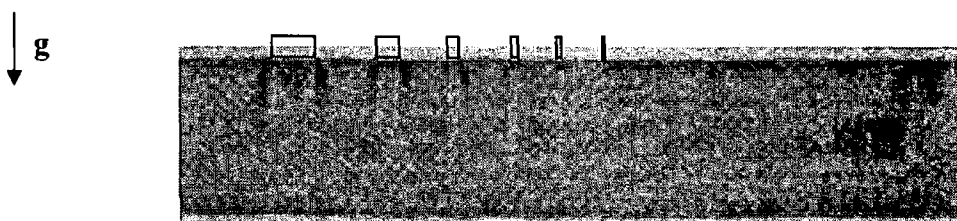


Figure 6-25 ST image of 20 nm seed Cu/ 100 nm Ti on Si wafer (wfr.D4P3d: ref#R30F365-2).

The ST image (Fig 6-25) displays the well-known Pendellösung or Kato fringes, which are explained in Chapter 2. The Pendellösung fringes are distorted due to the metal-induced strains in the Si substrate. The destruction of the fringes is greater at the edge of the metal lines, which implies that the strain fields most significant at the

edge of the metal lines. In addition, the strain fields increase with increasing the metal line width.

*Step 5a. Cu metallisation (300 nm electroless Cu/ 20 nm Cu seed layer/ 100 nm Ti)--
-wafer no. D4P3D1 (s#99)*

Non-uniform strains are visible in the LAT image (Fig. 2-26) as a non-homogenous black/white contrast along the length of the lines, which is similar to the BRT topograph.

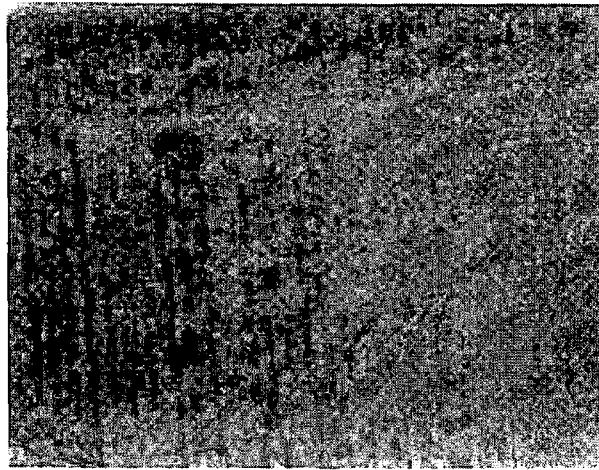


Figure 6-26 LAT image of 300 nm electroless Cu/ 20 nm seed Cu/ 100 nm Ti on Si wafer (wfrD4P3d1: ref#R30F325-1).

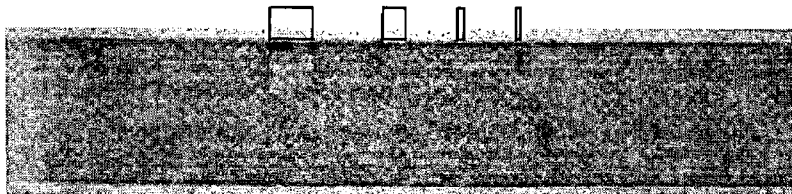


Figure 6-27 ST image of 300 nm electroless Cu/ 20 nm seed Cu/ 100 nm Ti on Si wafer (wfrD4P3d1: ref#R30F327-2).

Compared to step 4 (Fig. 6-25), the strains appear to be somewhat lower when depositing electroless Cu, as the Kato fringe distortion is much less significant.

Step 5b. Cu metallisation (300 nm Sputtered Cu/ 20 nm Cu seed layer/ 100 nm Ti)--- wafer no. B1, 4F

The strain fields generated by sputtered Cu seems to be different from those created by electroless Cu.

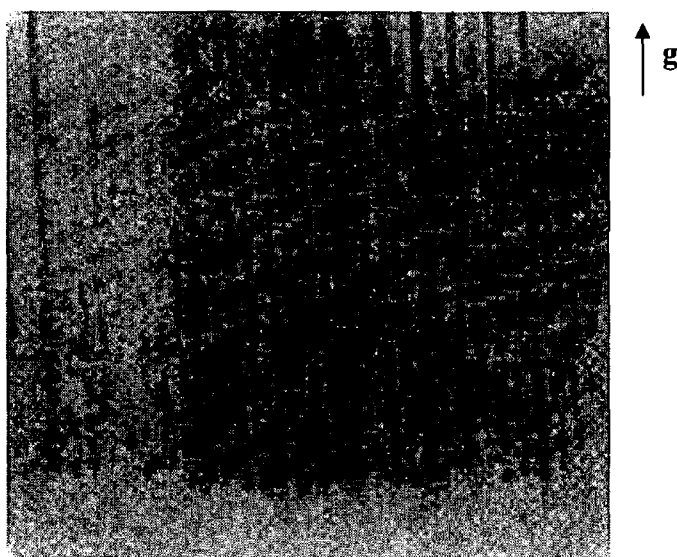


Figure 6-28 LAT image of 300 nm sputtered Cu/ 20 nm Cu seed/ 100 nm Ti lines on Si wafer (wfr. B1, 4F: ref#R30F341-1).

The ST image in this step is taken from standard film, which has a lower resolution. The grain size on the film is about 1 μm in contrast with a grain size of about 40 nm for VRP-M film. However, Figure 6-29 displays a similar tendency to the LAT image.

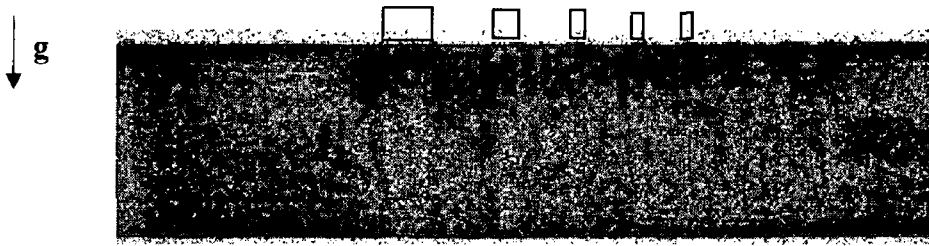


Figure 6-29 ST image of 300 nm sputtered Cu/ 20 nm Cu seed/ 100 nm Ti lines on Si wafer (wfr.B1,4F: ref#R30F344-2).

The destruction of Kato fringes due to sputtered Cu is more obvious than for electroless Cu. The orientational contrast is also observed in this image (Fig. 2-29) but is not significant enough to make a measurement.

BATCH 2: DAMASCENE PATTERN

Similar to batch 1, the images are separated into back-reflection topographs (large area, BRT and section, BRST) and transmission (large area, LAT and section, ST) topographs following each process step individually.

BRT and BRST images

All topographs generated by the BRT and BRST methods are taken with the $\bar{2} \bar{2} 8$ harmonic reflection with a penetration depth (t_p) of 65.7 μm .

Step 2. RIE etch (SiO_2 on Si)---wafer no. DCU12

At this step, the SiO_2 was etched to create a damascene pattern. The LA-BRT and BRST are shown in Figures 6-30 and 6-31.

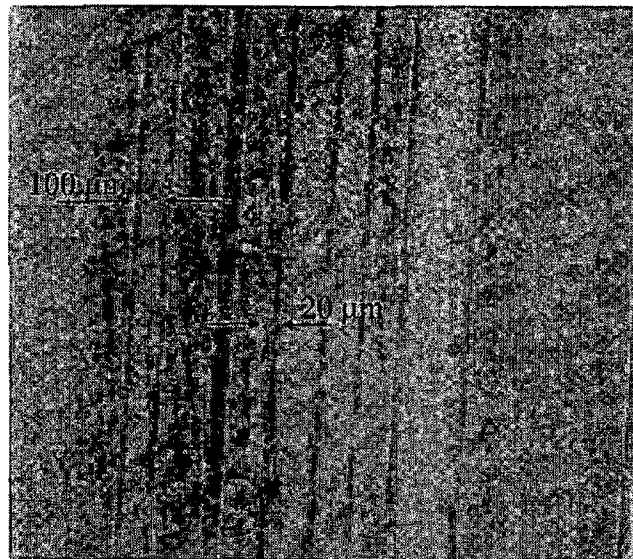


Figure 6-30 LA-BRT image of RIE etching on SiO_2 of Si wafer (wfr.DCU12: ref#R30F406-5).

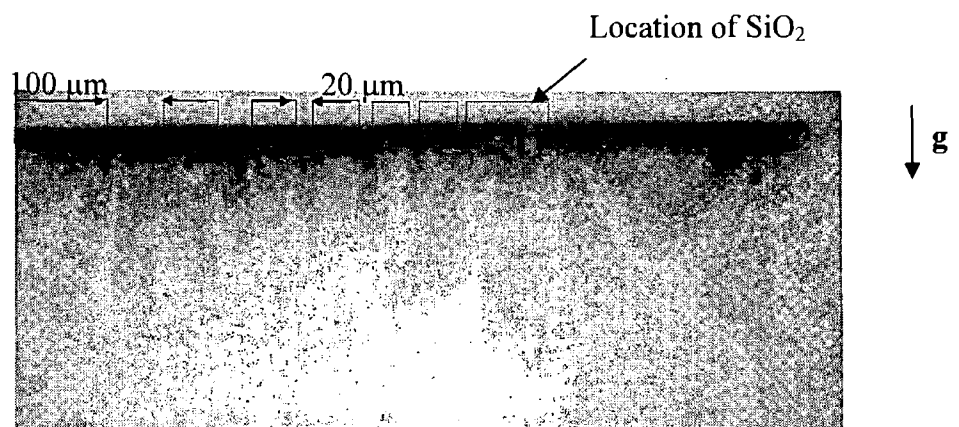


Figure 6-31 BRST image of RIE etching on SiO_2 of Si wafer (wfr. DCU12: ref#R30f409-2).

Figure 6-30 illustrates the black/white contrast in the section transmission topograph. The high strains in the Si substrate due to the SiO₂ layer are observed clearly in this image at the edge and underneath the oxide lines. The strain fields appear to be larger in this image due to a high thermal in the oxidation process.

Step 7a. CMP 300 nm electroless Cu/ 20 nm Cu Seed/ 100 nm Ti ---wafer no. DCU2

The electroless Cu was deposited on Cu seed and Ti layers and then the excess Cu was removed using chemical mechanical polishing. The BRT and BRST are depicted in Figures 6-32 and 6-33, respectively.

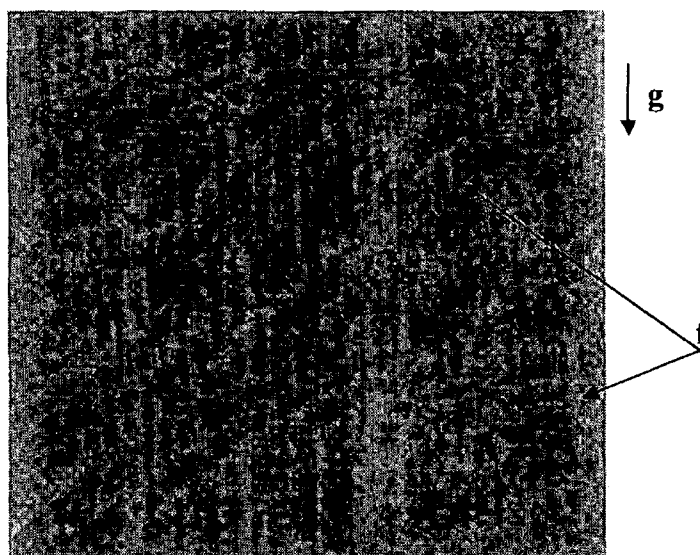


Figure 6-32 LA-BRT image of 300 nm electroless Cu/ 20 nm Cu seed/ 100 nm Ti on damascene pattern after CMP process (wfr.DCU2: ref#R30F378-2).

As before, the LA-BRT (Fig. 6-32) depicts a non-uniformity in the stresses/strains imposed on the Si due to the excess materials i.e. Ti, Cu seed and electroless Cu (Arrows **f**).

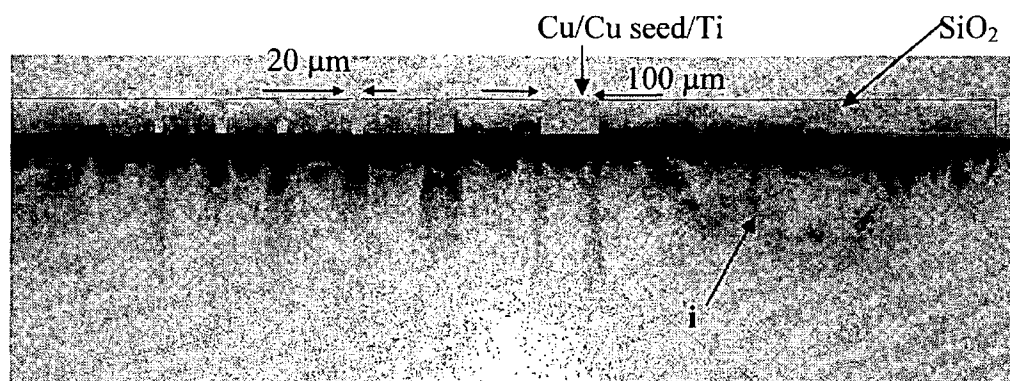


Figure 6-33 BRST image of 300 nm electroless Cu/ 20 nm Cu seed/ 100 nm Ti on damascene pattern after CMP process (wfr. DCU2: ref#R30F382-4).

The BRST image (Fig 6-33) shows the usual black/white stain related contrast. In addition, a number of oxygen related defects are visible as small black dots near the surface of the Si [171]. These are indicated by Arrows **i** in the topograph.

Step 7b. CMP 300 nm sputtered Cu/ 20 nm Cu Seed/ 100 nm Ti ---wafer no. DCU10

The non-uniform strain fields are also visible in the following LA-BRT image (Fig. 6-34) due to the CMP process as indicated in Arrows **f**.

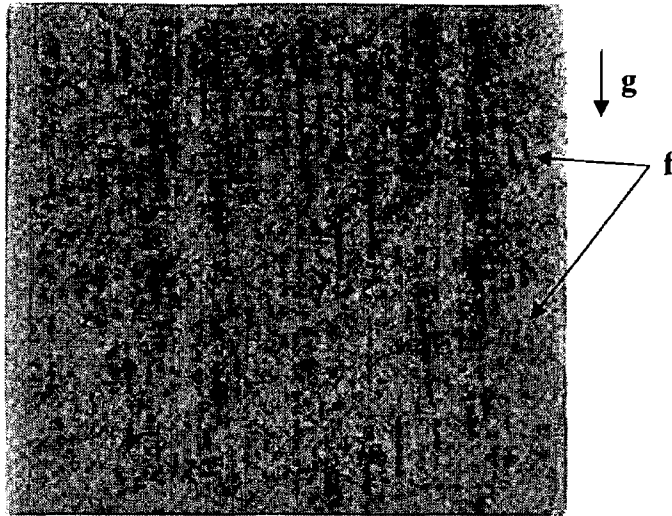


Figure 6-34 LA-BRT image of 300 nm sputtered Cu/ 20 nm Cu seed/ 100 nm Ti on damascene pattern after CMP process (wfrDCU10: ref#R30F366-2).

Similar to the BRST image of the electroless Cu sample, the black/white contrast and a number of black dots (oxygen related defects) are observed in the BRST image of sputtered Cu (Fig. 6-35). However, little if any orientational contrast is visible.

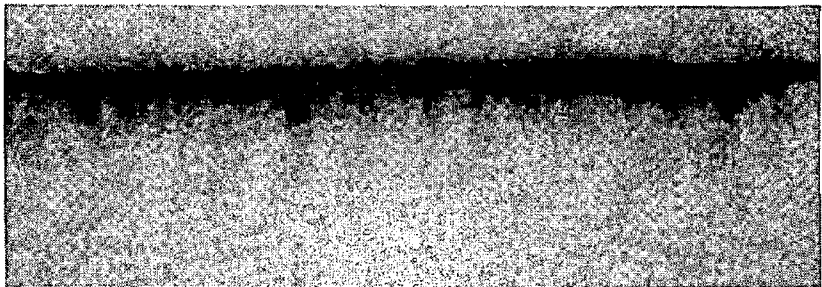


Figure 6-35 BRST image of 300 nm sputtered Cu/ 20 nm Cu seed/ 100 nm Ti on damascene pattern after CMP process (wfrDCU10: ref#R30F370-4).

LAT and ST images

The LAT and ST images are generated by the $1\ 1\ 1$ reflection. The same samples and positions were used for BRT and BRST. The sample was turned 180° and tilted 18° to perform the LAT and ST experiments. The x-rays entered via the backside of the sample.

Step 2. RIE etch (SiO_2 on Si)---wafer no. DCU12

The black/white contrast is visible in the LA-BRT image (Figure 6-36). Arrow m is the region of a pattern defect during processing. The ST image (Fig. 6-37) shows highly distorted Pendellösung fringe patterns due to the oxidation process-induced strain. This image (Fig. 6-36) is taken from a standard film, with a lower resolution than in the other images. In addition, the film itself also processes some artefacts, observed as black dots, and these are not oxygen related defects.

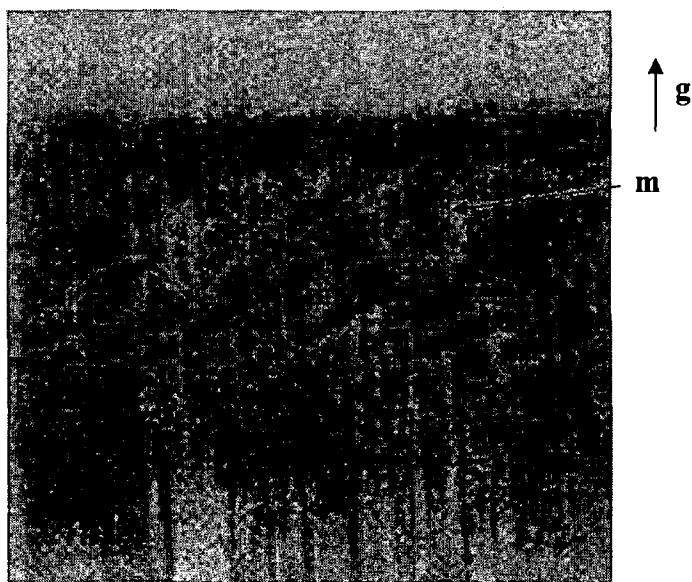


Figure 6-36 LAT image of RIE etched SiO_2 on Si wafer (wfr. DCU12: ref#R30F405-1).

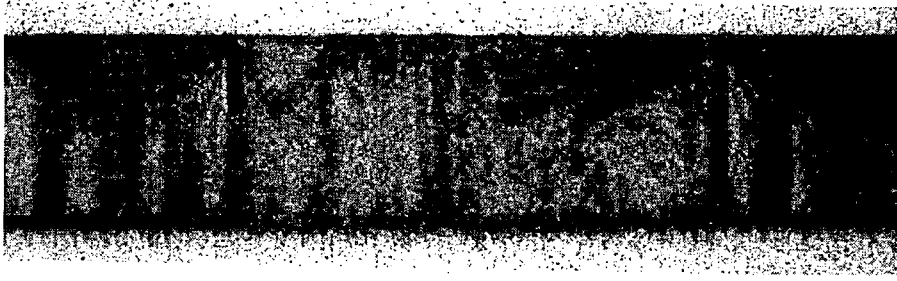


Figure 6-37 ST image of RIE etched on SiO₂ on Si wafer (wfr. DCU12: ref#R30F411-2).

Step 7a. CMP 300 nm electroless Cu/ 20 nm Cu Seed/ 100 nm Ti ---wafer no. DCU2

The strain fields, most likely due to extinction contrast at the edges of metal lines are less intense after the deposition of the electroless Cu metallisation and CMP processing. This phenomenon was observed by Sullivan [146], i.e. the oxide surrounding the metal line relaxes the strain in the metal in proportion to the ratio of the elastic moduli of the two materials given as $\epsilon_m = \epsilon_{ox} \left(\frac{E_{ox}}{E_m} \right)$, where ϵ_m , ϵ_{ox} are the strains imposed on metal and oxide layers, respectively, and E_m , E_{ox} are the elastic moduli of the metal and oxide layers, respectively. Sullivan observed that the surrounding oxide absorbed elastically the lateral metal expansion during any annealing process and then the metal returned back to its starting point. For the vertical metal expansion, the relaxation by the surrounding oxide takes up only a portion of the strains because the volume is constrained by the vertical trench wall. However, the rest of strain can be captured during the deposition of the overlying oxide [146].

The LAT and ST taken from 111 reflections are shown in Figure 6-38 and 6-39, respectively.

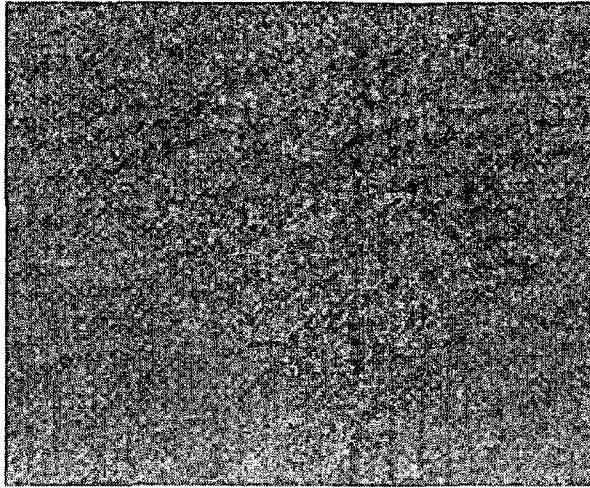


Figure 6-38 LAT image of 300 nm electroless Cu/ 20 nm Cu seed/ 100 nm Ti on damascene pattern (wfr. DCU2: ref# r36f121).

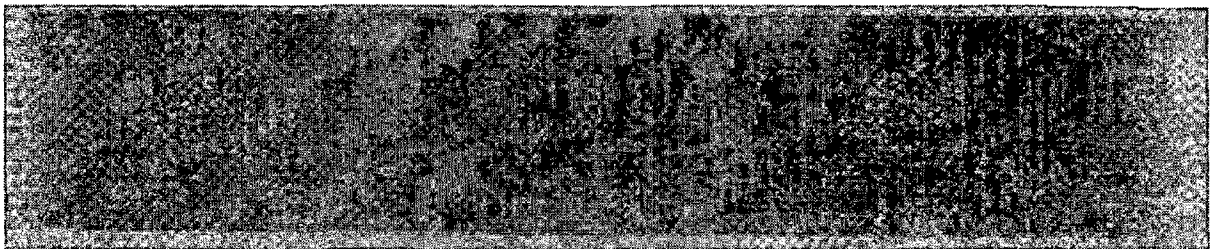


Figure 6-39 ST image of 300 nm electroless Cu/ 20 nm Cu seed/ 100 nm Ti on damascene pattern (wfr. DCU2: ref# r30f392-1).

The distortion of the lattice planes near the metal edges appears to be much less than the *Pre*-metallisation (SiO_2 on Si wafer) as the intensity of black/white contrast is lower. It implies that the depositions of Cu, seed layer and barrier layer (Ti) relieves some residual strain fields, which are generated due to the oxidation process. However, the oxygen related defects are not observed in this reflection due to an unsuitable exposure time during measurement.

Step 7b. CMP 300 nm sputtered Cu/ 20 nm Cu Seed/ 100 nm Ti ---wafer no. DCU10

The LAT image (Fig. 6-40) of the sample with the sputtered Cu displayed a large distribution of oxygen related defects in the Si wafer across the sample.

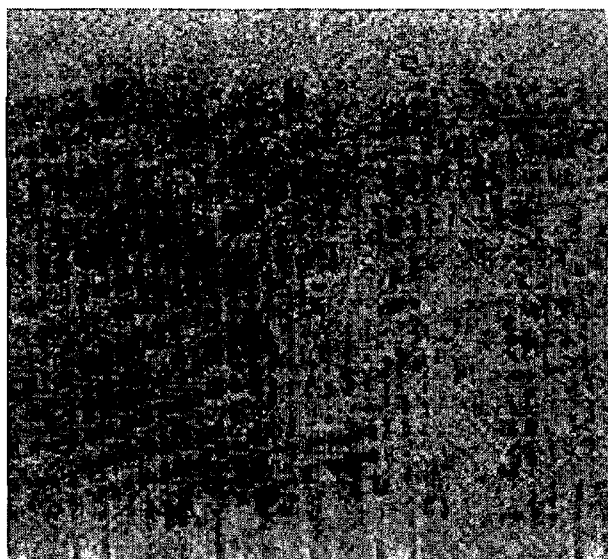


Figure 6-40 LAT of 300 nm electroless Cu/ 20 nm Cu seed/ 100 nm Ti on damascene pattern (wfr.DCU10: ref#R30F371-1).

These black dots, which are images of oxygen related defects are also easily visible throughout the sample depth in the ST of Figure 6-41. Then could be due to thermal processing during the sputtering and CMP steps. For the sputtering step, the temperature inside the chamber could be up to 200°C and the sample was polished with NH₄OH (ammonia hydroxide) and BTA during the CMP step. BTA is a mono-polymer that forms to protect copper during the polishing process. However, it can be cleared away by heating up to 300°C. In addition, the Kato fringes have totally disappeared due to the presence of the large numbers of the oxygen related defects/precipitates. The orientational contrast is visible but not considerable enough to measure.

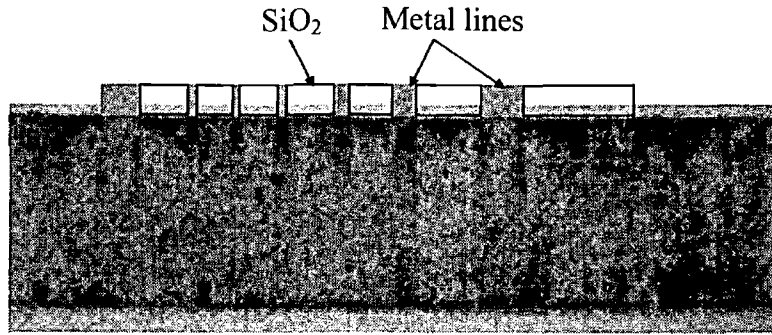


Figure 6-41 ST of 300 nm electroless Cu/ 20 nm Cu seed/ 100 nm Ti on damascene pattern (wfrDCU10: ref#R30F377a-2).

6.3.1.2 Temperature Dependence of the Electroless and Sputtered Cu Metallisation Processing Induced Strain Fields in Si Substrate

To study the temperature dependence of the Cu metallisation process induced stress distributions in the Si wafers, the measurements were performed on the same samples as for the previous measurements. The samples were mounted on a heating stage. The x-ray topographs were then recorded at room temperature (RT), 100, 200, 300 and 400 °C in both LA-BRT and BRST modes.

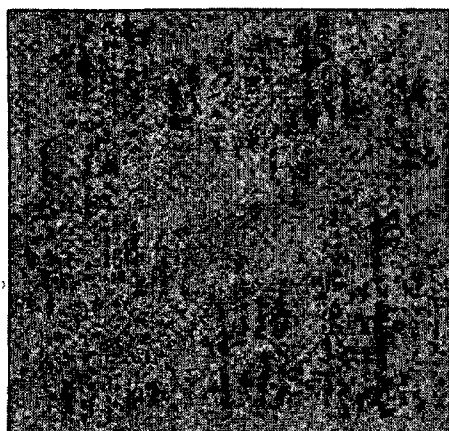
Again, the topographs are examined for the *Pre-* and *Post-* Cu metallisation cases of lift-off and damascene patterns for both electroless and sputtered Cu metallisation. The results are divided into 2 sections; batch 1: lift-off pattern and batch 2: damascene pattern. All topographs are generated by the $\bar{2} \bar{2} 8$ harmonic reflection with a penetration depth (t_p) of 65.7 μm . Silicon samples were cut from wafers, grown in the [001] direction. The copper line pattern was deposited on the silicon substrate parallel to the $\langle 110 \rangle$ direction. Each set of metallisation lines is comprised of 6, 8, 10, 20, 40, 60 and 100 μm wide structures. Only the lines, of width 20 and 100 μm , are considered in these discussions.

BATCH 1: LIFT-OFF PATTERN

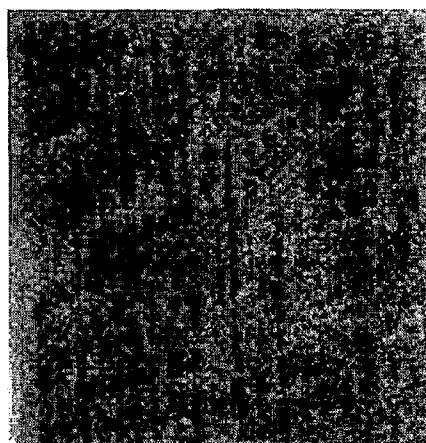
The results for *Pre-metallisation* (Step 4: 20 nm Cu seed/ 100 nm Ti on Si wafer) and *Post-metallisation* (Step 5a: 300 nm electroless Cu/ 20 nm Cu seed/ 100 nm Ti on Si wafer and Step 5b: 300 nm sputtered Cu/ 20 nm Cu seed/ 100 nm Ti on Si wafer) will be examined in this discussion.

Step 4. Lift-off (20 nm Cu seed layer/ 100 nm Ti)---wafer no. D4P3d

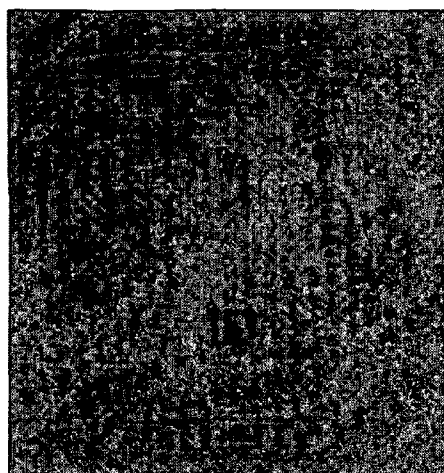
BRT and BRST images for RT, 100, 200, 300 and 400 °C are illustrated in Figure 6-42 and 6-43, respectively.



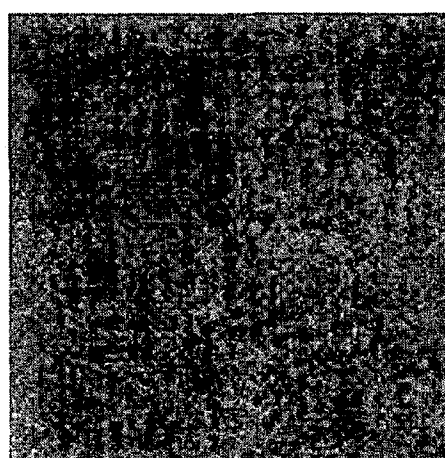
(a)



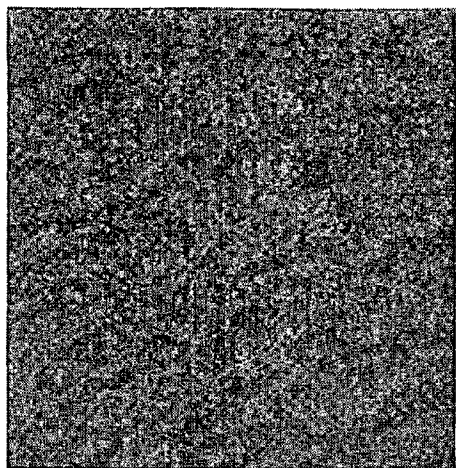
(b)



(c)

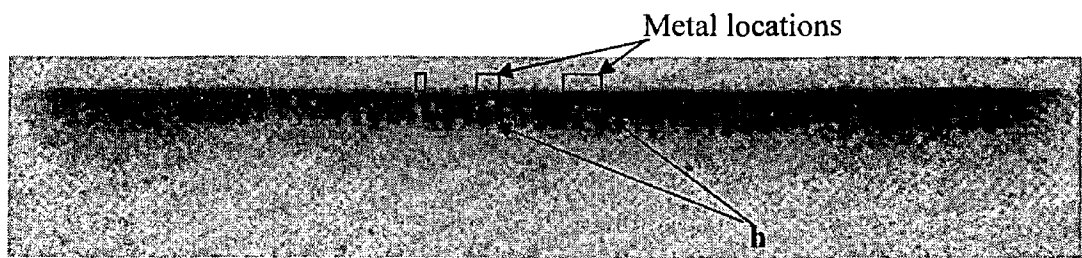


(d)

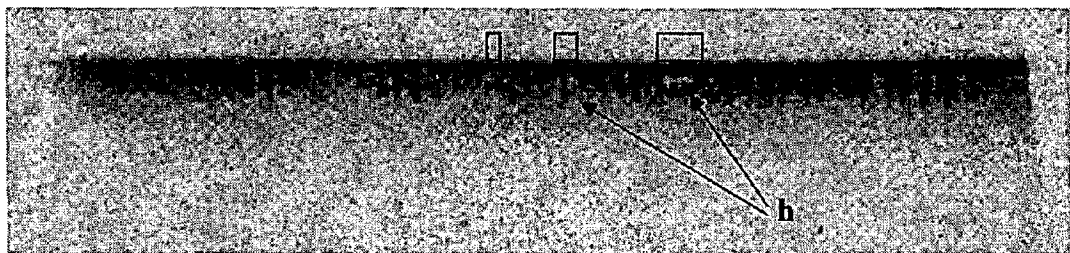


(e)

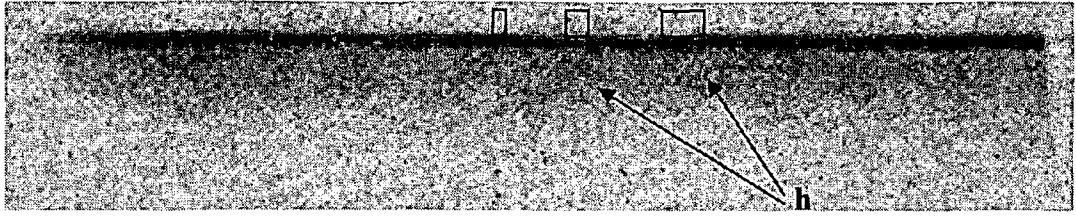
Figure 6-42 BRT images for *Pre-metallisation* step (20 nm Cu seed/ 100 nm Ti on Si wafer) at (a) RT, (b) 100 °C, (c) 200°C, (d) 300°C and (e) 400°C (wfr. D4P3D: ref # r36f38, r36f40, r36f42, r36f44 and r36f46).



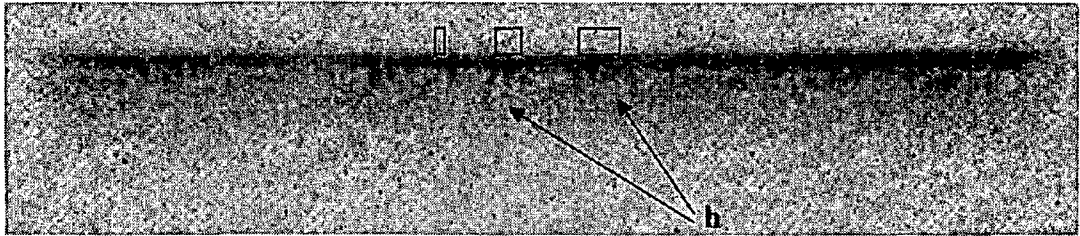
(a)



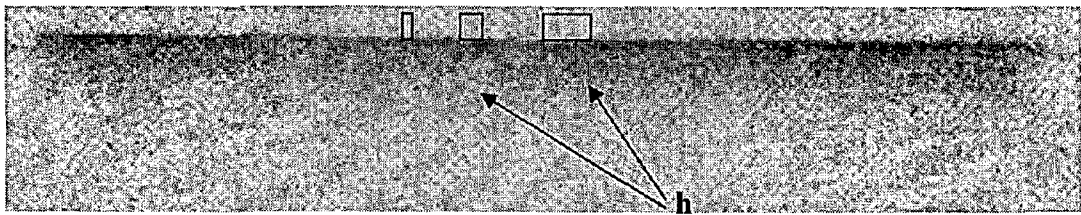
(b)



(c)



(d)



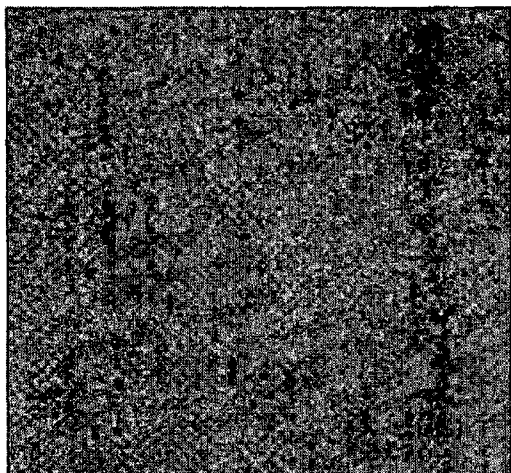
(e)

Figure 6-43 BRST images for *Pre-metallisation* step (20 nm Cu seed/ 100 nm Ti on Si wafer) at (a) RT, (b) 100 °C, (c) 200°C, (d) 300°C and (e) 400°C (wfr. D4P3D: ref # r36f39, r36f41, r36f43, r36f45 and r36f47).

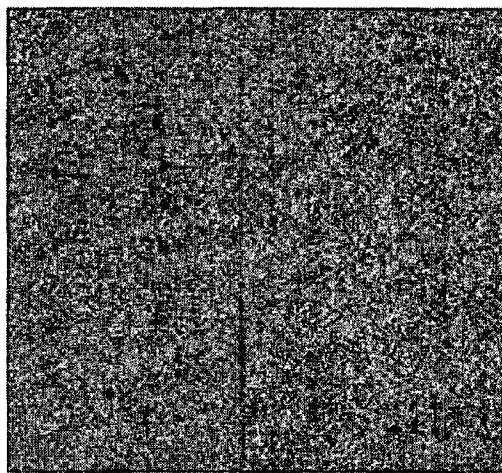
The topographs for both LA-BRT and BRST show that the strain fields near the edge of the metal lines (Arrows **h**) are relieved when the sample was heated up to 200°C. When the sample was continuously heated up to 300°C, the strain fields became more intense at the edge of the metal lines and the strains appear to extend deeper in the Si than that at RT. Subsequently, the strain field changes little at 400°C.

Step 5a. Cu metallisation (300 nm electroless Cu/ 20 nm Cu seed layer/ 100 nm Ti)---wafer no. D4P3D1 (s#99)

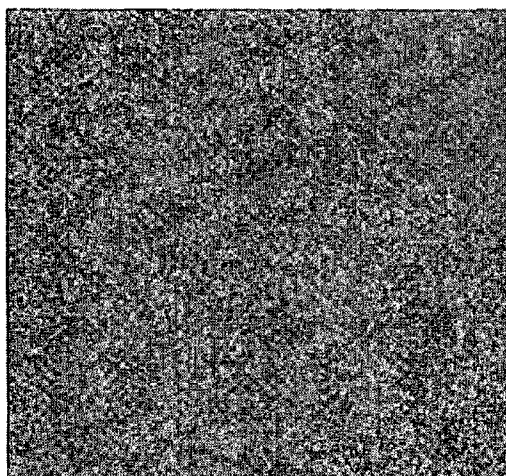
The *Post*-metallisation of electroless Cu was investigated and illustrated in Figure 6-44 for LA-BRT.



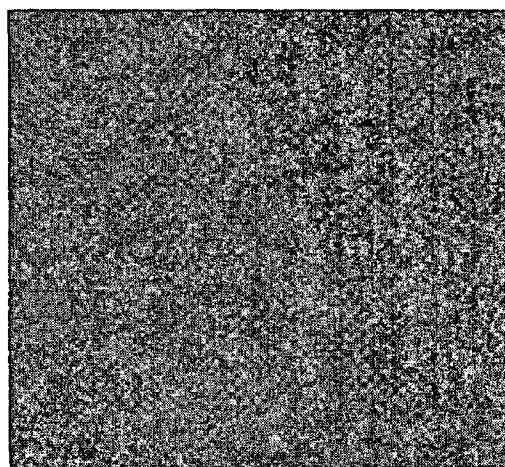
(a)



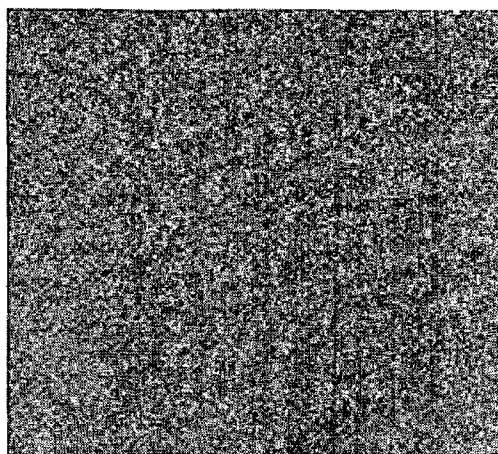
(b)



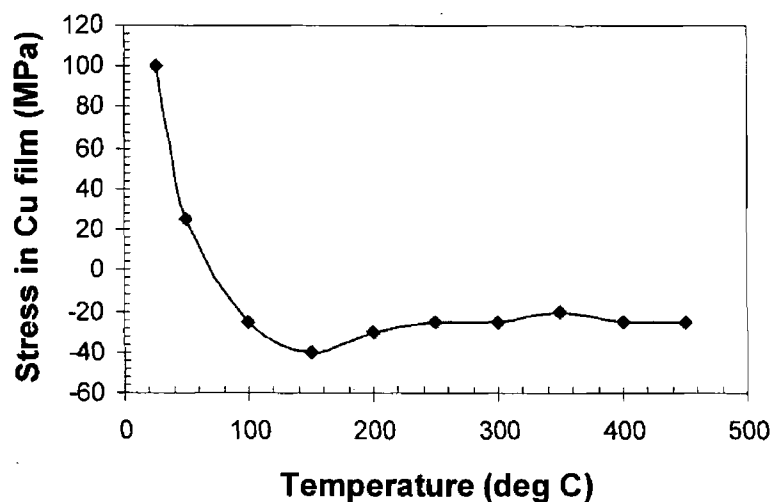
(c)



(d)



(e)



(f)

Figure 6-44 LA-BRT images for *Post-metallisation* step (300 nm electroless Cu/ 20 nm Cu seed/ 100 nm Ti on Si wafer) at (a) RT, (b) 100 °C, (c) 200°C, (d) 300°C, (e) 400°C (wfr. D4P3D: ref # r36f5-1, r36f9, r36f11, r36f13 and r36f15) and (f) the stress in Cu film from Reidel *et al.* [178].

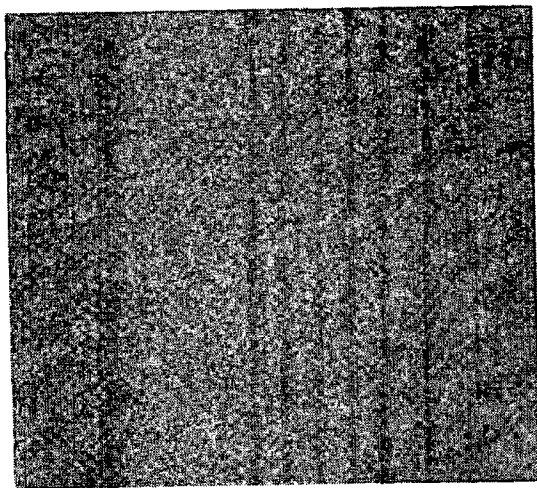
The LA-BRT results suggest that the strain fields in the Si wafers are much less intense for the *Post-metallisation* samples. However, when the sample was heated, the strains became greater as the extinction contrast at the metal edges is greater in intensity. The greatest contrast intensity is at the maximum temperature of 400°C.

In this case, the BRST measurement could not be taken due to a damaged beam collimation slit. Riedel *et al.* [178] investigated this phenomenon in the 500 nm thick Cu film deposited by CVD at wafer condition 170 °C. Although the Cu was deposited by different technique, a similar phenomenon was observed as the stress in the Cu film changed from tensile to compressive during heating as illustrated in Figure 6-44 (f). This implies that the stress imposed on Si due to the Cu metallisation and temperature dependence is transformed from compression to tension. In addition, the stress became zero at a temperature about 75 °C. This could be the reason why the contrast intensity as stress in Si in the topograph (Fig. 6-44) is greater when the temperature is increased to 400 °C. At room temperature, the Cu film put Si into either tensile or compressive, and the stress imposed in Si liberated at elevated temperature ($T = 100\text{--}200\text{ °C}$) as the black/white contrasts in topographs became weak in Fig. 6-44 (b-c). Subsequent, the stress in Si underneath the Cu film transform to the opposite state at increasing temperature ($T = 300\text{--}400\text{ °C}$) as the black/white contrasts in topographs Fig. 6-44 (d-e) are greater in intensity. This heating temperature-stress transformation phenomenon was simulated using FEM and will be described later in this chapter.

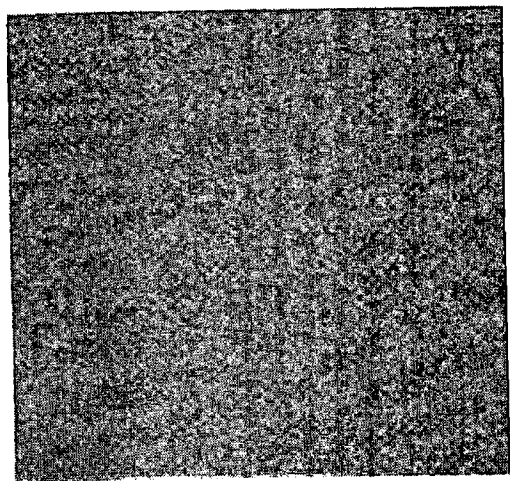
Step 5b. Cu metallisation (300 nm Sputtered Cu/ 20 nm Cu seed layer/ 100 nm Ti)--- wafer no. B1, 4F

LA-BRT and BRST images of the sample at RT, 100, 200, 300 and 400 °C are shown in Figure 6-45 and 6-46, respectively. From the LA-BRT topographs, the extinction contrast created due to the sputtered Cu deposition shows a greater intensity than that of the electroless Cu at room temperature. A black/white contrast at the line edges is clearly visible in both LA-BRT and BRST topographs at room temperature. As a function of temperature (Fig. 6-45(a) – (e)), the strain fields appear to be relieved when the temperature increases to 200°C, after which the strain fields in Si appear to intensify, as the black/white intensities are greater in the topographs for 300 and 400°C. Again, a train transition through a zero strain point, as per Riedel [178], could also be occurring in this case. However, the strain-induced contrast is

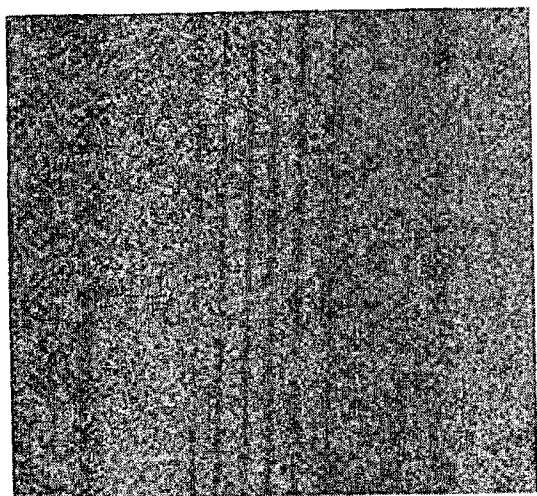
still smaller than for the room temperature case. The BRST images show a similar tendency to the LA-BRT topographs.



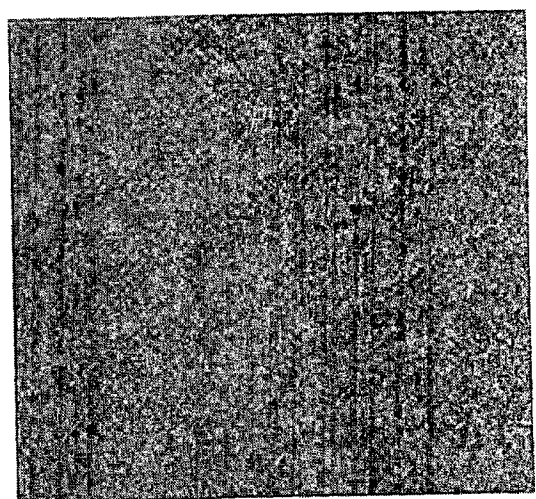
(a)



(b)



(c)

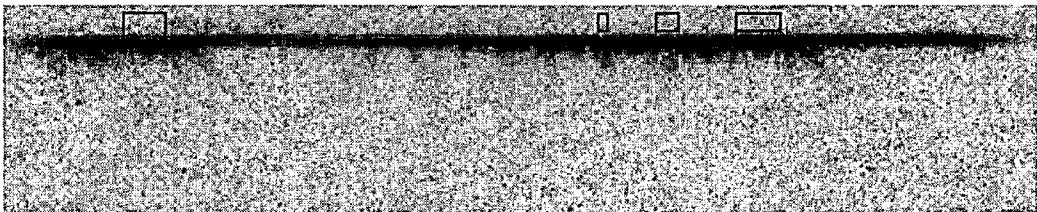


(d)

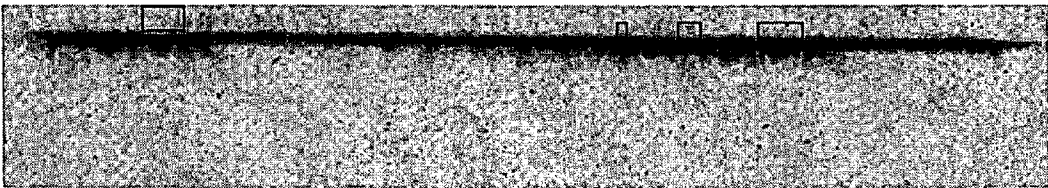


(e)

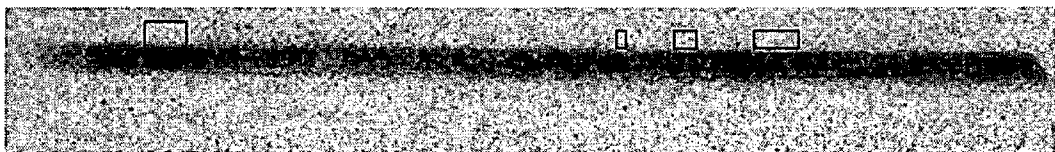
Figure 6-45 LA-BRT images of *Post-metallisation* (300 nm sputtered Cu/ 20 nm Cu seed/ 100 nm Ti on Si wafer) at temperature (a) RT, (b) 100°C, (c) 200°C, (d) 300°C and (e) 400°C (wfr. B1,4F: ref # r36f18, r36f20, r36f22, r36f24 and r36f26).



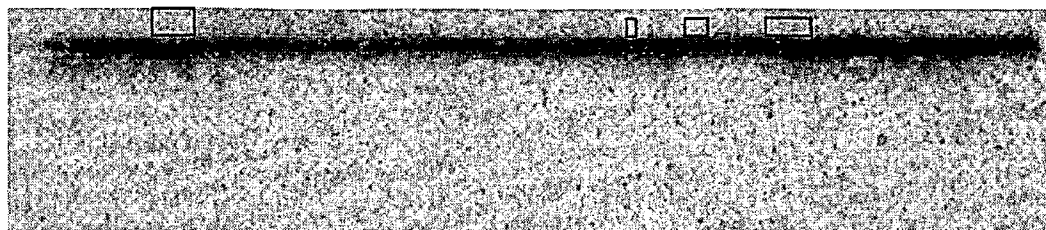
(a)



(b)



(c)



(d)

Figure 6-46 BRST images of the *Post*-metallisation sample (300 nm sputtered Cu/ 20 nm Cu seed/ 100 nm Ti on Si wafer) at (a) RT, (b) 100°C, (c) 200°C and (d) 300°C (wfr. B1,4F: ref # r36f19, r36f21, r36f23 and r36f25).

BATCH 2: DAMASCENE PATTERN

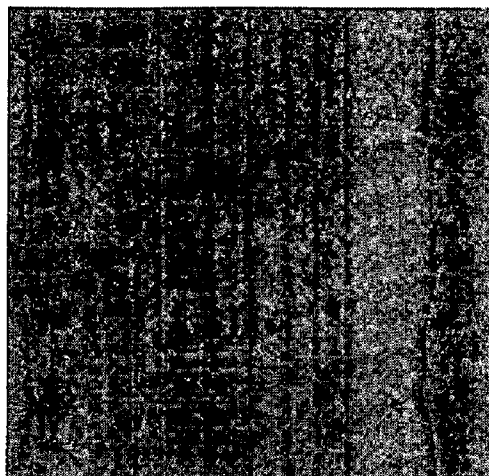
Similar to batch 1, the samples (as in the previous section) were heated to RT, 100, 200, 300 and 400 °C. The LA-BRT and BRST images were recorded. The topographs of the *Pre*- (Step 2) and *Post*-Cu metallisation samples (Step 7(a)-(b)) are illustrated herewith.

Step 2. RIE etch (SiO₂ on Si)---wafer no. DCU12

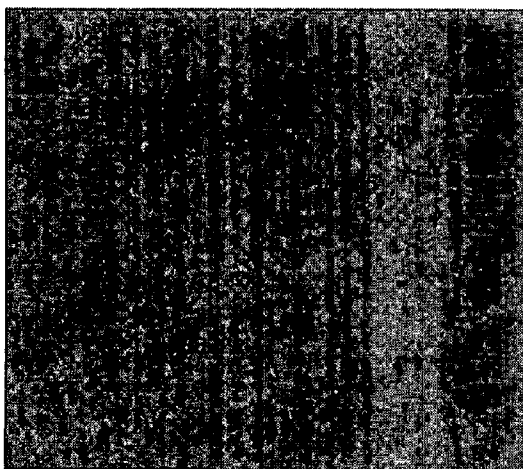
The LA-BRT images (Figure 6-47 (a)- (e)) indicate that the strain fields imposed in the Si substrate at the pattern edges do not differ greatly when the temperature was varied.



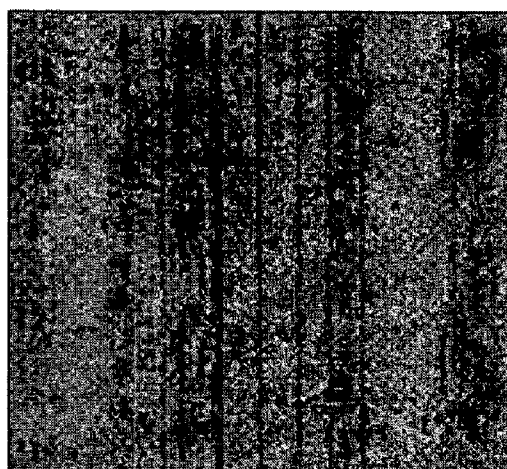
(a)



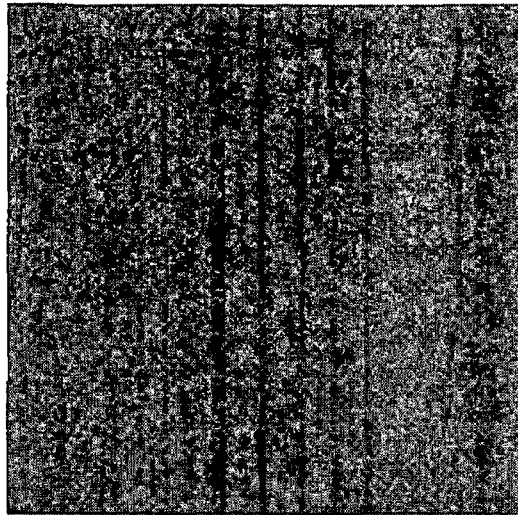
(b)



(c)



(d)



(e)

Figure 6-47 LA-BRT of the *Pre*-Cu metallisation sample (SiO_2 pattern on Si wafer) at (a) RT, (b) 100, (c) 200, (d) 300 and (e) 400 °C (wfr.DCU12: ref#r36f83, r36f85, r36f87, r36f89 and r36f91).

However, the BRST topographs (Fig. 6-48) do seem to show that the strain fields are relieved when the temperature is increased. Nevertheless, the temperature is still not high enough to relieve the entire strain field in the Si substrate due to the oxidation process.



(a)



(b)



(c)



(d)

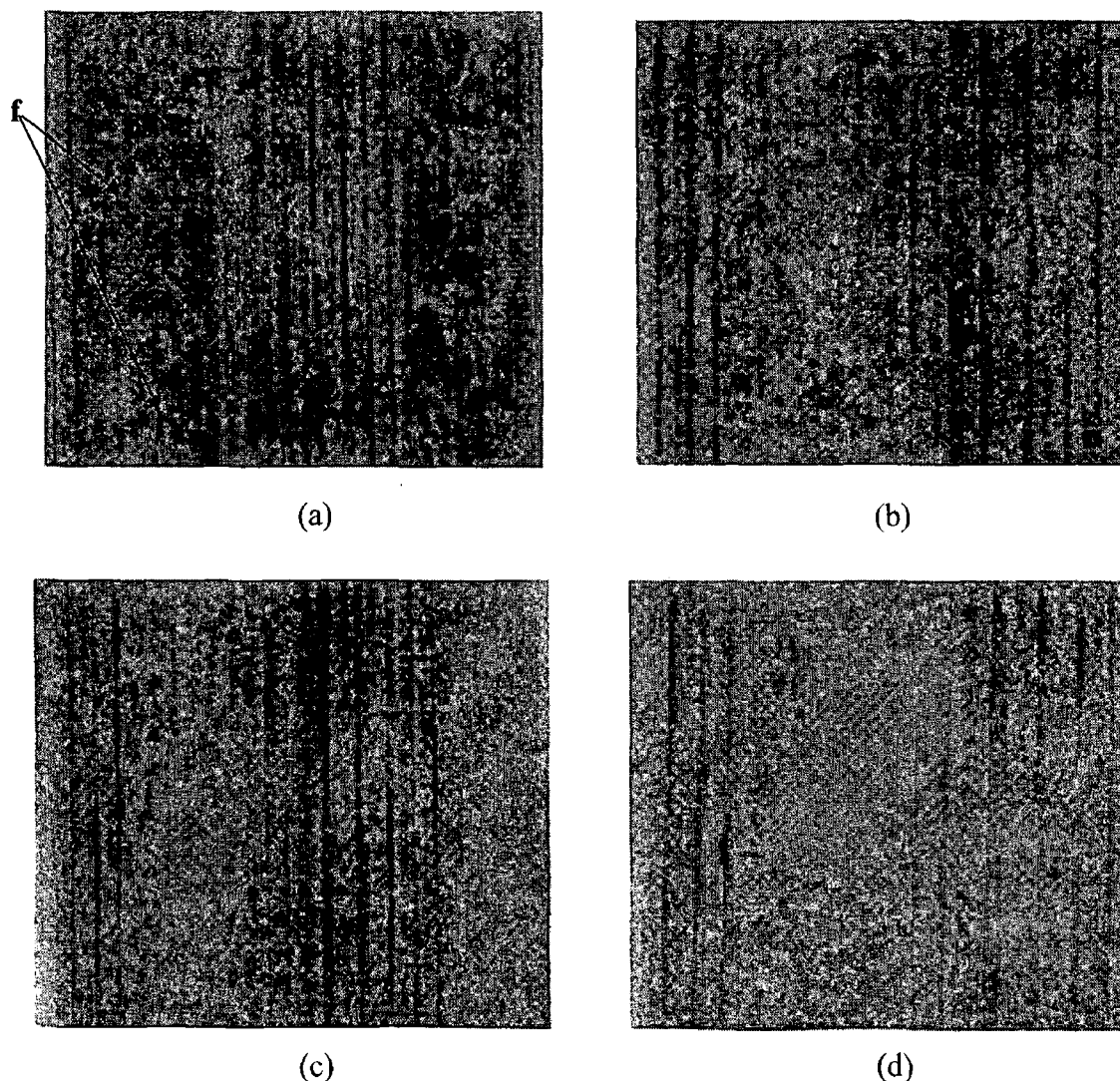


(e)

Figure 6-48 BRST images of the *Pre-Cu* metallisation sample (SiO_2 pattern on Si wafer) at (a) RT, (b) 100, (c) 200, (e) (d) 300 and (e) 400°C (wfr.DCU12: ref#r36f84, r36f86, r36f88, r36f90 and r36f92).

Step 7a. CMP 300 nm electroless Cu/ 20 nm Cu Seed/ 100 nm Ti ---wafer no. DCU2

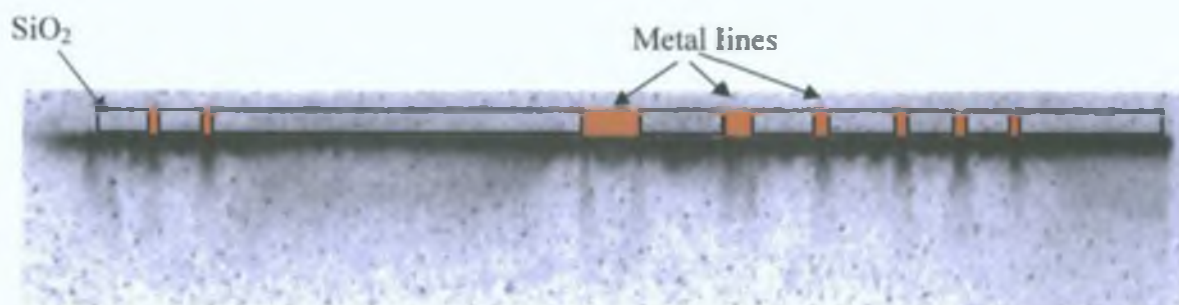
Figures 6-49(a)- (e) are the LA-BRT images of the electroless Cu sample after the CMP process. The images show that there are inhomogeneous strain fields imposed on the Si, perhaps due to residual metal on the surface after the CMP process (Arrows **f**). At room temperature, the strains in Si for the *Post*-electroless Cu metallisation are smaller than those of the *Pre*-Cu metallisation as the extinction contrast is lower in intensity. At the highest temperature, most strains in the Si wafer appear to be relieved for the *Post*-electroless Cu metallisation. This indicates that most of the strain fields in the Si wafer are liberated after the electroless Cu metallisation. This can be confirmed by BRST images shown in Figures 6-50 (a)-(e).





(e)

Figure 6-49 LA-BRT images of the *Post-Cu* metallisation sample (300 nm electroless Cu/ 20 nm Cu seed/ 100 nm Ti on damascene patterned Si wafer) at (a) RT, (b) 100, (c) 200, (d) 300 and (e) 400°C (wfr.DCU2: ref#r36f95, r36f97, r36f99, r36f101 and r36f103).



(a)



(b)

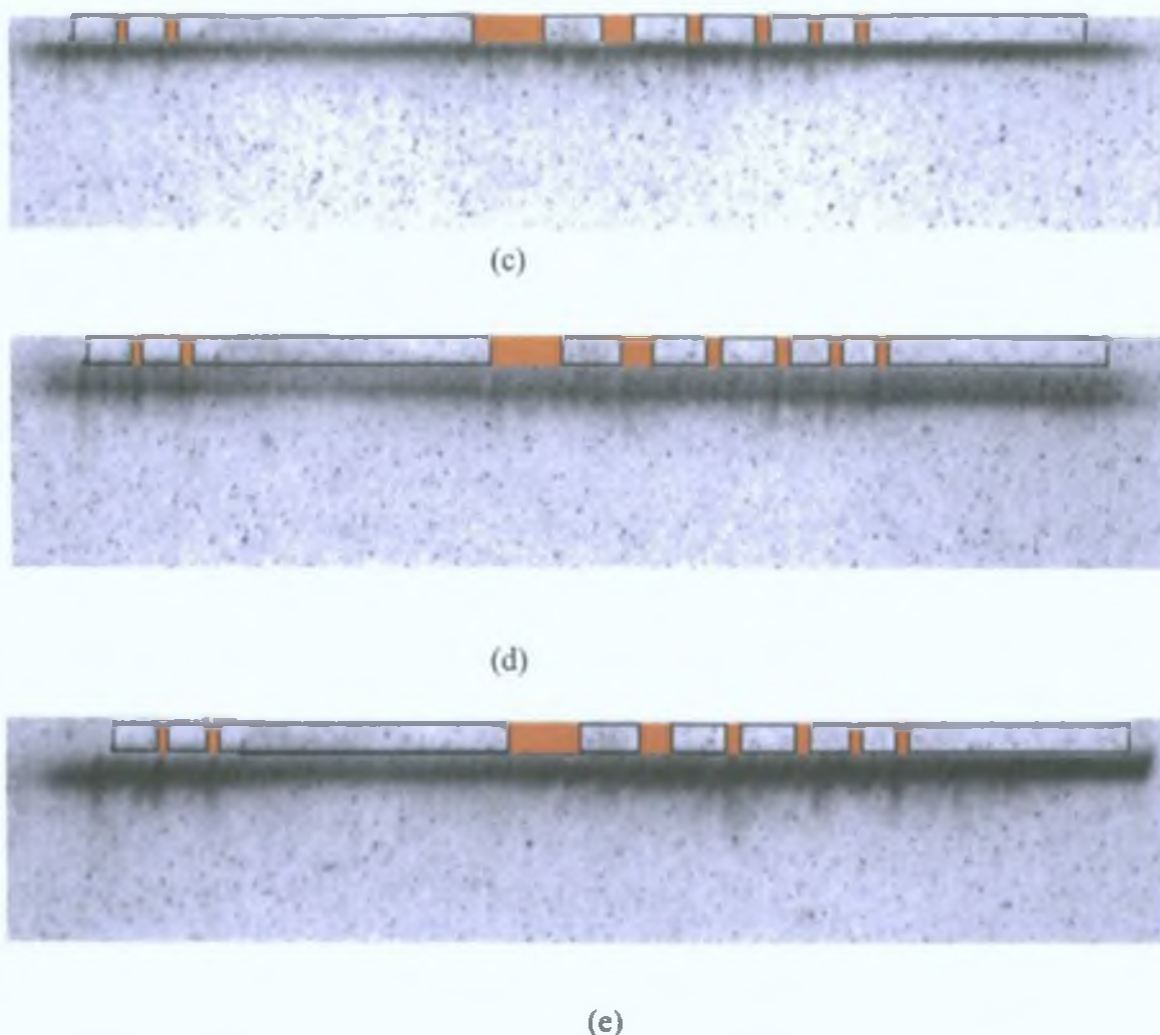
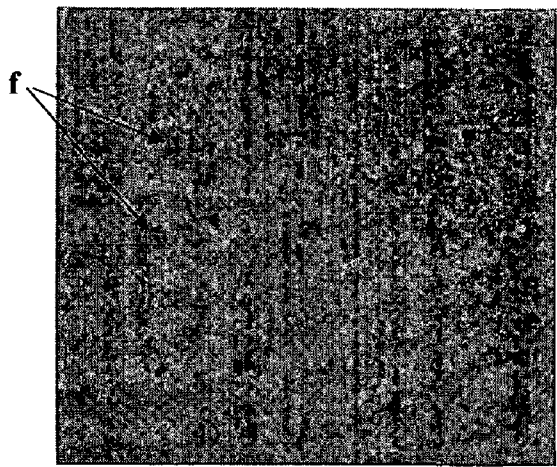


Figure 6-50 BRST images of the *Post*-Cu metallisation sample (300 nm electroless Cu/ 20 nm Cu seed/ 100 nm Ti on damascene patterned Si wafer) at (a) RT, (b) 100, (c) 200, (d) 300 and (e) 400°C (wfr.DCU2: ref#r36f95, r36f97, r36f99, r36f101 and r36f103).

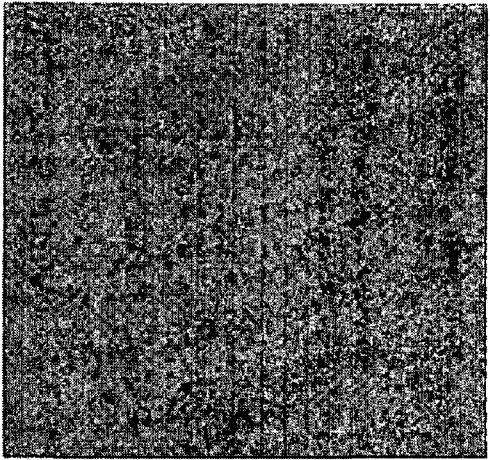
Step 7b. CMP 300 nm sputtered Cu/ 20 nm Cu Seed/ 100 nm Ti ---wafer no. DCU10

These LA-BRT (Figure 6-51 (a)-(e)) and BRST (Figure 6-52 (a)-(e)) images for the *Post*-sputtered Cu metallisation display a similar behaviour to the electroless metallisation. The strain fields in the Si substrate are relieved when the sample was heated. Most of the strains disappear at a temperature of 400 °C. The strains in Si,

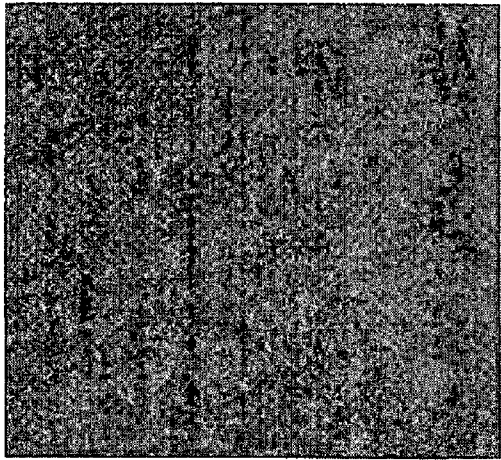
possibly due to metal residuals from the CMP process, also appear in the LA-BRT images (Fig. 6-51 (a)-(e)) as indicated by Arrows f.



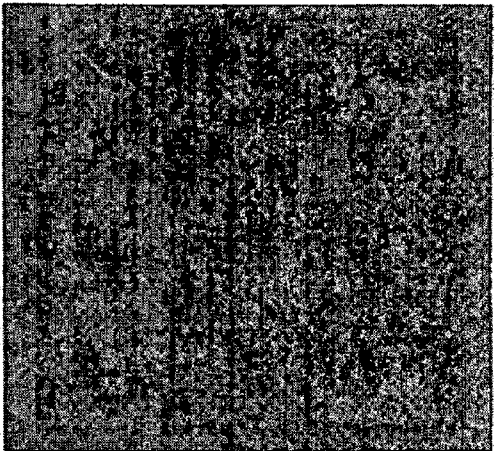
(a)



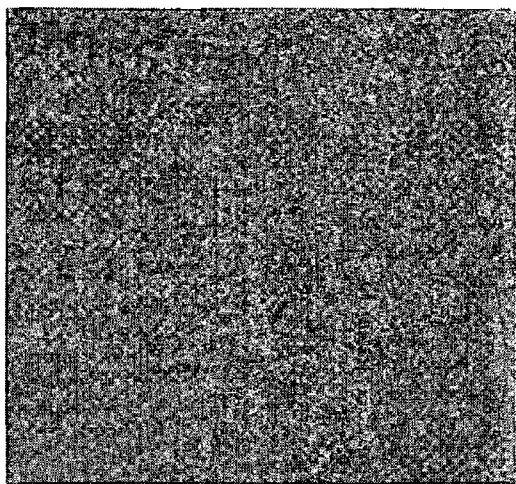
(b)



(c)

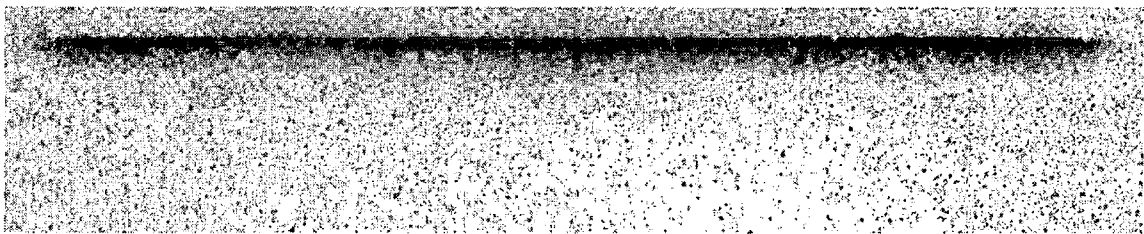


(d)

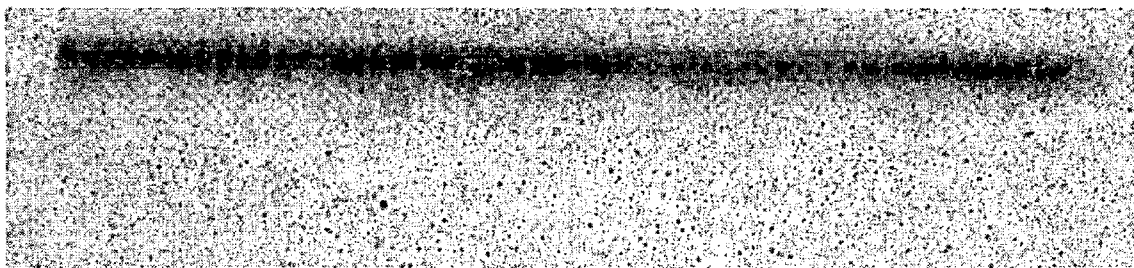


(e)

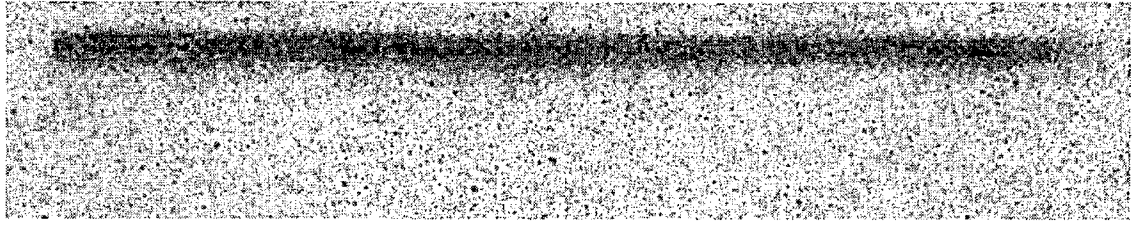
Figure 6-51 LA-BRT images of the *Post*-Cu metallisation sample (300 nm sputtered Cu/ 20 nm Cu seed/ 100 nm Ti on damascene patterned Si wafer) at (a) RT, (b) 100, (c) 200, (d) 300 and (e) 400°C (wfr.DCU10: ref#r36f73, r36f75, r36f77, r36f79 and r36f81).



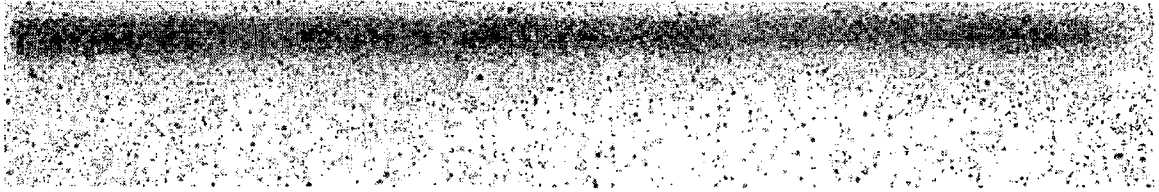
(a)



(b)



(c)



(d)



(e)

Figure 6-52 BRST images of the *Post*-Cu metallisation sample (300 nm sputtered Cu/ 20 nm Cu seed/ 100 nm Ti on damascene patterned Si wafer) at (a) RT, (b) 100, (c) 200, (d) 300 and (e) 400°C (wfr. DCU10: ref#r36f74, r36f76, r36f78, r36f80 and r36f82).

6.3.1.4 Geometry Line Width and Cu thickness Dependence of the Electroless Cu Metallisation Process Induced Strain Fields in Si Substrate

To study these factors, 500 nm of electroless Cu was deposited on the lift-off pattern. Much larger strain fields imposed on the Si are now observed due to a thicker electroless Cu deposition as depicted in Figures 6-53 and 6-54 respectively.

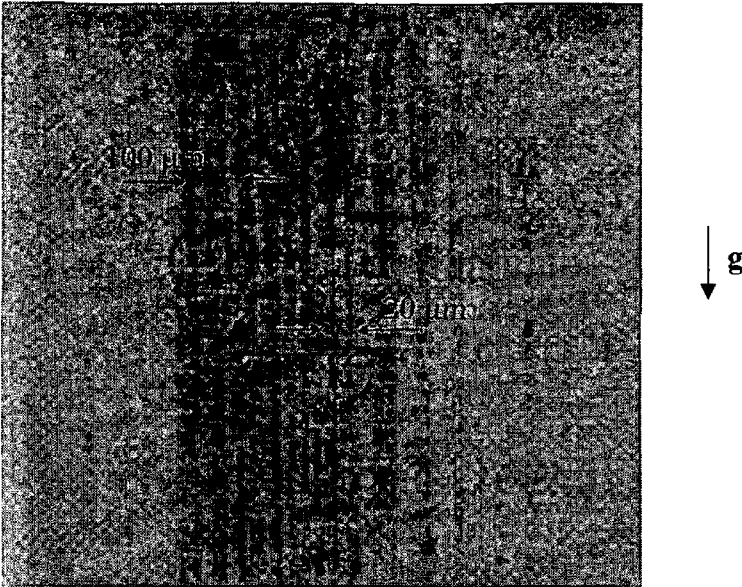


Figure 6-53 LA-BRT of 500nm *Post*-electroless Cu metallisation/ 20 nm Cu seed/ 100 nm Ti on Si using lift-off pattern (wfr. D4P3c: ref#R30F328-2).

The very strong contrast near the metal line edges in Figure 6-53 confirms the increase in strain fields with increasing electroless Cu thickness compared to the 300 nm *Post*-electroless Cu metallisation image (Fig. 6-20). A rough estimation of the stress/strain imposed on Si for electroless Cu deposition is based on a calculation of the thermal stress due to large difference in CTE (Coefficient of Thermal Expansion) since the temperature of the deposition solution was 80°C during the Cu deposition. The calculation of the maximum value of stress for a uniform film when the behaviour is purely elastic is given by

$$\sigma_{\max} = \Delta\alpha \cdot E \cdot \Delta T / (1 - \nu) \quad \text{Eq. 6- 31}$$

where σ_{\max} = the maximum generated thermal stress, $\Delta\alpha$ = the difference of CTE between Si and Cu ≈ 13.6 ppm/°C, E = Young's modulus ≈ 162.3 GPa and ν = Poisson's ratio = 0.28 [172]. From eq. (1), the estimation of maximum stress is of the order of 100 MPa.

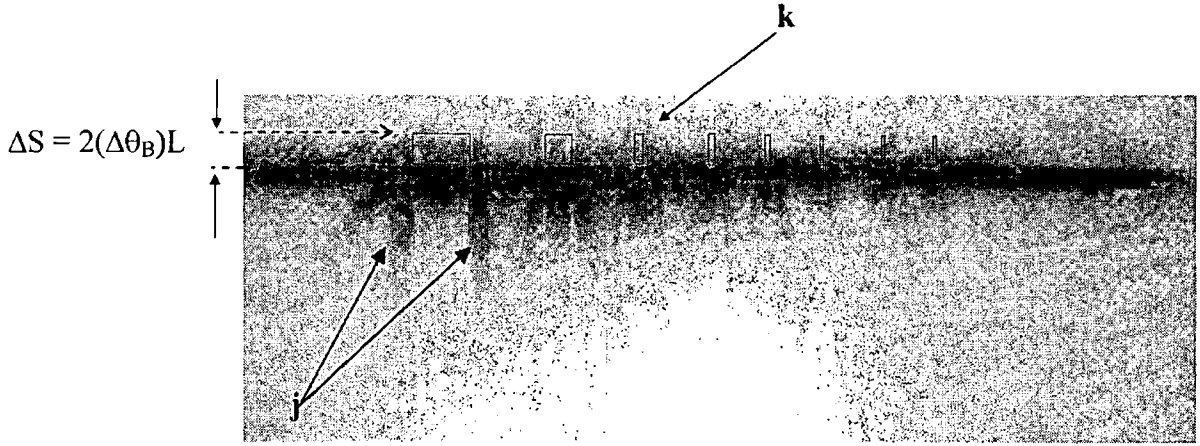


Figure 6-54 BRST of 500nm *Post*-electroless Cu metallisation/ 20 nm Cu seed/ 100 nm Ti on Si using lift-off pattern (wfr. D4P3c: ref#R30F332-8).

The $\overline{228}$ BRST of Figure 6-54 shows the very strong black and white contrast (extinction contrast) within the highly strained Si substrate (Arrows j) near the edges of the metal lines. In addition, the severely strained Si near the edge of Cu lines also appears via the orientational contrast mechanism. The orientational contrast is observed as a lifting of the image of highly strained Si near the line edges above the image of the rest of the Si (Arrow k). The orientational contrast can be observed if this misorientation exceeds the x-ray beam divergence ($\Delta\phi$), which is equal to 0.238 mrad for beamline F-1 in HASYLAB. The height of the orientational contrast shift is $\Delta S = 2(\Delta\theta_B)L$, where $\Delta\theta$ is the effective misorientation, L is the distance between sample and film (50 mm in this case). This can yield quantitative estimates for the magnitude of strain in the underlying silicon as described in the Chapter 3, in that $\Delta\theta_B \cong \gamma_{xy}$.

In the case of the 100 μm wide Cu line, $\Delta S \approx 0.05$ mm, therefore, $\Delta\theta_B \cong \gamma_{xy} \cong 5 \times 10^{-4}$ or 0.05%. This implies that the magnitudes of shear stresses are given by $|\tau_{xy}| = G|\gamma_{xy}|$, where E = shear modulus = 162.3 GPa [172]. Thus, the limit on the stress magnitudes is of the order of $|\tau_{xy}| \approx 81$ MPa.

In the case of the 20 μm wide Cu line, $\Delta S \approx 0.08 \text{ mm}$, $\Delta\theta_B \cong \gamma_{xy} \cong 8 \times 10^{-4}$ or 0.08%. Thus, $|\tau_{xy}| \approx 130 \text{ MPa}$. These are both of the same order of magnitude as the stresses estimated using Eq. 6-31.

From both the calculation and experiments, the orientational contrast shows that the stress near the Cu line edge increases with decreasing Cu line width. The relationship between the Cu line width and the stresses near the line edge can be clarified using FEM, which will be described in the next section. However, the higher stress due to the 20 μm wide Cu line could result from the interference via a merging of the topographic images near both edges of this metal line. To eliminate this issue, the extinction contrast at the edge of the metal lines has been examined closely. The extinction contrast illustrates the opposite tendency as shown in Fig. 6-54 (Arrows j) in which the contrast is more pronounced near the line edge of the 100 μm wide Cu line and declines with decreasing line widths. This is confirmed by the LAT and ST images (Figure 6-55 and 6-56).

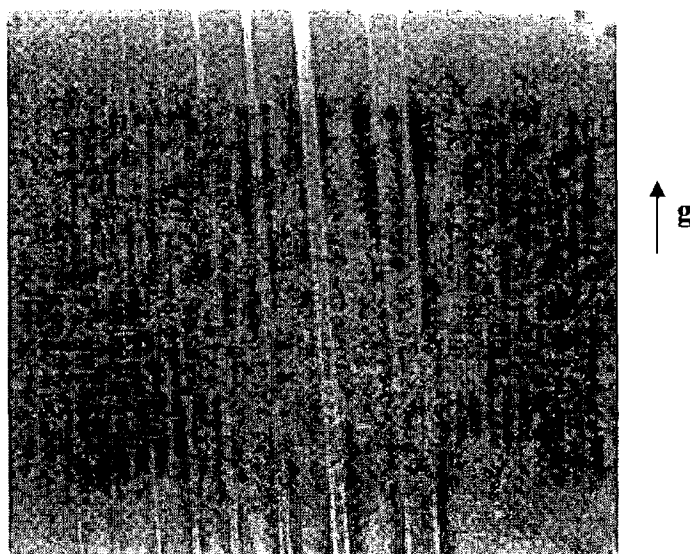


Figure 6-55 LAT image of 500nm *Post*-electroless Cu metallisation/ 20 nm Cu seed/ 100 nm Ti on Si using lift-off pattern (wfr. D4P3c: ref#R30F338-1).

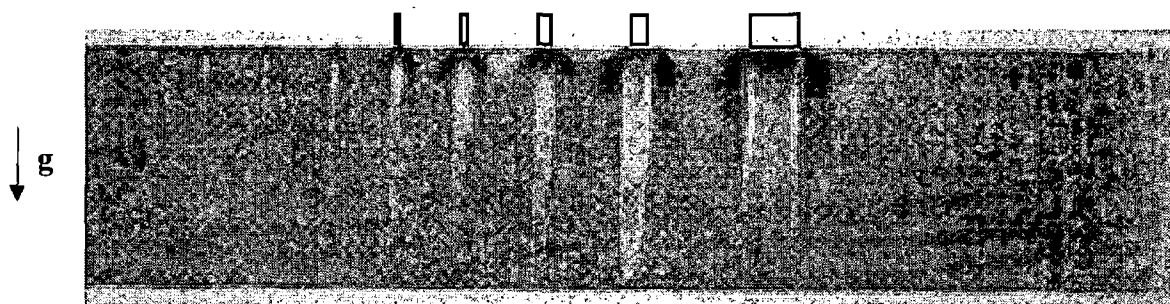


Figure 6-56 ST image of 500nm *Post*-electroless Cu metallisation/ 20 nm Cu seed/ 100 nm Ti on Si using lift-off pattern (wfr. D4P3c: ref#R30F337-2).

The ST image (Fig. 6-56) illustrates severe destruction of the Kato fringes, which implies high strain fields in the Si crystal. Some orientational contrast is visible in this image. However, the misorientation is too small to measure in this case. The strains, as observed via the extinction contrast annihilation of the Pendellösung fringes, are deeper and greater in intensity with increasing the line width. Therefore, it confirms the relationship between the line width and strain fields, in that the strain fields in the Si substrate increase with increasing geometry line widths.

6.3.2 Finite Element Modeling Results and Discussions of Cu Metallisation

Finite element modeling was used to simulate the strain fields in the Si wafers based solely on the temperature difference. While this simulation may be limited, it will allow us to focus in on what is one of the main sources of strain. An understanding of this, its inclusion or elimination as a source of stress, will allow us to determine or pinpoint other mechanisms of stress induction. The experimental details including the geometry, dimension and materials properties of Cu sample are described in Chapter 6, section 6.2.3 (Experimental details of FEM). The simulation was carried with two main objectives as follows:

- To evaluate the strain field in the Si wafers due to the Cu metallisation (*Post-Cu* metallisation step) and to compare with SXRT and MRS results. In this case, the difference in temperature was set to 60 °C ($\Delta T = 60$ °C), which is an estimation of the difference between the electroless deposition bath (80 °C) and room temperature.
- To examine the influence of the heating process at elevated temperature ($T = 100, 200, 300$ and 400 °C) on the stresses in the Si substrate in the Cu metallisation sample and compared to SXRT results.

6.3.2.1 Simulation of the *Post-Cu Metallisation*

Figures 6-57 to 6-59 illustrate the simulated strain fields in the Si wafer due to the thermal processing of Cu metallisation for a line width of 20 μm for σ_{xx} , σ_{yy} , τ_{xy} , respectively. The simulations show that the strain fields build up near the edge of the metal line for both normal and shear strains. This is in line with our SXRT observations.

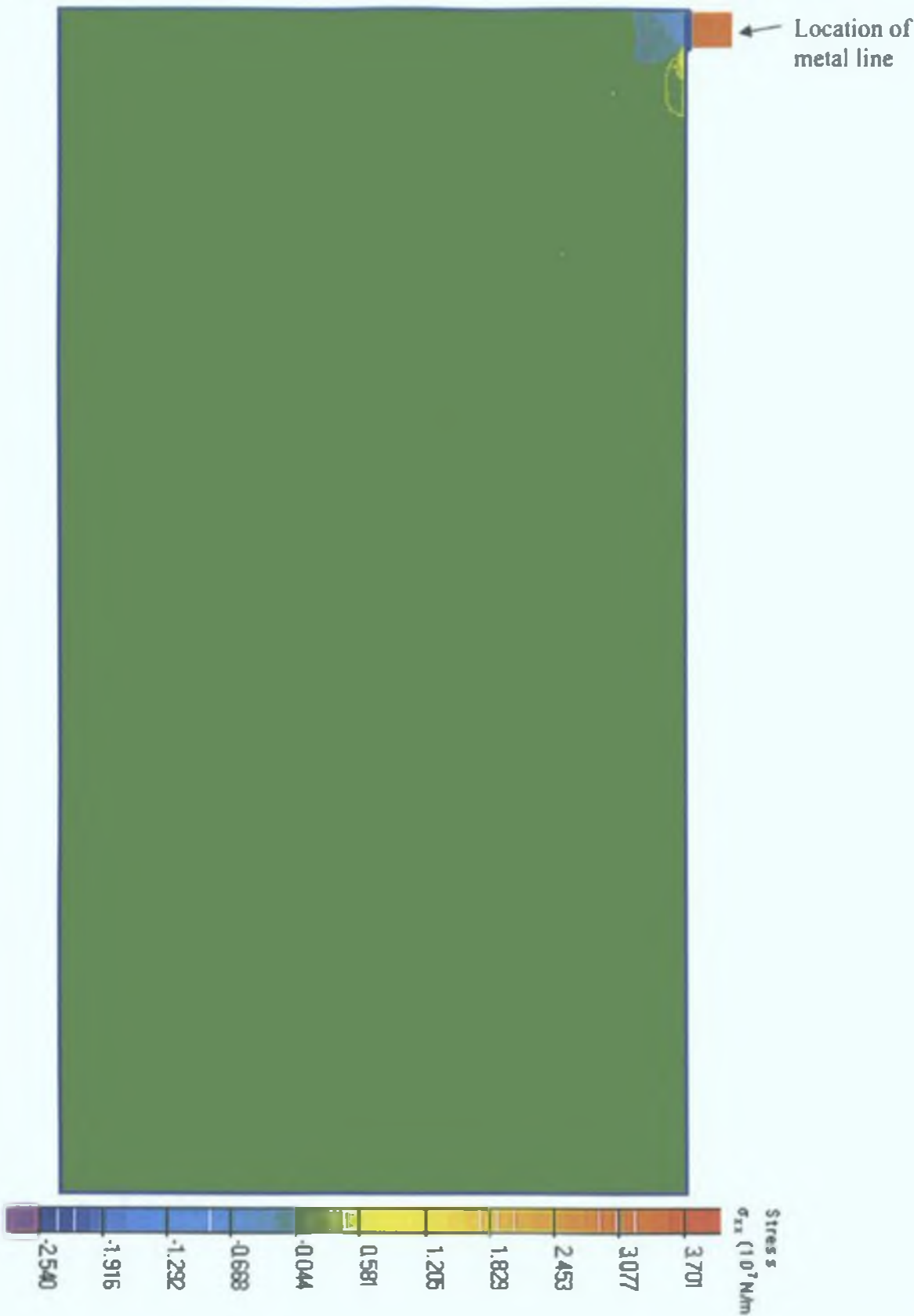


Figure 6-57 FEM of the normal stress in the X-direction (σ_{xx}) for the 20 μm wide Cu metallisation.

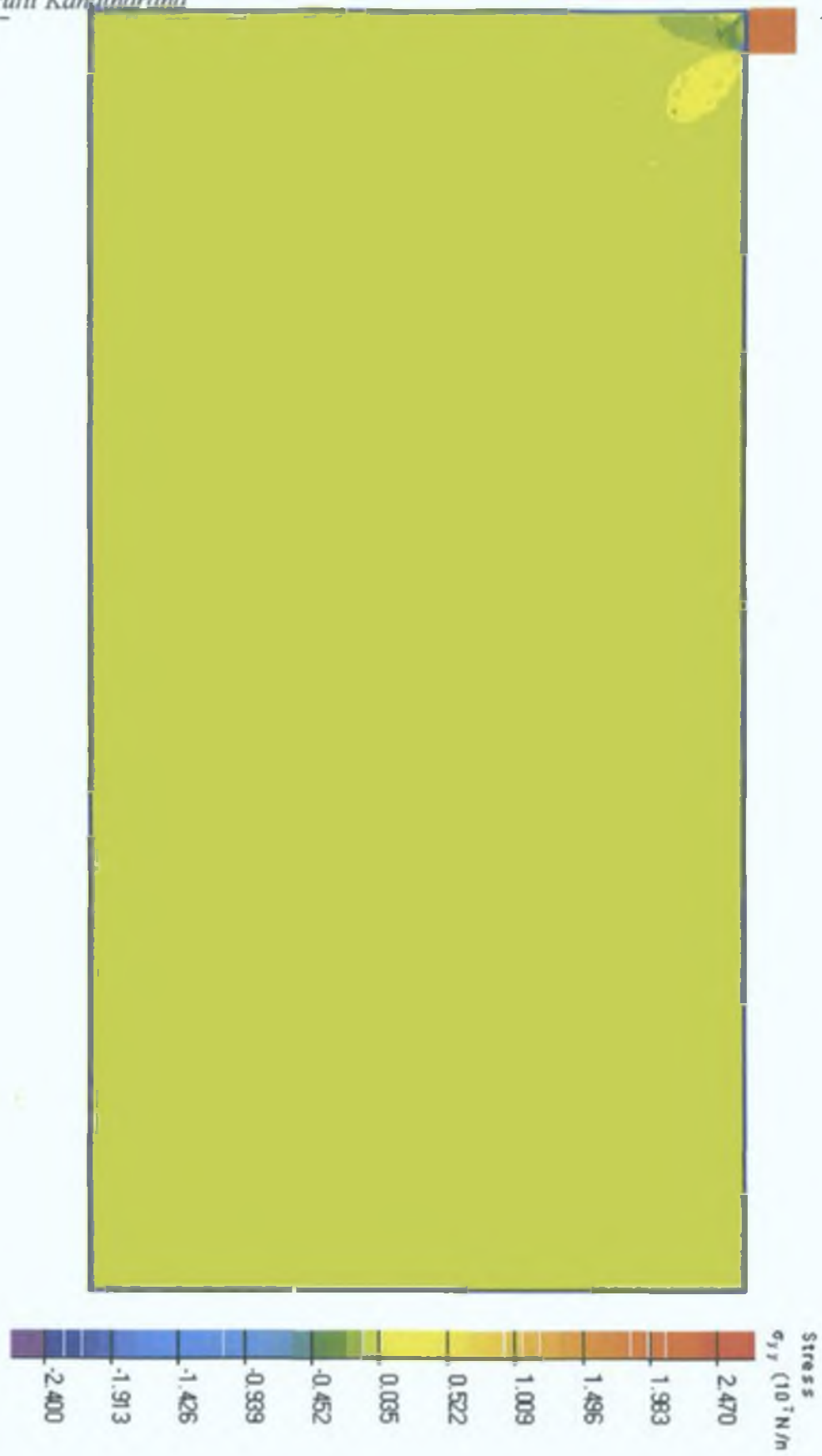


Figure 6-58 FEM of the normal stress in the Y-direction (σ_{YY}) for the 20 μm wide Cu metallisation.

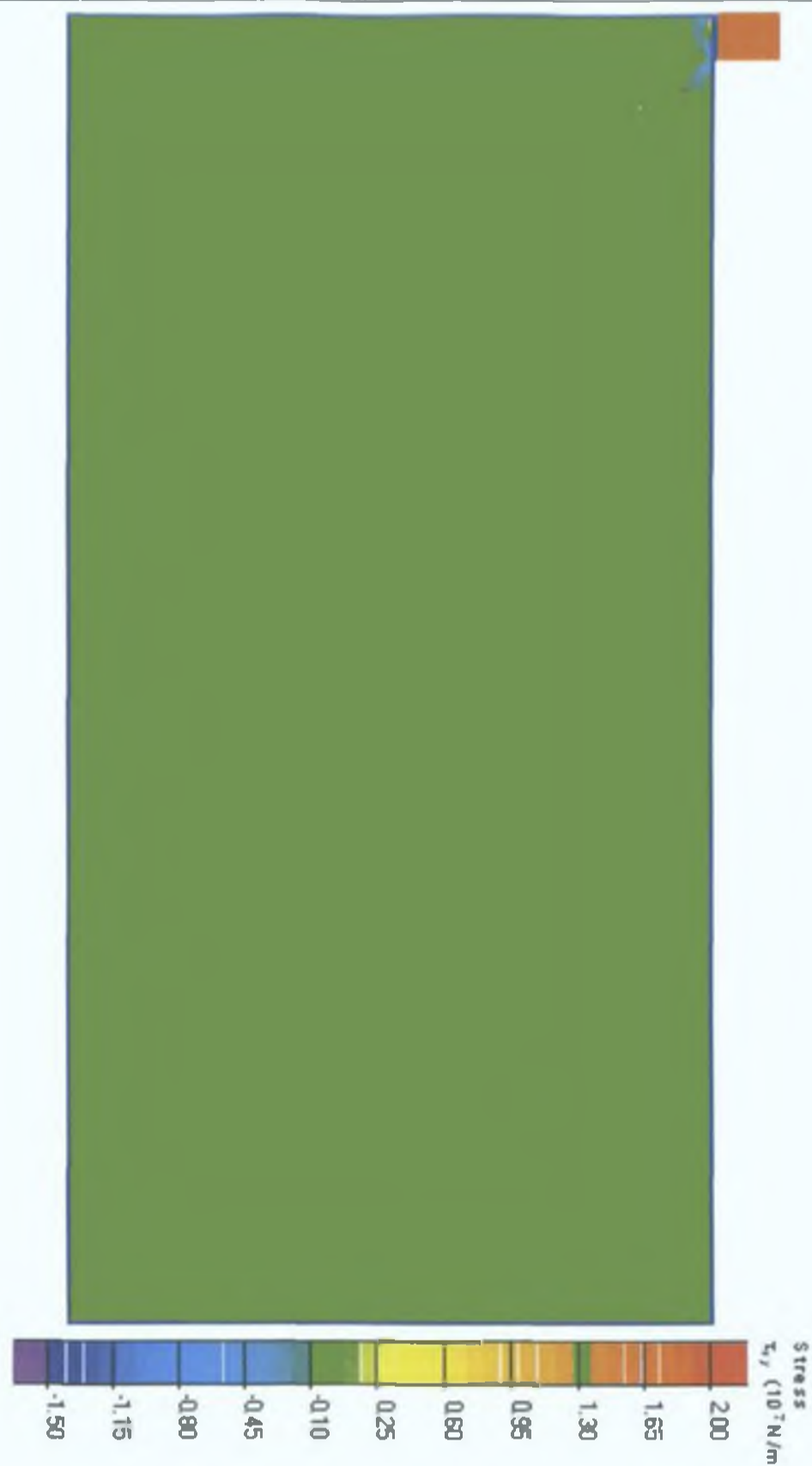


Figure 6-59 FEM of the shear stress (τ_{xy}) for the 20 μm wide Cu metallisation.

The simulations were performed for line widths of 0.1, 0.5, 1.0, 2.0, 5.0, 10, 20, 40, 60 and 100 μm . The normal stresses (σ_{xx}) along the interface between the Si and metal layer are illustrated in Figure 6-60.

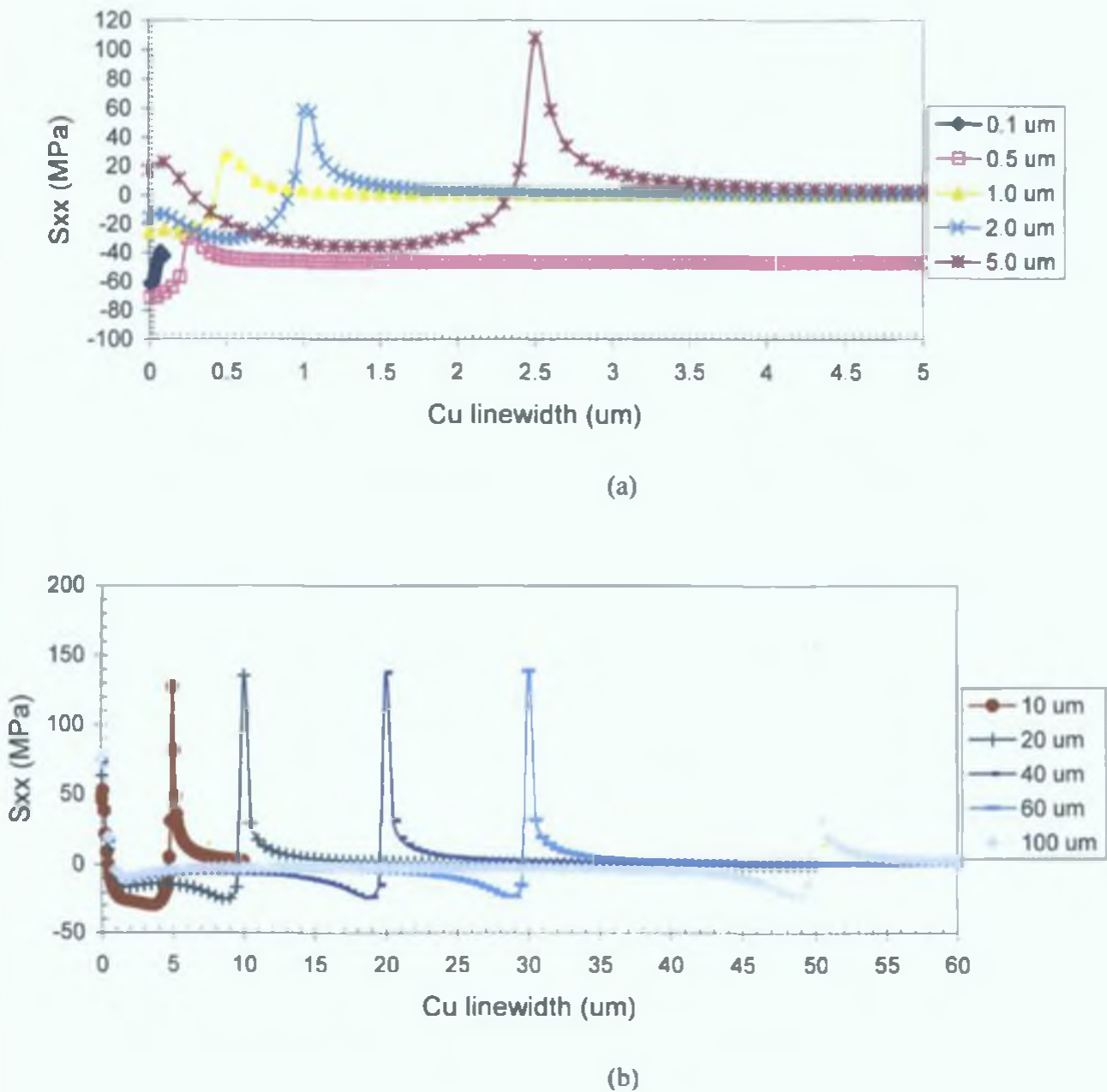


Figure 6-60 The FEM simulation of the normal stress in the X direction (σ_{xx}) along the Si/metal interface for copper line widths of 0.1, 0.5, 1.0, 2.0, 5.0, 10, 20, 40, 60 and 100 μm . Note:

positive and a negative signs represent tensile and compressive stresses, respectively.

As expected the stresses build up near the edge of the metal lines. The compressive stresses were found in the Si underneath the metal layer near the edge of the metal lines. One can also see that the compressive stress in the Si underneath the metal layers decreases with increasing line width.

In contrast, the stresses outside the edge of the metal lines are separated into two cases, i.e. line width less than 1 μm and larger or equal to 1 μm . When the line widths are less than 1 μm , a compressive stress in the Si wafer outside the edge is observed. The stress in the Si wafer outside the edge changed state into a tensile stress when the Cu line widths are larger or equal to 1 μm . The transition in stress commences for line widths of approx. 6 μm . The relationship between the stress at the edge outside the Cu line and the Cu line width is illustrated in Figure 6-61.

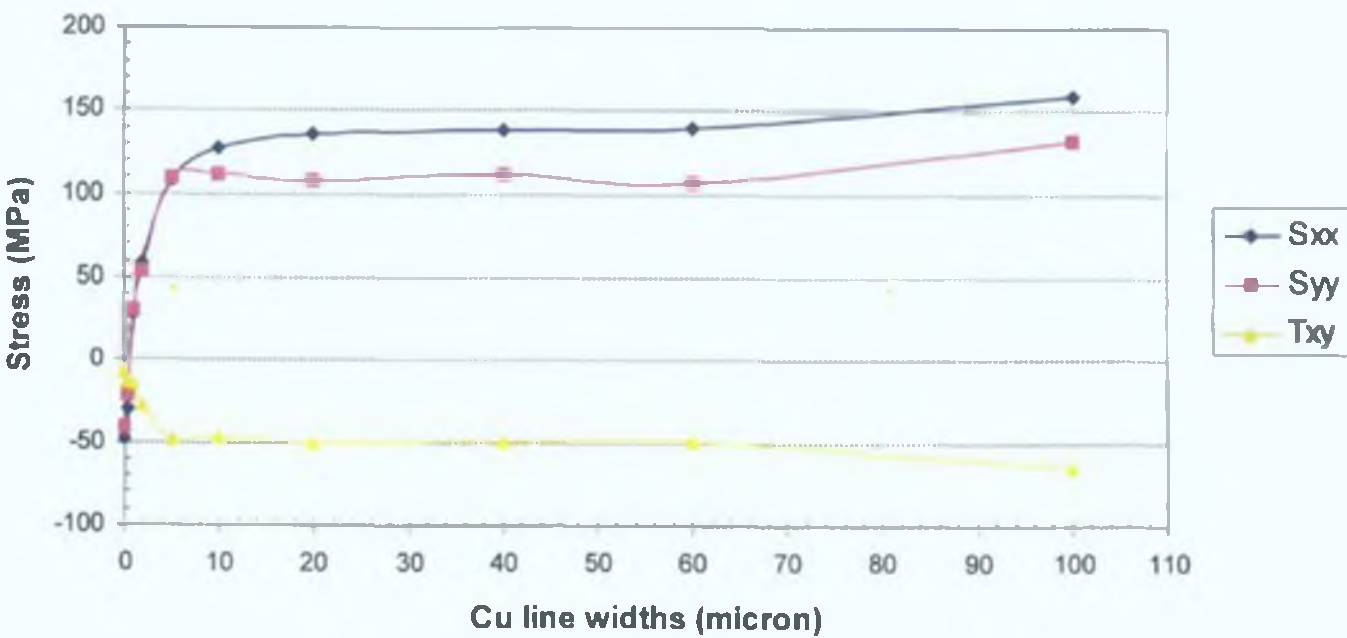


Figure 6-61 The outcome of the FEM simulation of the relationship between the normal stresses (σ_{xx} , σ_{yy}) and shear stress (τ_{xy})

outside the edge of the metal lines as a function of the copper line widths.

The FEM result in Fig. 6-61 shows that the compressive stress outside the edge of the metal line decreases significantly with increasing the Cu line width when the Cu line widths are less than 6 μm . The stress changes to tensile stress when the Cu line widths are larger or equal to 1 μm . It is estimated that the relationship of σ_{xx} (S_{xx}) and the Cu line widths are given by

$$\sigma_{xx} = 139.5 - 195.5 \exp(-\text{Culinewidth}/2.3) \text{ MPa} \quad \text{Eq. 6-32}$$

where Cu linewidth is given in microns.

A comparison of the σ_{xx} (S_{xx}) between FEM data and the empirical Equation 6-32 is depicted in Figure 6-62.

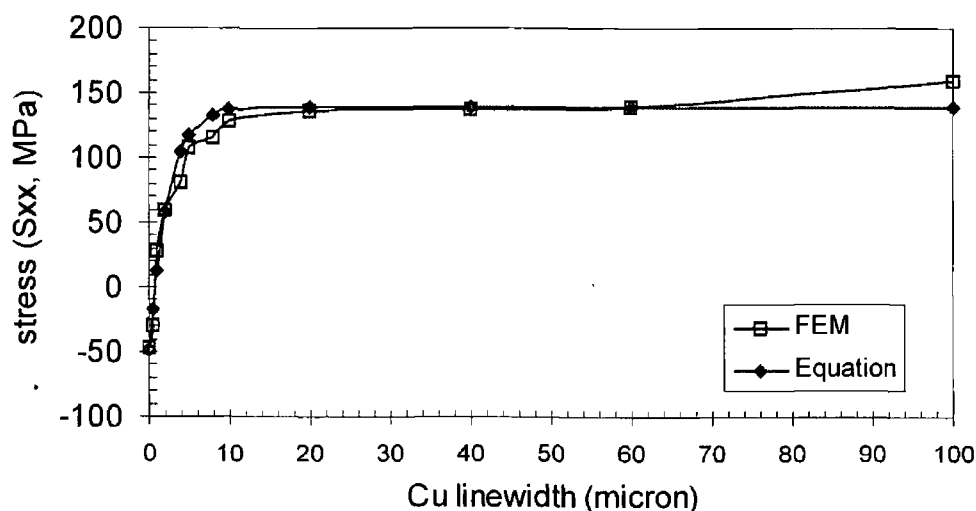


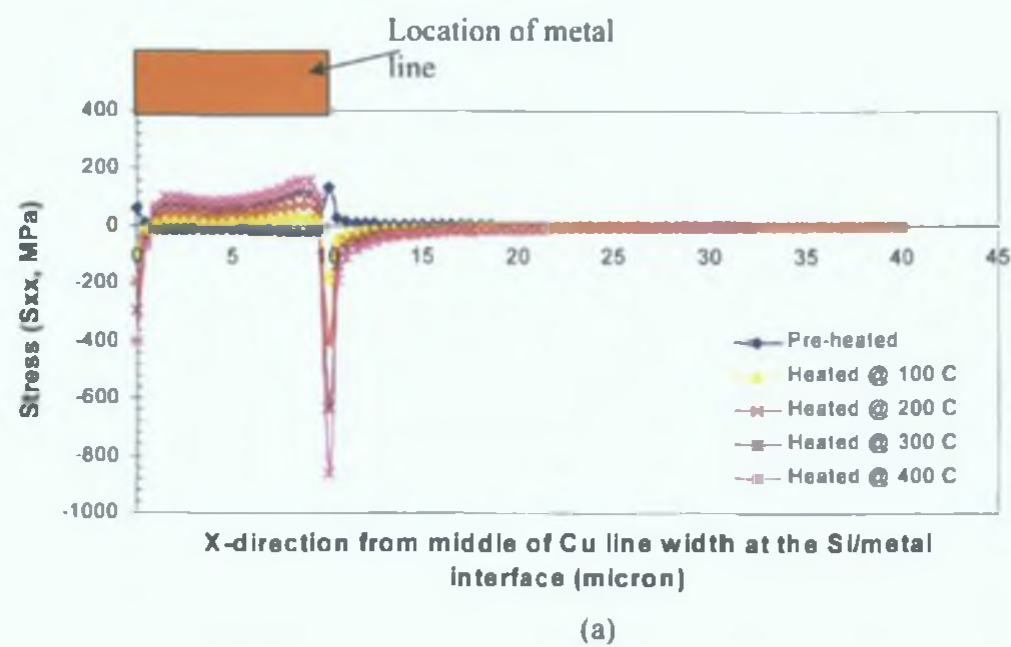
Figure 6-62 A comparison of the normal stress in X direction (σ_{xx}) from FEM data and the empirical equation as a function of the Cu line widths.

From Figure 6-62, the σ_{xx} and the Cu line width are related in terms of the exponential distribution. This result will be compared to the result from MRS and

will be discussed later in this chapter (section 6.3.3.3 Influence of Cu line width on the stress distributions in Si wafers).

6.3.2.2 Simulation of the Cu Metallisation due to the Heating Effect

As an example, we now describe the FEM carried out for the 20 μm line width Cu metallisation, which was annealed at 100, 200, 300 and 400 $^{\circ}\text{C}$. A comparison of stresses in the Si wafer for the *Post*-Cu metallisation before and after annealing along the Si/metal interface is shown in Figure 6-55 for (a) σ_{xx} (b) σ_{yy} and (c) τ_{xy} .



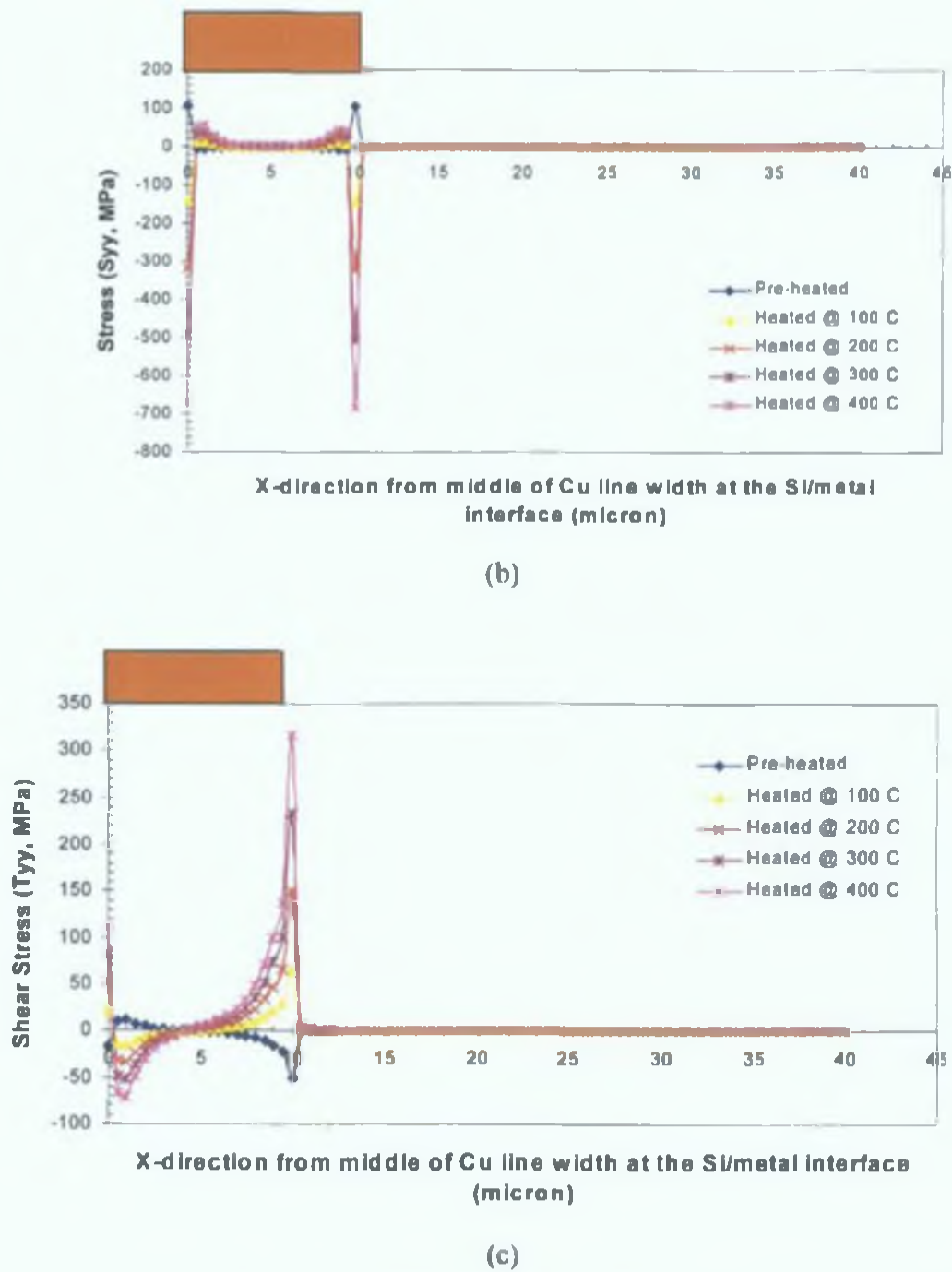


Figure 6-63 The FEM simulation of the induced strains for the *Pre*-heated and *Post*-Heated copper metallisation (a) σ_{xx} (b) σ_{yy} and (c) τ_{xy} along the X-direction from the middle of the metal lines ($X = 0 \mu\text{m}$) to the edge of the metal ($X= 10 \mu\text{m}$) at the Si/metal interface ($Y= 150 \mu\text{m}$).

The FEM results show that the stress distributions in the Si wafer at the edge of the Cu line are compressive for σ_{XX} and σ_{YY} , and tensile for τ_{XY} at room temperature (*Pre-heated*). After the sample was heated at elevated temperature from 100 to 400 °C, the stress transformed into the opposite state (i.e. tensile became compressive, and compressive became tensile). Although the strain transition point is slightly different from the SXRT result (Figs. 6-44 and 6-45), this FEM result (Fig. 6-63) confirms the correlation of the strain transition phenomenon with the SXRT results.

6.3.3 Micro-Raman Spectroscopy Results and Discussions

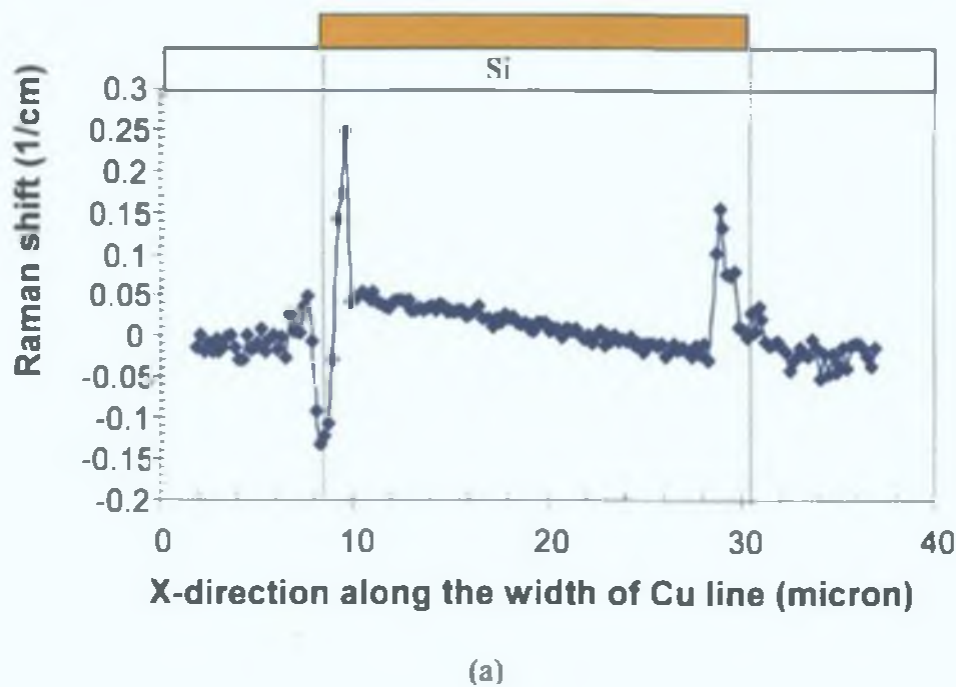
Micro-Raman spectroscopy was used to evaluate the stress distributions in the Si substrate due to the Cu metallisation. As mentioned in the experimental chapter, the MRS measurements were performed only on the 20 and 100 μm line widths Cu metallisation samples, except for the measurement of the line width dependence and annealing effect. The aims of these measurements were as follows:

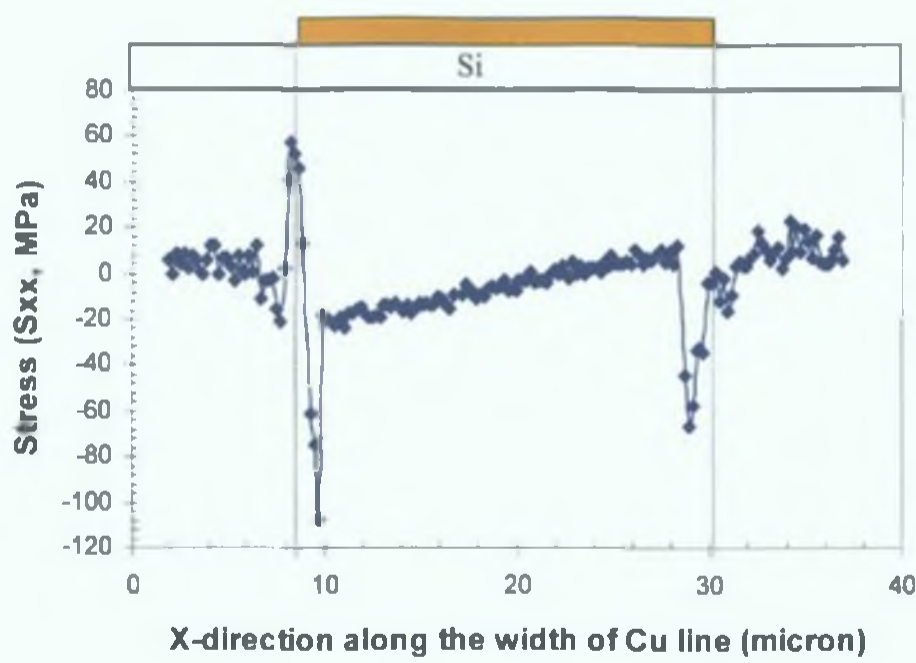
- To evaluate quantitatively the stresses in the Si substrate due to the electroless Cu metallisation, the measurements of *Pre*- and *Post*-metallisation electroless Cu samples were performed and compared to the SXRT results.
- To compare the stress in Si due to the Cu metallisation process with two different techniques, i.e. the electroless plating and sputtering techniques, the *Post*-metallisation electroless and sputtered Cu samples were measured.
- To study the influence of the copper line width on the strain fields in the Si substrate due to the Cu metallisation, the *Post*-metallisation electroless Cu samples were investigated.
- To study the effect of annealing on electroless Cu metallisation as a function of the line width, the *Post*-metallisation electroless Cu sample was annealed at 400 °C and subsequently measured.

It is worth noting that the Raman shift and the measured stress can be used only in the Si regions.

6.3.3.1 Electroless Copper Metallisation Induced Stresses in Si Substrate

To study the electroless Copper metallisation induced stresses in the Si substrate, MRS measurements on the 20 μm line width *Pre-* and *Post-* metallisation samples were performed. The Raman shift (a) and the normal stress in the X direction (b) for the *Pre-* and *Post-* electroless Cu metallisation samples with a 20 μm line width are illustrated in Figure 6-64 and 6-65, respectively.





(b)

Figure 6-64 (a) The Raman shift (cm^{-1}), and (b) the normal stress (σ_{xx} , MPa) for the 20 μm Cu line width *Pre*-metallisation sample (ref# D4P3d).

The MRS (Fig. 6-64(b)) shows that a tensile stress is generated in the Si substrate near the edge outside of the metal line due to the Ti and metal seed layers before the Cu metallisation step. The maximum magnitude of the stress is about 60 MPa.

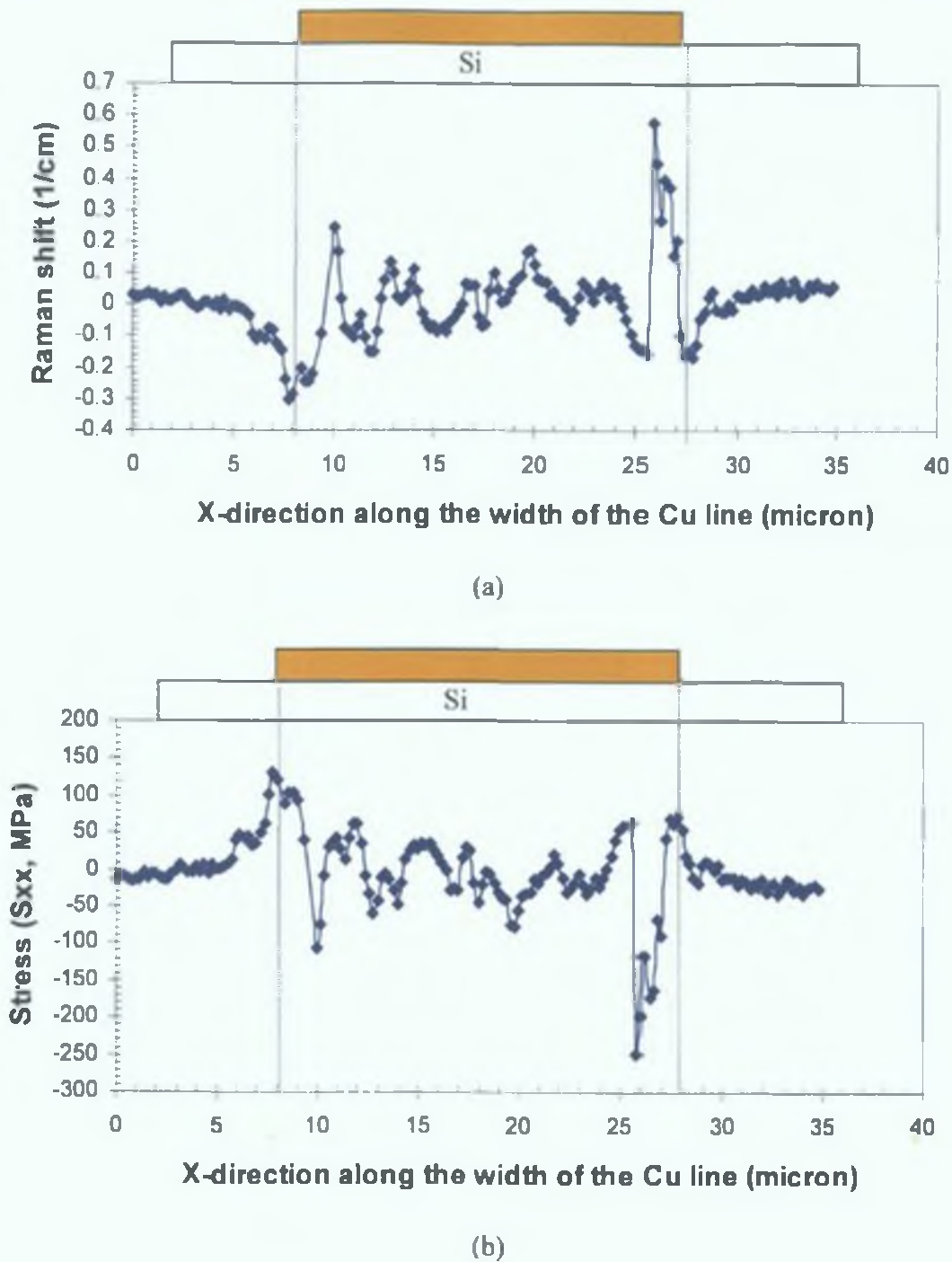


Figure 6-65 (a) Raman shift (cm^{-1}) and (b) Stress (σ_{xx} , MPa) for the 20 μm Cu line width *Post*-Cu metallisation sample (Ref# s-97).

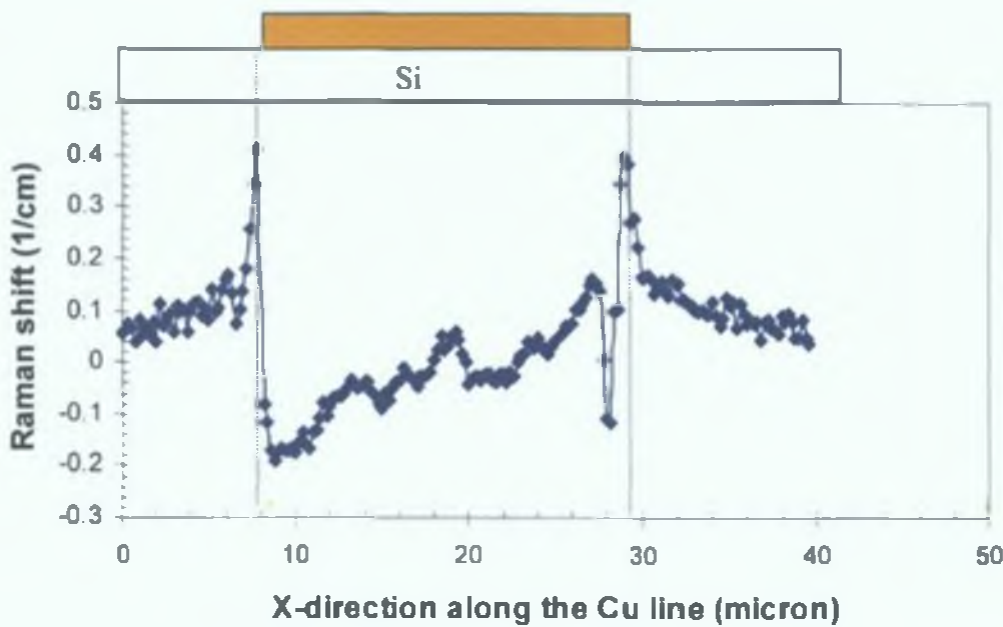
For these measurements, it appears that the electroless Cu metallisation created an even greater tensile stress in the Si wafer near the edge of the Cu line with the magnitude of ~ 150 MPa. This magnitude of the tensile stress correlates to stress calculated from the orientational contrast in the BRST image of *post*-electroless

metallisation (Fig. 6-55), the general stress calculation from Eq. 6-31, and σ_{xx} simulated via FEM at the outside of the metal line in Figure 6-61.

6.3.3.2 Electroless vs. Sputtered Copper Metallisations

A comparison of the stresses in the Si wafer due to the metallisation techniques, i.e electroless plating versus sputtering techniques, is obtained in this section. The measurements were performed on the 20 μm Cu line widths using the lift-off pattern.

The Raman shift (a) and normal stress, σ_{xx} (b) for the electroless Cu metallisation was given in Figure 6-65 above. Figure 6-66 illustrates the Raman shift (a) and stress (σ_{xx}) in the Si due to the 20 μm line width sputtered Cu metallisation.



(a)

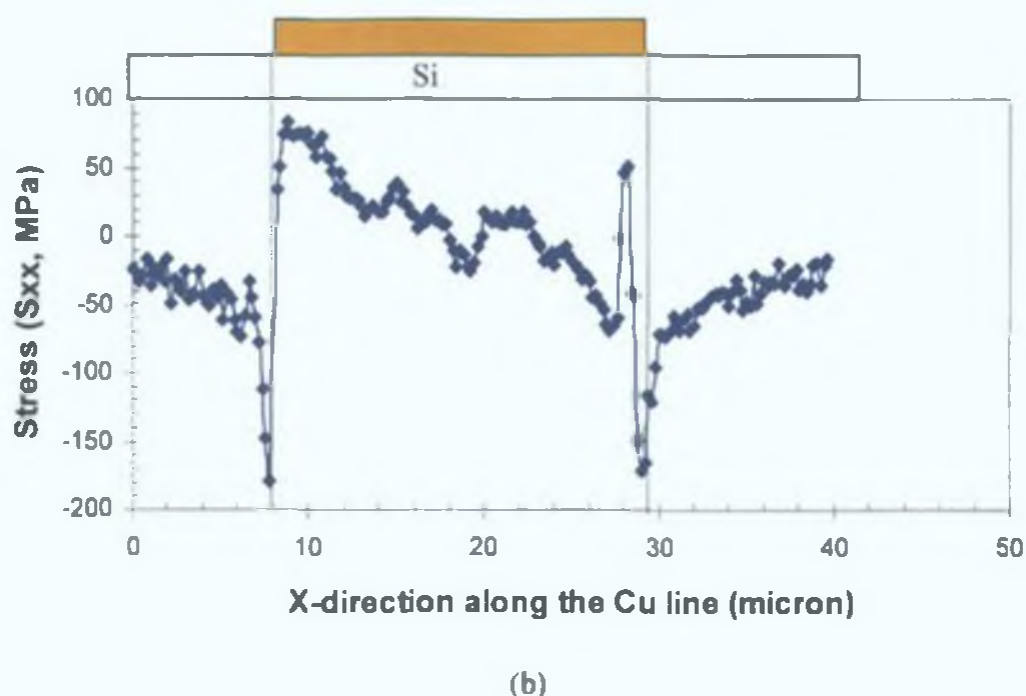


Figure 6-66 (a) Raman shift (cm^{-1}) and (b) Stress, σ_{xx} (MPa) of the 20 μm line width sputtered Cu metallisation by lift-off pattern (ref# B1-4F).

For the sputtering technique, the compressive stress in the Si wafer near the edge outside of the metal line was of the order of ~ -180 MPa. It can be seen from Figs. 6-65 and 6-66 that the stress magnitude in the Si due to the electroless deposition and sputtering of the Cu metallisation is of the same order but opposite in state. For the same copper geometry and line width, the electroless Cu metallisation places the Si near the outside edge of the metal line in a tensile stress, whereas, the sputtered Cu metallisation puts the Si near the outside edge the metal line in compression. This could be related to the creation of the copper and its texture, grain size as well as self-annealing after deposition. Yamada *et al.* reported that the grain size of the sputtered Cu (max. $\sim 1.8 \mu\text{m}$) is much smaller than for electroless Cu (max. $\sim 4 \mu\text{m}$); therefore it could be possible that the recrystallisation process in the sputtered Cu is slower than the electroless Cu resulting in a different stress state [177]. In addition, it has been known that the sputtered films are normally in compression and thus the underneath Si is put in tension.

6.3.3.3 Influence of Cu LineWidth on the Stress Distributions in Si Wafers

The MRS measurements were carried out on the *Post*- 500 nm electroless Cu metallisation sample. This sample is called the *Pre*-annealed sample. The normal stresses (σ_{xx}) for 2, 4, 6, 8, 10, 20 and 100 μm Cu line widths were measured and are illustrated in Figure 6-67.

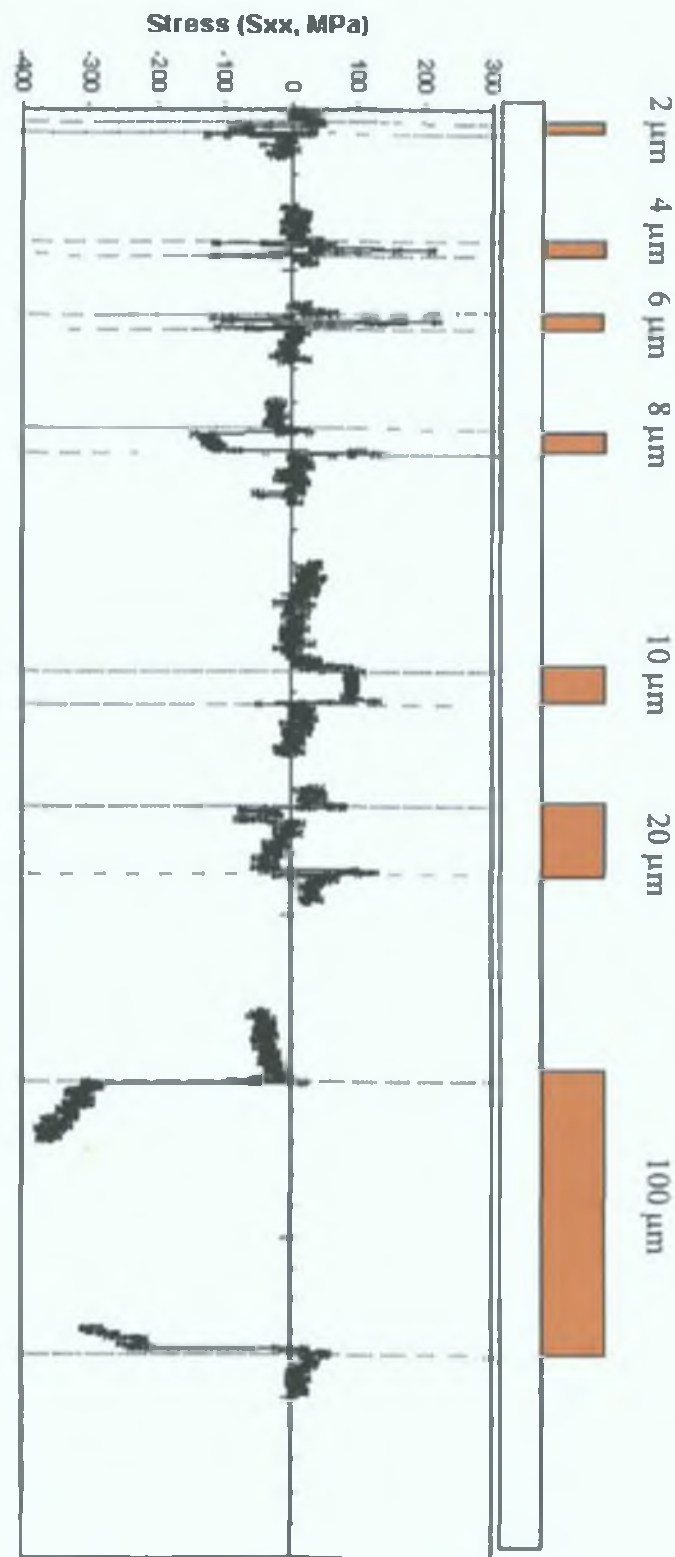


Figure 6-67 The normal stress (σ_{xx}) in the Si substrate just below the Si/metal interface due to the 500 nm electroless Cu

metallisation as a function of Cu line widths (Pre-annealed sample).

Figure 6-67 shows that the stresses imposed in the Si substrate due to the Cu metallisation are dependent on the Cu line width. The MRS results indicate that the stresses build up near the edge of the metal line. The relationship between the Cu line width and stress (σ_{xx}) in Si near the edge of the Cu line is shown in Figure 5-68.

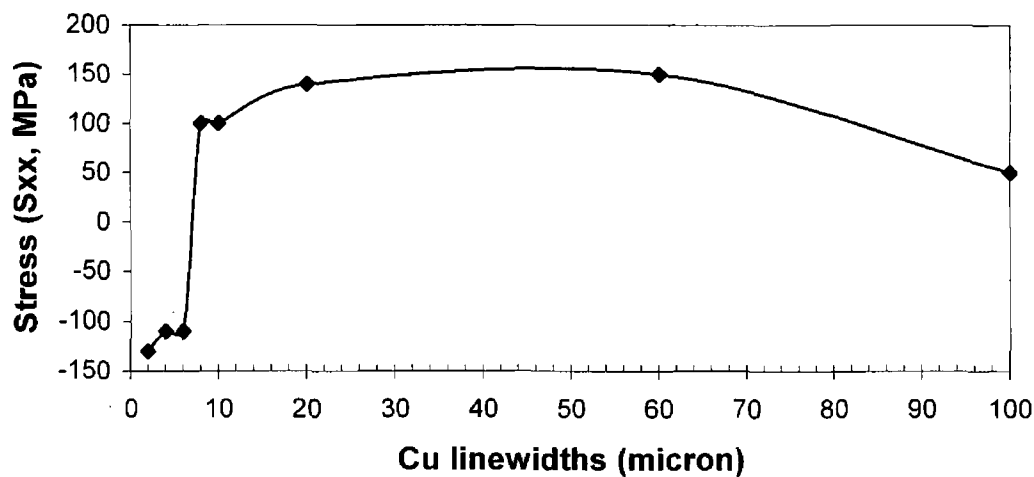


Figure 6-68 The relationship between the normal stresses (σ_{xx} , MPa) in the Si substrate calculated from the Raman shift and the Cu line widths of the *Pre-annealed* sample.

The normal stresses imposed in the Si wafer due to the electroless Cu metallisation are compressive near the edge of the Cu line when the Cu line width less than $\sim 10\ \mu\text{m}$. The normal stress in Si changes to tensile stress when the Cu line width is larger than $\sim 10\ \mu\text{m}$. In addition, when the Cu line width is larger than $\sim 10\ \mu\text{m}$, the magnitude of the tensile stress seems to be almost independent of the Cu line width. The estimation of Eq. 6-33 indicates that the stress (σ_{xx}) due to the electroless Cu metallisation is related to the Cu line width in terms of an exponential distribution. This result correlates with the FEM simulation (Fig. 6-62). The equation of the experimental MRS curve is

$$\sigma_{xx} = 115.6 - 281.4 \exp(-\text{Cu line width}/5.5) \qquad \text{Eq. 6- 33}$$

A comparison of the normal stress (σ_{xx}) from the experimental MRS data, the calculated FEM distribution and the empirical estimates of Eqs. 6-32 and Eq. 6-33 are shown in Figure 6-69.

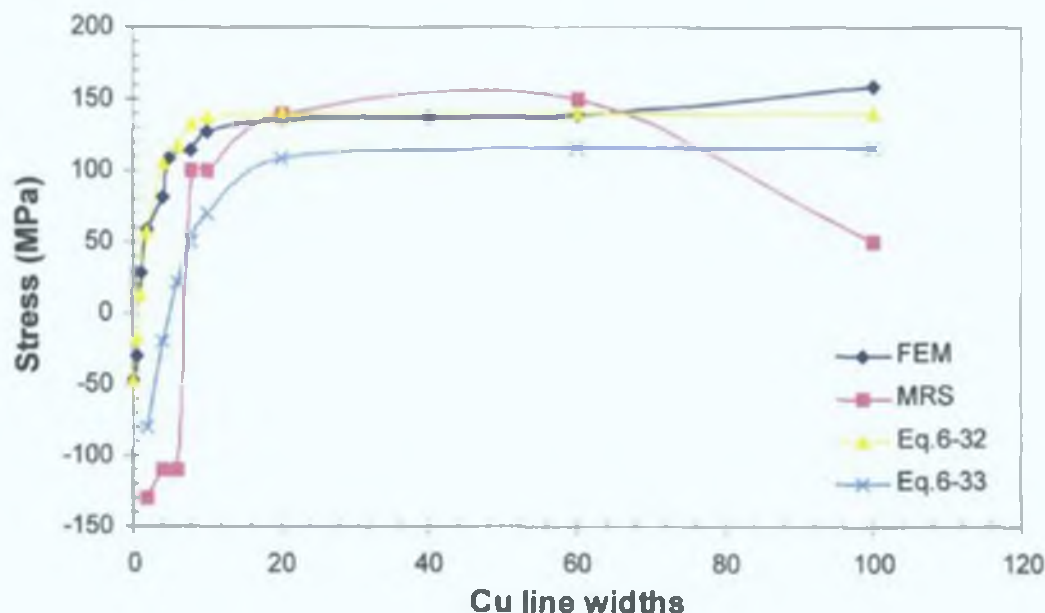


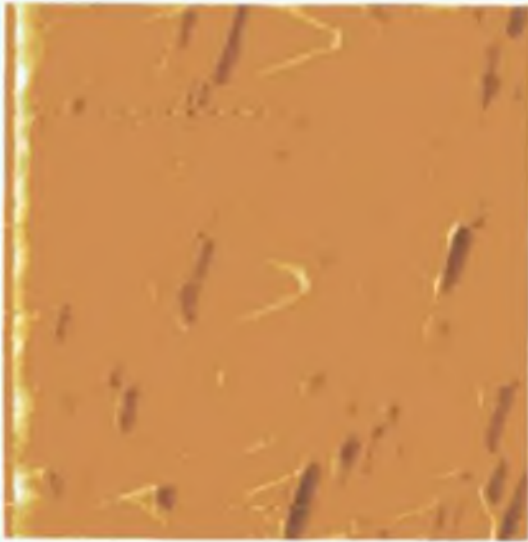
Figure 6-69 A comparison of the normal stress in the X direction (σ_{xx}) from experimental MRS data, the FEM simulation and the empirical estimations of Eq. 6-32 and Eq. 6-33.

Figure 6-69 suggests that the generated stress versus line width (L) tendency is a function of the geometrical arrangement. In addition, both FEM and MRS results confirm that the stress (σ_{xx}) due to the electroless copper metallisation is empirically related to the Cu line width in terms of an exponential distribution (Eq. 6-32 and 6-33). However, the MRS data for $20 < L < 100 \mu\text{m}$ does clearly indicate that the stress imposed on the Si due to the Cu metallisation does appear to decrease with line width. This phenomenon could be explained in terms of a self-annealing effect in the Cu line [174] - [176].

Graham *et al.* [175] found that the copper self- annealing is a function of the copper line widths in that the smaller Cu line widths require a higher activation energy to achieve full recrystallisation than the wider ones. In addition, Lagrange *et al.* [176]

investigated the Cu self-annealing phenomenon as a function of the Cu thickness, and found that the self-annealing is slowed down for a thinner Cu layer due to physical restrictions, while the thicker layer approached the grain size of recrystallised copper, forcing growth to proceed in two dimensions (2-D). Therefore, the stress relief tends to be lower when the layer is thinner due to the physical limitation. Brongersma *et al.* [174] agrees with Lagrange *et al.* [176]. Nevertheless, Brongersma also mentioned that a very rapid primary crystallisation occurred from the top surface down just after deposition, which was then followed by a slower lateral recrystallisation producing large secondary grains. The physical limitation of the Cu lines could explain the self-annealing phenomenon as a function of the Cu volume in that the recrystallisation process could not occur when the Cu line width becomes very small since the density of grains per volume, is not large enough for the recrystallisation process to occur. Therefore, the stress in Si due to the small Cu line widths is still frozen within, whereas the stress in the Si due to the wider Cu metallisation is relieved by the self-annealing process. From MRS and FEM results in Figure 6-69, it can be concluded that the stress generated in the Si is mainly due to the geometrical effect without self-annealing at $L < 20 \mu\text{m}$, whereas the self-annealing may influence the stress imposed on Si for $20 < L < 100 \mu\text{m}$. The latter phenomenon can be examined using Atomic Force Microscopy of the Cu grain density (AFM).

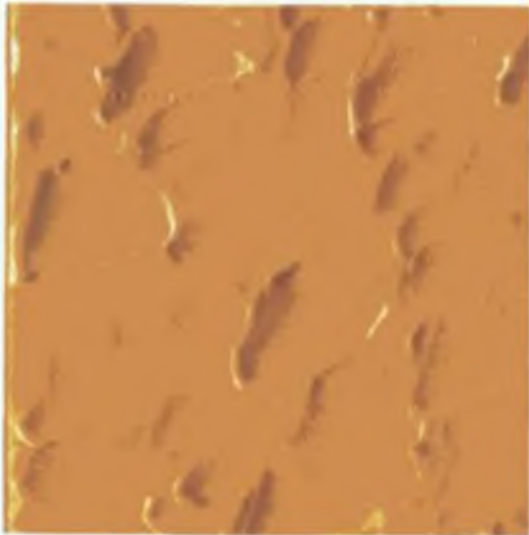
To investigate the grain size/density in the copper as a function of the Cu line widths due to the self-annealing effect, atomic force microscopy (AFM) was indeed performed using Pacific Nanotechnology AFM system series 2002. A contact mode with 2 Hz scan rate and $2.15 \mu\text{m}$ sampling area were employed in this experiment. The AFM results for Cu line widths of 2, 4, 8, 10, 20, 60 and $100 \mu\text{m}$ are illustrated in Figures 6-70 (a)-(g), respectively.



(a)



(b)



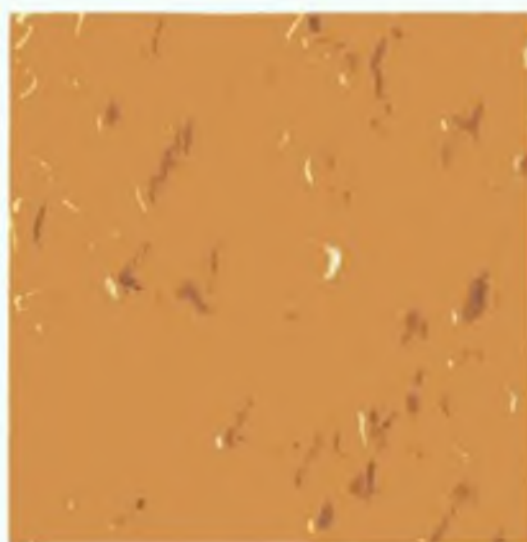
(c)



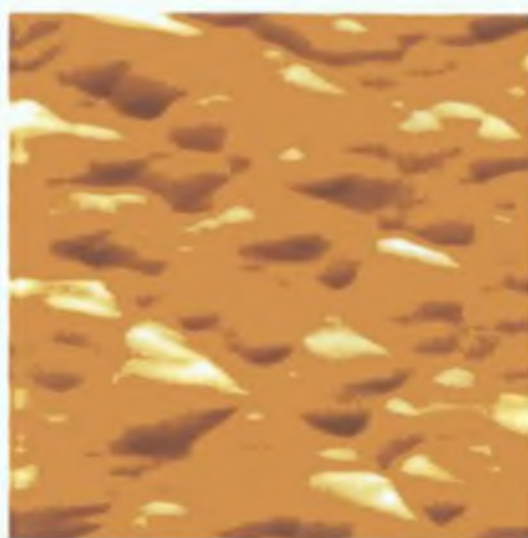
(d)



(e)



(f)



(g)

Figure 6-70 AFM results for the electroless Cu as a function of the Cu line widths of (a) 2 μm , (b) 4 μm , (c) 8 μm , (d) 10 μm , (e) 20 μm , (f) 60 μm and (g) 100 μm . Note: image dimensions: 2.15 μm x 2.15 μm .

The AFM results (Fig. 6-70) show that the grain sizes of the Cu lines are about 0.3-0.5 μm for line widths of 2 μm – 20 μm and thereafter start forming copper clusters when the Cu line width gets bigger, i.e. $L > 60 \mu\text{m}$. This implies that the cluster formation is related to the relief of some stress in the Cu lines and thus also in the underlying Si. This result confirms that the self-annealing phenomenon influence the stress in Si only when $20 < L < 100 \mu\text{m}$.

6.3.3.4 Effect of Annealing Process on Stress Distributions in Si Substrate due to the Electroless Cu Metallisation

In this part, we report on the measurements were performed on the annealed 500 nm electroless Cu samples, henceforth called the *Post-annealed* samples with 2, 4, 8, 10, 20, 60 and 100 μm Cu line widths. This experiment is to investigate the impact of thermal processing steps on the Cu metal strain, etc. Some detail on what sort of thermal steps would/could be involved is essential. The normal (σ_{xx}) stresses in the Si substrate at the Si/metal interface calculated from the Raman shift in the Si under these Cu lines are illustrated in Figure 6-71.

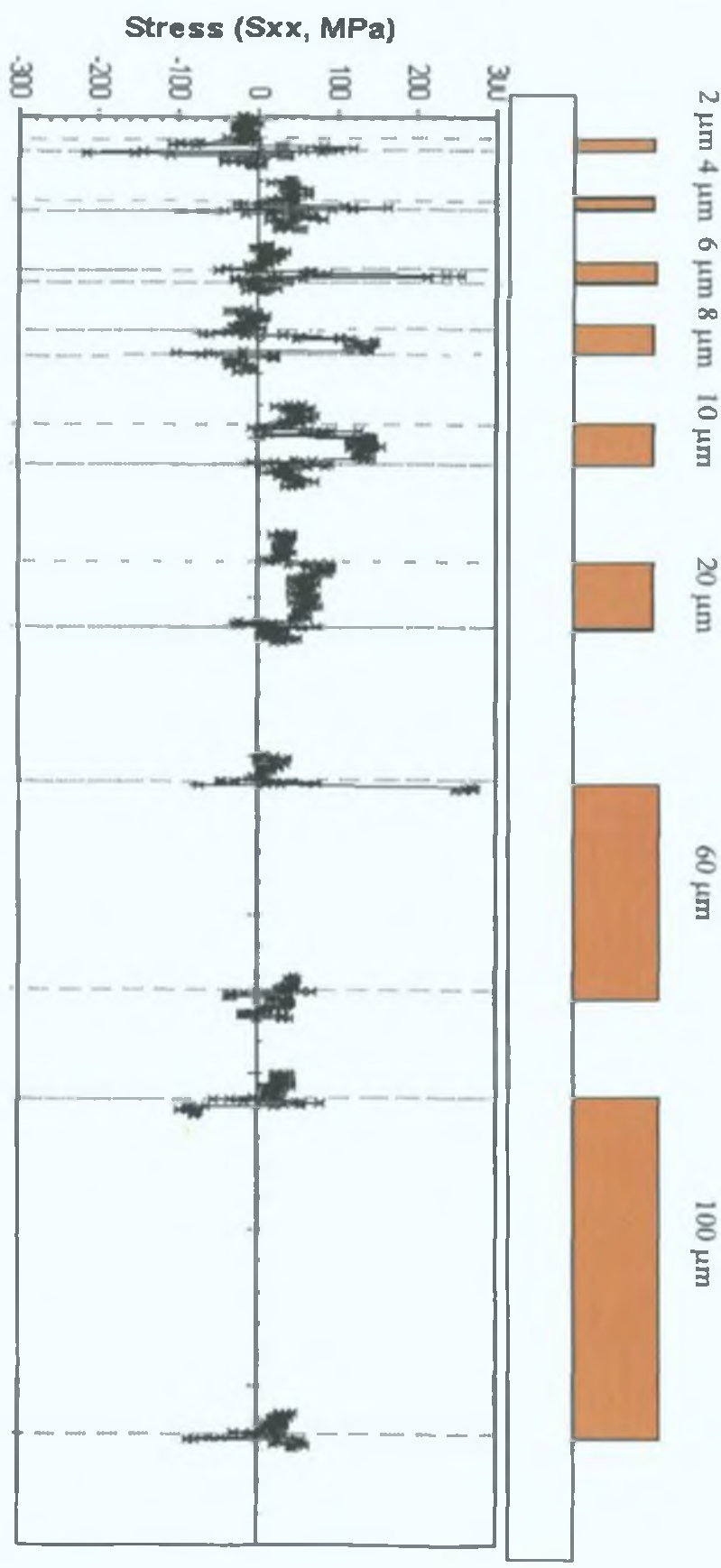


Figure 6-71 The normal stress (σ_{xx}) in the Si substrate just below the

Si/metal interface due to the 500 nm electroless Cu metallisation as a function of Cu line width after annealing at 400 °C (*Post-annealed sample*).

The relationship between the Cu line width and the stress imposed in the Si near the edge of the Cu line due to the effect of annealing is shown in Figure 6-72 below.

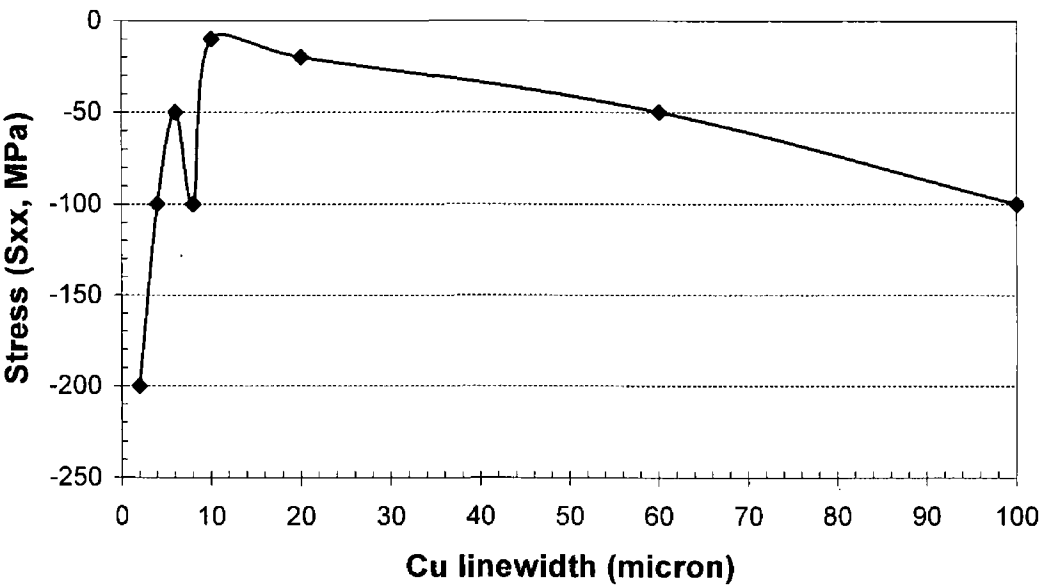


Figure 6-72 Relationship of the normal stress (σ_{xx}) in Si imposed due to the Cu metallisation near the edge of the metal line after annealing at 400 °C as a function of Cu line width.

Figure 6-72 shows that the normal stresses in Si are shifted to the compressive state for the entire range of the Cu line widths after annealing. However, the overall shape of the curve for the relationship of the *Post-annealed* sample stress and Cu line width is similar to that for the *Pre-annealed* sample (Fig. 6-69) in that the stresses increase with increasing Cu line widths for line widths below ~10 μm . Subsequently, the tendency changes as the normal stresses decrease with increasing Cu line width in the 10-100 μm range.

Again, the AFM measurement was performed using the same system and the same settings as previously used to investigate the grain size/density of the Cu as a function of the Cu line widths after annealing at 400 °C. The AFM result for Cu line widths of 4, 6, 8, 10, 20, 60 and 100 μm are portrayed in Figures 6-73 (a) – (g), respectively.



2.15 μm

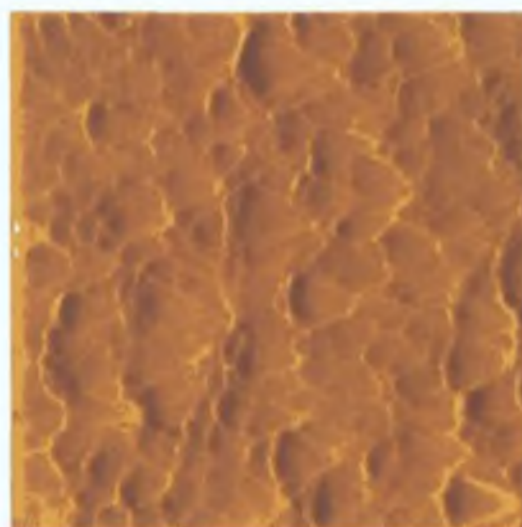
(a)



(b)



(c)



(d)

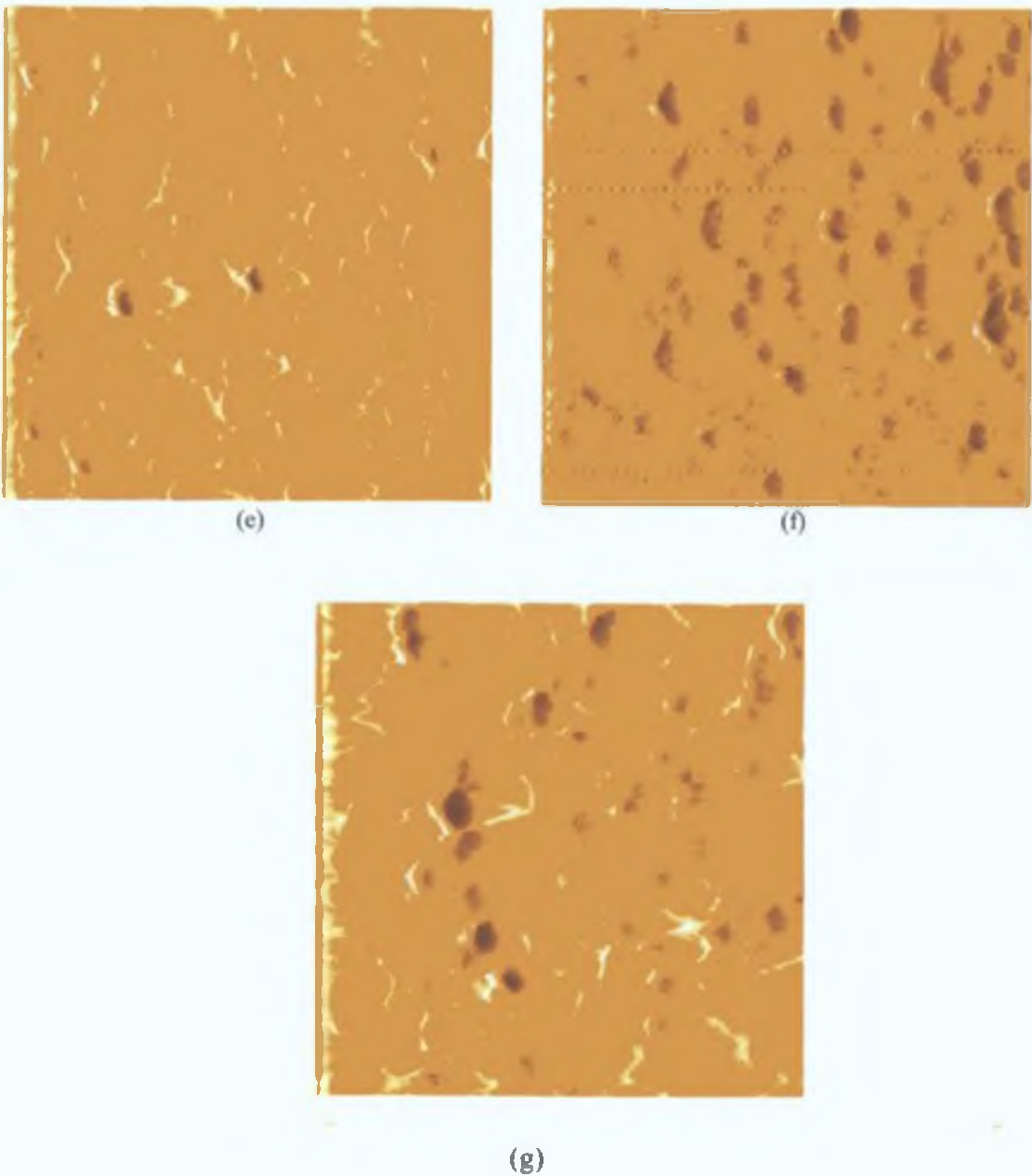


Figure 6-73 AFM results for the electroless Cu on Si samples as a function of the Cu line widths of (a) 4 μm , (b) 6 μm , (c) 8 μm , (d) 10 μm , (e) 20 μm , (f) 60 μm and (g) 100 μm after annealing at 400 °C.

The AFM results in Figures 6-73 (a)–(g) show that the grain sizes of the Cu lines are similar tendency to the AFM results of the *Pre-annealed* one (Figs. 6-70 (a)-(g)).

In this case, the grain sizes of the Cu lines are about 0.3-0.35 μm for line widths less than 10 μm and thereafter start forming copper clusters with an average grain size of about 0.2 μm when the Cu line width gets bigger, i.e. $L > 60 \mu\text{m}$. This suggests the stress imposed on the Si substrate, as a function of the Cu line widths should be about the same, if the stress were correlated to Cu grain size. However, this result does not appear to explain the shift of the stress in the Si due to the Cu lines to a compressive state.

The shift of the stress imposed on the Si due to the annealing step is possibly due to the thermal mismatch between the Si, the metal layers, and the any possible new metallic compounds created in the metal layers. This may be resolved by using XRD, which will be described in the next section.

6.3.4 X-Ray Diffraction (XRD) Results and Discussions

The aim of this measurement is to investigate if new intermetallic compounds are produced in the annealing atage as noted in the MRS results and subsequent discussion. The *Pre*- and *Post*-annealed samples were classified as follows:

- *Pre*-metallisation sample and *Post*-annealed
- *Post*-electroless Cu metallisation and *Post*-annealed
- *Post*- sputtered Cu metallisation and *Pre*-annealed
- *Post*-sputtered Cu metallisation and *Post*-annealed

The XRD measurements were performed using a Philips X'Pert PRO XRD system with a model PW3040 (mppc) x-ray generator and a model PW3050/65 goniometer. The XRD patterns were compared with standard patterns from the Powder Diffraction File Release 2000, Data Sets 1-50 plus 70-88, International Centres for Diffraction data [173].

The XRD pattern of the *Pre*-metallisation and *Post*-annealed sample is illustrated in Figure 6-74 below.

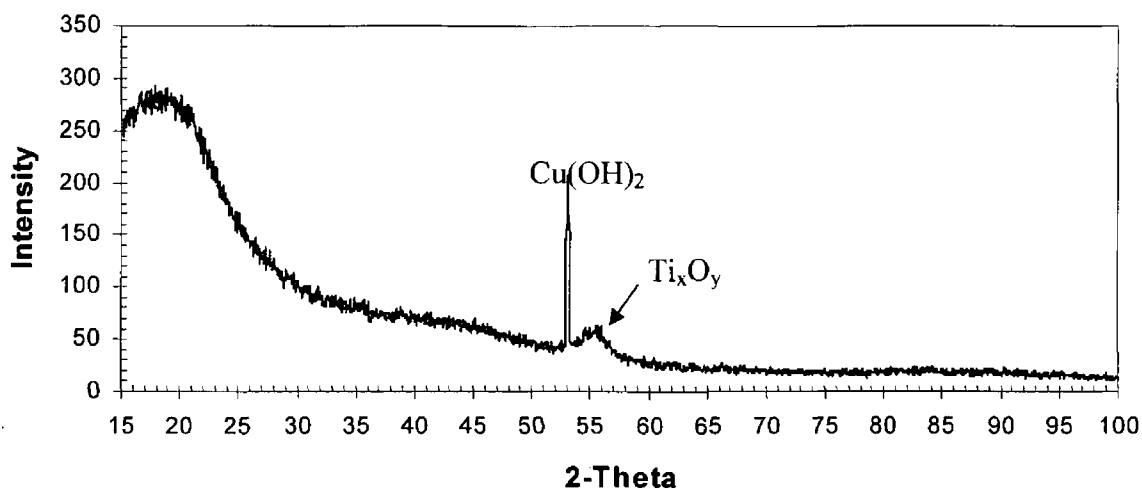


Figure 6-74 The XRD pattern of the Pre-metallisation (20 nm Cu seed/ 100 nm Ti/ Si) sampled, which was annealed at 400 °C.

From Figure 6-74, two peaks are distinguishable in the XRD pattern at 2θ values of 53.05° and 56° . Compared to the standard XRD patterns, it is likely that the peak at 53.05° is due to $\text{Cu}(\text{OH})_2$ (72-0140) and the peak at 56° is from a compound of Ti and O, e.g. Ti_6O_{11} (76-1266) or Ti_7O_{13} (85-1059), etc. This suggests strongly that the annealing step generated an oxide compound in the metal layers.

The XRD pattern of the *Post*-electroless Cu metallisation sample before annealing is depicted in Figure 6-75.

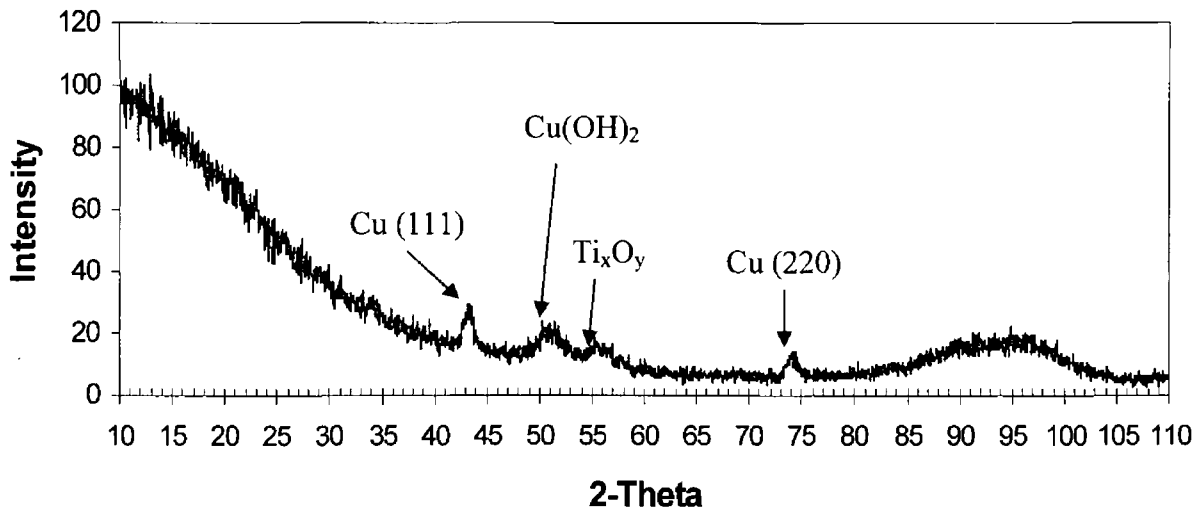


Figure 6-75 The XRD pattern of the *Post-electroless, Pre-annealed* Cu metallisation sample.

The XRD pattern in Figure 6-75 indicates that the Cu electroless plating technique created Cu predominantly orientated along $\langle 111 \rangle$ and $\langle 220 \rangle$ planes. In addition, the Ti-oxide compound and $\text{Cu}(\text{OH})_2$ are visible as in the pre-metallisation process.

The sample was then annealed, i.e., the *Post-electroless, Post-annealed* Cu sample, and investigated using XRD. The XRD result is depicted in Figure 6-76.

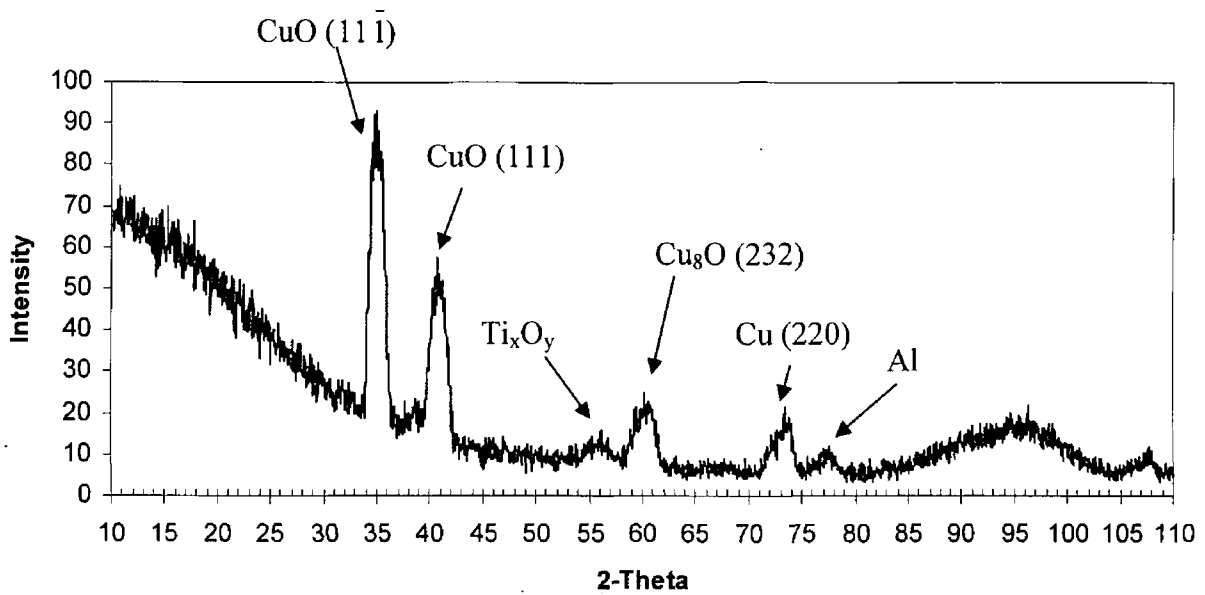


Figure 6-76 The XRD pattern of the *Post*-electroless Cu metallisation sample, which was annealed at 400 °C.

After annealing, the Cu is oxidised and produces CuO and Cu₈O compounds. The peak at 78° indicates the Al material, which is most likely from the Al sample holder during the XRD measurement.

The *Post*-sputtered Cu metallisation sample for both *Pre*- and *Post*- annealing is also evaluated using XRD. The XRD patterns of the *Pre*- and *Post*- annealed samples of the *Post*-sputtered Cu metallisation are illustrated in Figures 6-77 and 6-78.

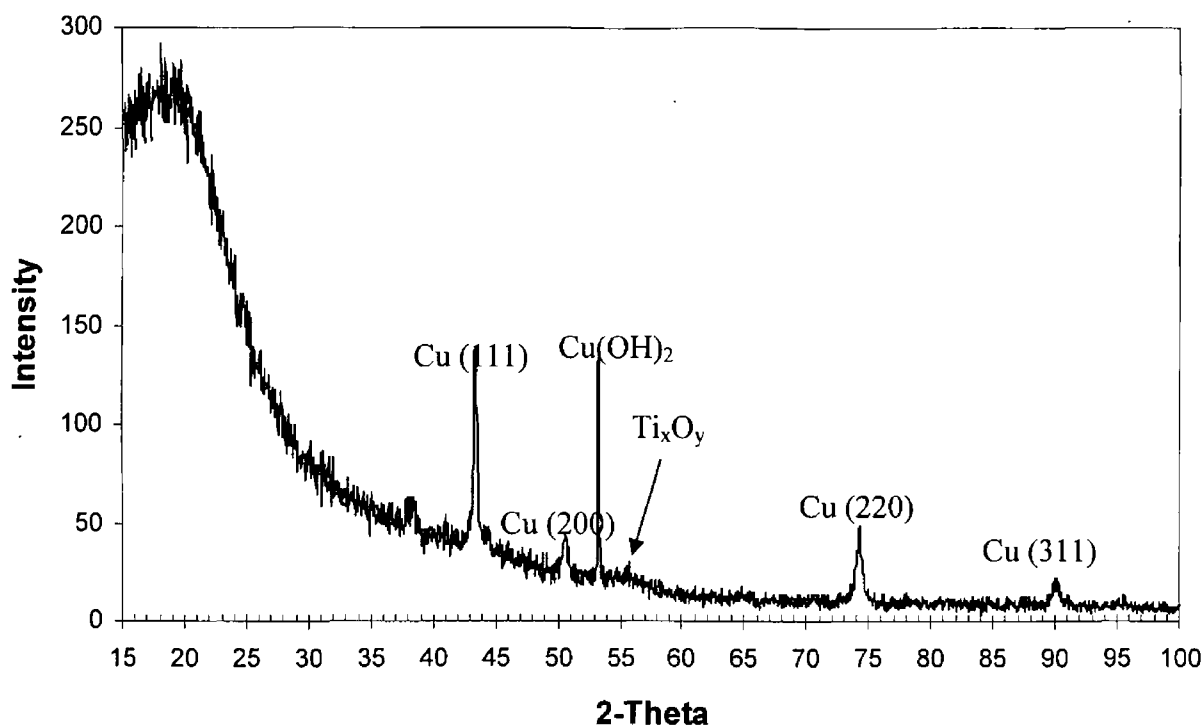


Figure 6-77 The XRD pattern of the *Post-sputtered, Pre-annealed* Cu metallisation sample.

The XRD of the *Post-sputtered* Cu metallisation sample reveals that the copper deposited using the sputtering technique consists preferentially of several film textures, i.e. $\langle 111 \rangle$, $\langle 200 \rangle$, $\langle 220 \rangle$ and $\langle 311 \rangle$. In addition, the Ti-oxide compound and $\text{Cu}(\text{OH})_2$ are also visible as indicated in Fig. 6-77.

The sample was then annealed and the XRD measurement was performed. The XRD pattern of the *Post-annealed, Post-sputtered* Cu metallisation is shown in Figure 6-78.

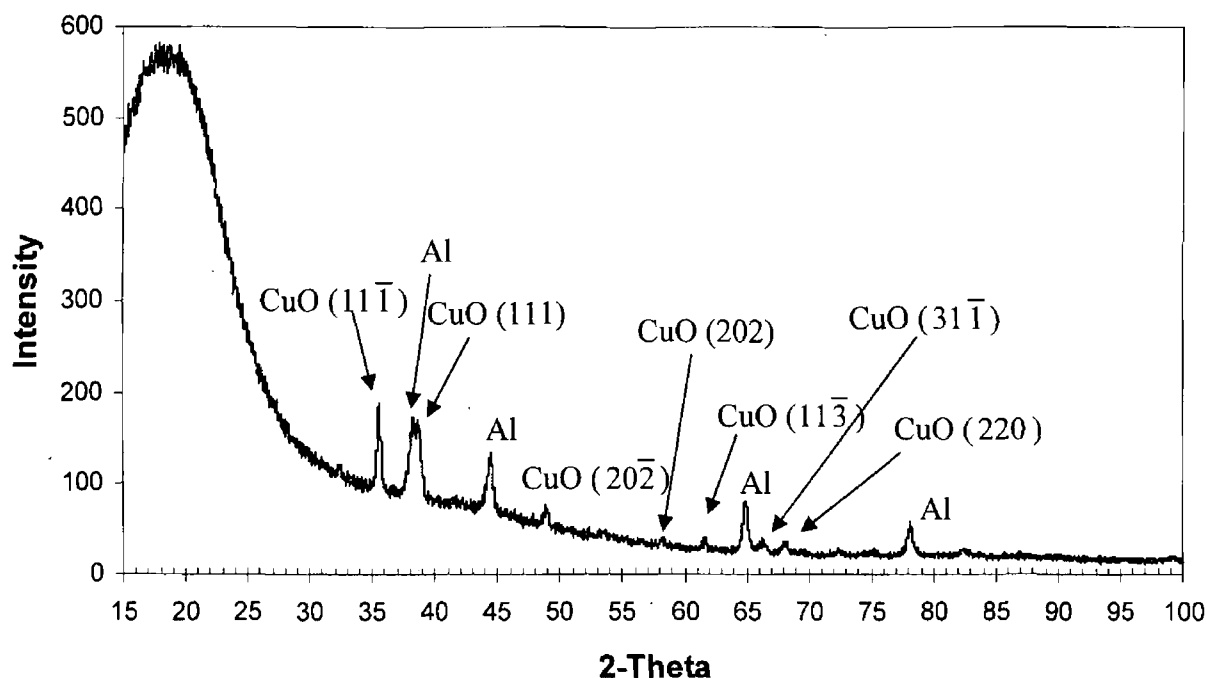
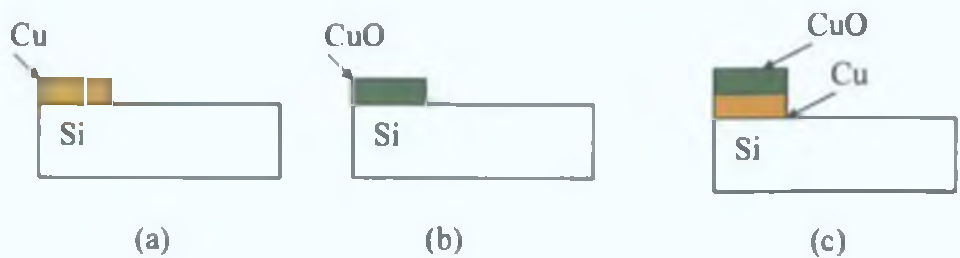


Figure 6-78 The XRD pattern of the *Post*-sputtered Cu metallisation sample after annealing at 400 °C.

The XRD pattern of the *Post*-annealed *Post*-sputtered Cu metallisation sample shows that the annealing process generated an additional CuO compound, which is in good agreement with the *Post*-annealed *Post*-electroless Cu metallisation sample. In addition, Al peaks were visible in the XRD pattern. Again, this Al most likely is from the sample holder during XRD measurement.

From the XRD results, we can comment on the possible impact on the stresses distributions in the Si substrate due to the electroless and sputtered Cu metallisation, and the effect of annealing as follows:

- After annealing, a CuO compound was found in both electroless and sputtered Cu metallisation samples. This could result in the shift of the stress state of Si substrate as exhibited by the MRS measurement. In this circumstance, three cases were calculated and compared, i.e. (a) Cu/Si, (b) CuO/Si, and (c) CuO/Cu/Si as shown below;



This approximation of the maximum stress imposed in Si due to bilayer systems of cases (a) Cu/Si and (b) CuO/Si can be evaluated Eq. 6-31, i.e.

$\sigma_{\max} = \Delta\alpha \cdot E \cdot \Delta T / (1 - \nu)$, where $\Delta\alpha = 13.6$ ppm/ $^{\circ}\text{C}$ for Cu-Si and ~ 21.2 ppm/ $^{\circ}\text{C}$, and ΔT is the temperature different between the strained and unstrained condition. For CuO-Si as a result of the maximum stress of ~ 100 MPa for case (a) Cu/Si and ~ 250 MPa for case (b) CuO/Si. For case (c) CuO/Cu/Si, a multilayer system is given by Hsueh [180] as

$$\sigma_1 = \frac{2(3z + 2t_1)}{t_1^2} \sum_{i=1}^n E_i t_i (\alpha_i - \alpha_1) \Delta T, \text{ where } z = \text{total thickness and } t_1 =$$

substrate thickness. The approximate stress calculated in case (c) is ~ 150 MPa. All cases give the stress in Si in compressive state. This magnitudes suggest the higher stress imposed in Si could be greater after the Cu sample was annealed. In addition, this estimation suggests that the CuO layer appeared after annealing put stress into Si to compressive state.

6.4 Conclusions

The aim of this chapter is to study the stress imposed in the Si substrate due to the Cu metallisation techniques used in IC processing. The SXRT technique showed that the stresses in Si due to the electroless Cu metallisation were intense at the edge of the metal lines and were compressive at the interface between Si and the metal layers, as confirmed by the theory of Meieran and Blech for extinction contrast in SXRT. This result agreed with the FEM simulations.

Two metallisation techniques were used in this study: the electroless plating technique and the sputtering technique. SXRT results indicated that the Cu deposited using the sputtering technique generated greater stress in the Si than when using the electroless plating technique. This was further elucidated using the XRD results. This Cu texture could be related to the stress in the Si substrate in terms of the lattice mismatch in Cu itself, which increases the surface energy as described by Wong *et al.* [179], thus imposing an additional stress in Si. However, the MRS results suggested that the magnitude of the stresses in the Si wafers at the edge of the metal were alike, including when both electroless and sputtered Cu samples were heated to 100, 200, 300 and 400 °C. The SXRT topographs indicated that the stress was mostly relieved at 200°C and the stress (via black/white contrast) became greater with higher temperatures (300 and 400°C). This is due to the stress transition effect as outlined in this chapter.

The influence of the Cu line width on the stress in the Si wafer was studied. The stress distributions in Si as a function of the Cu line width for $2 \leq L \leq 100 \mu\text{m}$ electroless Cu lines were investigated. The FEM result is in accordance with the MRS results. In addition, the relationship between the stress and the Cu line width, studied using the MRS technique was divided into 2 ranges. For Cu line widths less than 20 μm , the stress increased with increasing the Cu line width due to the thermal stress without the self-annealing effect, whereas the stress decreased with increasing

line widths in the range of 20-100 μm due to the thermal stress with the self-annealing effect. This self-annealing phenomenon was observed using AFM.

The effect of the annealing process on the Cu metallisation was investigated using the MRS technique. It is observed that the stresses in the Si shifted to a compressive state after annealing at 400 °C. In addition, the relationship between the stress and the Cu line width of the *Pre*-annealed sample displays the same tendency as that of the *Post*-annealed sample. The XRD results indicated that the shift of the stress in Si wafer is possibly caused by the oxidation of Cu (CuO) during the annealing process. Even though the annealing process in manufacturing practice is usually in nitrogen atmosphere, this study can relate to ageing processes of oxygen, which can enter the package over the long term.

CHAPTER 7 CONCLUSIONS AND FUTURE PLANS

This project is aimed at examining the stress/strain imposed on Si substrates due to flip-chip reflow process and due to Cu metallization in IC processing. To evaluate these issues, synchrotron x-ray topography (SXRT) and micro-Raman spectroscopy (MRS) were employed. Both results were compared to finite element stress modelling (FEM) in order to understand the behaviour of the materials due to elevated process temperature steps. Finally, x-ray diffraction (XRD) was used to examine the material compounds, which could be related to the major sources of strain in the Si wafer due to these processes.

7.1 Solder Bump Reflow Process Induced Stress Distribution in Silicon Substrates

7.1.1 Summary

In the case of the flip-chip reflow process, the stress distributions in Si substrates due to the reflow process and UBM etching times were observed using synchrotron x-ray topography. It was found that after the reflow process, the x-ray topographic extinction and orientational contrasts were greater in areal dimension. In addition, a shear stress magnitude of the order of 100 MPa was observed via orientational contrast. These were attributed to the elevated temperatures used in the reflow process. After the removal of the Pb/Sn bumps, the orientational contrast due to the severe strain fields could not be observed in the topographs. This confirmed that the reflow process was one of the major sources of strain fields in the Si substrate. In addition, the shear strains simulated from FEM as well as the uniaxial stress data from MRS show similar results with respect to the SXRT measurements.

It is also found that after the reflow process, when the UBM etching time was increased from 15 to 25 minutes, the stress distributions in the Si substrates were visible via x-ray topography and were of the order of magnitude of 100 MPa.

However, for the 30 minutes etching time, no orientational contrast was observed in the BRST images. This suggests that the strain fields in Si substrate were now smaller and this could be due to the residual UBM layer and some passivation layers being etched off the sample.

The XRD measurements were performed on the etched back, *post*-reflowed process sample and compounds of Ni and Ti were visible. This confirmed that the stress imposed on the Si substrate represented by the orientational contrast in Figure 5-31(c) is generated from the Ni and Ti in the UBM layer. TEM revealed that several Ni, Sn and V compounds were found at the UBM/solder bump interface. Ni_3Sn_4 is a major intermetallic phase after the reflow process and this new intermetallic compound could be a major strain source in the Si substrate. Thus, it can be concluded that the major sources of the strain field after the reflow process are the Pb/Sn material which covered the UBM layer after reflow and the intermetallic materials which are generated during the elevated temperature steps.

MRS analysis indicated that the uniaxial stress (σ_{xx}) changed from a compressive stress of 100 MPa to a tensile stress of 300 MPa after the reflow process. It is found that the FEM result correlates well with the MRS result and this stress shift is primarily due to CTE differences in the materials in the ball grid array structure..

7.1.2 Future Plans

As mentioned in Chapter 5, moves towards using lead-free solder addresses the need for environmentally conscious assemblies. With respect to the green movement in the electronics industry, environmental issues result from the concern that lead-bearing materials, such as Sn/Pb solders, will end up in landfills. Lead can then possibly leach into ground water, causing a potential health hazard for current and future generations.

In response to this issue, the European Union (EU) has proposed banning lead from electronics by 2004 [89]. Correspondingly, Japan has established mandates that,

when taken together, will also eliminate lead from electronic products. Japanese firms are already manufacturing and marketing several lead-free consumer products. This also compels the U.S. electronics industry to develop materials and assembly practices to support this global movement.

In order to support a new solder material, UBM, passivation materials and dielectric materials will be substituted to compatible with new kinds of solder bumps. Therefore, the reliability of the mechanical stress will be one of a major concern. Several kinds of lead-free solder and other solder materials are focused as new candidates for the future. Therefore, understanding of the stress distribution in Si wafer of these following materials should be considered

- Sn-Ag-Cu alloy,
- Sn-Ag-In-Cu alloy
- Electroplating Cu materials or so-called Cu bump [1].

7.2 Copper metallisation Process Induced Stress Distribution in Silicon Substrates

7.2.1 Summary

The aim of this segment was to study the stress imposed in Si substrates due to the Cu metallisation techniques used in IC processing. The SXRT technique showed that the stresses in Si due to the electroless Cu metallisation were intense at the edge of the metal lines and were compressive at the interface between Si and metal layers, as confirmed by the theory of Meieran and Blech for extinction contrast in SXRT. This result agreed with the FEM simulations.

Two metallisation techniques were used in this study: the electroless plating technique and the sputtering technique. SXRT results indicated that the Cu deposited using the sputtering technique generated greater stress in the Si than when using the electroless plating technique. This was further elucidated using the XRD results.

The Cu deposited by the sputtering technique is composed of several lattice orientations, whereas the Cu deposited by the electroless plating technique consists of only $\langle 111 \rangle$ and $\langle 110 \rangle$ orientations. This Cu texture could be related to the stress in the Si substrate in terms of the cavity or lattice mismatch in Cu itself imposing an additional stress in Si. However, the MRS results exhibited that the magnitude of the stresses in the Si wafers at the edge of the metal were alike, including when both electroless and sputtered Cu samples were heated to 100, 200, 300 and 400 °C. The SXRT topographs indicated that the stress was almost relieved at 400°C due to the slower self-annealing effect compared to electroless Cu.

The influence of the Cu line width on the stress in the Si wafer was studied using FEM and MRS. Both results suggest that the generated stress versus line width (L) tendency is a function of the geometrical arrangement. The stress (σ_{xx}) due to the electroless copper metallisation can be empirically related to the Cu line width in terms of an exponential distribution (Eq. 6-32 and 6-33). In addition, the AFM results confirm that the stress generated in the Si for Cu line widths $L < 20 \mu\text{m}$ is due to the geometrical effect without the influence of the self-annealing. For line widths with $20 < L < 100 \mu\text{m}$ the stress imposed on the Si due to the Cu metallisation does appear to decrease with line width. This is most likely due to the self-annealing effect correlating with the geometrical effect.

The effect of the annealing process on the Cu metallisation was investigated using the MRS technique. The AFM result confirms the similar tendency of the stress as a function of the Cu line widths. It is observed that the stresses in the Si shifted to a compressive state after annealing at 400 °C. In addition, the relationship between the stress and the Cu line width of the *Pre-annealed* sample displays the same tendency as that of the *Post-annealed* sample. The XRD results indicated that the shift of the stress in Si wafer is possibly caused by the oxidation of Cu (CuO) during the annealing process.

7.2.2 Future Plans

Although the impact of a number of processing steps on the stress imposed in the Si substrate due to the Cu metallisation were performed in this study, several interesting issues could be examined in the future:

- Study the stress distributions in Si wafer due to electrochemical Cu metallisation in a dual damascene metallisation scheme, as this is an actual pattern in industry.
- Examine the influence of the low-k dielectric materials both inorganic and organic such as fluorosilicate glass (FSG), Black diamond™ (AMAT), Coral™ (Novellus) and SiLK™ (Dow Corning) on the stress in Si wafers due to the electrochemical Cu metallisation.
- Study the effect of barrier layers such as TiN, Ta and TaN on the stress distributions in Si wafer due to electrochemical Cu metallisation.

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Appendix A Publications

A-1

Investigation of Mechanical Stresses in Underlying Silicon due to Lead-Tin Solder Bumps via Synchrotron X-Ray Topography and Finite Element Analysis

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Investigation of Mechanical Stresses in Underlying Silicon due to Lead-Tin Solder Bumps via Synchrotron X-Ray Topography and Finite Element Analysis

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ABSTRACT

Solder based flip-chip packaging has prompted interest in many integrated circuit (IC) packaging applications due to its many advantages in terms of cost, package size, electrical performance, input/output density, etc. The ball grid array (BGA) is one of the most common flip-chip packaging techniques used for microprocessor applications. However, mechanical stresses induced by the flip-chip process can impact adversely on the reliability of production.

White beam synchrotron x-ray topography (SXRT), a non-destructive technique, has been employed to investigate the spatial extent of strain fields imposed on the underlying silicon substrate for Intel®Pentium®III microprocessors due to the lead-tin solder bump process for BGA packaging. Large area and section back-reflection SXRT images were taken before and after a simulation of the reflow process at 350°C in atmosphere. The presence of induced strain fields in the Si substrate due to the overlying bump structures has been observed via the extinction contrast effect in these x-ray topographs. In addition, orientational contrast effects have also been found after the reflow process due to the severe stresses in the underlying silicon beneath the lead bumps. The estimated magnitudes of stress, $|\sigma|$, imposed on the underlying silicon

were calculated to be 100 MPa. The spatial strains in the underlying silicon were relieved dramatically after the lead bumps were removed from the wafer, which confirms that the bumps are indeed a major source of strain in the underlying Si. Finite element analysis (FEA) has also been performed in 2-D plane strain mode. The magnitudes and spatial distribution of the stresses after the reflow process are in good agreement with the SXRT results.

INTRODUCTION

Since semiconductor devices have significantly decreased in geometry and enormously increased in electronic design complication, packaging technology has had a major influence on device performance and reliability. Flip-chip technology was launched to increase I/O count, improve electrical performance, reduce packaging size and be cost effective [1]. The Intel®Pentium®III microprocessor uses the popular ball grid array (BGA) packaging technique. A C4 (Controlled Collapse Chip Connection) technique has been employed for the solder bumping process. Ti/Ni based films were used as barrier layer metallisation (BLM) and a lead-tin solder bump with high lead content was formed using the C4 electroplating technique [1,2]. Due to the high Pb content in the solder, the solder reflow process needs to be carried out at a high temperature (up to 350°C) and in a nitrogen rich atmosphere.

The aims of this work are to evaluate the residual stress distribution in Si substrates due to the solder bump reflow processing of these ICs using white beam synchrotron x-ray topography, and to predict and compare this observed stress with Finite Element Analysis (FEA).

The white beam synchrotron x-ray topographic (WBSXRT) technique is well known as a method for visualising stress in crystals without damaging the samples. The experiment takes only a few minutes of exposure time for high resolution films. WBXRT is an imaging technique based on the difference in reflecting power between perfect and distorted regions in a crystal sample. Three dimensional stress/strain images can be obtained throughout the entire depth of the semiconductor material under investigation. Geometrical resolution is governed by the synchrotron beam local divergence on the sample and usually lies in the micron range [3].

Finite element analysis (FEA) has been used in packaging analysis since it is known to be an effective method for prediction of mechanical strains in multi-component, thermally loaded systems during and after packaging processes. Most of the current literature employs the FEA technique to simulate the mechanical stress in the flip chip after the underfill process, rather than after the solder bump reflow itself [4-6]. In this work, the mechanical stress induced by a solder bump reflow process has been analysed and compared to the SXRT results.

EXPERIMENTAL DETAILS

The x-ray topography measurements were performed at HASYLAB-DESY, Hamburg, Germany, utilising the continuous spectrum of synchrotron radiation from the DORIS III storage ring bending magnet. Details of the experiments are given in Refs. [3,7-9]. For large area back reflection topography (LA-BRT), reflections recorded on the film provide information on stress/strain distributions in the silicon near the surface (typically 10-100 μm from the surface). On the other hand, back reflection section topography (BRST) provides details of strain/dislocation distributions through a thin slice of the sample near the surface. Due to the high absorption of the Pb/Sn bumps and limitations on the x-ray energy penetration (penetration depth, t_p), the measurements were performed by permitting the x-ray beam to enter via the backside of a thinned down Si wafer ($\sim 150 \mu\text{m}$ thick). This Si thickness, however, is still large enough to evaluate the Pb/Sn bump induced strain without perturbation from the backside. Mechanical polishing was used to decrease the silicon thickness of the wafers.

The Pb/Sn solder bump samples were produced at Intel Ireland Fab Operations, by using C4 short loops of a standard $0.25 \mu\text{m}$ CMOS technology. This technology has been described in detail elsewhere[10]. The samples consist mainly of Silicon substrate (200 mm diameter and $\sim 700 \mu\text{m}$ thickness subsequently thinned down)/ Silicon epilayer/ Aluminium (Al) metal 5 interconnects and pad/ Silicon Nitride passivation/ Polyimide passivation/ BLM (Ti/Ni)/ Pb-Sn solder bump. The geometry is illustrated in Figure 1.

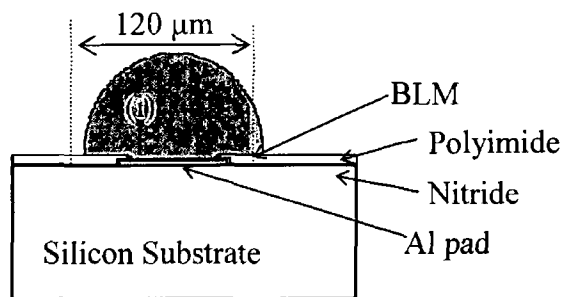


Figure 1. Geometry of Pb/Sn solder bump sample.

The samples were investigated in the following order: 1) *Pre*-reflowed process samples; 2) *Post*-reflowed process using a reflow process simulation at 350°C in atmosphere; and 3) Pb/Sn solder bumps removed from *post*-reflowed sample.

RESULTS AND DISCUSSIONS

WBSXRT analysis was performed at each step to ascertain the major sources of strain distribution in the silicon substrate due to the reflow process. LA-BRT and BRST images for these steps generated by the $\bar{3}\bar{3}9$ reflection are depicted in Figures 2-4. The scratches on the backside of the sample, which were generated from the mechanical thinning and polishing processes, are clearly observed in the image, e.g. see Arrows a in Fig. 3(a). A line across the image represents the approximate position for its corresponding BRST, which illustrates the strains/stresses throughout a slice of Si at this location, e.g. Fig. 2(b).

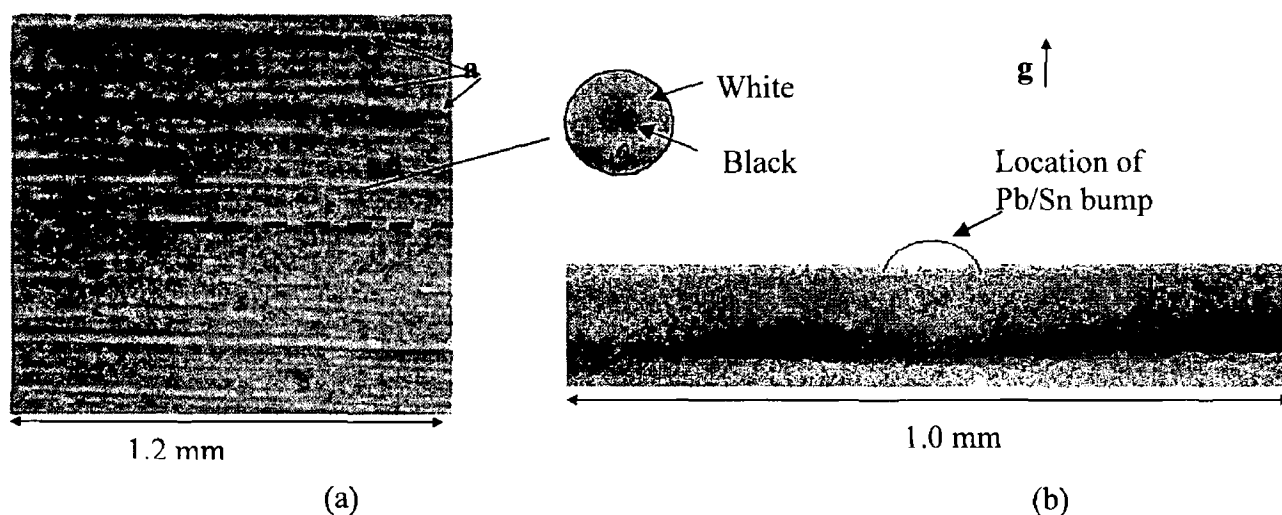


Figure 2. $\bar{3}\bar{3}9$ LA-BRT(a) and BRST(b) of *pre*-reflowed sample.

The region highlighted by the dotted circle in Fig. 2(a)) shows the image associated with the strain field in the underlying silicon due to a single Pb/Sn bump. The magnification of this area illustrates a black and white contrast surrounding the Pb/Sn bumps. The black area represents an increase in recorded intensity. This phenomenon is called the extinction contrast effect [11], and is related to the change in curvature of the crystal lattice planes under the lead bump due to induced strain. The change in lattice plane curvature, especially near the peripheries of the lead bump, will lead to an enhancement or diminution of diffracted intensity in these regions as illustrated in the LA-BRT images.

Figure 3 is the LA-BRT and BRST of the *post*-reflowed sample (sample was heated to 350°C in atmosphere as a reflow process simulation and cooled down to room temperature before measurement). The extinction contrast is observed out to a greater diameter. The strain fields thus extend laterally to a much greater extent than in the *pre*-reflow case (Fig.2(a)). Furthermore, the BRST image of Fig. 3(b) is dramatically different. It is noted that a lifting of the image of strained Si near the Pb/Sn edges above the image of the rest of the Si (dotted circles) occurred due to severe stress imaged via orientational contrast [3-4,12].

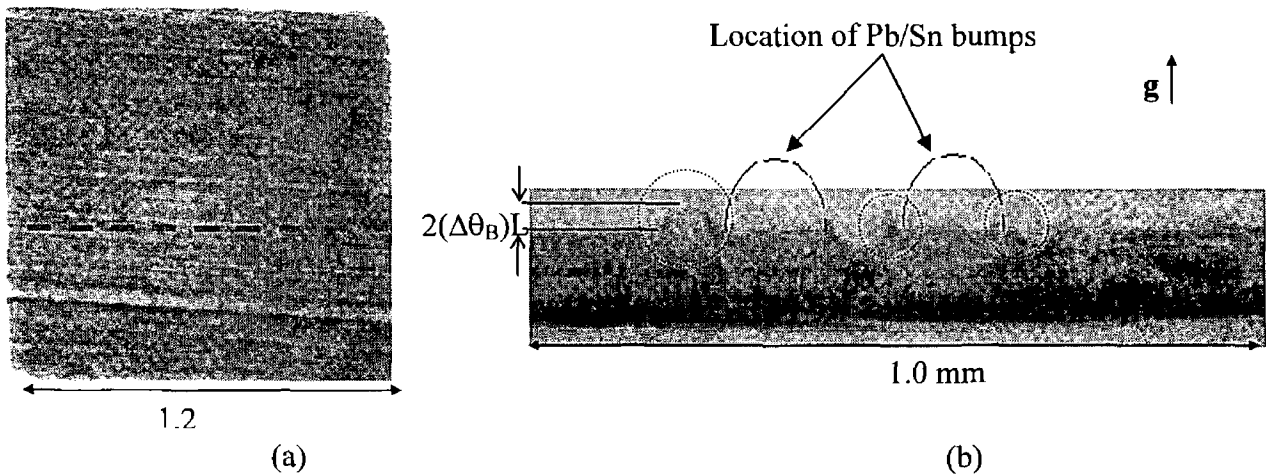


Figure 3. $\bar{3}39$ LA-BRT(a) and BRST(b) of the *post*-reflowed sample.

The orientational contrast can be observed if the misorientation exceeds the x-ray beam divergence ($\Delta\phi$), which is equal to 6×10^{-4} rad. The magnitude of the orientational contrast shift is $\Delta S=2(\Delta\theta_B)L$; where $\Delta\theta_B$ is the maximum shift in Bragg

angle of the severely strained regions and L is the distance between sample and film (in this case = 50 mm). This gives a quantitative estimate for the magnitude of strain in the underlying silicon via the equation:

$$\varepsilon \cong \Delta\theta_B = \frac{\Delta S}{2L} \quad (1)$$

In this case, $\varepsilon = 6.2 \times 10^{-4}$. The magnitudes of stresses are given by $|\sigma| = E|\varepsilon|$ where E , the Young's modulus of Si (isotropic) = 162.3 GPa [13]. Thus, the limit on the stress magnitudes of the order $|\sigma| \approx 100$ MPa.

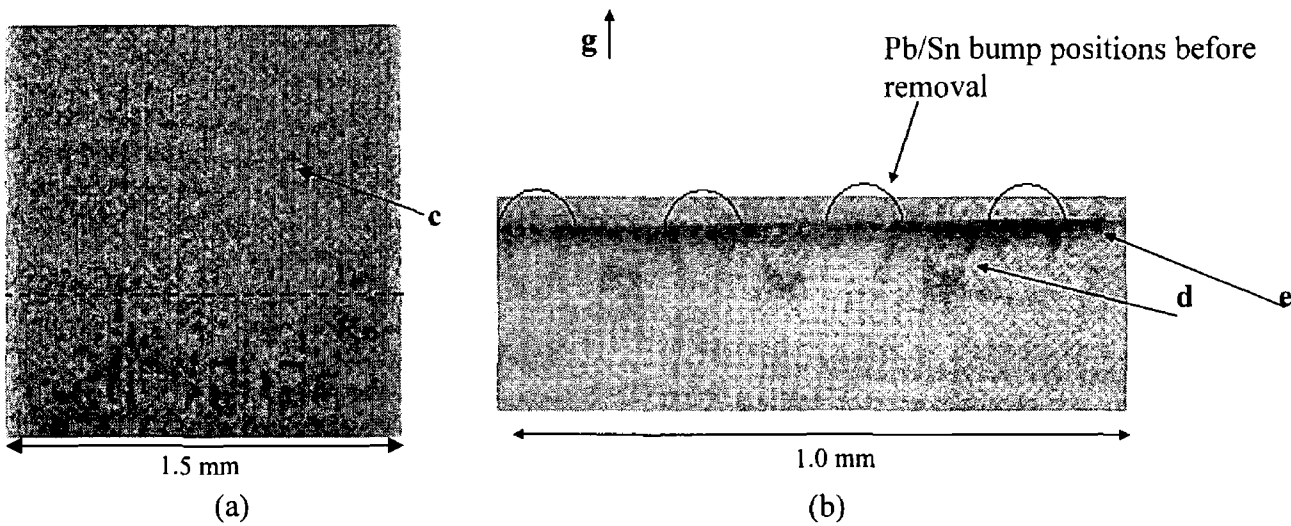


Figure 4. $\bar{3}39$ LA-BRT (a), and BRST (b) of *post*-reflowed sample after removing Pb/Sn bumps.

After the Pb/Sn bumps were reflowed and etched (step 3), residual strains in the underlying Si still appear in the topographs of Figure 4 (Arrows c). It is known that during the high temperature reflow process, inter-metallic compounds are formed at the interface of the Pb/Sn bump and the BLM layer. Considering the BRST image (Figure 4(b)), the strains distributed in the underlying silicon appear to be much smaller when the Pb bumps were removed. Little if any orientational contrast has been found in the BRST image as had previously been observed. However, some small stresses/strains are still present and are visible in the image as indicated by Arrow d (predominantly between bumps) and by Arrow e (near the surface, e.g. epilayer strain, process layers and metallisation). These results confirm that the Pb/Sn bumps are the major source of the strain.

For finite element analysis, two-dimensional (2-D) plane strain finite element models of the multilayer structure have been employed in this study. The geometry, dimensions and boundary conditions of the *post*-reflowed sample are illustrated in Figure 5.

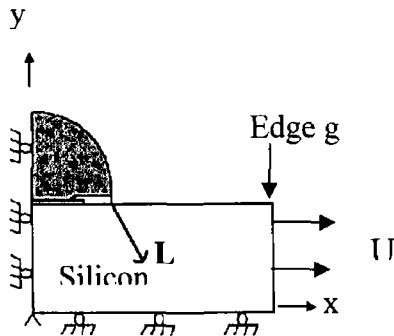


Figure 5. Geometry and boundary conditions of *post*-reflowed sample model.

Approximately 100,000 nodes were used to perform the simulation. The finite element analyses were carried out using Quickfield™ Professional version 4.2 [14]. Eight different materials were considered in these models: Si substrate, Al pad, polyimide passivation, silicon nitride passivation, Ti/Ni BLM, intermetallic layer and Pb/Sn solder bump. These materials are assumed to be isotropic and linearly elastic. To simulate the thermal solder reflow process, a uniaxial load (U) is applied to Edge g in the model. The FEA simulation (Figure 6) confirms the build-up of strain near the edges of the bumps, and the strain magnitudes are of the same order of magnitude as observed by SXRT.

Tensile

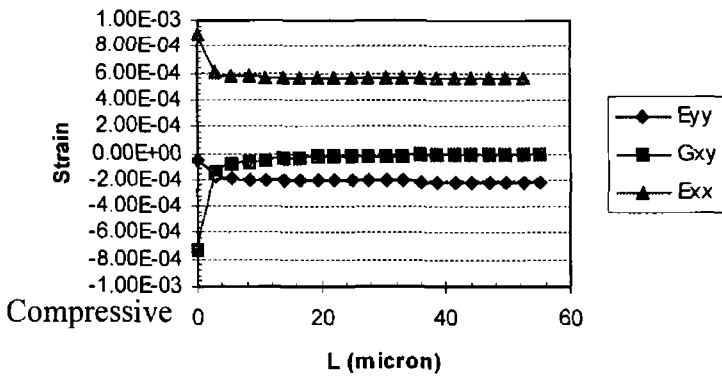


Figure 6. Finite element simulation of tensile/compressive strain distribution in Si along the $\bar{3}\bar{3}9$ direction in the *post*-reflowed sample. $L = 0$ indicates the position of

the periphery of the Pb/Sn bump, E_{xx} and E_{yy} = normal strains in x- and y- directions, and G_{xy} = shear strain.

CONCLUSIONS

White beam synchrotron x-ray topography confirms that the solder reflow process is a major source of strain in Si. This strain is particularly large near the peripheries of the Pb/Sn bumps after the reflow process. A comparison of WBSXRT topographs and FEA models indicate similar strain distributions within the Si substrate.

ACKNOWLEDGEMENT

This work was supported by the TMR-Contract ERBFMGECT950059 of the European Community. The support of T. Wroblewski at beamline F-1 is gratefully acknowledged. J.C. Fitzgerald and R.J. Dunne, Intel Ireland Fab Operations, performed the sample thinning. JK would like to thank the Intel Ireland Academic Relations Programme for contributions to her postgraduate support.

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Evaluation of mechanical stresses in silicon substrates due to lead–tin solder bumps via synchrotron X-ray topography and finite element modeling

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Abstract

Solder-based flip-chip packaging has prompted interest in integrated circuit (IC) packaging applications due to its many advantages in terms of cost, package size, electrical performance, input/output density, etc. The ball grid array (BGA) is one of the most common flip-chip packaging techniques used for microprocessor applications. However, mechanical stresses induced by the flip-chip process can impact adversely on the reliability of products. Synchrotron X-ray topography (SXRT), a non-destructive technique, has been employed to investigate the spatial extent of strain fields imposed on the underlying silicon substrate for Intel® Pentium® III microprocessors due to the lead–tin solder bump process for BGA packaging. Large area and section back-reflection SXRT images were taken before and after a simulation of the reflow process at 350 °C in atmosphere. The presence of induced strain fields in the Si substrate due to the overlying bump structures has been observed via the extinction contrast effect in these X-ray topographs. In addition, orientational contrast effects have also been found after the reflow process due to the severe stresses in the underlying silicon beneath the lead bumps. The estimated magnitudes of stress, $|\sigma|$, imposed on the underlying silicon were calculated to be of the order of 100 MPa. The spatial strains in the underlying silicon were relieved dramatically after the lead bumps were removed from the wafer, which confirms that the bumps are indeed a major source of strain in the underlying Si. Finite element modeling (FEM) has also been performed in two-dimensional (2-D) plane strain mode. The magnitudes and spatial distribution of the stresses after the reflow process are in good agreement with the SXRT results.

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Keywords: X-ray topography; Flip-chip; Finite element modeling; Ball grid array; Stress

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1. Introduction

Since semiconductor devices have decreased significantly in geometry and increased enormously in electronic design complication, packaging technology has had a major influence on device performance and reliability [1]. Flip-chip technology was launched to increase I/O count, improve electrical performance, reduce packaging size and be cost effective [1]. The Intel®Pentium®III microprocessor uses the popular ball grid array (BGA) packaging technique. A C4 (Controlled Collapse Chip Connection) technique has been employed for the solder bumping process [2,3]. Ti/Ni-based films were used as barrier layer metallisation (BLM) and a lead–tin solder bump with high lead content was formed using the C4 electroplating technique [1,4]. Due to the high Pb content in the solder, the solder reflow process needs to be carried out at a high temperature (up to 350 °C) and in a nitrogen-rich atmosphere [5].

The aims of this work were to evaluate the residual stress distributions in Si substrates due to the solder bump reflow processing of these ICs using white beam synchrotron X-ray topography, and to predict and compare this observed stress with finite element modeling. The residual stress in Si is an important parameter as it affects the piezoresistivity value and it could lead to a shift in electrical parameters of the devices such as mobility, transconductance, etc. [6,7]. As the device geometry becomes smaller and smaller, high residual stress in Si could result in the failure of the device. Large stresses can also lead to device failure via, for example, package delamination or cracking [1].

The synchrotron X-ray topographic (SXRT) technique is well known as a method for visualising stress in crystals without damaging the samples. This technique provides a map of strain or defect distributions based on the theory of X-ray diffraction. Image contrast on the recording films is generated via the difference in diffracted intensity between perfect and distorted regions in a single crystal sample. Since the advantageous characteristics of synchrotron radiation include very high intensity beams, continuous spectrum of wavelengths, good collimation and a high degree of polarization, the experiment takes only a few minutes of exposure time for high-resolution films and micrometre resolution images can be readily obtained [8]. Three-dimensional images can be obtained throughout the entire depth of the semiconductor material under investigation depending on the wavelength of the diffracting beam. Geometrical resolution is governed by the synchrotron beam divergence and usually lies in the μm range at beamline F-1 at HASYLAB used in this study [9]. This spatial resolution is given by the relation $\delta = HL/D$, where H is the radiation source dimension, L is the source–sample distance, and D is the sample–plate distance [8]. Since Tuomi et al. introduced SXRT with high-resolution results in 1974 [10], many scientists have utilised this technique to investigate dislocations and other defects in crystals. Subsequently, the theory of the contrast mechanisms has been explained concisely by Authier et al. [11]. Blech and Meieran elucidated the extinction and anomalous phenomena in X-ray topography images made with characteristic X-rays of strained Si during device processing [13–15]. Strain generated by thermal oxide and metallisation processes was simulated and related to the topographic images [12–15]. Schwuttke has also investigated and related similar X-ray topography images of semiconductor dislocations and strain fields due to device processing [16–18]. In later studies, Epelboin modified the Blech and Meieran theory for strain and Kato's theory for diffraction to investigate stress in Si due to a superposed film [19]. Strains and dislocations in semiconductor materials during device processing have been investigated using SXRT [9,20,21,28]. In addition, the strain fields in Si due to wire bonding and packaging of an EPROM device were studied using SXRT [22].

Finite element modeling (FEM) has been used in packaging analysis since it is known to be an effective method for prediction of mechanical strains in multi-component, thermally loaded systems during and after packaging processes. Most of the current literature employs the FEM technique to simulate the mechanical strain in the flip-chip after the underfill process, rather than after the solder bump reflow itself [23–25]. The residual stress in the Si can be increased after the underfilling process. In particular, if no flow underfill material is used, there will be a large difference between the coefficients of thermal expansion (CTEs) of Si, the underfill and the PCB, which can lead to large induced stresses. In this work, the mechanical strain induced by a solder bump reflow process has been analysed and compared to the SXRT results.

2. Experimental details

The X-ray topography measurements were performed at HASYLAB-DESY, Hamburg, Germany, utilising the continuous spectrum of synchrotron radiation from the DORIS III storage ring bending magnet source. The ring operated at a positron energy of 4.45 GeV and at typical currents of 80–150 mA. The back-reflection Laue pattern of topographs was recorded on Geola VRP-M Holographic films having an emulsion grain size of about $0.04\ \mu\text{m}$ [8,9,20,26]. The experimental arrangements for both large area and section back-reflection topographies are illustrated in Fig. 1a and b. For large area back-reflection topography (LA-BRT), reflections recorded on the film provide information on strain

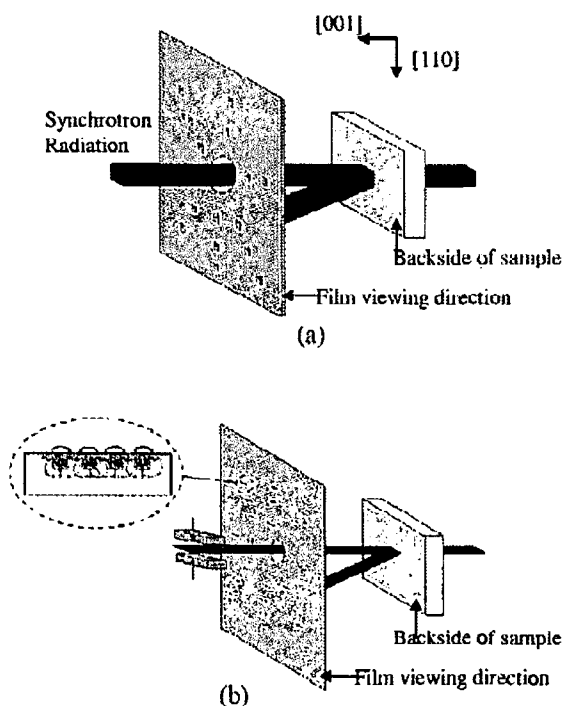


Fig. 1. Experimental setups for (a) large area back-reflection topography (LA-BRT) and (b) section back-reflection topography (BRST).

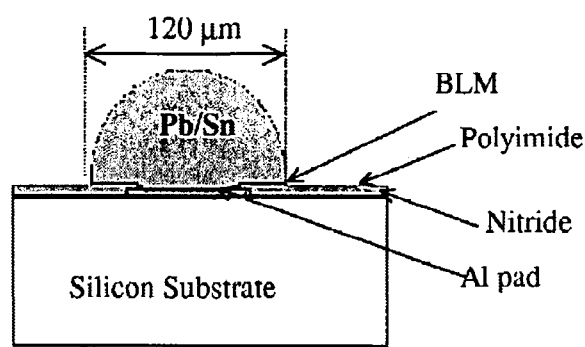


Fig. 2. Geometry of Pb/Sn solder bump sample.

distributions in the silicon near the surface (typically 10–100 μm from the surface). Back-reflection section topography (BRST) provides details of defect distributions through a thin slice of the sample near the surface. Due to the high absorption of the Pb/Sn bumps and limitations on the X-ray energy penetration (penetration depth, t_p), the measurements were performed by permitting the X-ray beam to enter via the backside of a thinned down Si wafer ($\sim 150\text{ }\mu\text{m}$ thick). This Si thickness, however, is still large enough to evaluate the Pb/Sn bump-induced strain without perturbation from the backside. Mechanical polishing was used to decrease the silicon thickness of the wafers.

The Pb/Sn solder bump samples were produced at Intel Ireland Fab Operations, by using C4 short loops of a standard $0.25\text{ }\mu\text{m}$ CMOS technology. This technology has been described in detail elsewhere [27]. The samples consist mainly of Silicon substrate (200 mm diameter and $\sim 700\text{ }\mu\text{m}$ thickness, subsequently thinned down)–Silicon epilayer–Aluminium (Al) metal 5 interconnects and pad–Silicon Nitride passivation–Polyimide passivation–BLM (Ti/Ni)–Pb/Sn solder bump. The geometry is illustrated in Fig. 2.

The samples were investigated in the following order:

1. *pre-reflowed* process samples;
2. *post-reflowed* process using a reflow process simulation at $350\text{ }^\circ\text{C}$; and
3. Pb/Sn solder bumps removed from the *post-reflowed* sample.

3. Results and discussion

SXRT analysis was performed at each step to ascertain the major sources of strain distribution in the silicon substrate due to the reflow process. LA-BRT and BRST images for these steps, generated by the $\bar{3}39$ reflection, are depicted in Figs. 3–5. The scratches on the backside of the sample, which were generated from the mechanical thinning and polishing processes, are clearly observed in the image (e.g. see arrows d in Fig. 3b). A line across the image represents the approximate position for its corresponding BRST, which illustrates the strains throughout a slice of Si at this location (e.g. Fig. 3c).

The region highlighted by the dotted circle in Fig. 3b shows the image associated with the strain field in the underlying silicon due to a single Pb/Sn bump. The magnification of this area illustrates a

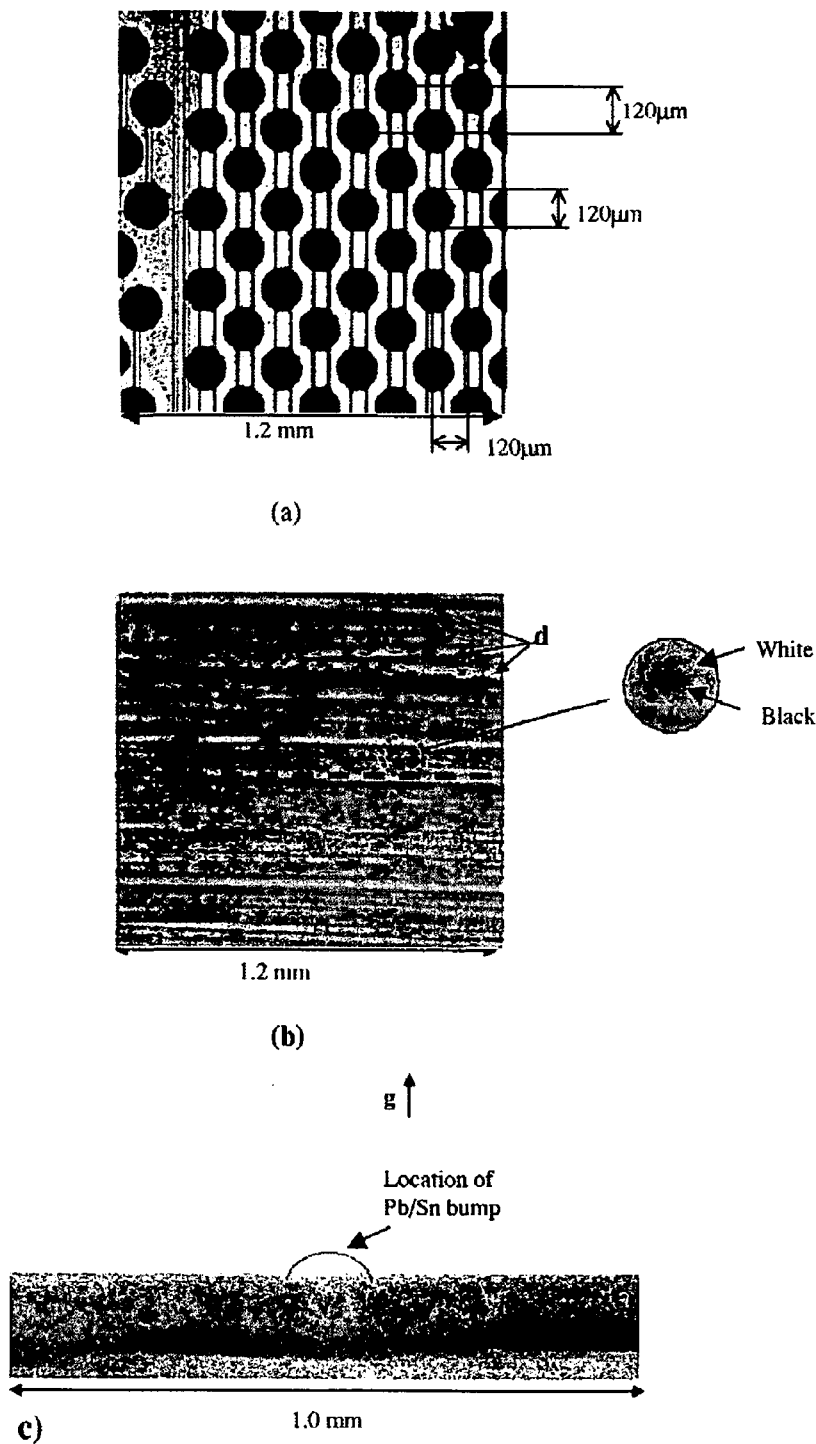


Fig. 3. (a) An optical micrograph of the area examined using X-ray topography, (b) 339 LA-BRT and (c) BRST of pre-reflowed sample.

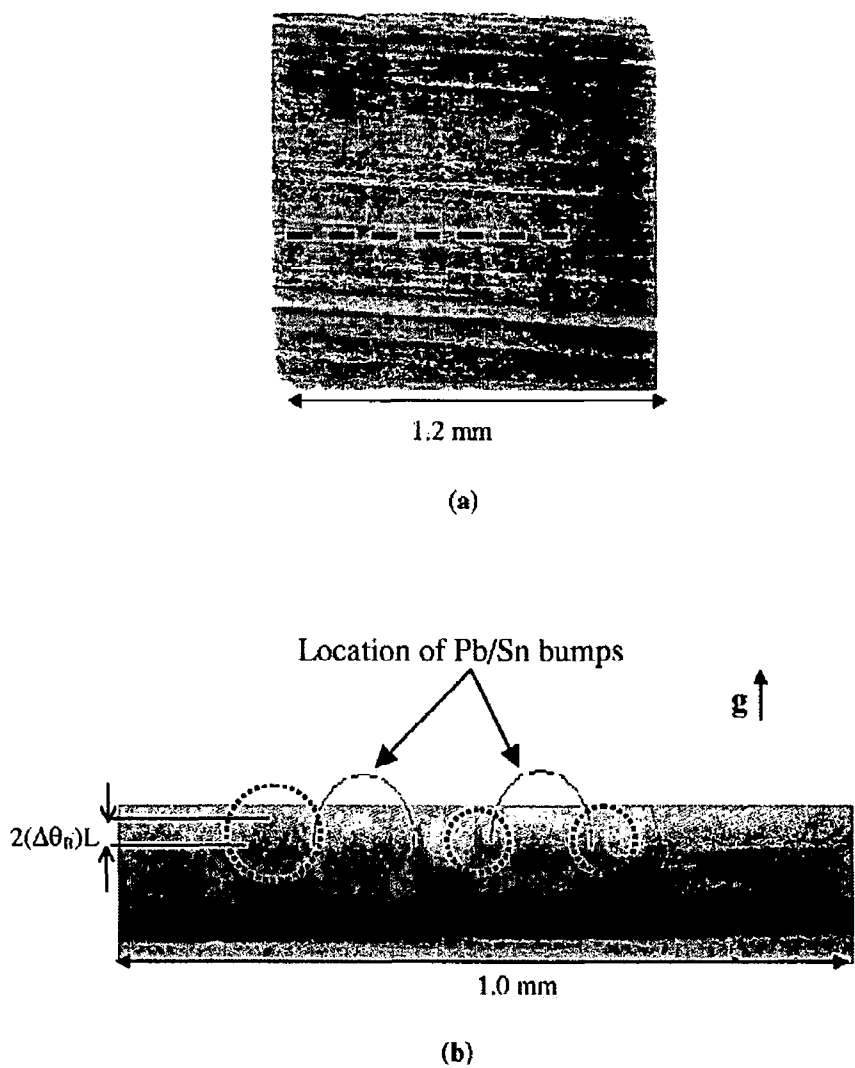


Fig. 4. 339 LA-BRT (a) and BRST (b) of the *post*-reflowed sample.

black and white contrast surrounding the Pb/Sn bumps. The black area represents an increase in recorded intensity. This phenomenon is called the extinction contrast effect [12], and is related to the change in curvature of the Si crystal lattice planes under the lead bump due to induced strain. The change in lattice plane curvature, especially near the peripheries of the lead bump, will lead to an enhancement or diminution of diffracted intensity in these regions as illustrated in the LA-BRT images.

Fig. 4 shows the LA-BRT and BRST, respectively, of the *post*-reflowed sample (the sample was heated to 350 °C as a reflow process simulation and cooled to room temperature before measurement). The black–white circular areas in Fig. 4a are larger than in Fig. 3b. Consequently, the change in lattice plane curvature near the peripheries of the lead bump is larger than in the *pre*-reflow case (Fig. 3b). Furthermore, the BRST image of Fig. 4b is dramatically different. It is noted that a lifting of the

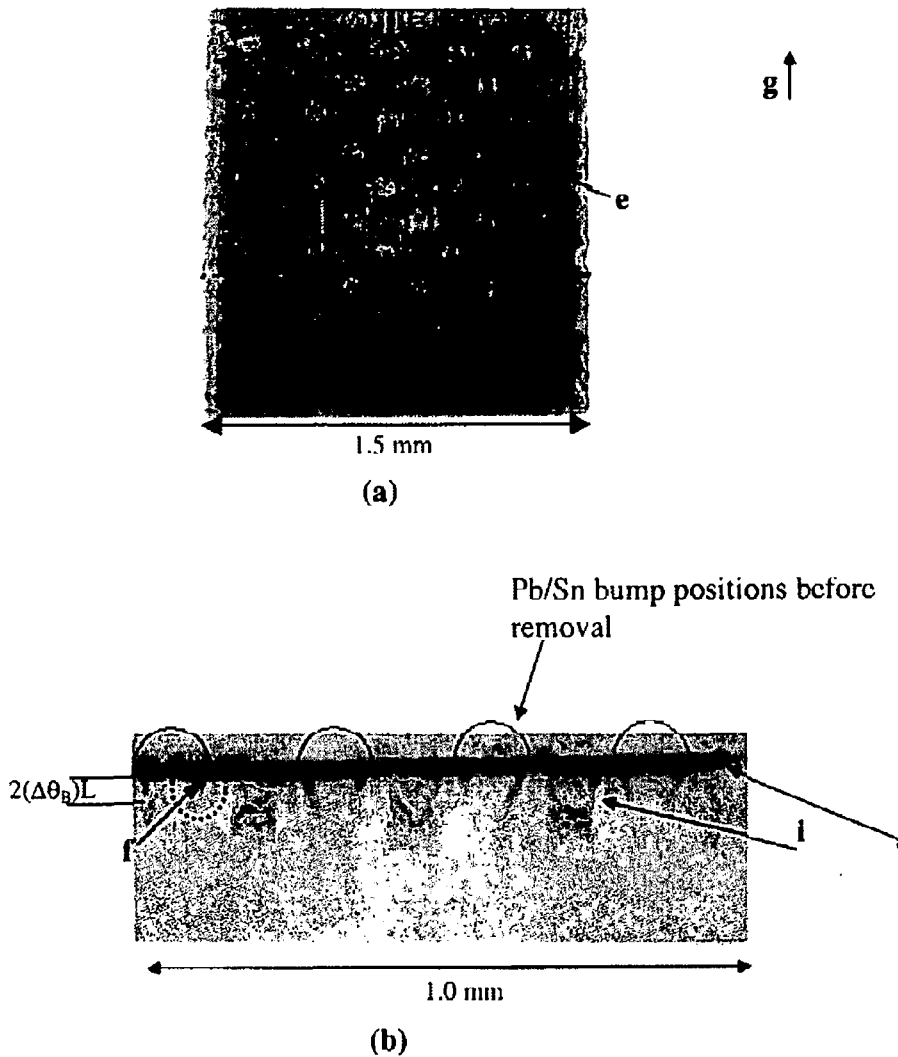


Fig. 5. $\overline{339}$ LA-BRT (a) and BRST (b) of *post-reflowed* sample after removing Pb/Sn bumps.

image of strained Si near the Pb/Sn edges above the image of the rest of the Si (dotted circles in Fig. 4b) occurred due to severe strain imaged via orientational contrast [8,28,29].

The orientational contrast can be observed if the misorientation exceeds the X-ray beam divergence ($\Delta\phi$), whose vertical full width at half-maximum (FWHM) is 6×10^{-4} rad at beamline F-1 in HASYLAB. The magnitude of the orientational contrast shift is $\Delta S = 2(\Delta\theta_B)L$, where $\Delta\theta_B$ is the maximum shift in Bragg angle of the severely strained regions and L is the distance between sample and film (in this case 50 mm). From Bragg's law, $2d \sin \theta_B = \lambda$, $\Delta\theta_B$ is the total change in Bragg angle (θ_B), which comprises lattice dilatation and the component of the rotation of the lattice planes around the normal to the plane of incidence, i.e. tilt (α) [30]:

$$\Delta\theta_B = \frac{\Delta d}{d} \tan \theta_B + \alpha \quad (1)$$

where d is the distance between the diffracting planes, and Δd is the deflection of the planes parallel to g . In the case of the white beam technique, the dilatation component of the change in Bragg angle $(\Delta d/d) \tan \theta_B$ cannot be obtained in this calculation since the white beam radiation provides a large number of wavelengths, which give a diffracting wavelength for any dilated planes. Therefore, the misorientation ($\Delta \theta_B$) is equal to the tilt component (α) only and is related directly to shear strain (γ_{xy}), i.e. tilt $\alpha \cong |\Delta H/\Delta V| \cong \gamma_{xy}$, where ΔH is the distance over which a lattice plane tilts along the surface direction, and ΔV is the vertical distance in the sample over which the planes are tilted. This gives a quantitative estimate for the magnitude of strain in the underlying silicon via the equation

$$\gamma_{xy} \cong \Delta \theta_B = \frac{\Delta S}{2L} \tag{2}$$

In this case Eq. (2) yields $\gamma_{xy} = 6.2 \times 10^{-4}$. The magnitudes of stresses are given by $|\sigma| = E|\gamma_{xy}|$, where E is the Young’s modulus of Si (isotropic), 162.3 GPa [31]. Thus, the upper limit on the stress magnitudes are of the order of $|\sigma_{xy}| \approx 100$ MPa.

After the Pb/Sn bumps were reflowed and etched (step 3), residual strains in the underlying Si still appear in the $\overline{339}$ back-reflection topographs of Fig. 5 (arrows e). It is known that during the high temperature reflow process, inter-metallic compounds are formed at the interface of the Pb/Sn bump and the BLM layer [32–34]. Considering the BRST image (Fig. 5b), the strains distributed in the underlying silicon appear to be much smaller when the Pb bumps were removed, as the orientational contrast related streaks pointing upwards are very short. However, the orientational contrast related images of the misorientated Si now point predominantly downwards into the Si substrate (arrow f), indicating that the lattice plane tilt has changed sign from the previous case of Fig. 4b. The maximum shear stress estimated from this orientational contrast is about 100 MPa, which is the same order as the stress value of the *post*-reflowed sample, but of opposite sign. In addition, other strains are still present and are visible in the image as indicated by arrow i (predominantly between bumps) and by arrow j (near the surface, e.g. epilayer strain, process layers and metallisation). These results confirm that the Pb/Sn bumps are the major source of the strain.

3.1. Finite element modeling

For finite element analysis, two-dimensional (2-D) plane strain finite element models of the multilayer structure have been employed in this study. The geometry, dimensions and boundary conditions of the *post*-reflowed sample are illustrated in Fig. 6.

Approximately 100,000 nodes were used to perform the simulation. The finite element analyses were carried out using Quickfield™ Professional version 4.2 [35]. Eight different materials were considered in these models: Si substrate, Al pad, polyimide passivation, silicon nitride passivation, Ti/Ni BLM, intermetallic layer and Pb/Sn solder bump. These materials are assumed to be isotropic and linearly elastic. A plane strain mode was assumed in this simulation. The stress–strain relation for the plane strain condition is

$$\sigma = E\varepsilon \tag{3}$$

$$E = \frac{E}{(1 + \nu)(1 - 2\nu)} \begin{bmatrix} (1 - \nu) & \nu & 0 \\ \nu & (1 - \nu) & 0 \\ 0 & 0 & (1 - 2\nu)/2 \end{bmatrix} \tag{4}$$

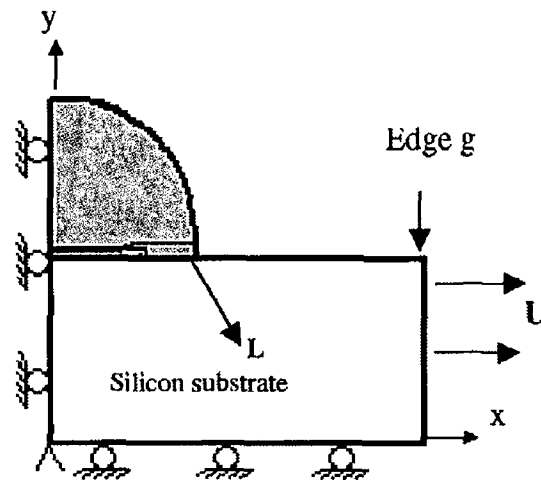


Fig. 6. Geometry and boundary conditions of *post-reflowed* sample model. L is the direction normal to the $\bar{3}39$ planes in Si.

where E is the elastic modulus, ν is Poisson's ratio, and \mathbf{E} is the elastic modulus tensor [36]. To simulate the thermal solder reflow process, a uniaxial load (U) of 100 MPa is applied to edge g in the model (see Fig. 6). Two types of FEM modeling were initially carried out: (a) examining the strains generated by differences in temperature between the Si substrate and the metallisation and (b) the simpler uniaxial load model of Fig. 6. Both models produce similar results. The simpler uniaxial load model is used, due to the complexity of interpreting subtle temperature-related effects on the multilayer metallisation between the Pb/Sn bump and the underlying substrate. While it may not be fully accurate, the uniaxial load model will capture the main features of the BGA-imposed strain fields, in particular locating regions of strain enhancement. The FEM simulation (Fig. 7) confirms the build-up of strain near the edges of the bumps, and the strain magnitudes are of the same order of magnitude as observed by SXRT.

In order to compare the BRST image of the *post-reflowed* sample (Fig. 4b) and the FEM results,

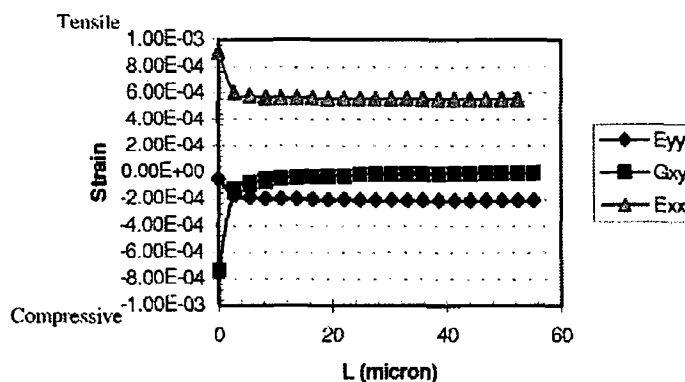


Fig. 7. Finite element simulation of tensile/compressive strain distribution in Si along the $\bar{3}39$ direction in the *post-reflowed* sample. $L = 0$ indicates the position of the periphery of the Pb/Sn bump, E_{xx} and E_{yy} are normal strains in the x - and y -directions, respectively, and G_{xy} is the shear strain. The direction of L is indicated in Fig. 6.

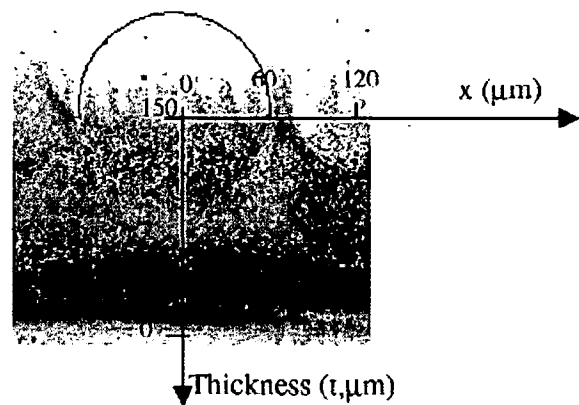


Fig. 8. An overlay of the dimensions used in the FEM simulation upon the $\overline{339}$ BRST image of the left-hand side Pb/Sn bump of Fig. 4b.

the geometries and dimensions used in the simulation are overlaid on the corresponding BRST image, as shown in Fig. 8.

The displacement vectors (\mathbf{H}_i) of the $\overline{339}$ lattice planes, calculated at each point i within the FEM discretisation within a selected region of the simulated Si, are plotted along the cross-section of the post-reflowed sample as illustrated in Fig. 9 [13]. In this work, the vector \mathbf{H}_i is normal to the lattice displacement and deviates from the lattice direction due to an imposed strain field.

This FEM simulation demonstrates that the Pb/Sn bump is under tension and that it induces compressive stress in the Si directly underneath the central regions of the solder bump and tensile stress near the edge of the bump due to the reflow process. This result is in good agreement with Chen et al. [37].

A merged image of the back-reflection topograph and the shear strain simulation shows that the strain fields build up significantly at the periphery of the bump and cause a severe distortion of lattice planes around this edge. Since the values of $\Delta\theta_b$ corresponding to these enhanced values of shear strain, γ_{xy} , easily exceed the FWHM beam divergence, the orientational contrast is visible at the edge of the bump in the BRST image as illustrated in Fig. 10. It is noted that the values in Fig. 10 refer to the shear strain (γ_{xy}) contours.

4. Conclusions

White beam synchrotron X-ray topography confirms that the solder reflow process is a major source of strain in Si IC processing. This strain is particularly large near the peripheries of the Pb/Sn bumps after the reflow process. A comparison of SXRT topographs and FEM models is in good agreement in terms of the major strain distributions within the Si substrate. In addition, the calculation of lattice displacement using FEM found that the Pb/Sn is in tensile stress after the reflow process and places the Si underneath the bump in compressive stress. The stress changes to tensile stress near the edge of the bump. This is in broad agreement with the orientational contrast observed in the corresponding X-ray topographs.

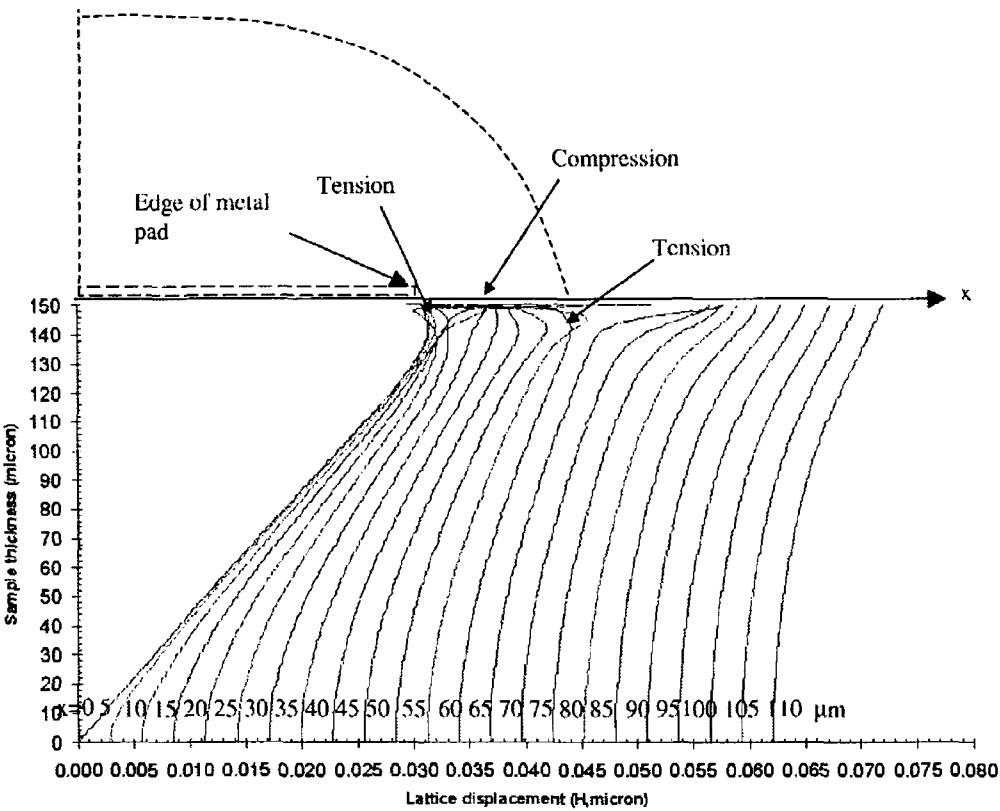


Fig. 9. The lattice displacement of the 339 lattice planes calculated for a selected region of the simulated Si under the periphery of the Pb/Sn bump.

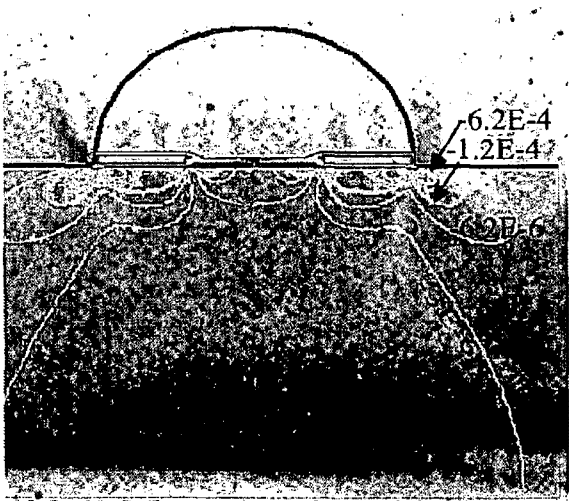


Fig. 10. The BRST of the post-reflowed sample (Fig. 3b) and shear strain contours calculated using the FEM simulation.

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A-3

Examination of mechanical stresses in silicon substrates due to lead–tin
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modeling

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Examination of mechanical stresses in silicon substrates due to lead–tin solder bumps via micro-Raman spectroscopy and finite element modelling

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Abstract

Due to the fact that semiconductor devices have decreased significantly in geometry and increased enormously in electronic design complication, flip-chip packaging technology was launched to increase input/output count, improve electrical performance, reduce packaging size and be cost effective. The Intel®Pentium®III microprocessor uses the popular ball grid array (BGA) packaging technique. BGA is one of the most common flip-chip packaging techniques used for microprocessor applications. However, mechanical stresses induced by the flip-chip process are major concerns for the reliability of such devices.

Micro-Raman spectroscopy (μ RS) is a powerful technique for investigating the spatial extent of strain fields in microelectronic devices. In this study, the strain fields imposed on the underlying silicon substrate due to the lead–tin solder bump process in BGA packaging have been investigated in *pre*- and *post*-reflowed samples using μ RS and finite element modelling (FEM). For *pre*-reflowed samples, an approximate uniaxial compressive stress of 200 MPa is developed near the edge of the under bump metallization (UBM). However, a tensile stress up to \sim 300 MPa is found for *post*-reflowed samples.

Two-dimensional (2D) plane strain FEM has also been performed. The magnitudes and spatial distribution of the stresses after the reflow process are in good agreement with the micro-Raman results.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

As microelectronics device features become smaller with an increase in functionality and higher levels of performance, the intricacy of semiconductor packaging technology grows proportionally. The idea of attaching the semiconductor

die directly to the substrate (printed circuit board, PCB) by introducing flip-chip technology, which simply turns the chip upside down so that its termination can be connected directly to the pads on the substrate [1], has been in existence for some time. With this technique the IC package is omitted, saving cost, space and weight. The developments of flip-chip

and beam leaded die were advanced by IBM [2] and AT&T over the past 30 years. Since then, the technology has evolved [3] to encompass a wide variety of materials and techniques for bumping, bonding and underfilling. Flip-chip technology can be classified into ball grid array (BGA), pin grid array (PGA), chip scale packaging (CSP), etc, which are examples of common packages used in advanced microprocessors [4]. Worldwide-consolidated efforts between academia and industry are aimed at overcoming the difficulties associated with chip-on-board (COB) technology. The issue of mechanical failure due to the mismatch of the coefficient of thermal expansion (CTE) between silicon die, barrier layer metallization (BLM) and the PCB, and thermal stresses during the deposition and reflow process has a particular impact on the reliability of the production.

The Intel® Pentium® III microprocessor uses the popular ball grid array (BGA) packaging technique. A C4 (controlled collapse chip connection) technique has been employed for the solder bumping process [5, 6]. Ti/Ni based films were used as BLM and a lead-tin solder bump with high lead content was formed using the C4 electroplating technique [7, 8]. Due to the high Pb content in the solder, the solder reflow process needs to be carried out at a high temperature (up to 350 °C) and in a nitrogen rich atmosphere [9].

The aims of this work are to evaluate the residual stress distributions in the Si substrate due to the solder bump reflow processing of these ICs using micro-Raman spectroscopy (μ RS) and to predict and compare this observed stress with finite element modelling (FEM).

In order to measure the packaging process induced strain fields in Si devices several methods can be used, e.g., transmission electron microscopy (TEM), laser scanning substrate curvature measurements, x-ray diffraction (XRD), x-ray topography (XRT), microtensile testing, μ RS, etc. Each technique has its own advantages and disadvantages. For instance, TEM is a very powerful tool which can provide stress/strain information with high resolution in the nanometre range. However, the analysis of TEM requires sophistication and expertise and is time consuming. In addition, the sample under test must be cleaved and properly prepared. XRT provides information in terms of visualized stress/strain distributions in a crystal material with a simple experimental set-up [10]. The spatial strain distribution can be calculated via orientational contrast; however the sign of the strain field cannot be readily examined [11]. On the other hand, μ RS provides information on the magnitudes and signs of stress/strain distributions via the observation of Raman peak shifting [12]. It is a non-destructive technique and requires no sample preparation.

μ RS has been developed rapidly for the evaluation of stress/strain distributions in microelectronic devices. De Wolf and her group have published many papers on the theory and applications of μ RS to microelectronic device structures [12, 14–16]. One such application is IC packaging and the spatial stresses in Si after IC packaging were investigated using μ RS by Chen *et al* [15]. A tensile stress in the Si with a magnitude of about 170 MPa was found near the edge of one type of Pb/Sn bump.

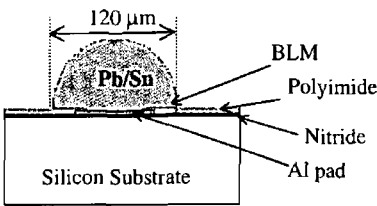


Figure 1. Geometry of the Pb/Sn solder bump sample.

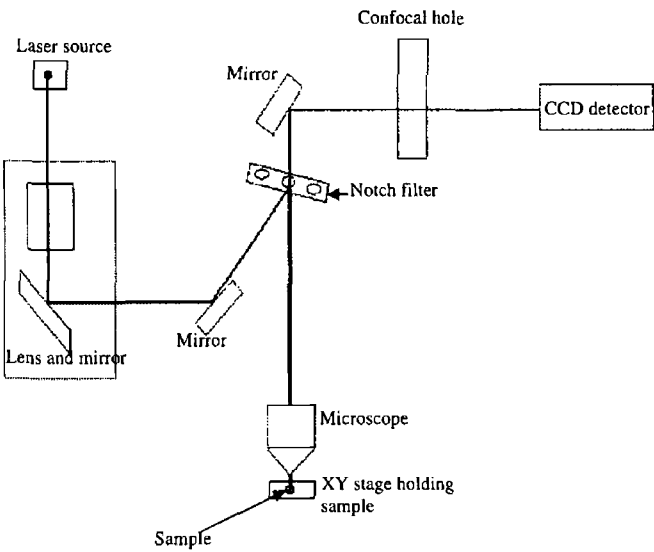


Figure 2. The μ RS system set-up.

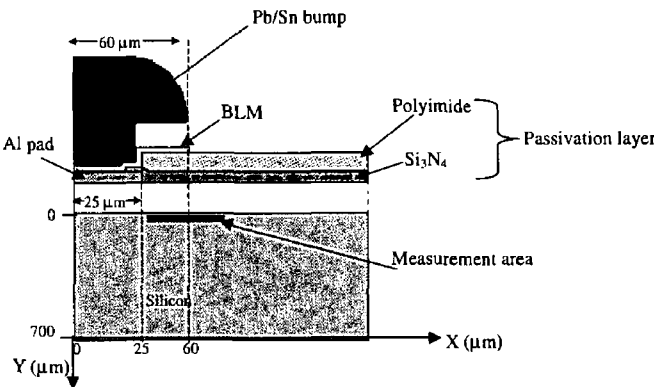


Figure 3. Geometry and dimensions of the *pre-reflowed* process sample. The solid area represents the measurement area via X–Y mapping.

2. Experimental details

The Pb/Sn solder bump samples were produced at Intel Ireland Fab Operations, by using C4 short loops of a standard 0.25 μ m CMOS technology. This technology has been described in detail elsewhere [9]. The samples consist mainly of silicon substrate (200 mm diameter and \sim 700 μ m thickness subsequently thinned down)/silicon epilayer/aluminium (Al) metal 5 interconnects and pad/silicon nitride passivation/polyimide passivation/BLM (Ti/Ni)/Pb–Sn solder bump. The geometry is illustrated in figure 1.

In this study, the samples were investigated in the following order: (1) *pre-reflowed* process samples and (2) *post-reflowed* process sample using a reflow process simulation at 350 °C in atmosphere.

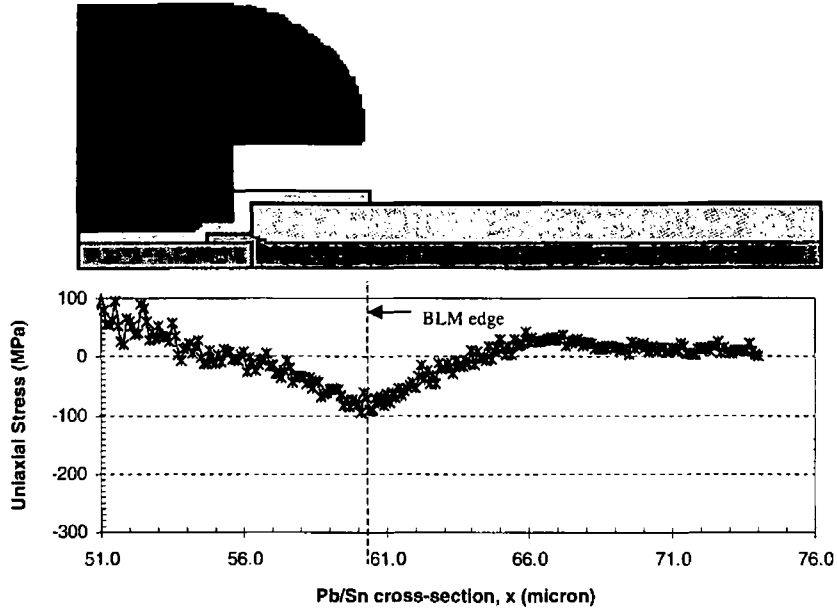


Figure 4. The calculated uniaxial stress of the *pre*-reflowed process sample along the *X* direction. The dotted line at 60 μm indicates the edge of BLM layer. The negative sign refers to compressive stress.

A Jobin–Yvon LabRam HR μRS system using a 488 nm Ar^+ laser was used in this study. The system set-up is shown in figure 2. The incident beam is focused through a $100\times$ objective microscope on to the sample. An automatic *X–Y* stage with a minimum movement of $0.1 \mu\text{m}$ was used to move the sample during the measurements. The scattered light from the sample was collected in back-scattering mode through the same microscope and passed directly through a notch filter. At this point, the Rayleigh scattering was reflected out and only the Raman beam passed through the notch filter and, subsequently, straight through a confocal hole. This scattered beam is carried towards a CCD detector-based spectrometer. The Raman shift is then obtained.

A plasma line at 560 cm^{-1} was used as an internal calibration of the measurements to eliminate environmental and CCD temperature fluctuations during the experiments. A resolution of $\pm 0.05 \text{ cm}^{-1}$ is possible for strain-free Si samples using this method. This calibration method is described elsewhere by De Wolf [16].

To examine the stresses/strains imposed in the Si substrate due to the reflow process, the samples were cleaved near the middle of the Pb/Sn bumps and investigated in cross-sectional configuration. The geometry and dimensions of each sample are illustrated in figures 3 and 6.

The spatial strain distribution in the Si sample can be examined from the measured frequencies of Raman peaks compared with those of a strain-free reference Si sample at 521 cm^{-1} . The relationship between Raman shift and linear strain was derived by Chen and De Wolf [17] for the TO peak along (110) and is given by

$$\sigma_{xx} \text{ (MPa)} = -434\Delta\omega \text{ (cm}^{-1}\text{)} \quad (1)$$

where σ_{xx} = the uniaxial stress in MPa and $\Delta\omega$ = the Raman shift between the measured Raman peak of strained Si (ω_j) compared with that of strain-free Si (ω_0); $\Delta\omega = \omega_j - \omega_0$, ω_j = the measured frequency of the silicon Raman peak and ω_0 = the frequency of the silicon Raman at stress free state. Equation (1) is consistent with the geometries in this paper in

the case of uniaxial stress assumption when the micro-Raman measurement is performed along (110).

3. Results and discussions

It has been well known that the cleavage of a sample can alter the stress measured by μRS [18] in addition to the heating effect from the laser source [13]. For the cleavage effect, Yogishita *et al* [18] compared stress distributions in Si wafers due to shallow trench isolation (STI) before and after Si wafer cross-sectional cleavage using three-dimensional (3D) FEM and μRS . It was discovered that the uniaxial stress in the cross-section direction (σ_{zz}) tends to be about 150 MPa in tension due to a bending of the newly exposed surface after cleavage. However, this had little or no effect on σ_{xx} which is considered in this study. For the heating effect, the measurement with the lowest laser power and minimum measurement time can be used to minimize the impact of the latter issue. Thus, the stresses generated during the reflow process can be measured reasonably accurately and conclusions as to the tendencies for stress generation can still be safely reached.

The micro-Raman analysis was performed at each step in the sample processing in order to examine the reflow process induced stresses in the underlying Si. One half of the sample cross-section geometry of the *pre*-reflowed process sample is depicted in figure 3.

For the *pre*-reflowed process sample, the Pb/Sn bump takes on a mushroom shape. The Pb/Sn bump contacts the BLM layer after the reflow process (*post*-reflowed process sample) and this area is signified as the edge of the Pb/Sn bump in this study. The micro-Raman data was collected near the interface of the Si and passivation/metal layers. The uniaxial stresses (MPa) calculated using equation (1) of the *pre*-reflowed process sample in *X*-mapping mode is indicated in figure 4. It is noted that *Y* is the distance from the interface between the Si and metal/passivation layers down to the backside of the wafer.

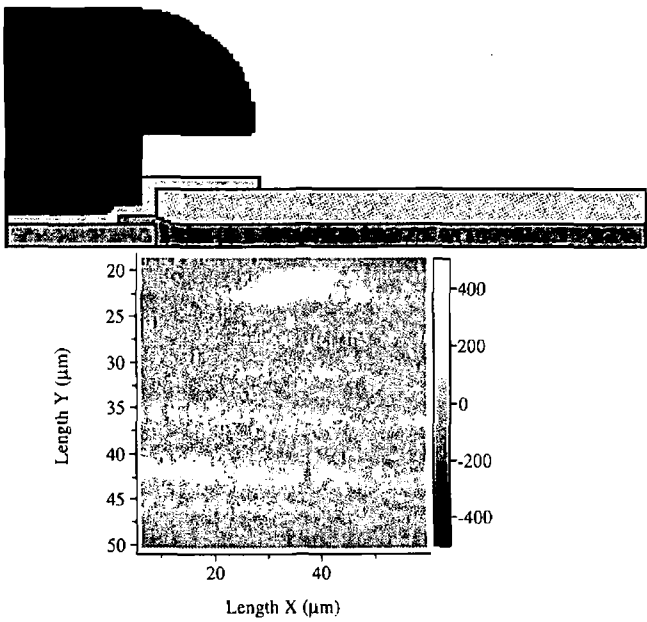


Figure 5. The 2D uniaxial stress of the *pre*-reflowed process sample. Note that the negative sign and positive sign refer to compressive and tensile stresses, respectively.

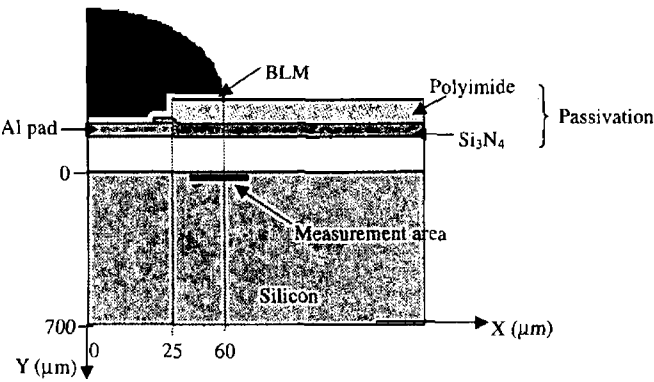


Figure 6. The geometry and approximate dimensions of the *post*-reflowed process sample. The positions $X = 25\ \mu\text{m}$ and $60\ \mu\text{m}$ are the edges of the metal pad and of the Pb/Sn bump, respectively. The position $Y = 0\ \mu\text{m}$ is the interface between the Si and the metal/passivation layers.

From the X mapping, one can observe that the stress is compressive underneath the Pb/Sn bump near the BLM edge with a maximum magnitude of about 100 MPa. In addition, the X - Y mapping in figure 5 illustrates that this is reasonably uniform throughout the remainder of the sampled Si when compared to the *post*-reflow case, which will now be outlined.

The sample was then heated to $350\ ^\circ\text{C}$ and subsequently cooled down to room temperature, and this is defined as the *post*-reflowed process sample. The sample was cleaved near the middle of the Pb/Sn bumps as for the *post*-reflowed sample. The geometry and experimental dimensions are depicted in figure 6. The X and X - Y Raman mapping data of the *post*-reflowed process sample are illustrated in figures 7 and 8, respectively.

Figure 7 shows that the Si at the interface with the metal/passivation layers near the edge of the Pb/Sn bump is in tensile stress and reaches a maximum magnitude of about 250 MPa at that interface as indicated by arrow b. Figure 8 indicates that the stress in the Si wafer (below the interface) is

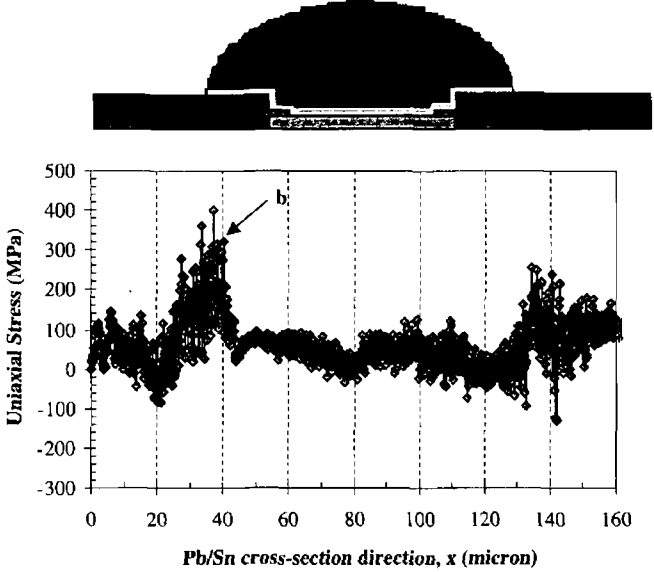


Figure 7. The calculated uniaxial stress of the *post*-reflowed process sample along the Pb/Sn bump cross section (X direction).

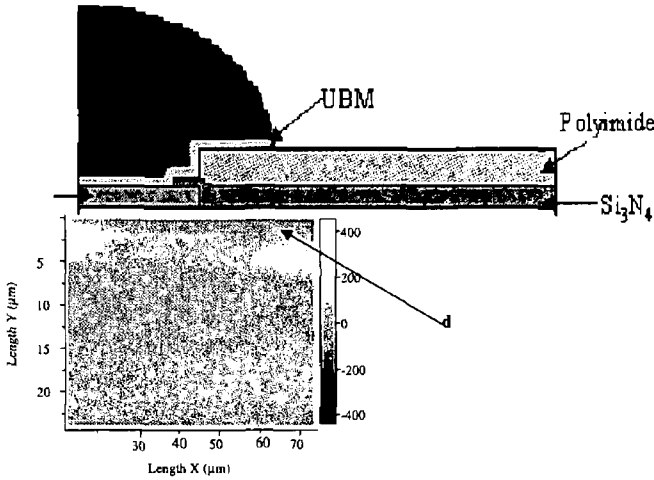


Figure 8. The X - Y Raman mapping (2D) of uniaxial stress of the *post*-reflowed process sample.

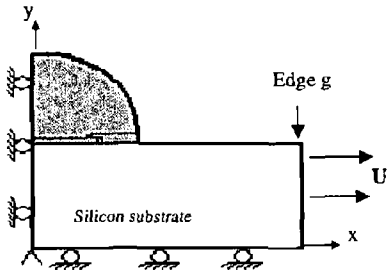


Figure 9. Geometry and boundary conditions of *post*-reflowed sample FEM model.

more non-uniform after the reflow process. While it is difficult to observe in this figure, the stress near the Pb/Sn bump edge *does* become tensile as seen in figure 7, and this is indicated by the region labelled 'd' in figure 8. A comparison of the stress distributions in the Si wafer between *pre*- and *post*-reflowed samples (figures 4 and 7) indicates that the stress in the Si wafer near the edge of the Pb/Sn bump changes from ~ 200 MPa compressive to a tensile uniaxial stress of maximum value ~ 250 MPa. Since the Pb/Sn solder attached

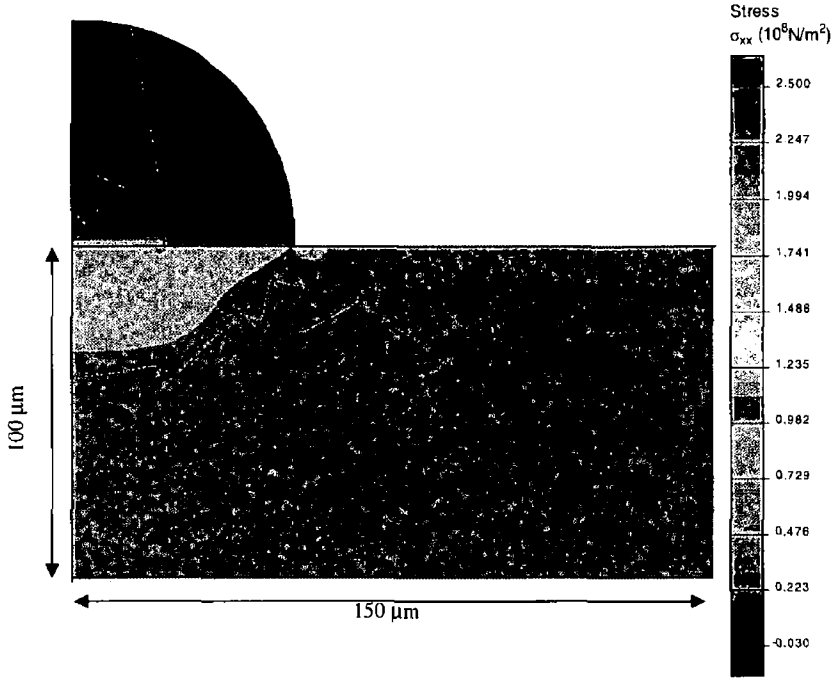


Figure 10. Finite element simulation of strain distribution in Si due to the reflow process of the Pb–Sn solder bump. Negative sign is compressive strain, positive sign is tensile.

to the UBM/passivation layers becomes ball shaped after the reflow process, the thermal stress due to the CTE mismatch of the Pb/Sn solder, UBM and passivation layers can generate greater stress through the Si wafer near the edge of the Pb/Sn bump due to the fact that more of the bump interface area is now in direct contact with the UBM and passivation layers.

4. Finite element modelling (FEM)

For the finite element analysis, two-dimensional (2D) plane strain finite element models of the multilayer structure have been employed in this study. The geometry, dimensions and boundary conditions of the *post*-reflowed sample are illustrated in figure 9.

Approximately 100 000 nodes were used to perform the simulation. The FEM was carried out using Quickfield™ Professional version 4.2 [19]. Eight different materials were considered in these models: Si substrate, Al pad, polyimide passivation, silicon nitride passivation, Ti/Ni BLM, intermetallic layer and Pb/Sn solder bump. These materials are assumed to be isotropic and linearly elastic. A plane strain mode was assumed in this simulation [20]. The stress–strain relation for the plane strain condition is

$$\sigma = E\varepsilon \quad (3)$$

$$\mathbf{E} = \frac{E}{(1+\nu)(1-2\nu)} \begin{bmatrix} (1-\nu) & \nu & 0 \\ \nu & (1-\nu) & 0 \\ 0 & 0 & (1-2\nu)/2 \end{bmatrix} \quad (4)$$

where E is the elastic modulus, ν is Poisson's ratio, and \mathbf{E} is the elastic modulus tensor [20]. To simulate the thermal solder reflow process, a uniaxial load (U) of 100 MPa is applied to edge g in the model (see figure 9). Two types of FEM

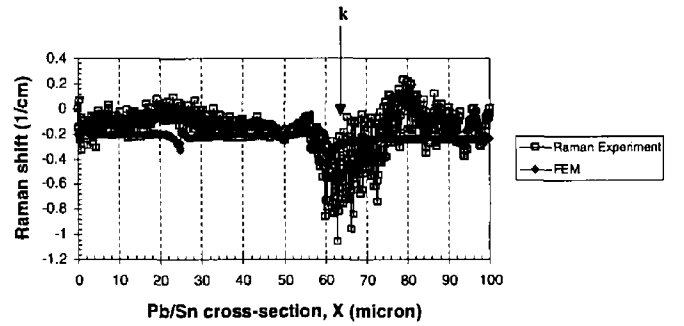


Figure 11. Comparison of the Raman shift (cm^{-1}) between the micro-Raman experimental data and FEM data.

were initially carried out: (a) examining the strains generated by differences in temperature between the Si substrate and the metallization; and (b) the simpler uniaxial load model of figure 9. Both models produce similar results. The simpler uniaxial load model is used due to the complexity of interpreting subtle temperature-related effects on the multilayer metallization between the Pb/Sn bump and the underlying substrate. While it may be not fully accurate, the uniaxial load model will capture the main features of the BGA-imposed strain fields, in particular, locating regions of strain enhancement. The σ_{xx} of the FEM simulation is shown in figure 10. The tensile stress builds up at the edge of Pb/Sn bump due to the reflow process with a maximum magnitude of 200 MPa. This result correlates to the μRS result in figure 7. It confirms the build-up of strain near the edges of the bumps and the strain magnitudes are of the same order of magnitude as observed by synchrotron x-ray topography (SXRT) in our previous experiments described elsewhere [11]. The FEM data at the Si/metal interface was calculated back to Raman shift using equation (1) and plotted along the X direction as illustrated in figure 11. The μRS results and the FEM simulation illustrate that the tensile stress distributions

in the Si wafer due to the reflow are of the same order ($\sim 200\text{--}250\text{ MPa}$, i.e., Raman shift $\Delta\omega \approx -0.6$) near the edge of Pb/Sn bump near arrow k. There is an excellent correlation in the shape and distribution of the strain induced Raman shifts near the edge of the metal bump. To date the feature observed at $X \approx 25\text{ }\mu\text{m}$ has not been accounted for, but is most likely related to the Al pad/ Si_3N_4 interface.

5. Conclusions

Using micro-Raman strain spectroscopy we have found that the strain fields due to the reflow process for Pb/Sn BGA on Si technology changes from compressive to tensile after the reflow process at $350\text{ }^\circ\text{C}$. This could be due to a number of possibilities: (a) the Pb/Sn bump imposes stress on the Si wafer during the reflow process because a ball shaped Pb/Sn bump is formed after the reflow process and the Pb/Sn is attached to the UBM layer across a greater area; and (b) other new materials are generated at the Si interface, i.e., intermetallic materials between UBM and Pb/Sn. A uniaxial stress of about 250 MPa was found at the edge of the high lead content Pb/Sn bump after the reflow process. This result is in good agreement with FEM analysis.

Acknowledgments

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A-4

White Beam Synchrotron X-Ray Topography Studies of Pb/Sn Ball Grid
Array Induced Strain in Si Substrate

Hamburger Synchrotronstrahlungslabor HASYLAB am Deutschen
Elektronen-Synchrotron DESY, User Meeting, 2000

White Beam Synchrotron X-Ray Topography Studies of Pb/Sn Ball Grid Array Induced Strain in Si Substrate

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Solder based flip chip packaging has been rapidly developed and is used in many integrated circuit (IC) applications. The ball grid array (BGA) is one of the most commonly used solder based packaging techniques due to improved electrical performance, input/output (I/O) density, cost, packaging size, etc. In order to improve the limitations of this packaging technique, several properties have been examined before and after the packaging processes. The mechanical stress induced by the solder bump process is one of the major concerns for the reliability of IC production.

White beam back-reflection topography in both large area (BRT) and section (BRST) modes has been employed to investigate the strain field distribution in the underlying silicon beneath lead-tin bumps. This is primarily due to the elevated temperature fabrication steps in the lead-tin solder bump process. The spatial stress distribution beneath the lead bumps was observed in the sample before and after a simulation of the solder bump reflow process at 350°C in atmosphere.

The topography images were recorded on Geola VRP-M films having an emulsion grain size of about $0.05\ \mu\text{m}$. The distance from the sample to the film was set at 50 mm for all samples. The beam size was approximately $1.5\ \text{mm} \times 1.5\ \text{mm}$. The topographs appearing in this report have been generated on a system comprising of a CCD camera, frame grabber and appropriate software.

Due to the high absorption of lead alloys and the approximately $700\ \mu\text{m}$ thickness of the silicon substrate, the samples were thinned down to $150\ \mu\text{m}$. The strain fields in the Si material beneath the Pb/Sn bumps were imaged by allowing the x-rays to enter the sample via the backside (i.e. non-metallized surface). Figures 1 and 2 are large area and section $9\ \bar{3}\ \bar{3}$ topographs, respectively, of the lead bump sample before the reflow process, with a penetration depth (t_p) of $125\ \mu\text{m}$.

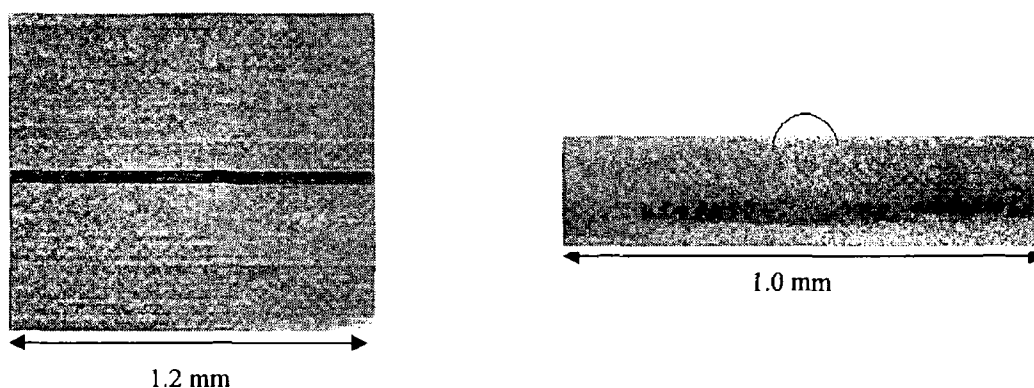


Figure 1 and 2: $9\ \bar{3}\ \bar{3}$ large area and section back reflection x-ray topographs of strain field in silicon substrate beneath lead bump alloys before reflow process.

In Figure 1, the strains imposed on the underlying silicon due to a single lead bump have been observed as a black and white contrast. This phenomenon is called the extinction contrast effect[1] and is related to the change in curvature of the crystal lattice planes under the lead bump due to induced strain. It is worth noting that the change in the lattice plane curvature will lead to an increase (black) or reduction (white) in recorded intensity. The BRST image also gave a clear black/white contrast in the underlying silicon beneath the lead bump.

The samples were reflowed at 350°C in atmosphere and the $9\bar{3}\bar{3}$ BRT and BRST images for these when cool to room temperature are shown in Figure 3 and 4.

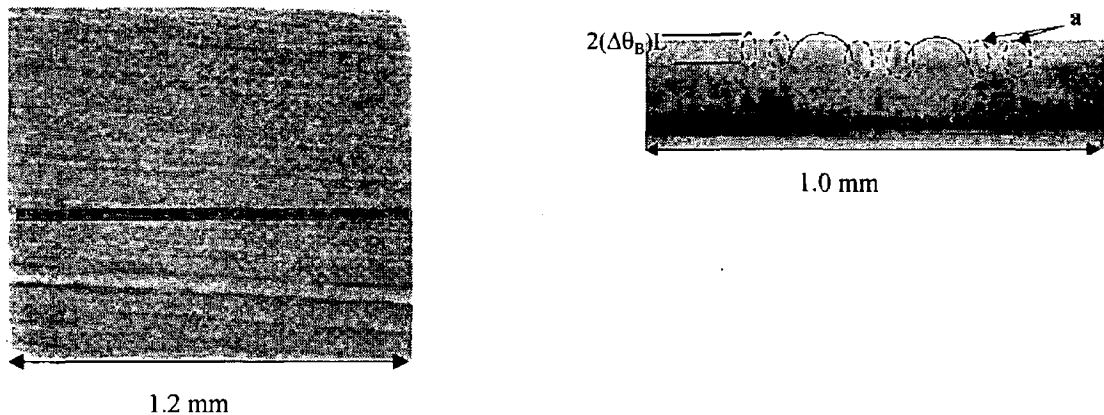


Figure 3 and 4: $9\bar{3}\bar{3}$ large area and section back reflection topographs of strain field in silicon substrate beneath lead bump alloys after simulation of reflow process.

Figure 3 (BRT image) showed an increase in the intensity and spatial distribution of black/white contrast due to changes in the strain field in the underlying silicon beneath the lead bumps. In addition, orientational contrast (Arrow a) has been obtained in the BRST image (Figure 4). The lifting of the images of strained Si near the edges of the lead bump is due to the severe distortion of the silicon lattice planes at the elevated temperatures of the reflow process. The estimated magnitude of stresses was calculated from the orientational contrast as in the following equation[2]:

$$\Delta\theta_B = \frac{\Delta d}{d} \tan \theta_B + \alpha = \varepsilon_{\perp} \tan \theta_B + \alpha$$

where θ_B = the Bragg angle,
 α = the component of the rotation of the lattice planes around the normal
to the plane of incidence, i.e. tilt,
 ε_{\perp} = the component of strain perpendicular to the diffraction planes,
 d = the distance between the diffraction planes,

Δd = the deflection of the planes parallel to the diffraction
vector \bar{g}

From the image, estimated limits on the stress magnitudes are $|\sigma_{\perp}| \approx 43\text{-}97$ MPa.

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A-5

White Beam Synchrotron X-Ray Topography Studies of Copper
interconnect in IC processing Induced Strain in Si Substrate

Hamburger Synchrotronstrahlungslabor HASYLAB am Deutschen
Elektronen-Synchrotron DESY, User Meeting, 2001

White Beam Synchrotron X-Ray Topography Studies of Copper Interconnect in IC processing Induced Strain in Si Substrate

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Copper (Cu) has been replaced rapidly with Aluminum alloy (Al/Cu) in Integrated Circuit (IC) industry due to an advantage of high conductivity, high melting point and etc, as a result of high speed limit of the device, low electromigration failure. Therefore, the mechanical reliability such as thermal strain is a major concern. Several techniques are utilised to deposit Cu on the device such as electroless plating, Chemical Vapour Deposition (CVD) and Sputtering metallisations. In this work, the electroless technique was used for Cu metallisation.

White beam back-reflection topography in both large area (BRT) and section (BRST) modes were employed to investigate the strain field distribution in the underlying silicon due to electroless Cu metallisation. The details of this technique are explained in Ref 1. The sample is comprised of Bare <100> Si/ 100 nm Ti (Barrier layer)/ 20 nm Cu seed layer/ 500 nm Cu metallisation.

The topography images were recorded on Geola VRP-M films having an emulsion grain size of about 0.04 μm . The distance from the sample to the film was set at 50

mm for all samples. The beam size was approximately 1.5 mm x 1.5 mm. The topographs appearing in this report have been generated on a system comprising of a CCD camera, frame grabber and appropriate software.

All topographs of the samples were generated by the $\bar{2} \bar{2} 8$ harmonic reflection with a penetration depth (t_p) of 65.7 μm . Each set of metallisation lines consists of 6, 8, 10, 20, 40, 60 and 100 μm wide structures. Only lines, which are 40 and 100 μm wide, are considered in these discussions. The results of LA-BRT and BRST are illustrated in Figure 1(a) and (b).

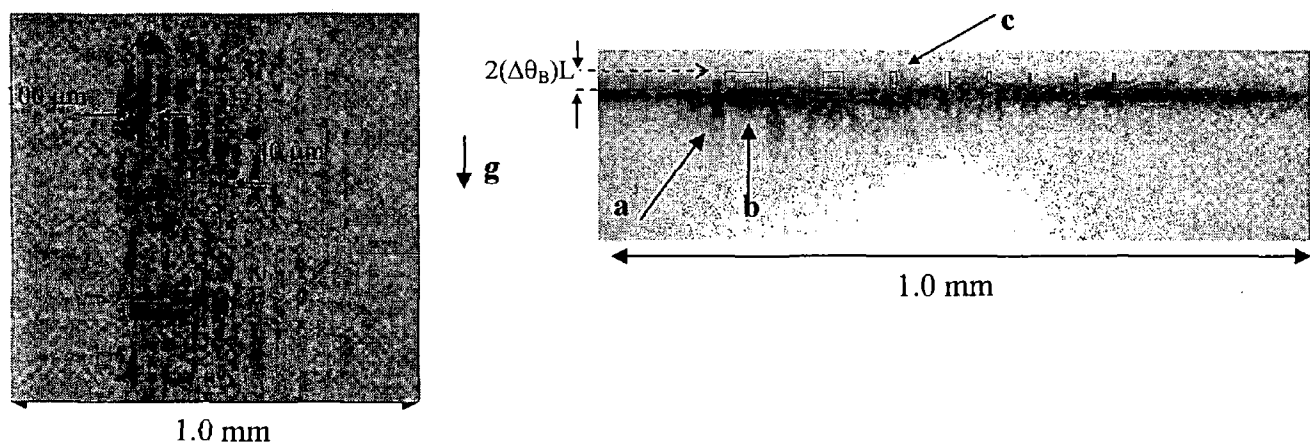


Figure 1: the LA-BRT (a) and BRST (b) of the electroless Cu sample.

These dark lines are created by stresses imposed in the Si substrate due to the metal layers and are observed as a black and white contrast. The stresses are particularly large at the metallisation edges. The phenomenon is called the extinction contrast effect [2-3]. This phenomenon is related to the distortion of the Si lattice planes induced by either tensile or compressive stress at the interface between the metal and Si. The distortion of the lattice planes leads to an enhancement or diminution of diffracted intensity in these regions as illustrated in the LA-BRT images. The black and white contrast is illustrated in Figure 1(a) along the discontinuity generated at the edge of the metal lines. An estimation of the stress/strain imposed in Si for electroless Cu is based on the calculation of thermal stress due to a large difference

in CTE (Coefficient of Thermal Expansion) because the temperature of the deposition solution was only 80°C during Cu metallisation. The calculation of the maximum value of stress for a uniform film when the behaviour is purely elastic is

$$\sigma_{\max} = \Delta\alpha \cdot E \cdot \Delta T / (1 - \nu) \quad (1)$$

when σ_{\max} = the maximum thermal stress, $\Delta\alpha$ = the difference of CTE between Si and Cu ≈ 13.6 ppm/°C, E = Young's modulus ≈ 162.3 GPa and ν = Poisson's ratio = 0.28 [4-5]. From eq. (1), the estimation of maximum stress is of the order of 100 MPa.

The cross-section image is shown in Figure 1(b). The strain fields are observed clearly in this cross-section image as a black contrast from both edge and underneath of the metal lines as indicated Arrows a and b, respectively. In addition, the severely strained Si near the edge of Cu lines is also illustrated as an orientational contrast (Arrow c). The orientational contrast is observed as a lifting of the image of highly strained Si near the line edges above the image of the rest of the Si (Arrow e). The orientational contrast can be observed if this misorientation exceeds the x-ray beam divergence ($\Delta\phi$), which is equal to 6×10^{-4} rad for beamline F-1 in HASYLAB. The magnitude of the orientational contrast shift is $\Delta S = 2(\Delta\theta_B)L$; where $\Delta\theta_B$ is the maximum shift in Bragg angle of the severely strained regions and L is the distance between sample and film (in this case = 50 mm). This gives a quantitative estimate for the magnitude of strain in the underlying silicon via the equation:

$$\varepsilon \cong \Delta\theta_B = \frac{\Delta S}{2L} \quad (2)$$

In the case of the 100 μm wide Cu line, $\Delta S \approx 0.05$ mm, therefore, $\varepsilon = 5 \times 10^{-4}$. The magnitudes of stresses are given by $|\sigma| = E |\varepsilon|$ where E , the Young's modulus of Si (isotropic) = 162.3 GPa [6]. Thus, the limit on the stress magnitudes is of the order of $|\sigma| \approx 81$ MPa. In case of the 40 μm wide Cu line, $\Delta S = 0.08$ mm, then, $\varepsilon = 8 \times 10^{-4}$. Therefore, $|\sigma| \approx 130$ MPa.

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A-6

Mapping of Mechanical Stresses in Silicon Substrates due to Lead-Tin
Solder Bump Reflow Process via Synchrotron X-Ray Topography
and Finite Element Modeling

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Mapping of mechanical stresses in silicon substrates due to lead–tin solder bump reflow process via synchrotron x-ray topography and finite element modelling

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Abstract

White beam synchrotron x-ray topography (WBSXRT) is a non-destructive technique, which is capable of analysing the strain and/or dislocation distribution in single crystal materials. This paper discusses the application of WBSXRT to the analysis of strain fields due to the microelectronic packaging of integrated circuits. A ball grid array package containing an Intel® Pentium® III microprocessor was employed to investigate the spatial extent of strain fields imposed on the underlying silicon substrate due to the reflow process for lead–tin solder bumps.

Large area and section back-reflection SXRT images were taken before and after the reflow process at 350°C in atmosphere. The effects of strain imposed by the overlying bump structures in these x-ray topographs have been observed principally via orientational contrast. This was also the situation after the reflow process due to severe stresses in the underlying silicon beneath the lead bumps. The estimated magnitudes of shear stress, $|\tau_{xy}|$, imposed on the underlying silicon were calculated to be of the order of 100 MPa. A simulation of the orientational contrast at the edge of bump was performed based on the kinematical theory of x-ray diffraction (Rantamäki R *et al* 1999 *J. Appl. Phys.* **86** 4298). The degree of lattice distortion is well fitted to the topographs of the post-reflow sample. The spatial strain in the underlying silicon was relieved dramatically after the lead bumps were removed from the wafer, which confirms that the solder bump formation is indeed a major source of strain in the underlying Si. Finite element modelling was performed in two-dimensional plane strain mode. The magnitudes and spatial distribution of the stresses after the reflow process are in good agreement with the SXRT results.

1. Introduction

Flip-chip technology was launched to increase I/O count, improve electrical performance, reduce packaging size and be cost effective [5]. The Intel® Pentium® III microprocessor

uses the popular ball grid array (BGA) packaging technique. A C4 (controlled collapse chip connection) technique has been employed for the solder bumping process. Ti/Ni based films were used as barrier layer metallization (BLM) and a lead–tin solder bump with high lead content was formed using the C4

electroplating technique [5, 6]. Due to the high Pb content in the solder, the solder reflow process needs to be carried out at a high temperature (up to 350°C) and in a nitrogen rich atmosphere.

The aims of this paper are to evaluate the residual stress distribution in Si substrates due to the solder bump reflow processing of these integrated circuits (ICs) using white beam synchrotron x-ray topography (WBSXRT), and to predict and compare this observed stress with finite element modelling (FEM).

The WBSXRT technique is well known as a method for visualizing stress in crystals without damaging the samples. The experiment takes only a few minutes of exposure time for high resolution films. WBXRT is an imaging technique based on the difference in reflecting power between perfect and distorted regions in a crystal sample. Three-dimensional stress/strain images can be obtained throughout the entire depth of the semiconductor material under investigation. Geometrical resolution is governed by the synchrotron beam divergence and usually lies in the μm range at beamline F-1 at HASYLAB used in this paper [8]. This spatial resolution is given by the relation $\delta = HD/L$, where H is the radiation source dimension, L the source-sample distance, and D the sample-plate distance [7].

FEM has been used in packaging analysis since it is known to be an effective method for prediction of mechanical strains in multi-component, thermally loaded systems during and after packaging processes. Most of the current literature employs the FEM technique to simulate the mechanical stress in the flip-chip after the underfill process, rather than after the solder bump reflow itself [9, 11]. In this paper, the mechanical stress induced by a solder bump reflow process has been analysed and compared to the SXRT results.

2. Experimental details

The x-ray topography measurements were performed at HASYLAB-DESY, Hamburg, Germany, utilizing the continuous spectrum of synchrotron radiation from the DORIS III storage ring bending magnet. Details of the experiments are given in [1, 8, 12]. For large area-back reflection topography (LA-BRT), reflections recorded on the film provide information on stress/strain distributions in the silicon near the surface (typically 10–100 μm from the surface). On the other hand, back-reflection section topography (BRST) provides details of strain/dislocation distributions through a thin slice of the sample near the surface. Due to the high absorption of the Pb/Sn bumps and limitations on the x-ray energy penetration (penetration depth, t_p), the measurements were performed by permitting the x-ray beam to enter via the backside of a thinned down Si wafer ($\sim 150 \mu\text{m}$ thick). This Si thickness, however, is still large enough to evaluate the Pb/Sn bump induced strain without perturbation from the backside. Mechanical polishing was used to decrease the silicon thickness of the wafers.

The Pb/Sn solder bump samples were produced at Intel Ireland Fab Operations, by using C4 short loops of a standard 0.25 μm CMOS technology. This technology has been described in detail elsewhere [10]. The samples consist mainly of silicon substrate (200 mm diameter and

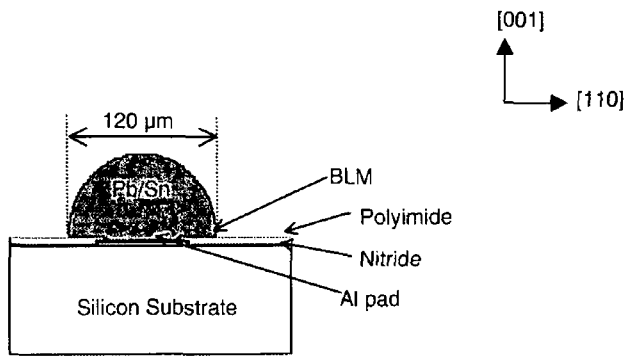


Figure 1. Geometry of Pb/Sn solder bump sample.

$\sim 700 \mu\text{m}$ thickness subsequently thinned down)/silicon epilayer/aluminium (Al) metal 5 interconnects and pad/silicon nitride passivation/polyimide passivation/BLM (Ti/Ni)/Pb–Sn solder bump. The geometry is illustrated in figure 1.

The samples were investigated in the following order: (1) pre-reflowed process samples; (2) post-reflowed process using a reflow process simulation at 350°C in atmosphere.

3. Results and discussion

WBSXRT analysis was performed at each step to ascertain the major sources of strain distribution in the silicon substrate due to the reflow process. LA-BRT and BRST images for these steps generated by the $[3\bar{3}9]$ reflection are depicted in figures 2 and 3. The scratches on the backside of the sample, which were generated from the mechanical thinning and polishing processes, are clearly observed in the image, e.g. see arrows *a* in figure 2(a). Note that other samples were examined to that the influence of sample thinning. This included bare thinned Si wafers, and the only strains observed in these samples were due to the mechanical thinning/scratching. These penetrated no deeper than $\sim 20\%$ of the thinned sample thickness and never influenced the upper surface, which was the region of interest. A line across the image represents the approximate position for its corresponding BRST, which illustrates the strains/stresses throughout a slice of Si at this location (e.g. figure 2(b)).

The region highlighted by the dotted circle in figure 2(a) shows the image associated with the strain field in the underlying silicon due to a single Pb/Sn bump. The magnification of this area illustrates a black and white contrast surrounding the Pb/Sn bumps. The black area represents an increase in recorded intensity. This phenomenon could be due to either extinction contrast or orientational contrast, or a combination of both. The extinction contrast [11] is related to the change in curvature of the crystal lattice planes under the lead bump due to induced strain. The change in lattice plane curvature, especially near the peripheries of the lead bump, will lead to an enhancement or diminution of diffracted intensity in these regions as illustrated in the LA-BRT images. On the other hand, the orientational contrast is impacted by the misorientation of the lattice planes due to severe strains imposed in the Si substrate [1].

Figure 3 shows the LA-BRT and BRST of the post-reflowed sample (sample was heated to 350°C in atmosphere as a reflow process simulation and cooled down to room temperature before measurement). The black/white contrast

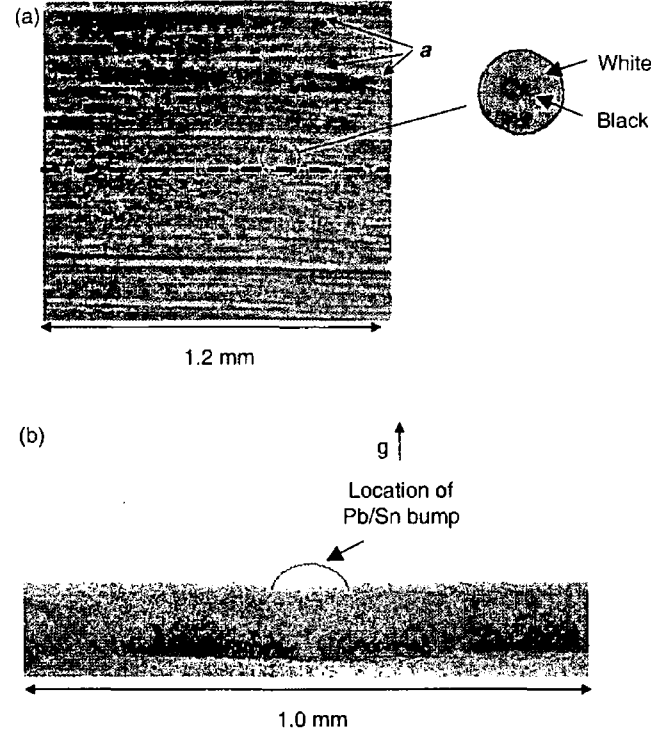


Figure 2. ($\bar{3}\bar{3}9$) LA-BRT (a) and BRST (b) of pre-reflowed sample.

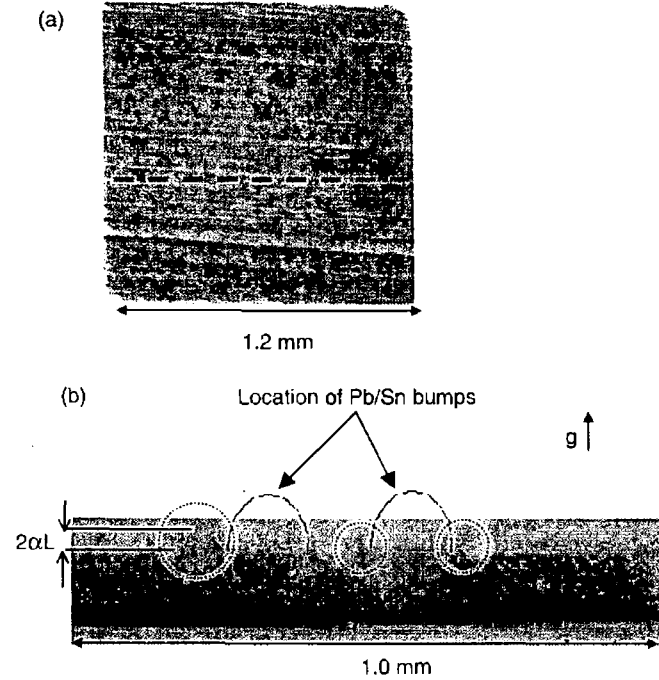


Figure 3. ($\bar{3}\bar{3}9$) LA-BRT (a) and BRST (b) of the post-reflowed sample.

is observed out to a greater diameter. The strain fields thus extend laterally to a much greater extent than in the pre-reflow case (figure 2(a)). Furthermore, the BRST image of figure 3(b) is dramatically different. It is noted that a lifting of the image of strained Si near the Pb/Sn edges above the image of the rest of the Si (dotted circles) occurred due to severe stresses being imaged via orientational contrast [4, 7].

For the white beam x-ray topography used in these experiments, orientational contrast appears practically always [7]. The magnitude of the orientational contrast shift is $\Delta S =$

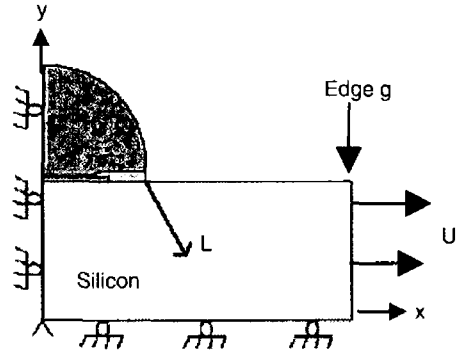


Figure 4. Geometry and boundary conditions of post-reflowed sample model.

$2(\alpha)L$, where α is the maximum apparent shift in the Bragg angle due to the strain-induced tilt of the diffracting planes, especially in severely strained regions and L the distance between sample and film (in this case = 50 mm). Assuming that this tilt is induced by shear strain near the bump-silicon interface, we can arrive at a rough estimate for the magnitude of strain in the underlying silicon via the equation

$$\gamma_{xy} \approx \tan \alpha \cong \alpha = \frac{\Delta S}{2L} \quad (1)$$

In this case, $\varepsilon = 6.2 \times 10^{-4}$. The magnitudes of stresses are given by $|\tau| = E|\gamma|$ where E , the Young modulus of Si (isotropic) = 162.3 GPa [13]. Thus, the limit on the stress magnitudes is of the order $|\tau_{xy}| \approx 100$ MPa.

For finite element analysis, two-dimensional plane strain finite element models of the multilayer structure have been employed in this paper. The geometry, dimensions and boundary conditions of the post-reflowed sample are illustrated in figure 4.

Approximately 100 000 nodes were used to perform the simulation. The finite element analyses were carried out using Quickfield™ Professional version 4.2 [18]. Eight different materials were considered in these models: Si substrate, Al pad, polyimide passivation, silicon nitride passivation, Ti/Ni BLM, intermetallic layer and Pb/Sn solder bump. Two types of FEM were initially carried out: (a) examining the strains generated by differences in temperature between the Si substrate and the metallization and (b) the simpler uniaxial load model of figure 4. Both models produce similar results. The simpler uniaxial load model is used, due to the complexity of interpreting subtle temperature-related effects on the multilayer metallization between the Pb/Sn bump and the underlying substrate. While it may be not fully accurate, the uniaxial load model will capture the main features of the BGA-imposed strain fields, in particular locating regions of strain enhancement. The FEM simulation (figure 5) confirms the build-up of strain near the edges of the bumps, and the strain magnitudes are of the same order of magnitude as observed by SXRT.

To understand the impact of the stress on the Si substrate due to thermal processing, a simulation of the orientational contrast in the BRST image is created. The simulation of the orientational contrast in the BRST of the post-reflowed process sample is based on the calculation of Rantamäki [14]. In this case, the kinematical theory is used to correlate the

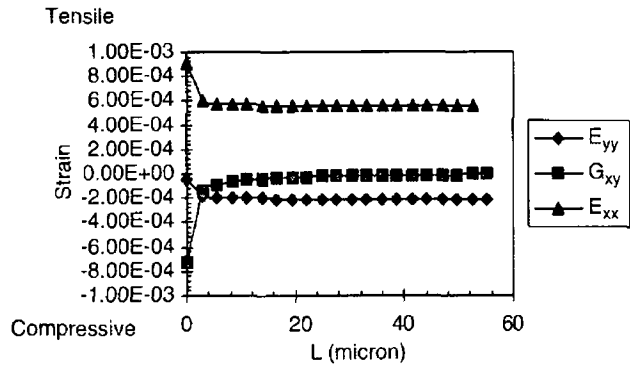


Figure 5. Finite element simulation of tensile/compressive strain distribution in Si along the $[3\bar{3}9]$ direction in the post-reflowed sample. $L = 0$ indicates the position of the periphery of the Pb/Sn bump, E_{xx} and E_{yy} = normal strains in x - and y -directions, and G_{xy} = shear strain.

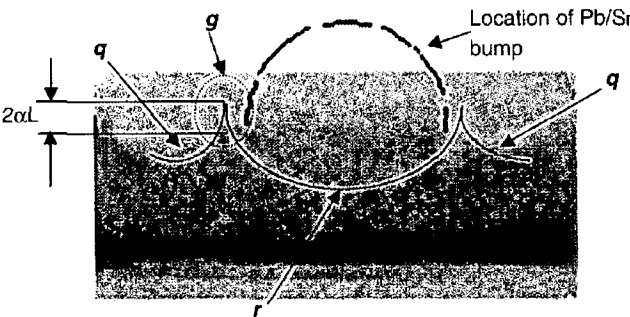


Figure 6. The BRST image of the post-reflowed process sample. The lines represent possible contours of identifiable orientational contrast. Arrows q and r are orientational contrast contours/features outside the Pb/Sn bump and underneath the Pb/Sn bump, respectively.

orientational contrast in section topographs with the degree of distortion of the lattice planes. It is assumed that the BRST is influenced by the orientational contrast only. Figure 6 shows contours of clear orientational contrast (solid line) in the Si substrate due to the Pb/Sn bump reflow process. For example, the region indicated by arrow g is most probably an orientational contrast region due to severe distortion of the lattice plane.

The simulation of the orientation contrast in this paper is based on the dimension of the sample as illustrated in figure 7. T is the sample thickness = $150\text{ }\mu\text{m}$, t_i is the depth from the back surface where the lattice planes start distorting. x is the coordinate direction from the middle of the Si underneath the Pb/Sn bump and $\Delta\theta(x)$ defines a misorientation of the lattice plane with respect to the (001) plane.

The calculation and simulation method is modified from the theory in [1], which defines each misorientation ($\Delta\theta$) of the (001) plane as a function of its position x via $\Delta\theta(x)$. Therefore, the (001) plane at any given point i is rotated by $\Delta\theta_i$. To simulate the orientational contrast, the direction and orientation are defined as given in figure 8.

It is assumed that A is in the $[110]$ direction and B is the direction of the normal of the reflecting plane (hkl), which is the $[3\bar{3}9]$ direction in this simulation; B_A is a projection of B on A and $\Delta\omega$ is the tilt of the lattice plane around an axis parallel to A . Thus, F is the direction of the distorted lattice plane ($h_r k_r l_r$). The misorientation $\Delta\theta(x)$ of the $(\bar{3}39)$ plane with

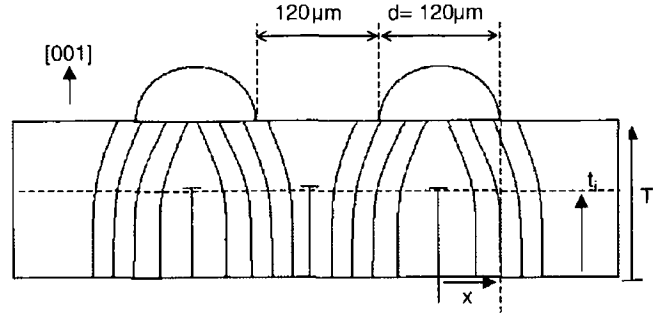


Figure 7. The dimensions of the Pb/Sn sample for the simulation of the orientational contrast.

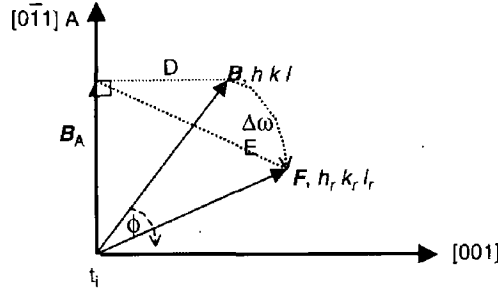


Figure 8. The direction and orientation of the lattice plane for the orientational simulation.

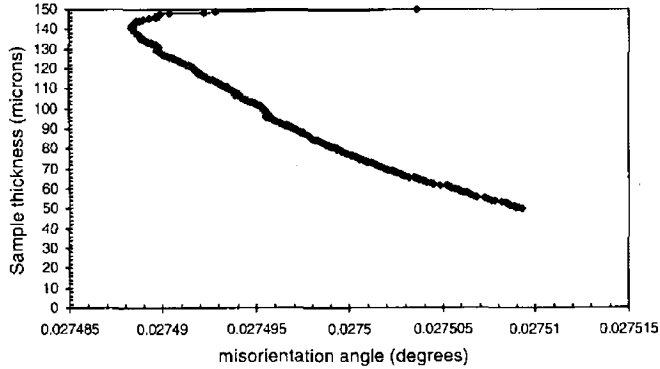


Figure 9. The simulation of the principal orientational contrast distortional features in the BRST image of the post-reflowed sample.

respect to the (001) plane from the BRST of the post-reflowed process sample due to the reflow process is calculated and shown below $\Delta\theta(x) = (1/T) \cosh(2|x|)$ for lattice planes underneath the Pb/Sn bump, $\Delta\theta(x) = (1/T) \cosh 2(d - |x|)$; $|x| = d/2$ for lattice planes outside the Pb/Sn bump.

The simulation of the orientational contrast calculated from equation above is illustrated in figure 9. The image is similar to the main contrast distortion features in the BRST image from the experiment (figure 6).

For the situation examined above, conventional x-ray diffraction techniques cannot determine the angle of the lattice distortion due to the absorption of the Pb material. However, the lattice displacement can be estimated from the FEM results, which allows one to estimate the expected lattice distortion of the Si $(\bar{3}39)$ planes. A plot of the misorientation of the $(\bar{3}39)$ lattice planes referenced to the edge of the Pb/Sn bump is also calculated from the FEM simulations and is depicted in figure 10. The lattice distortion is shown only at the edge of the bump since it gives the maximum degree of misorientation, $\Delta\theta_{\text{max}}$.

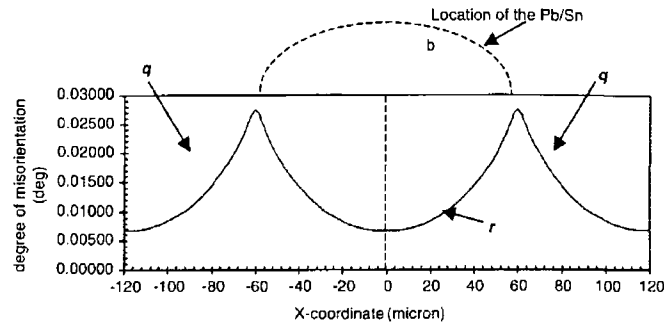


Figure 10. The misorientation of the $(\bar{3}\bar{3}9)$ Si lattice plane at the edge of the Pb/Sn bump ($X = 60 \mu\text{m}$), as a function of depth into the Si, due to the reflow process.

It appears that the most severe distortion of the lattice planes occurs near the Si/metal layer interface where $T = 140\text{--}150 \mu\text{m}$. This $\Delta\theta_{\text{max}}$ of about 0.027° (0.4 mrad) is larger than the beam divergence ($\approx 0.0238 \text{ mrad}$) and corresponds to a maximum stress of 100 MPa . Therefore, this is the most likely cause of the orientational contrast near the edge of the Pb/Sn bump in the experimental BRST image (figure 6).

4. Conclusions

WBSXRT confirms that the solder reflow process is a major source of strain in Si. This strain is particularly large near the peripheries of the Pb/Sn bumps after the reflow process. A comparison of WBSXRT topographs and FEM models indicate similar strain distributions within the Si substrate. The simulation of the orientational contrast and the FEM lattice distortion showed that the orientational contrast is the largest contributor to the contrast in the topographs, given the severe lattice tilts encountered in the Si.

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