Simulation of the impact of stress induced piezoelectric charge in GaAs MESFETs

by

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Declaration

I hereby certify that this material, which I now submit for assessment on the program of study leading to the award of Doctor of Philosophy is entirely my own work and has not been taken from the work of others save and to the extent that such work has been cited and acknowledged within the text of my work.

Signed: ______ **Date:** 20.02.95.

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List of Symbols

$\boldsymbol{a}^e$	nodal displacement vector for the element e
$\boldsymbol{B}$	$= \boldsymbol{LN}$
$\vec{B}$	induction vector
$\boldsymbol{C}$	stiffness matrix
$\boldsymbol{D}$	compliance matrix
$\vec{D}$	displacement vector
D	domain representing the device geometry
∂D	boundary of D
$\boldsymbol{d}$	piezoelectric tensor
d_{14}	piezoelectric constant
d_{11}, d_{12}, d_{44}	components of the compliance matrix
$\vec{E}$	electric field
E	magnitude of the electric field
E	Young's modulus
E_c	conduction band edge
E_{cr}	critical electric field in the field-dependent mobility model
E_{dr}	driving force in the field-dependent mobility model
E_g	band gap energy
E_i	intrinsic Fermi level
E_x	x component of $\vec{E}$ $(= \vec{E} \cdot \vec{\imath}\,)$
$\boldsymbol{F}$	body force
$\vec{F}$	$= -\operatorname{grad} \Phi_n$
$\vec{F}_l$	force per unit length

F_l	magnitude of $\vec{F}_l$
g_m	transconductance
$\vec{H}$	magnetic field
I_D	drain current
$\vec{\imath}$	unit vector in the direction of the x axis
$\vec{J}$	total current density
$\vec{J}_n$	electron current density
$\vec{J}_p$	hole current density
$\boldsymbol{K}^e$	element stiffness matrix
$\vec{k}$	unit vector in the z direction
k	Boltzmann constant
$\boldsymbol{L}$	strain-displacement matrix
L	substrate length
L_g	gate length
m	electron mobility parameter
$\boldsymbol{N}$	matrix of shape functions
N_A	acceptor concentration
N_D	donor concentration
N_c	effective density of states in conduction band
N_v	effective density of states in valance band
N_{dose}	ion dose
$N_{ref,n}$	electron mobility parameter
n	electron concentration
n_0	equilibrium electron concentration
n_S	electron concentration at the Schottky contact
n_i	intrinsic concentration
$\boldsymbol{P}$	polarization vector
$\boldsymbol{P}^*$	polarization vector in crystallographic coordinates
p	hole concentration

p_0	equilibrium hole concentration
p_S	hole concentration at the Schottky contact
q	electronic charge
R	recombination/generation term
R_p	projected range
ΔR_p	standard deviation of R_p
$\Delta R_{p,lat}$	lateral standard deviation of R_p
$\vec{r}_1$, $\vec{r}_2$	space vectors
r_1, r_2	magnitudes of $\vec{r}_1$ and $\vec{r}_2$
r_o	output resistance
STS	subthreshold current slope
T	temperature
T_d	dielectric thickness
T_g	gate thickness
T_s	substrate thickness
t	time variable
U	strain energy
$\boldsymbol{u}$	displacement vector
$\hat{\boldsymbol{u}}$	approximated displacement vector
u, v, w	components of $\boldsymbol{u}$
V_{DS}	drain-to-source voltage
V_{GS}	gate-to-source voltage
V_a	applied voltage
V_{th}	threshold voltage
ΔV_{th}	threshold voltage shift
$\vec{v}_n$	electron drift velocity
$\vec{v}_p$	hole drift velocity
v_n	magnitude of the electron drift velocity
v_{sat}	electron saturation velocity

v_n^T	thermionic emission velocity for electrons
v_p^T	thermionic emission velocity for holes
W	work done by external forces
x, y, z	gate coordinate system
Δx, Δz	mesh spacing in the x and z directions
x_1, x_2, x_3	crystallographic coordinate system
α	rotation angle
α_n	electron mobility parameter
$\boldsymbol{\beta}$	rotation matrix
β	electron mobility parameter
$\boldsymbol{\varepsilon}$	strain tensor (vector representation)
ε	permittivity
ε_0	absolute permittivity
ε_x, ε_y, ε_z, γ_{yz}, γ_{xz}, γ_{xy}	components of the strain tensor
μ_n	electron mobility
μ_n^I	impurity-dependent electron mobility
μ_n^E	field-dependent electron mobility
μ_{n0}	electron mobility parameter
μ_n^0	electron mobility parameter
$\mu_{min,n}$	electron mobility parameter
$\mu_{max,n}$	electron mobility parameter
μ_p	hole mobility
$\vec{\nu}$	outward normal unit vector
ν	Poisson's ratio
Π	total potential energy
ρ	electric charge density
ρ_{pz}	piezoelectric charge density
$[\sigma]$	stress tensor
$[\sigma^*]$	stress tensor in crystallographic coordinates

$\boldsymbol{\sigma}$	stress tensor (vector representation)
σ_{xx}, σ_{yy}, σ_{zz}, σ_{yz}, σ_{xz}, σ_{xy}	components of the stress tensor
σ_d	average dielectric stress
Φ_B	Schottky barrier height
Φ_n	electron quasi-Fermi level
Φ_p	hole quasi-Fermi level
Ψ	electrostatic potential
Ψ_S	electrostatic potential at the Schottky contact
Ψ_{bi}	built-in potential

Simulation of the impact of stress induced piezoelectric charge in GaAs MESFETs

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Abstract

This work presents the methodology involved in applying numerical electronic device simulation, and specifically, the application of this methodology to the study of piezoelectric effects in GaAs MESFETs. Firstly, a three-dimensional (3D) numerical simulation package EVEREST, developed for the simulation of silicon electronic devices, has been enhanced by the introduction and verification of models for GaAs device physics. Then a 2D finite element program for the simulation of mechanical stresses in the MESFET structure and a program for the extraction of piezoelectric charge from the numerically calculated stresses have been produced. The force load model applied to the metal/dielectric/GaAs structure is suggested as a good mathematical representation of the physical processes involved. The impact of stress induced piezoelectric charge, substrate doping and varying gate length on the electrical characteristics of epitaxial and ion-implanted MESFETs have been determined by numerical simulation using the EVEREST device simulator. Comparison between experimental data and simulation results has been presented. Finally, conclusions and suggestions for further study have been given.

Chapter 1

Introduction

The first gallium arsenide (GaAs) MEtal Semiconductor Field-Effect Transistor (MESFET) was announced in 1966 by Mead [1]. The use of a metal-semiconductor Schottky barrier instead of a diffused *p-n* junction or insulated gate to control the current flow was of great importance, for the formation of a localized diffused junction or a high quality semiconductor-insulator interface in GaAs proved nearly impossible. The MESFET evolved into a high speed microwave device due to the simplicity of device operation and design, and the unipolar operation of the device.

GaAs MESFETs have shown extrinsic current gain cut off frequencies above 100 GHz, minimum noise figures less than 1 dB, and associated gain better than 13 dB at 18 GHz [2]. The use of the GaAs MESFET for digital applications began in 1974 and has developed over years into a well-established LSI technology [3, 4], recently beginning to fulfill the promise for high-speed VLSI circuits [5].

Although widely used and studied, GaAs as a semiconductor material shows a remarkable set of problems which include material production and a series of second order effects in processed electronic devices. Being a binary compound, GaAs exhibits much higher defect densities when compared to silicon wafers. A very high surface state density (10^{12} cm^{-2} or higher) is typical at the surface of GaAs in contrast to the silicon surface (10^{10} cm^{-2} or less) when a high-density SiO_2 film is thermally grown by oxidation [6, 7].

The second order effects include such phenomena as backgating or sidegating, high subthreshold current, orientation effects, a set of short-channel effects, etc. This is only a short list of those effects that directly influence the threshold voltage of MESFETs, which is one of the most important electrical parameters of FETs.

In this work we shall concentrate on the orientation effect which is due to crystal anisotropy in GaAs. It manifests itself in the form of threshold voltage variations with a functional dependence on MESFET gate orientation on a wafer and it is due to the piezoelectric nature of the GaAs crystal. The effect is so important that one of the main design rules in GaAs IC production is that all MESFET gates on a wafer must run in the same direction [8]. The motivation governing this work is not only based on the wish to reduce scattering of MESFET electrical characteristics through the enhanced knowledge of piezoelectrically induced orientation effects, but also on a possible improvement of the MESFET parameters by intentionally induced piezoelectric charge.

The goals of this study are to contribute to the methodology involved in applying numerical electronic device simulation, and specifically, the application of this methodology to the study of piezoelectric effects in GaAs MESFETs.

We tried to fulfil the goals of this study through several steps. Firstly, a three-dimensional (3D) numerical simulation package EVEREST [48], developed for the simulation of silicon electronic devices, has been enhanced by the introduction and verification of models for GaAs device physics. Then a 2D finite element program for the simulation of mechanical stresses in the MESFET structure has been written. Furthermore, a program for the extraction of piezoelectric charges from the numerically calculated stresses has been produced. A separate program for calculation of the piezoelectric charge from an analytical approach has also been developed. The effects of piezoelectric charges determined by the two aforementioned methods on the electrical characteristics of MESFETs have been determined by numerical simulation using the EVEREST package. The results for epitaxial and ion-implanted MESFETs with different technological parameters have been obtained and compared. Finally, conclusions and suggestions have been given.

Chapter 2 presents a survey of research related to the piezoelectric effect. A short review of GaAs MESFET numerical simulation is also given.

Chapter 3 presents the basic semiconductor equations. The assumptions implicit in the drift-diffusion approximation of carrier transport are briefly described. Boundary conditions and models for GaAs physical phenomena are reviewed, and then results of several MESFET simulations are discussed.

Chapter 4 introduces the linear elasticity theory and explains the usage of the Finite Element Method (FEM) for simulation of mechanical stresses in the MESFET structure. The derivation of induced piezoelectric charge

from the obtained stress fields is explained. The results obtained through the application of FEM simulation and an analytical approach are compared.

Chapter 5 expands on the influence of stress-induced piezoelectric charge on the electrical characteristics of MESFETs. Two types of MESFETs, epitaxial and ion-implanted, are analysed.

Chapter 6 presents the conclusions of the study and offers suggestions for further study.

Chapter 2

Survey of research

GaAs MESFET technology holds much promise in the future for high-speed low-power device implementation. However, serious problems still lie in the path of the development of this technology for IC production. These problems include material production and second order effects such as backgating, high subthreshold current, orientation effects, temperature dependence of electrical characteristics, effects of donor diffusion from highly doped contact regions, effects of deep traps, variations of mobility parameters with changes in gate lengths and consequent variations of electrical characteristics.

Indeed, if one only considers the problems associated with the threshold voltage V_{th} of MESFETs, a number of effects can be seen: a) V_{th} varies considerably over a given wafer; b) V_{th} varies with changes in the gate length L_g; c) V_{th} varies with the FET gate orientation on a wafer (commonly reffered to as orientation effects). We shall concentrate on the research related to the orientation effects.

It is well known that in GaAs, a zinc-blende crystal based on the cubic space group F$\bar{4}$3m [9], the two $<011>$ directions are not identical[1] (see Fig. 2.1 for definition of orientations). This property has been used to explain the asymmetric cracking, bending and dislocation formation in III-V compound semiconductors [10, 11, 12].

The earliest work carried out in the area of orientation effects is that of Lee *et al.* [14], who investigated the dependence of the electrical characteristics of MESFETs on their orientation. In this study planar GaAs MESFETs with a CVD Si_3N_4 annealing cap were fabricated on (100) surfaces of semi-insulating GaAs substrates using multiple localized ion-implantation directly into the

[1]The two different $<011>$ crystal directions can be easily identified using the preferential etching method [13].

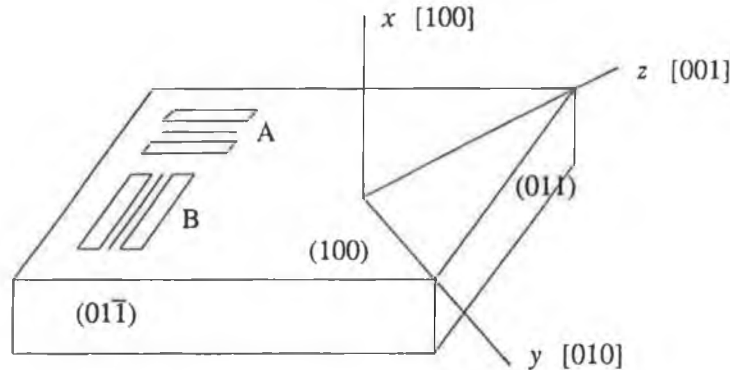

Figure 2.1: Definition of orientations. The gate of the MESFET A is oriented in the [011] direction, and the gate of the MESFET B in the [01$\bar{1}$] direction. The MESFET A will be called the [011] FET and the MESFET B will be called the [01$\bar{1}$] FET. Both MESFETs are processed on the (100) crystallographic surface.

substrate. Devices oriented in the [011] direction exhibited a higher threshold voltage V_{th} than those oriented in the [01$\bar{1}$] direction. Furthermore, the value of V_{th} varied substantially with gate length L_g for orientation in the [01$\bar{1}$] direction, but it was nearly independent of L_g for the [011] direction over the range of gate lengths from 1 to 50 μm.

Similar work was reported in 1983 by Yokoyama *et al.* [15], wherein a CVD SiO_2 annealing cap was used. They noted similar effects to those of Lee *et al.* but they occured for reversed orientations, i.e. the threshold voltage shifts were of opposite sign. Yokoyama *et al.* also noted that the K-value[2] decreased unexpectedly for short-gate-length [011] FETs and they observed that this behaviour was absent in [01$\bar{1}$] FETs.

In that same year Sadler and Eastman [16] conducted experiments on MESFETSs in which a capless arsine anneal was used. They noted almost identical variations of V_{th} in both directions. Their results would conform to a "normal" short-channel effect, i.e. to the fact that there would be an increase in donor concentration due to the lateral straggle of ion-implanted n^+ regions and also possibly due to stress enhanced preferential lateral diffusion during the post-implant anneal. It is clear that the dielectric overlayer plays a significant role as Sadler and Eastman observed very little orientation dependence when no dielectric was present. This stress can be caused by thermal expansion mis-

[2]Using an approximation of $(I_D)^{1/2} = (K)^{1/2}(V_{GS} - V_{th})$, the threshold voltage is determined as an extrapolated value of V_{GS} for $I_D = 0$, and $\sqrt{K}$ is determined as the inclination of the extrapolation line.

match between the substrate and thin film overlayers, alloying of the metal contacts or wafer deformation due to thermal processing.

In 1984 Chang *et al.* [17] reported that the threshold voltages of FETs in the [011] and [01$\bar{1}$] directions had a strong dependence on radial distance from the centre of the wafer, while [001] and [010] orientated FETs exhibited no such dependence and had better device uniformity. This observation was explained by the presence of piezoelectric charge. The same group of authors in the paper by Asbeck *et al.* [18] derived a simple analytical model for the stress induced piezoelectric charge.

In 1985 Ohnishi *et al.* [19] resolved the problem of the conflicting data of Lee *et al.* [14] and Yokoyama *et al.* [15] by attributing the difference in sign of the V_{th} shift to differences in the overlayers used. They proved, by X-ray diffraction measurements, that SiO_2 and Si_3N_4 films imposed opposite stresses on GaAs; the SiO_2 films being in compression, while the Si_3N_4 films were in tension. As will be shown later, the opposite signs of the stresses account for the differing V_{th} shifts.

Asbeck *et al.* [18], Chang *et al.* [17], Ohnishi *et al.* [19], and Onodera *et al.* [20] confirmed that the orientation dependence of V_{th} is decreased as the dielectric layer is thinned down by plasma etching, which is consistent with the conclusion of Sadler and Eastman [16] that with the use of capless annealing there is no preferred direction for MESFETs fabricated on (100) GaAs surfaces. We can further conclude that the stress imparted by the gate metal is negligible as well as the stress enhanced preferential diffusion. The reason for the former is obvious since the threshold voltage shifts are considerably reduced and practically negligible for FETs without dielectric overlayers. The reason for the latter is that the stress enhanced preferential diffusion ought to occur during post-implant annealing, but not during dielectric overlayer etching. This diffusion should cause orientation dependence even when the dielectric layer is completely thinned down to the zero thickness. Note that the lateral stretch of n^+ implanted ions still exists as a separate problem.

Kanamori *et al.* [21] conducted experiments in which external mechanical stresses were directly applied to the GaAs substrate. Almost the same voltage shifts were observed for FETs with and without a SiO_2 overlayer and the authors concluded that the gate metal stress is mainly responsible for the threshold voltage shift, which is in contrast to all previously published results.

McNally *et al.* [22] also used externally applied loads. In their exper-

iments the same device was put into both tension and compression, which clearly demonstrated the piezoelectric effect. Ramirez *et al.* [23] calculated the stresses induced by an overlayer using a 2D finite element method and estimated the V_{th} shift by means of the moment-arm method. Good agreement was found with the experimental work of McNally *et al.* [22].

McNally *et al.* [24] extended the work of Ramirez *et al.* [23] performing the 2D device simulations to evaluate the effects of stress induced piezoelectric charge distributions.

Considering the numerical simulation of electrical characteristics of GaAs MESFETs, there are several approaches. Although the MESFET analytical analysis underwent various improvements since the first analytical model applicable to GaAs MESFETs [25], a 2D simultaneous solution of Poisson's equation and the electron current continuity equation is required to rigorously analyse the current flow under the Schottky gate of MESFETs. The standard drift-diffusion approximation of current flow has been widely used [26]-[36], but other approaches with more sophisticated equations for the physical and mathematical modelling of MESFETs have been implemented as well, e.g. the Monte Carlo method [37]-[42] and the energy balance equations [43]-[46].

Chapter 3

Simulation of GaAs MESFETs

3.1 Basic semiconductor equations

The basic semiconductor equations can be derived from Maxwell's equations (3.1)-(3.4), several relations obtained from the solid-state physics of semiconductors and various assumptions.

$$\mathrm{rot}\,\vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t} \tag{3.1}$$

$$\mathrm{rot}\,\vec{E} = -\frac{\partial \vec{B}}{\partial t} \tag{3.2}$$

$$\mathrm{div}\,\vec{D} = \rho \tag{3.3}$$

$$\mathrm{div}\,\vec{B} = 0 \tag{3.4}$$

$\vec{E}$ and $\vec{D}$ are the electric field and displacement vector, $\vec{H}$ and $\vec{B}$ are the magnetic field and induction vector, respectively. $\vec{J}$ denotes the conduction current density, ρ is the electric charge density, and t is the time variable.

The basic set of semiconductor equations consists of Poisson's equation and two current continuity equations. While the derivation of Poisson's equation is practically straightforward, the derivation of the current continuity equations is quite demanding [47].

Poisson's equation is given by

$$\varepsilon\,\mathrm{div}\;\mathrm{grad}\,\Psi = -\rho \tag{3.5}$$

where ε denotes the permittivity and Ψ is the electrostatic potential. The relation between the electrostatic potential Ψ and the electric field $\vec{E}$ is

$$\vec{E} = -\,\mathrm{grad}\,\Psi. \tag{3.6}$$

The space charge density ρ can be further broken apart into

$$\rho = q(p - n + N_D - N_A) \tag{3.7}$$

where p (n) represents the hole (electron) concentration, N_D (N_A) the donor (acceptor) concentration, and q the electronic charge.

We can now rewrite Poisson's equation into the well known form

$$\varepsilon \,\mathrm{div}\ \mathrm{grad}\, \Psi = -q(p - n + N_D - N_A). \tag{3.8}$$

The current continuity equations for holes and electrons are

$$q\frac{\partial p}{\partial t} = -\,\mathrm{div}\, \vec{J}_p - qR \tag{3.9}$$

$$q\frac{\partial n}{\partial t} = \mathrm{div}\, \vec{J}_n - qR \tag{3.10}$$

where $\vec{J}_n$ ($\vec{J}_p$) is the electron (hole) current density. The quantity R is a function describing the net generation or recombination of electrons and holes. The current continuity equations (3.9) and (3.10) are generally valid as they represent the fundamental balance law, i.e. the fact that sources and sinks of the conduction currents are fully compensated by the time variation of the mobile charge. The next necessary step is to define the hole and electron current densities.

In general, the hole and electron current densities can be expressed as

$$\vec{J}_p = qp\vec{v}_p \tag{3.11}$$

$$\vec{J}_n = -qn\vec{v}_n \tag{3.12}$$

where $\vec{v}_p$ ($\vec{v}_n$) is the hole (electron) drift velocity. We see that the current density is the product of the unit charge, the particle concentration and the average velocity of particles. The major problem of semiconductor simulation is to find expressions which relate the average or drift velocities for electrons $\vec{v}_n$ and holes $\vec{v}_p$ to the electric field $\vec{E}$ and to the carrier concentrations n and p.

Without giving a detailed derivation, we present the final form of the current relations as implemented in the semiconductor device simulation package EVEREST [48]. The current densities, derived from the Boltzmann transport equation,

$$\vec{J}_p = -q\mu_p p \,\mathrm{grad}\, \Phi_p \tag{3.13}$$

$$\vec{J}_n = -q\mu_n n \,\mathrm{grad}\, \Phi_n \tag{3.14}$$

together with the equations for the carrier concentrations, given by the Maxwell–Boltzmann approximation,

$$p = n_i \exp\left(\frac{\Phi_p - \Psi}{kT/q}\right) \tag{3.15}$$

$$n = n_i \exp\left(\frac{\Psi - \Phi_n}{kT/q}\right) \tag{3.16}$$

allow us to express the current densities in the form

$$\vec{J}_p = -q\mu_p \left[(kT/q)\,\mathrm{grad}\,p + p\,\mathrm{grad}\,(\Psi - (kT/q)\ln n_i)\right] \tag{3.17}$$

$$\vec{J}_n = q\mu_n \left[(kT/q)\,\mathrm{grad}\,n - n\,\mathrm{grad}\,(\Psi + (kT/q)\ln n_i)\right] \tag{3.18}$$

where the terms $\mathrm{grad}\,(\ln n_i)$ represent possible dependence of the intrinsic concentration n_i on position; μ_n (μ_p) is the electron (hole) mobility, k is the Boltzmann constant, T is the temperature in Kelvins, Φ_n (Φ_p) is the electron (hole) quasi-Fermi level [47, 49].

To summarize results obtained so far, we shall rewrite the basic set of semiconductor equations. It consists of Poisson's equation (3.19), the continuity equations for electrons (3.20) and holes (3.21), and the current relations for electrons (3.22) and holes (3.23)

$$\varepsilon\,\mathrm{div}\,\mathrm{grad}\,\Psi = -q(p - n + N_D - N_A) \tag{3.19}$$

$$q\frac{\partial n}{\partial t} = \mathrm{div}\,\vec{J}_n - qR \tag{3.20}$$

$$q\frac{\partial p}{\partial t} = -\,\mathrm{div}\,\vec{J}_p - qR \tag{3.21}$$

$$\vec{J}_n = q\mu_n \left[(kT/q)\,\mathrm{grad}\,n - n\,\mathrm{grad}\,(\Psi + (kT/q)\ln n_i)\right] \tag{3.22}$$

$$\vec{J}_p = -q\mu_p \left[(kT/q)\,\mathrm{grad}\,p + p\,\mathrm{grad}\,(\Psi - (kT/q)\ln n_i)\right]. \tag{3.23}$$

These equations form the mathematical model of semiconductor device operation and have to be solved numerically for given boundary conditions. The model is known as the drift-diffusion approximation of current flow. Although it is valid for a broad range of engineering applications, conditions do exist for which its validity is not guaranteed or not certain. However, as we are bound to perform a trade-off between accuracy and complexity of our model, the more general and sophisticated results are too complex to give a rigorous and still sufficiently simple model for the purpose of device simulation.

More details about assumptions and simplifications introduced to derive the set of basic semiconductor equations can be found in [47], but for the

purpose of clarity we shall sketch some of the assumptions introduced in the model.

The situation with Poisson's equation is simple. The permittivity ε, which is in principle a tensor of rank two, will be treated here as a scalar quantity ($\varepsilon = 12.9\varepsilon_0$ for GaAs and ε_0 is the absolute permittivity [50]).

The major assumptions in the derivation of the drift-diffusion approximation of carrier transport, originally formalized in 1950 by van Roosbroeck [51], state that: 1) the carriers have to undergo many collisions in the time intervals of interest; and 2) the changes in the carriers electrostatic potential energy over distances equal to the mean free path have to be small compared with the average thermal energy.

The many collisions assumption poses strong limitations on the drift-diffusion approximation when micron and submicron devices are considered. The one-dimensional Monte-Carlo simulation [52] has shown that electrons accelerated from an initial state of zero average velocity can travel distances up to 1 μm before they have experienced sufficiently many collisions to reach a state of equilibrium with the crystal lattice. Due to this effect, called velocity overshoot, significant variations of the electric field over the distance less than 0.5 to 1 μm, or temporal variations in less than 2.5 to 25 ps invalidate the many collisions assumption in GaAs.

The second assumption states that the drift-diffusion approximation is valid only if carriers travel under low electric field.

To express the full severity of the problem we shall add three more assumptions which had to be introduced to obtain the current relations (3.22) and (3.23) from the Boltzmann transport equation:

- All scattering processes have been assumed to be elastic. Therefore, polar optical phonon scattering, which is a major scattering mechanism in GaAs, has been neglected.

- The spatial variation of external forces is neglected which implies a slowly varying electric field vector.

- The semiconductor has been assumed to be infinitely large. In a real device the distribution function is changed in a complex manner in the vicinity of boundaries, for instance contacts [53] and interfaces [54]. It can be expected that the drift-diffusion approximation fails within a few mean free paths of boundaries.

3.2 Boundary conditions

The basic semiconductor equations are defined over the domain D representing the device geometry. The boundary ∂D of the three-dimensional problem is piecewise smooth and can be split into two parts

$$\partial D = \partial D_P \cup \partial D_A \tag{3.24}$$

where ∂D_P represents the parts which correspond to real "physical" boundaries like contacts, and ∂D_A consists of artificial boundaries which are introduced to enable simulation.

It is obvious that an artificial boundary can not be introduced completely arbitrarily. Taking into account knowledge of the operation of a device it is possible to define somewhat natural boundaries which separate the device from its environment. A typical example is the reduction of the height of the simulated region to several microns instead of simulating a device over a typical wafer thickness of 500 microns.

At the non-contact (artificial) boundaries we assume that no current flows out of the semiconductor, and that the non-contact boundaries of the simulated region are far enough from the active channel so that changes of the potential in the direction perpendicular to the boundary vanish at that boundary. It is important to note that it is up to the device engineer who performs the simulation to check that the height of the simulated region is large enough, because the above conditions will be automatically forced by the solution process. Thus we define the Neumann boundary conditions [49]

$$\vec{J}_p \cdot \vec{\nu} = -\vec{J}_n \cdot \vec{\nu} = \text{grad}\,\Psi \cdot \vec{\nu} = 0 \tag{3.25}$$

where $\vec{\nu}$ is the outward normal unit vector from the boundary.

Ohmic contacts are idealized by assuming infinite contact recombination velocities and space charge neutrality. Hence, carriers are in thermodynamic equilibrium and both quasi-Fermi levels equal the applied voltage V_a

$$\Phi_p = \Phi_n = V_a. \tag{3.26}$$

We also have the Dirichlet boundary conditions for the electrostatic potential and for both carrier concentrations

$$\Psi = V_a + \Psi_{bi} \tag{3.27}$$

$$n = n_0 \tag{3.28}$$

$$p = p_0 \tag{3.29}$$

where n_0 and p_0 are the values of the corresponding variables for space-charge neutrality and at equilibrium

$$np - n_i^2 = 0 \tag{3.30}$$

$$n - p - N_D + N_A = 0. \tag{3.31}$$

These two conditions can be arranged into

$$n_0 = \frac{\sqrt{(N_D - N_A)^2 + 4n_i^2} + (N_D - N_A)}{2} \tag{3.32}$$

$$p_0 = \frac{\sqrt{(N_D - N_A)^2 + 4n_i^2} - (N_D - N_A)}{2}. \tag{3.33}$$

If we have one type of dopant dominating the other type, the built-in potential Ψ_{bi} can be simplified

$$\Psi_{bi} \doteq \frac{kT}{q} \ln\left(\frac{N_D}{n_i}\right) \quad \text{for} \quad N_D >> N_A \tag{3.34}$$

$$\Psi_{bi} \doteq -\frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right) \quad \text{for} \quad N_A >> N_D. \tag{3.35}$$

The second type of contact is the Schottky barrier or rectifying contact. The physics of the Schottky barrier contact is extraordinarily complex. For the purpose of simulation highly simplified models are commonly in use. For the electrostatic potential one can assume the Dirichlet boundary condition

$$\Psi = \Psi_S = V_a + \Psi_{bi} - \Phi_B \tag{3.36}$$

where Ψ_S is the potential on the Schottky contact, Φ_B represents the Schottky barrier height which is a characteristic quantity of the metal and the semiconductor with which the Schottky contact is fabricated. Fig. 3.1 shows the Schottky barrier energy band diagram in equilibrium ($V_a = 0$). Ψ_{bi} is again the built-in voltage, but in this case defined as

$$\Psi_{bi} = \frac{E_c - E_i}{q} \tag{3.37}$$

where $E_c - E_i$ is the difference between the conduction band edge and the intrinsic Fermi level in the semiconductor. In GaAs, in contrast to the Silicon case, $E_c - E_i$ differs from $E_g/2$ due to the pronounced difference between N_c and N_v.

For electron and hole concentrations it is more difficult to give boundary conditions which are physically reasonable and still sufficiently simple for

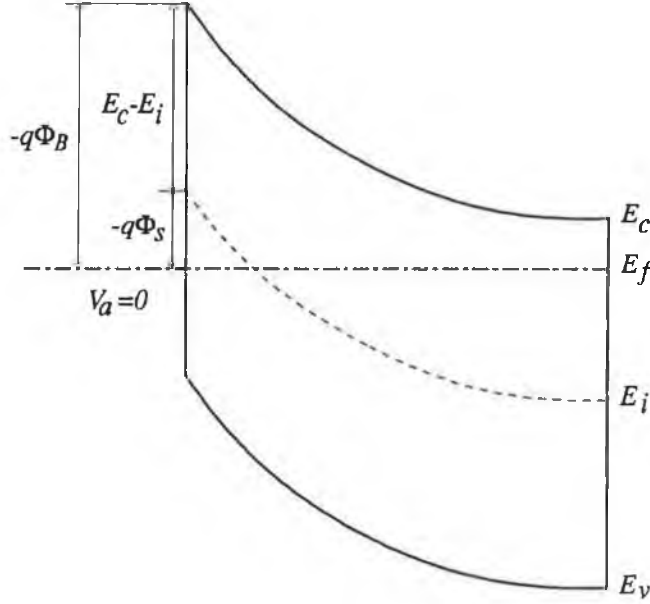

Figure 3.1: Schottky barrier energy band diagram in equilibrium ($V_a = 0$).

modelling. We model Schottky contact electron (n_S) and hole (p_S) carrier concentrations by

$$n = n_S = N_c \exp\left(-\frac{\Phi_B}{kT/q}\right) \tag{3.38}$$

$$p = p_S = \frac{n_i^2}{N_c} \exp\left(\frac{\Phi_B}{kT/q}\right) \tag{3.39}$$

which, with the conditions for the quasi-Fermi levels

$$\Phi_n = \Phi_p = V_a, \tag{3.40}$$

satisfies the equilibrium condition $n_S p_S = n_i^2$.

It is worth noting that the carrier concentrations at a Schottky contact depend in general on the current density passing through the contact. The boundary conditions arising from the thermionic emission/diffusion theory [55, 56] are more physical

$$\vec{J}_n \cdot \vec{\nu} = -qv_n^T(n_S - n_0) \tag{3.41}$$

$$\vec{J}_p \cdot \vec{\nu} = qv_p^T(p_S - p_0) \tag{3.42}$$

where v_n^T (v_p^T) represents the thermionic emission velocity for electrons (holes). The conditions (3.38) and (3.39) are the special case of (3.41) and (3.42) for infinite thermionic emission velocities.

3.3 GaAs models and parameters

The basic semiconductor equations just determine the set of equations that has to be solved for given boundary conditions to simulate the internal behaviour of a device.

The geometry of a device and the distribution of dopants can be considered to be physical parameters as well. They shall be discussed separately for each simulated device.

There are additionally several physical parameters that have to be defined prior to the simulation of a device. Most of them are related to the energy band representation of semiconductors and to the carrier mobility models, and they have to be couched in a form suitable for the numerical simulation. Extensive reviews of GaAs physical parameters can be found in [9, 50, 57].

The electronic device simulator EVEREST has been enhanced by the following GaAs specific models for the energy band representation

$$E_g = 1.519 - \frac{5.405 \cdot 10^{-4} T^2}{204 + T} \quad (3.43)$$

$$N_v = 1.83 \cdot 10^{15} T^{3/2} \quad (3.44)$$

$$N_c = 8.63 \cdot 10^{13} T^{3/2} (1 - 1.93 \cdot 10^{-4} T - 4.19 \cdot 10^{-8} T^2) \quad (3.45)$$

$$n_i = \sqrt{N_c N_v} \exp\left(-\frac{E_g}{2kT}\right) \quad (3.46)$$

$$E_i = E_g - kT \ln \frac{N_c}{n_i} \quad (3.47)$$

where E_g is the energy gap in electron volts (eV) between the conduction and valence band, N_c (N_v) represents the effective electron (hole) concentration (in cm^{-3}), n_i is the intrinsic concentration (in cm^{-3}), and E_i is the intrinsic Fermi energy (in eV) [50]. Thus, for a temperature of 300 K we have

$$E_g = 1.423 \quad \text{eV} \quad (3.48)$$

$$N_v = 9.51 \cdot 10^{18} \quad \text{cm}^{-3} \quad (3.49)$$

$$N_c = 4.21 \cdot 10^{17} \quad \text{cm}^{-3} \quad (3.50)$$

$$n_i = 2.23 \cdot 10^{6} \quad \text{cm}^{-3} \quad (3.51)$$

$$E_i = 0.752 \quad \text{eV}. \quad (3.52)$$

The model of the effective electron concentration N_c takes into account the nonparabolicity of the conduction band edge. Contributions from the satellite valleys have not been included because they do not significantly influence the electron concentration at temperatures below 500 K. On the other

hand, the intervalley transfer due to high electric fields is included through the field-dependent mobility model. It is worth noting that this kind of physical inconsistency has become common practice in the numerical simulation of semiconductor devices, because very complex physics underlies the theory of operation of semiconductor devices.

No specific model for band gap narrowing has been defined for GaAs. This means that the intrinsic concentration is independent of the position.

Next, we shall discuss carrier mobilities. The primary interest of this work is to model and simulate n-type GaAs MESFETs. Thus, no model for the hole mobility will be given because all simulations are performed by assuming that the contribution of the hole current continuity equation can be neglected. Additionally, the hole quasi-Fermi level is kept constant throughout the whole MESFET structure, its value corresponding to the equilibrium hole concentration.

The electron mobility of GaAs is known to be a very complex function. In general, electrons and holes can be scattered by thermal lattice vibrations, ionized impurities, neutral impurities, vacancies, interstitials, dislocations, surfaces, and electrons and holes themselves. Many of these mechanisms, and especially their interactions, are very complicated and difficult to model. Thus, we end up by using phenomenological expressions to model various experimentally observed mobility phenomena.

The most fundamental process by which carriers are scattered is their interaction with lattice vibrations. The simple temperature dependent model for the electron mobility is given by

$$\mu_n = \mu_{n0}\left(\frac{T}{300}\right)^{-\alpha_n} \tag{3.53}$$

where μ_{n0} and α represent fitting parameters. The default values are chosen to be $\mu_{n0} = 7500$ cm^2/V·s and $\alpha_n = 1$ [58]. It is worth noting that there is a considerable scattering among the published data for μ_{n0} from 7500 cm^2/V·s [58] and 8500 cm^2/V·s [59, 60, 61], to 9000 cm^2/V·s [62].

A very similar situation exists when the impurity-dependent mobility is considered. We use

$$\mu_n^I = \mu_{min,n} + \frac{\mu_{max,n}(T/300)^{-\beta_n}}{[1 + (N_A + N_D)/N_{ref,n}]^{\alpha_n}} \tag{3.54}$$

where the fitting parameters have the following values: $\mu_{min,n} = 1500$ cm^2/V·s, $\mu_{max,n} = 6400$ cm^2/V·s, $\beta_n = 1$, $N_{ref,n} = 1.426 \cdot 10^{17}$ cm^{-3}, and $\alpha_n = 0.5385$

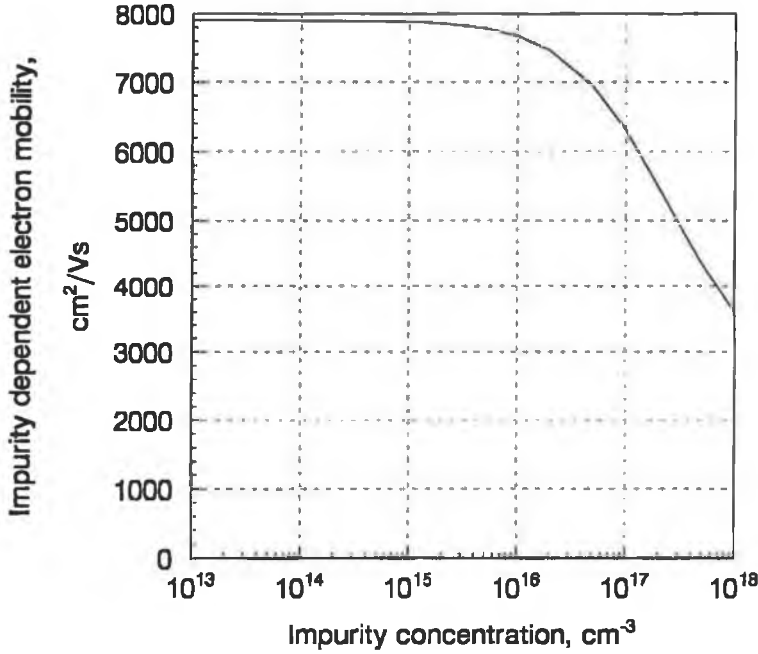

Figure 3.2: Impurity-dependent mobility μ_n^I as a function of the doping concentration $N_A + N_D$.

[36]. Several other ionized impurity scattering models have been presented that are more or less complex than (3.54) [33, 63]. Fig. 3.2 shows the mobility μ_n^I as a function of the doping concentration $N_A + N_D$.

The last model we shall present is the field-dependent mobility model

$$\mu_n^E(E) = \frac{\mu_n^I + v_{sat}\dfrac{E^3}{E_{cr}^4}}{1 + \dfrac{E^4}{E_{cr}^4}} \tag{3.55}$$

where $v_{sat} = 0.8 \cdot 10^7$ cm/s is the electron saturation velocity, $E_{cr} = 4.3$ kV/cm is the critical electrical field, $E = |\vec{E}|$ represents the magnitude of the electric field, and μ_n^I is the impurity-dependent mobility given by (3.54) [36].

Equations (3.54) and (3.55) reproduce the velocity-field curve obtained by Monte Carlo simulation in the constant electric field [64, 65].

Fig. 3.3 shows the mobility μ_n^E as a function of the electric field for $N_A + N_D = 10^{13}$ and 10^{17} cm^{-3}, which corresponds to the doping concentrations of the substrate and the active channel respectively of a typical MESFET, and Fig. 3.4 shows the electron velocity

$$v_n = \mu_n^E E \tag{3.56}$$

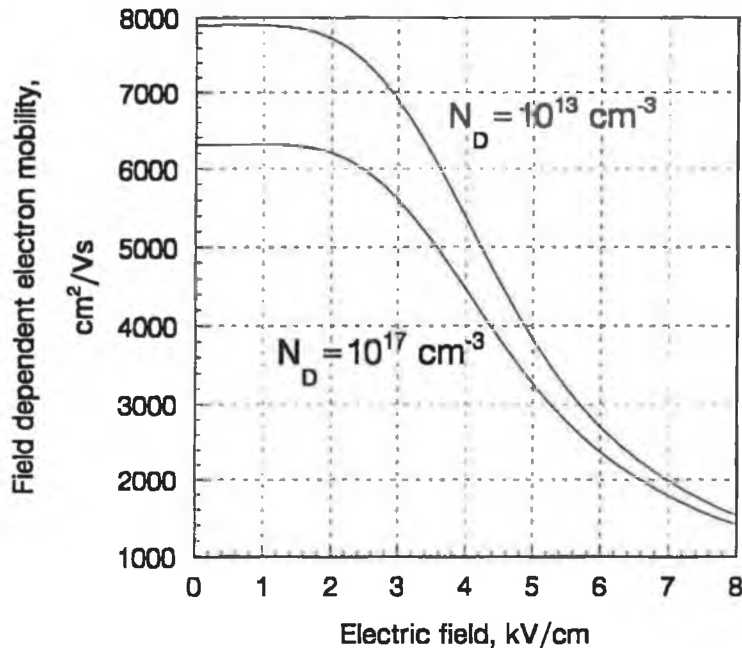

Figure 3.3: Field-dependent mobility μ_n^E as a function of the electric field for two different doping concentrations.

for the same doping concentrations.

No model for the hole mobility has been defined because all simulations have been performed by assuming that the contribution of the hole current continuity equation can be neglected. The hole quasi-Fermi level has been kept constant throughout the whole MESFET structure, its value corresponding to the equilibrium hole concentration.

3.4 Verification

In this section we shall present our attempts to obtain good agreement with experimental results for an ion-implanted MESFET. Recombination has been neglected and only DC simulation has been performed.

The structure of an ion-implanted MESFET is shown in Fig. 3.5. Gaussian and error function profiles are assumed for the donor impurity distribution in the vertical and lateral directions respectively. The values of the ion dose N_{dose}, the projected range R_p, the standard deviation ΔR_p, and the lateral standard deviation $\Delta R_{p,lat}$ for the n-channel and heavily doped contact regions are given in Table 3.1. In both cases 50% post-implant annealing efficiency has been

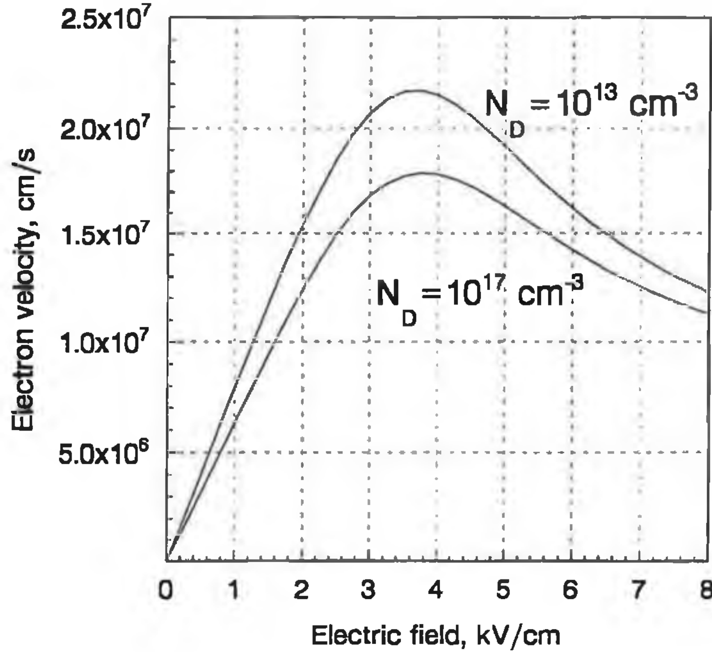

Figure 3.4: Electron velocity v_n as a function of the electric field for two different doping concentrations.

assumed. A T-shaped gate electrode has been used as an implantation mask for n^+ regions to reduce the series resistances between the active channel and ohmic contacts. The background doping is $N_A = 5 \cdot 10^{13}$ cm^{-3}. The Schottky barrier height is $\Phi_B = 0.95$ V, as measured for the WN$_x$ gate [66]. All these parameters and experimental data are taken from [36].

The first attempt, using the impurity-dependent mobility model (3.54) and the field-dependent mobility model (3.55), has shown considerably lower currents for $V_{GS} = 0.7$ and 0.5 V than the experiment, although the agreement for $V_{GS} = 0.3$ V was fairly good (Fig. 3.6).

The explanation is simple; the mobility is assumed to depend on the absolute electric field value. However, this physical picture is not valid when a strong built-in electric field appears perpendicular to the channel direction, as is the case below the Schottky gate. Because the electron current direction is almost perpendicular to the built-in field, electrons in the channel do not acquire any energy from the built-in field, which implies that under low drain bias conditions the electron mobility should be its low-field value. If the electron mobility depends on the magnitude of the electric field, the mobility value

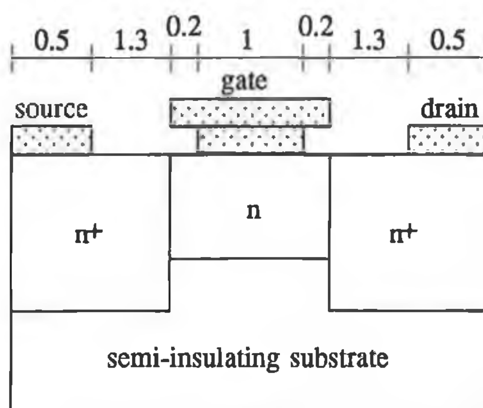

Figure 3.5: Schematic structure of an ion-implanted MESFET (all dimensions in microns). The width is 10 μm.

n-channel layer:	
N_{dose}	$2 \cdot 10^{12}$ cm^{-2}
R_p	0.0424 μm
ΔR_p	0.0254 μm
$\Delta R_{p,lat}$	0.0343 μm
n^+ contact regions:	
N_{dose}	$3 \cdot 10^{13}$ cm^{-2}
R_p	0.1559 μm
ΔR_p	0.0697 μm
$\Delta R_{p,lat}$	0.1007 μm

Table 3.1: Parameters for donor impurity profiles of 1 μm gate-length ion-implanted MESFET.

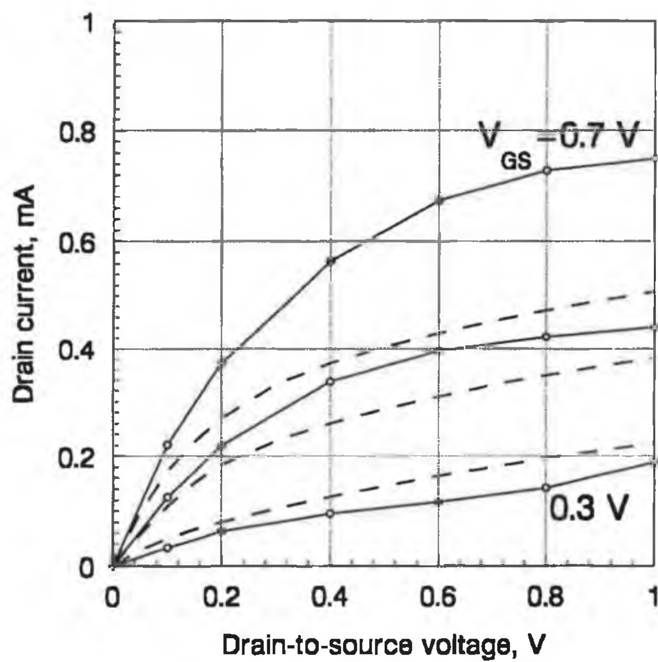

Figure 3.6: Drain currents for the 1 μm gate-length ion-implanted MESFET. The experimental data (full line) and calculated results (dashed line) for $V_{GS} = 0.7$, 0.5 and 0.3 V are shown. The agreement is relatively good only for $V_{GS} = 0.3$ V (the lowermost curves). Calculated results are obtained using the impurity-dependent low-field mobility μ_n^I and the magnitude of the electric field as the driving force for the field-dependent mobility model $\mu_n(|\vec{E}|)$.

and the electron current are seriously underestimated.

As the electron current flows in the direction of the gradient of the electron quasi-Fermi level (see (3.14)), the magnitude of the electric field in the field-dependent mobility model should be replaced by

$$E_{dr} = \frac{|\vec{E} \cdot \vec{F}|}{|\vec{F}|} \tag{3.57}$$

where

$$\vec{F} = -\operatorname{grad} \Phi_n . \tag{3.58}$$

Thus, the driving force E_{dr}, representing the projection of the electric field on the direction of current flow, should be used in the field-dependent mobility model instead of the magnitude $E = |\vec{E}|$.

Unfortunately, when the model (3.57) was implemented, it was not possible to get simulation results because either the iterative process was extremely slow (for low drain-to-source voltages) or diverged (for higher drain-to-source voltages).

Keeping in mind that the current flow is mostly parallel to the source-to-drain direction, i.e. the direction of the x axis in our simulations, it was decided to use the projection of the electric field on the x axis as a driving force for the field-dependent mobility model

$$E_{dr} = |\vec{E} \cdot \vec{\imath}\,| = |E_x| \tag{3.59}$$

where $\vec{\imath}$ is the unit vector in the direction of the x axis and E_x is the x component of the electric field $\vec{E}$. Although this approach is physically less sound than the projection of the electric field on the direction of the current flow, it has proved to be robust in terms of convergence problems, and it also resulted in increased current levels, as had been expected. Furthermore, the physicality of our assumption can be easily checked by inspecting vector plots of the electric field and electron current, Figs. 3.7 and 3.8 respectively. Note that the current flow is mainly parallel to the x axis.

Fig. 3.9 shows the results obtained using the mobility model dependent on $|E_x|$ (the $\mu(|E_x|)$ model), the mobility model dependent on $|\vec{E}|$ (the $\mu(|\vec{E}|)$ model), and experimental data. Note that for $V_{GS} = 0.3$ V the drain currents calculated by the aforementioned models are only slightly different, indicating that the built-in field perpendicular to the electron current flow is relatively small. For $V_{GS} = 0.5$ and 0.7 V the difference in I_D is much higher, as expected.

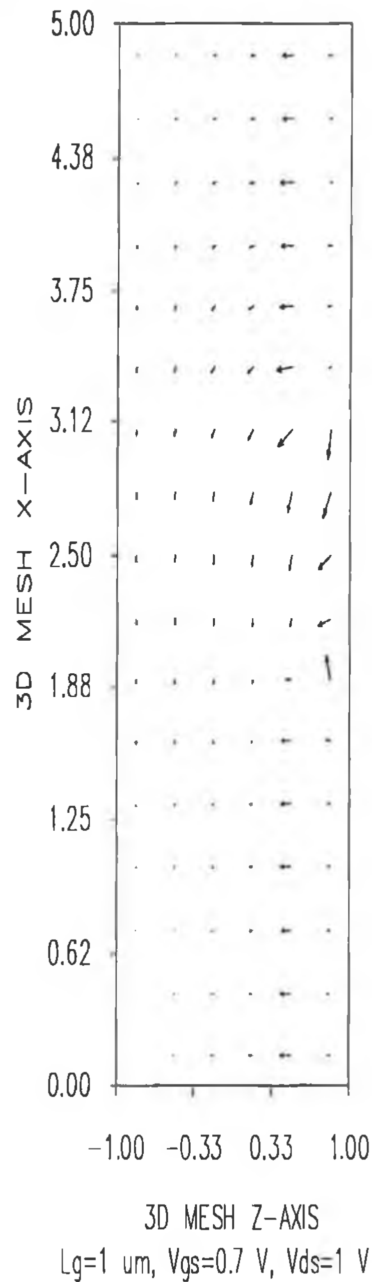

Figure 3.7: Vector plot of the electric field at V_{GS} = 0.7 V and V_{DS} = 1 V for the 1 μm gate-length ion-implanted MESFET. Contacts are deposited on the $x - y$ surface at $z = 1$ μm with the source metal going from x=0 to x=0.5 μm, the gate metal going from x=2 μm to x=3 μm, and the drain metal going from x=4.5 μm to x=5 μm.

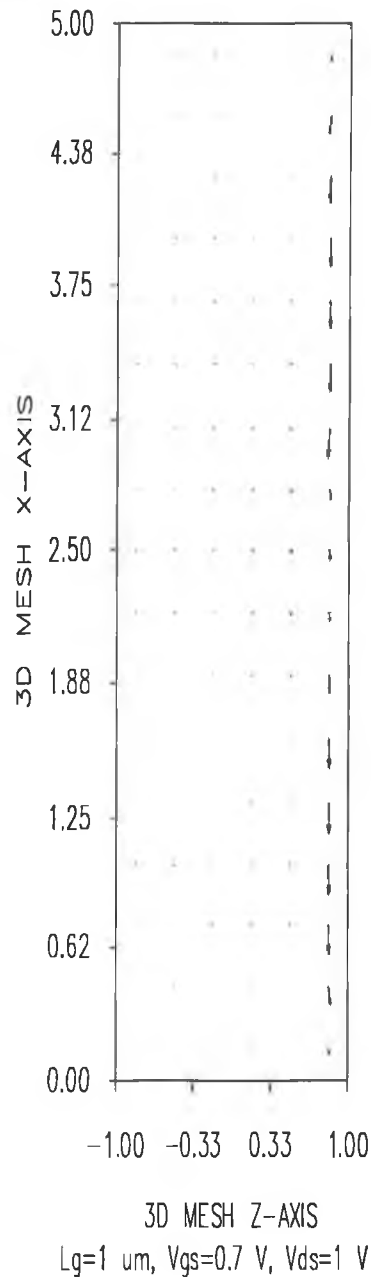

Figure 3.8: Vector plot of the electron current at $V_{GS} = 0.7$ V and $V_{DS} = 1$ V for the 1 μm gate-length ion-implanted MESFET. Contacts are deposited on the $x - y$ surface at $z = 1$ μm with the source metal going from x=0 to x=0.5 μm, the gate metal going from x=2 μm to x=3 μm, and the drain metal going from x=4.5 μm to x=5 μm.

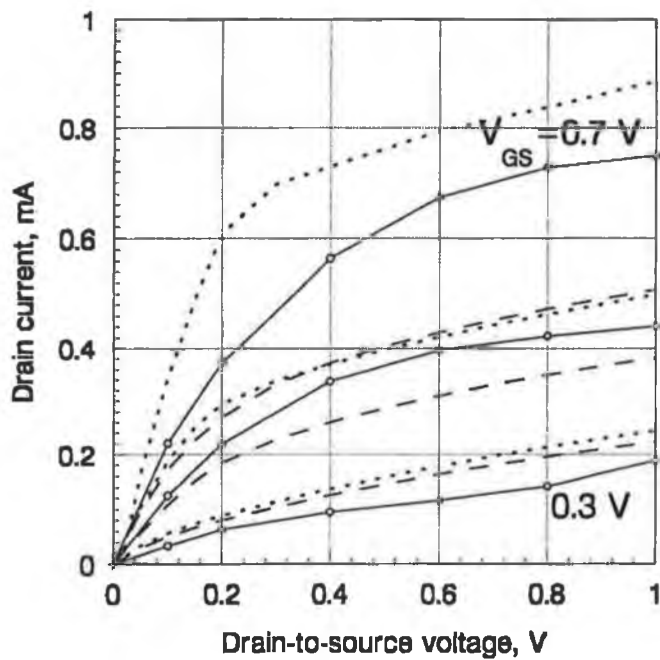

Figure 3.9: Drain currents for the 1 μm gate-length ion-implanted MESFET. The experimental data (full line) and results calculated by the $\mu(|E_x|)$ model (dotted line) for $V_{GS} = 0.7$, 0.5 and 0.3 V are shown (results calculated by the $\mu(|\vec{E}|)$ model (dashed line) are also given for comparison).

	μ_n^0 (cm^2/V·s)	v_{sat} (cm/s)	E_{cr} (kV/cm)
Hirose	μ_n^I	0.8·10^7	4.3
Set I	5500	0.8·10^7	4.3
Set II	4000	0.7·10^7	10.0
Yamasaki	2800	2.3·10^7	8.2

Table 3.2: Mobility parameters for four different mobility models.

As the drain current for $V_{GS} = 0.7$V was higher than the experimental one, instead of using the impurity-dependent mobility value μ_n^I for the low-field mobility in the field-dependent mobility model, we introduced a constant low-field mobility μ_n^0

$$\mu_n^E = \frac{\mu_n^0 + v_{sat}\dfrac{E_{dr}^3}{E_{cr}^4}}{1 + \dfrac{E_{dr}^4}{E_{cr}^4}}. \tag{3.60}$$

In order to see whether it is possible to obtain better agreement with experimental data we have performed several more simulations, varying the parameters μ_n^0, v_{sat} and E_{cr} in the model (3.60). Two sets of parameters give a good agreement with the experimental data

- Set I: $\mu_n^0 = 5500$ cm^2/V·s, $v_{sat} = 0.8 \cdot 10^7$ cm/s, $E_{cr} = 4.3$ kV/cm;
- Set II: $\mu_n^0 = 4000$ cm^2/V·s, $v_{sat} = 0.7 \cdot 10^7$ cm/s, $E_{cr} = 10$ kV/cm.

The results for these two sets are shown in Fig. 3.10 and the corresponding electron velocity curves are presented in Fig. 3.11. It is interesting to note that relatively high difference in the electron velocity characteristics results in relatively small difference in the drain currents.

3.4.1 Discussion on electron velocity models

It has been already mentioned in the previous section that the use of radically differing electron velocity characteristics resulted in a not so pronounced difference in the drain current curves for the 1 μm gate-length ion-implanted MESFET. Here we would like to elaborate further on this topic.

In Table 3.2 mobility parameters are given for the mobility models that are going to be discussed.

Hirose *et al.* [36] use the impurity-dependent low-field mobility and obtain an agreement with experimental data similar to the agreement achieved here

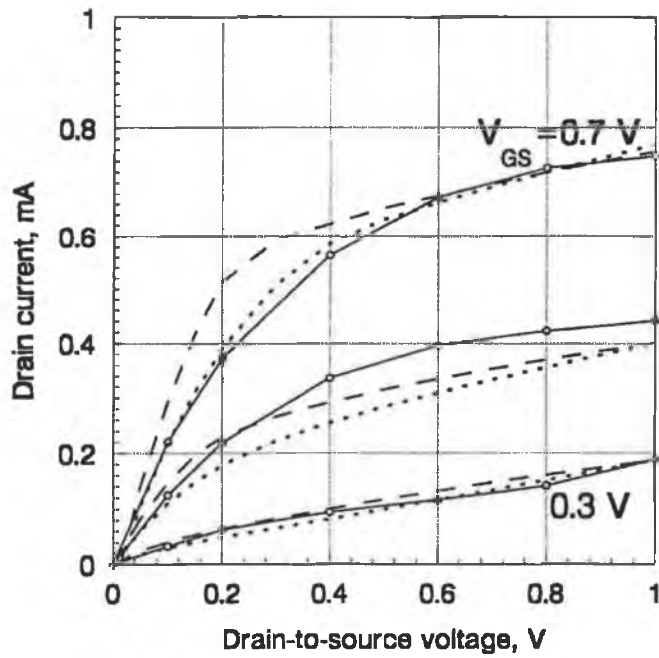

Figure 3.10: Drain currents for the 1 μm gate-length ion-implanted MESFET. The experimental data (full line), results calculated by the Set I (dashed line) and Set II (dotted line) mobility parameters for $V_{GS} = 0.7$, 0.5 and 0.3 V. The corresponding electron velocity curves are given in Fig. 3.11.

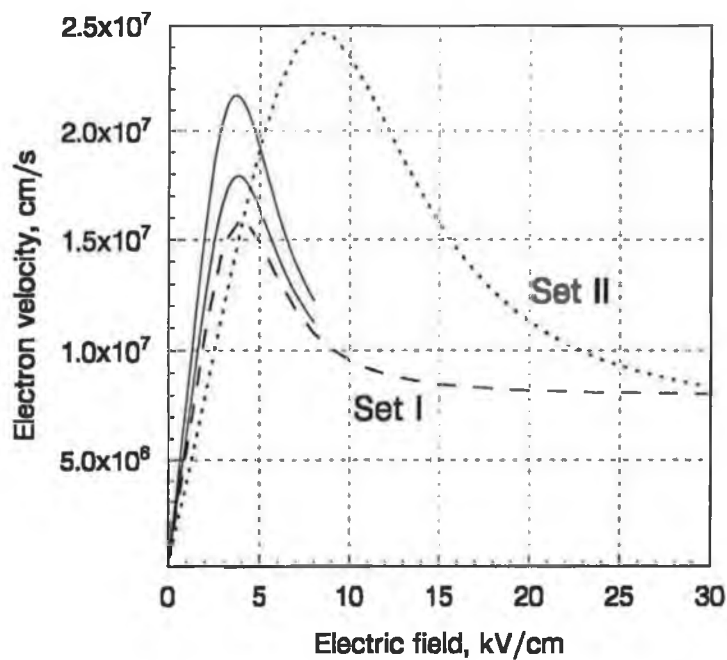

Figure 3.11: Electron velocity v_n as a function of the electric field for two different doping concentrations (full line: $N_D = 10^{13}$ and 10^{17} cm^{-3}), for Set I parameters (dashed line: $\mu_n^0 = 5500$ cm^2/V·s, $v_{sat} = 0.8 \cdot 10^7$ cm/s, $E_{cr} = 4.3$ kV/cm), and for Set II parameters (dotted line: $\mu_n^0 = 4000$ cm^2/V·s, $v_{sat} = 0.7 \cdot 10^7$ cm/s, $E_{cr} = 10$ kV/cm).

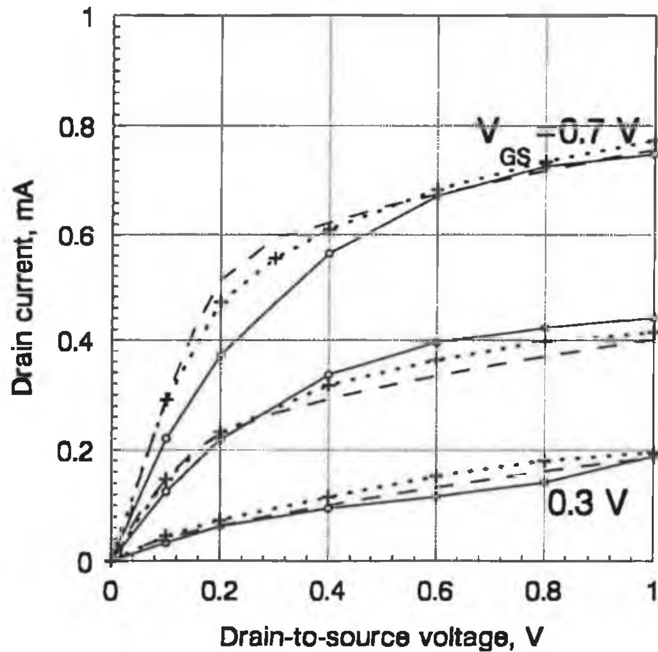

Figure 3.12: Drain currents for the 1 μm gate-length ion-implanted MESFET. The experimental data by Hirose *et al.* (full line), results calculated by Hirose *et al.* (dotted line), results calculated by the Set I mobility parameters (dashed line) for $V_{GS} = 0.7$, 0.5 and 0.3 V.

using the Set I parameters (see Fig. 3.12), the only difference being the low-field mobility parameter. The reason $\mu_n^0 = 5500$ cm^2/V·s is used may be due to the fact that Hirose *et al.* successfully implemented the mobility model dependent on the projection of the electric field on the gradient of the electron quasi-Fermi level, while this work deals with the projection of the electric field on the unit vector of the x axis.

When using substantially different electron velocity characteristic (Set II parameters - see Fig. 3.11), the resulting changes of the drain current are comparatively very small.

The question of what should be the preferred choice of mobility parameters for GaAs MESFET simulations is even more difficult to answer when we take into account the work by Yamasaki and Hirayama [67]. The velocity vs. electric field curve resulting from their set of parameters (see Table 3.2) is shown in Fig. 3.13. Note a much higher saturation velocity and practically no overshoot of the electron velocity around the critical electric field. Using this set of parameters they obtained very good agreement not only for a 1 μm

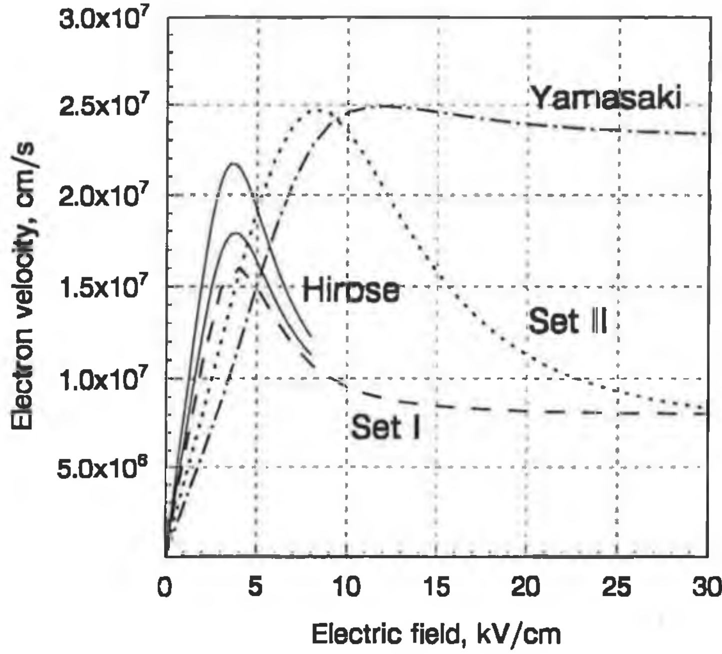

Figure 3.13: Electron velocity v_n as a function of the electric field for two different doping concentrations as given by Hirose *et al.* (full line: $N_D = 10^{13}$ and 10^{17} cm^{-3}), for Set I parameters (dashed line), for Set II parameters (dotted line), and Yamasaki and Hirayama parameters (dash-dot line).

gate-length ion-implanted MESFET, but also for 0.53 and 0.32 μm gate-length MESFETs. It is even more important to mention that they used the magnitude of the electric field as the driving force for the field-dependent mobility model, i.e. no projection of the electric field.

Finally, a mention must be made of Feng's work [68]. He developed a new electron velocity relationship of GaAs in which the nonequilibrium transport effects were included. The electron mobility relation

$$\mu = \frac{\mu_n^0 + v_0 \frac{E^4}{E_{cr}^5}}{1 + m \frac{E^5}{E_{cr}^5}}. \tag{3.61}$$

uses parameters μ_n^0, v_0, E_{cr} and m that depend on the gate length. The parameters obtained by fitting results of Monte Carlo particle simulations are listed in Table 3.3.

Feng's model has been used by Fardi and Hayes [69] to obtain very good agreement with results of Monte Carlo simulation for a 0.2 μm gate-length

L_g (μm)	0.2	0.4	0.6	0.8	1.0
E_{cr} (kV/cm)	11.5	7.0	5.6	4.7	4.0
m	0.48	0.57	0.71	0.77	0.85

Table 3.3: Gate-length dependent parameters for Feng's mobility model [68] ($\mu_0 = 6200$ cm^2/V·s, $v_0 = 1 \cdot 10^7$ cm/s).

MESFET. They also obtained a good agreement with the experimental results for 0.32 μm gate-length MESFET given by Yamasaki and Hirayama [67] with slightly modified mobility parameters, i.e. they used $E_{cr} = 11$ kV/cm and $m = 0.55$.

Fig. 3.14 shows the velocity curve used by Yamasaki and Hirayama for simulation of 1 μm to 0.32 μm gate-length MESFETs, Feng's model for 1 μm gate-length MESFET, and the model used by Fardi and Hayes for the simulation of Yamasaki's 0.32 μm gate-length MESFET. Note quite a substantial difference in electron velocity curves used by Yamasaki and Hirayama, on the one hand, and Fardi and Hayes, on the other hand, to represent the same experimental results.

This discussion clearly shows that the simulation of micrometer and submicrometer GaAs MESFETs may be regarded as an art with well-defined scientific background wherein the choice of proper parameters needs to be made under three main restrictions: 1) physicality of the model, 2) agreement with experimental data, and 3) numerical convergence.

3.5 MESFET simulations

We have simulated ion-implanted and epitaxial MESFETs with different gate lengths (2 μm, 1 μm, 0.7 μm and 0.5 μm). Although EVEREST is a 3D device simulator and MESFETs have been defined as 3D objects, all simulations are effectively two-dimensional because the device structure is bounded by two planes 1 μm apart in the y direction and no nodes have been defined between these two planes in the y direction. In all cases recombination has been neglected[1] and only DC analysis has been performed. When considering the mobility models, a rather conservative approach has been adopted, i.e. the impurity-dependent low-field mobility (3.54) and the mobility dependent on the magnitude of the electric field have been used in all simulations.

[1]Simulations of p-n diodes performed with Shockley-Read-Hall and Auger recombination mechanisms taken into account demonstrated negligible impact of these mechanisms.

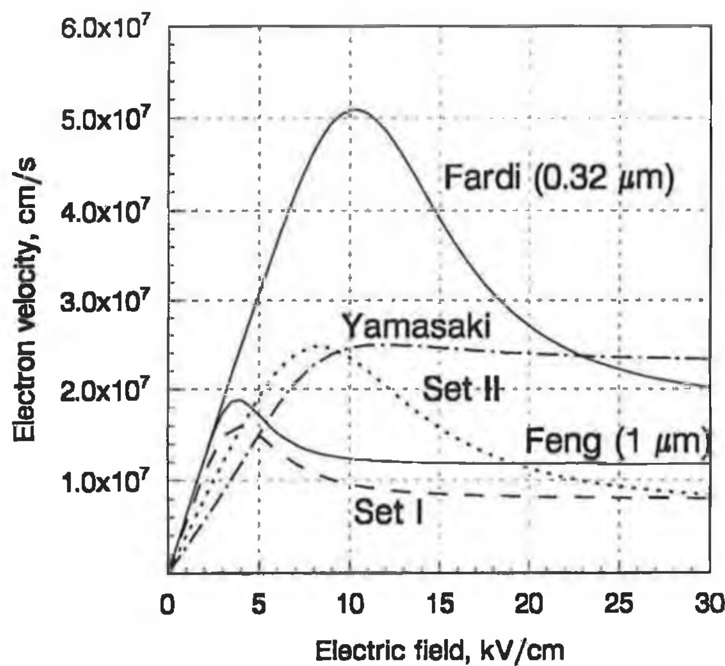

Figure 3.14: Electron velocity v_n as a function of the electric field for Yamasaki and Hirayama parameters (dash-dot line), Fardi and Hayes parameters (full line) and Feng's parameters (full line). Velocity curves for Set I parameters (dashed line) and Set II parameters (dotted line) are also shown for comparison. Note that Yamasaki and Hirayama used the same velocity characteristic for the simulation of MESFETs in the gate-length range from 1 μm to 0.32 μm.

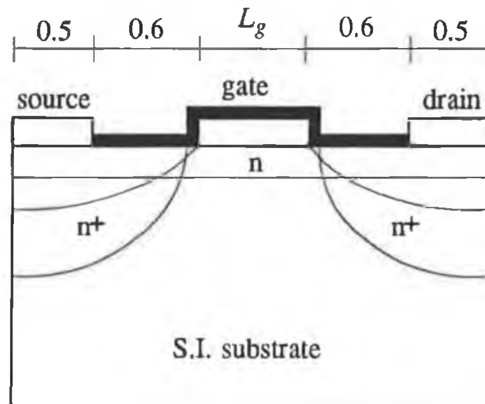

Figure 3.15: Schematic structure of an ion-implanted MESFET (all dimensions in microns). The width is 100 μm. The gate electrode is covered by a dielectric layer that is used to space off the deeper ohmic contact implant.

Although the comparison with experimental results for an ion-implanted MESFET suggests that different low-field mobility values and especially the electric field projected on the x axis, used as a driving force for the field-dependent mobility model, can improve accuracy of simulations, the discussion on electron velocity characteristics shows on the other hand that the best choice of mobility parameters can not be made only on the basis of known gate lengths. Thus, accepting the fact that we certainly introduce inaccurate device parameters in our simulations, we do it consistently assuming that there is no serious violation of the physical background of the simulations.

3.5.1 Ion-implanted MESFETs

Fig. 3.15 shows a schematic structure of an ion-implanted MESFET. All dimensions stay the same for all simulations except the gate length which varies, i.e. L_g = 2, 1, 0.7 and 0.5 μm. In contrast to the MESFET used for verification of the simulation procedure, two ion-implantations are performed to dope the ohmic contact regions. A third ion-implantation is used to dope a channel region. Ion-implantation parameters are given in Table 3.4. The Schottky barrier height is $\Phi_B = 0.95$ V.

Two different values for the background doping have been used, $N_A = 5 \cdot 10^{13}$ and $5 \cdot 10^{15}$ cm^{-3}. Four simulations (one for each gate length) performed with $N_A = 5 \cdot 10^{13}$ cm^{-3} are labelled 'ION', and the other four performed with $N_A = 5 \cdot 10^{15}$ cm^{-3} are labelled 'ION-P'.

n-channel implant:	
N_{dose}	$6 \cdot 10^{12}$ cm^{-2}
R_p	0.0424 μm
ΔR_p	0.0254 μm
$\Delta R_{p,lat}$	0.0343 μm
shallow n^+ contact implant:	
N_{dose}	$4 \cdot 10^{12}$ cm^{-2}
R_p	0.0262 μm
ΔR_p	0.0170 μm
$\Delta R_{p,lat}$	0.0226 μm
deep n^+ contact implant:	
N_{dose}	$1 \cdot 10^{13}$ cm^{-2}
R_p	0.0507 μm
ΔR_p	0.0294 μm
$\Delta R_{p,lat}$	0.0399 μm

Table 3.4: Parameters of donor impurity profiles for ION and ION-P simulations. For all three ion-implantations 50% post-implant annealing efficiency has been assumed. The deep n^+ contact implantation is performed through the 600 Å thick dielectric layer. This layer is also used to space off the deep contact implant from the gate.

Fig. 3.16 shows the transfer characteristics $I_D = \mathrm{f}(V_{GS})$ at $V_{DS} = 1$ V for all eight simulations. It can be seen that the four rightmost characteristics, obtained with the background doping $N_A = 5 \cdot 10^{15}$ cm^{-3}, show more efficient switch-off behaviour, which is due to better confinement of electrons within the active channel region. The confinement of electrons and its consequences on the accuracy of simulations will be addressed later in this chapter.

To be able to quantify the behaviour of a MESFET for low drain currents definitions for the threshold voltage and the subthreshold current slope are introduced as follows. The threshold voltage V_{th} is defined as the gate-to-source voltage V_{GS} for which the drain current I_D is 1 μA at $V_{DS} = 1$ V

$$V_{th} = V_{GS}\Big|_{I_D = 1\ \mu\mathrm{A\ at}\ V_{DS} = 1\ \mathrm{V}} \tag{3.62}$$

In order to measure the rate of current change around the threshold voltage, the subthreshold current slope STS is defined as the change of the gate-to-source voltage that produces a current change of one decade at $V_{GS} = V_{th}$ and

$V_{DS} = 1$ V

$$STS = \Delta V_{GS}\Big|_{\text{for 1 decade of } I_D \text{ change at } V_{GS}=V_{th} \text{ and } V_{DS}=1\text{ V}} \tag{3.63}$$

The subthreshold current slope is measured in V/decade.

Fig. 3.17 shows the threshold voltages for all eight simulations. The figure demonstrates the well-known decrease of the threshold voltage when the gate length is decreased [16, 19, 20]. The reason for that is related to the substrate doping. Firstly, when the drain currents of the ION and ION-P simulations are compared, it can be noticed that at the same V_{GS} the drain currents are higher for the simulations wherein the lower substrate doping has been used, i.e. the ION simulations, because lower substrate doping shows less resistance to the penetration of electrons into the substrate. The same line of reasoning leads to the conclusion that the effective resistance of the electron path through the substrate has to decrease when the gate length is decreased as the length of an effective substrate resistor is decreased. Consequently, the drain current increases for the same bias and also, the threshold voltage shifts towards more negative values.

Fig. 3.16 shows not only that the values of the threshold voltages are more uniform for varying gate lengths, but also that the subthreshold current slope is higher, which means that the MESFET can be turned on/off by smaller change of the gate-to-source voltage.

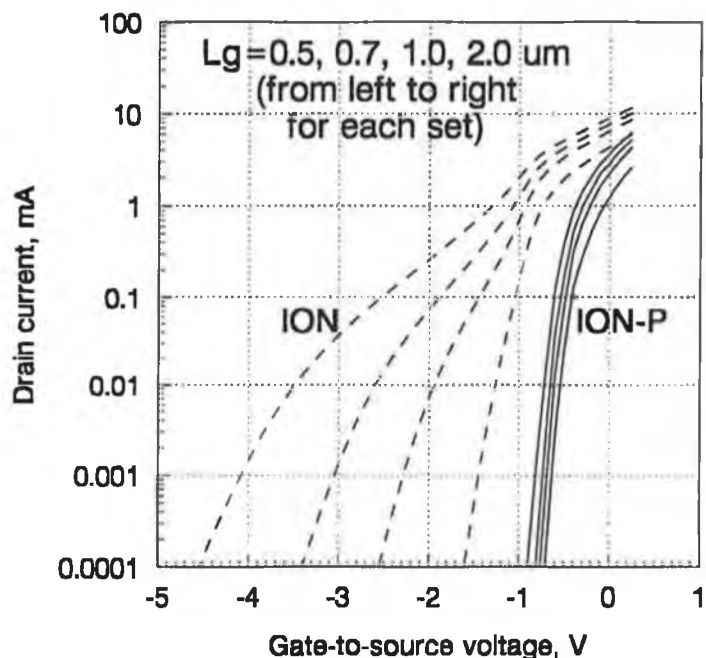

Figure 3.16: Transfer characteristics for V_{DS} = 1 V. The ION simulations have been performed with $N_A = 5 \cdot 10^{13}$ cm^{-3} (dashed line) and the ION-P simulations with $5 \cdot 10^{15}$cm^{-3} (full line).

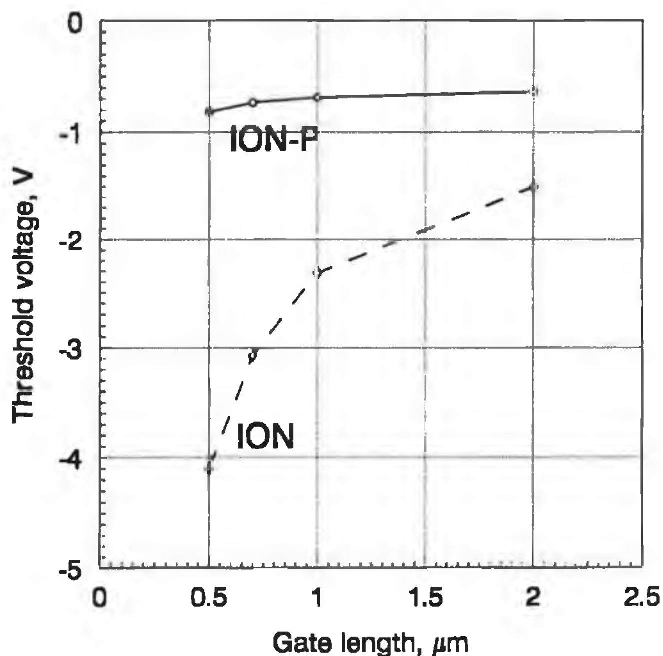

Figure 3.17: Dependence of the threshold voltage on the gate length for the ION simulations (dashed line: $N_A = 5 \cdot 10^{13}$ cm^{-3}) and ION-P simulations (full line: $N_A = 5 \cdot 10^{15}$cm^{-3}).

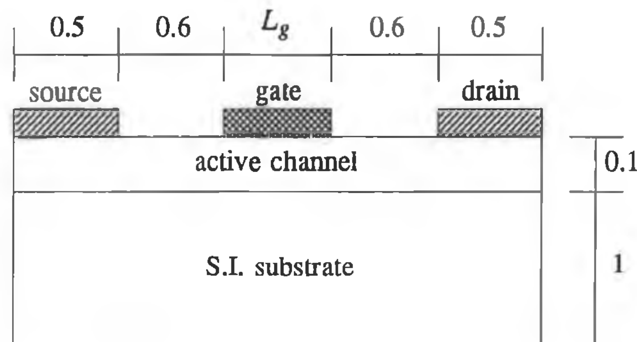

Figure 3.18: Schematic structure of an epitaxial MESFET (all dimensions in microns). The width is 250μm.

3.5.2 Epitaxial MESFETs

The structure of an epitaxial MESFET is shown in Fig. 3.18. All dimensions stay the same except the gate length which varies, i.e. L_g = 2, 1, 0.7 and 0.5 μm. The donor concentration of the active channel is $N_D = 2.3 \cdot 10^{17}$ cm^{-3}. Two different values for the background doping have been used, $N_A = 5 \cdot 10^{13}$ and $5 \cdot 10^{15}$ cm^{-3}. Four simulations (one for each gate length) performed with $N_A = 5 \cdot 10^{13}$ cm^{-3} are labelled 'EPI', and the other four performed with $N_A = 5 \cdot 10^{15}$ cm^{-3} are labelled 'EPI-P'. The Schottky barrier height is $\Phi_B = 0.95$ V.

Fig. 3.19 shows the transfer characteristics $I_D = f(V_{GS})$ at $V_{DS} = 1$ V for all eight simulations. As in the case of ion-implanted MESFETs, the switch-off mechanism of the EPI-P MESFETs is better due to higher p-type background doping, which impedes electron penetration deep into the substrate. This topic will be tackled again in the next section.

The threshold voltage dependence on the gate length is depicted in Fig. 3.20 for both sets of epitaxial MESFETs.

3.6 Discussion

In this section we are going to address the accuracy of our simulations and the consequences of using lightly and highly doped GaAs substrates.

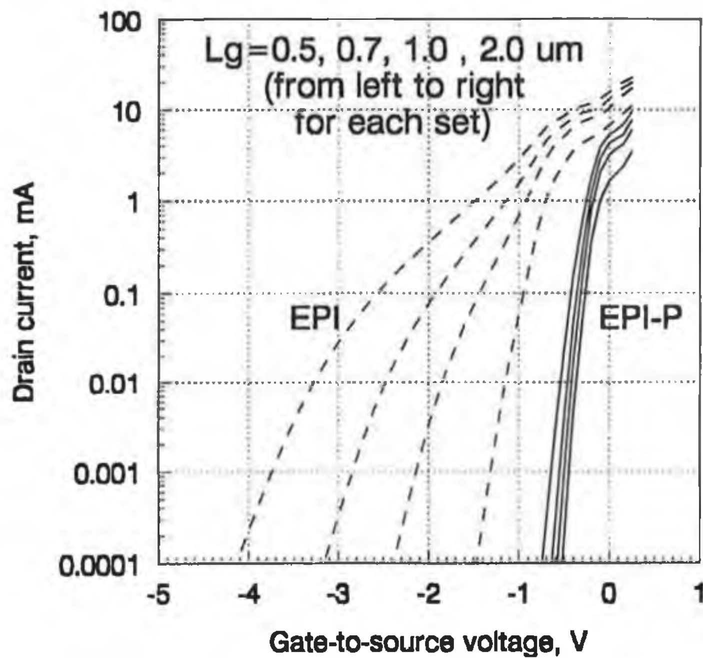

Figure 3.19: Transfer characteristics for $V_{DS} = 1$ V. The EPI simulations have been performed with $N_A = 5 \cdot 10^{13}$ cm^{-3} (dashed line) and the EPI-P simulations with $5 \cdot 10^{15}$cm^{-3} (full line).

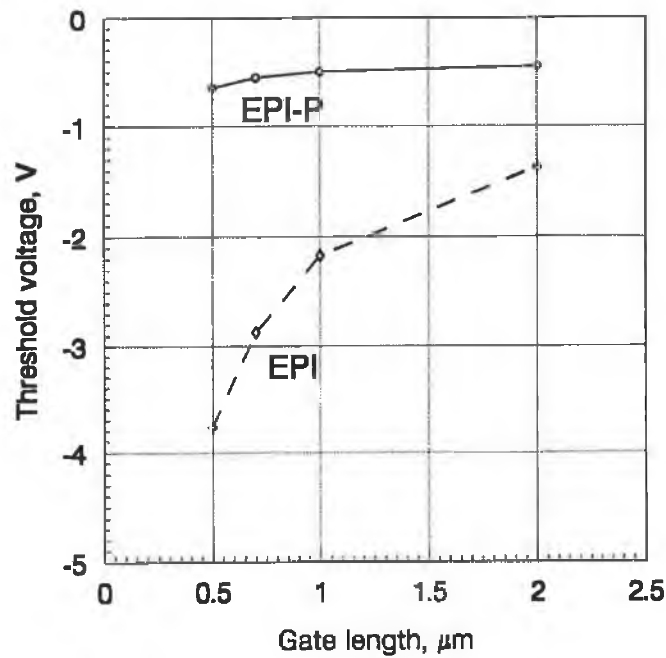

Figure 3.20: Dependence of the threshold voltage on the gate length for the EPI simulations (dashed line: $N_A = 5 \cdot 10^{13}$ cm^{-3}) and EPI-P simulations (full line: $N_A = 5 \cdot 10^{15}$cm^{-3}).

3.6.1 Accuracy of EPI and ION simulations

It has been already mentioned that at the non-contact boundaries the Neumann boundary conditions are automatically forced by the solution process. As the Neumann boundary conditions state that no current flows out of the semiconductor at non-contact boundaries, the simulation structure has to be large enough to allow electron current to vanish near non-contact boundaries.

Figures 3.21, 3.22 and 3.23 show the drain current distribution for $V_{GS} = -1$, -1.4 and -1.6 V, respectively, for the 0.7 μm gate-length epitaxial MESFET with the background doping $N_A = 5 \cdot 10^{13}$ cm^{-3}. It can be clearly seen how the electron current is being pushed into the substrate as a result of decreased gate-to-source voltage. While the current for $V_{GS} = -1.4$ V is still relatively well confined within the simulated region (see Fig. 3.22), in the case of $V_{GS} = -1.6$ V a part of the electron current that penetrates up to the $z = -0.5$ μm boundary of the simulated structure becomes more pronounced (see Fig. 3.23). Thus, it appears that the current swithes off because the simulated region is not large enough. The Neumann boundary conditions, although forced by the solution process, are not physically satisfied.

We conclude that EPI and ION simulations are accurate for the drain currents $I_D \geq 0.5$ mA. That was also confirmed by inspecting current densities for L_g up to 2 μm for both ION and EPI simulations. It is necessary to state that the current boundary of 0.5 mA is very strict in the sense that even ten times lower currents would not substantially differ from the currents that would have beeen obtained by the simulation over an enlarged simulation region.

The reduction of current due to too small simulation region expresses itself as an increase of the current slope for currents below 0.5 mA (see the transfer characteristics for the ION and EPI simulations in Figs. 3.16 and 3.19, respectively). It may be supposed that an acceptable approximation for the drain current for $I_D < 0.5$ mA and the corresponding threshold voltage can be obtained by extrapolating the current by the line that passes through the point $I_D = 0.5$ mA and has the same inclination as the calculated current at this point.

3.6.2 Accuracy of EPI-P and ION-P simulations

We have seen that the background doping $N_A = 5 \cdot 10^{13}$ cm^{-3} used in ION and EPI simulations does not provide confinement good enough for the electron current to vanish near non-contact boundaries at low currents.

Fig. 3.24 shows the current distribution at $I_D = 5$ μA for the 0.7 μm EPI MESFET. This current is 100 times smaller than the current for which the simulation is still valid.

The current distribution at $I_D = 5$ μA for the 0.7 μm EPI-P MESFET (Fig. 3.25) shows very good confinement in the near-threshold regime.

Thus, we conclude that the EPI-P and ION-P simulations are accurate from the point of view that natural boundary conditions at non-contact nodes are satisfied.

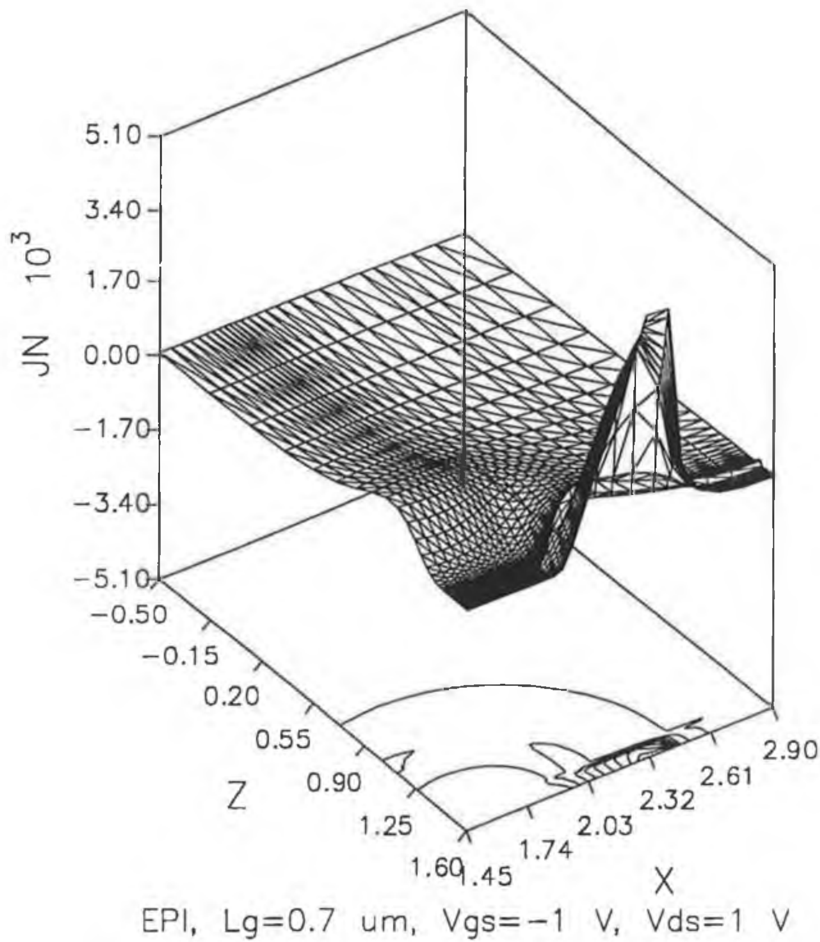

Figure 3.21: Electron current density distribution (in A/cm^2) at $V_{GS} = -1$ V and $V_{DS} = 1$ V ($I_D = 1.56$ mA) for the 0.7 μm gate-length epitaxial MESFET. Only one half of the drain side of the MESFET is shown to allow better insight into the current levels at the middle of the MESFET structure (contacts are deposited on the $x - y$ surface at $z = 1.6$ μm with the drain-half of the gate metal going from x=1.45 μm to x=1.8 μm, and the drain metal going from x=2.4 μm to x=2.9 μm). Compare this figure with the current densities for $V_{GS} = -1.4$ V shown in Fig. 3.22 and the current densities for $V_{GS} = -1.6$ V shown in Fig. 3.23.

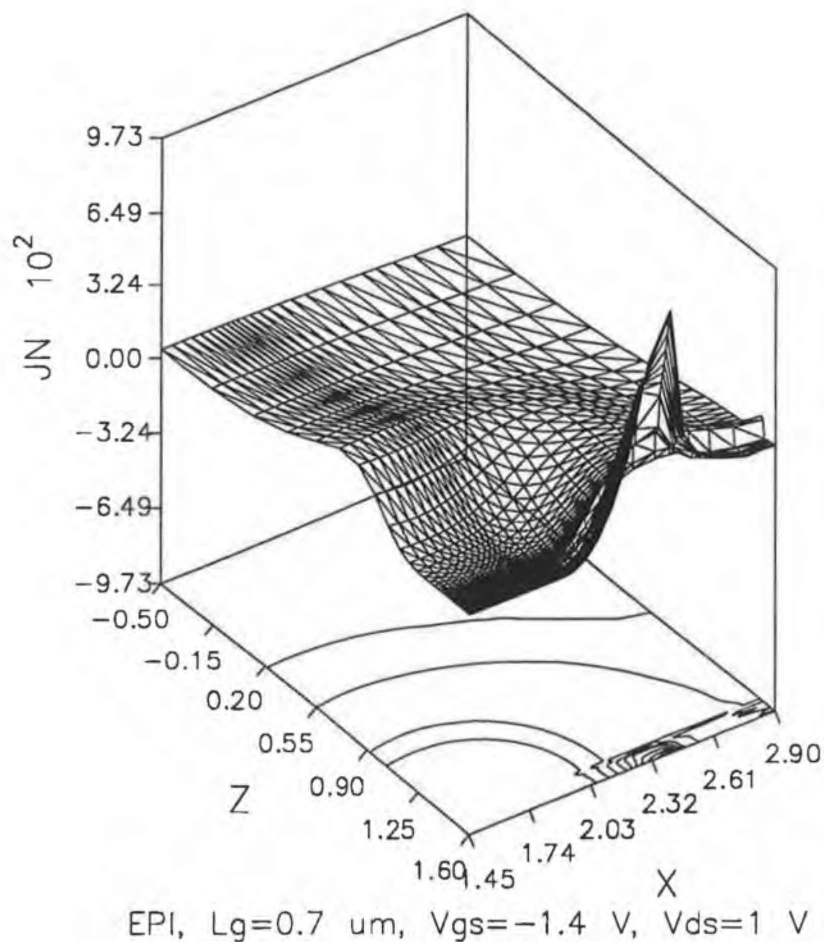

Figure 3.22: Electron current density distribution (in A/cm^2) at $V_{GS} = -1.4$ V and $V_{DS} = 1$ V ($I_D = 0.48$ mA) for the 0.7 μm gate-length epitaxial MESFET (see caption of Fig. 3.21).

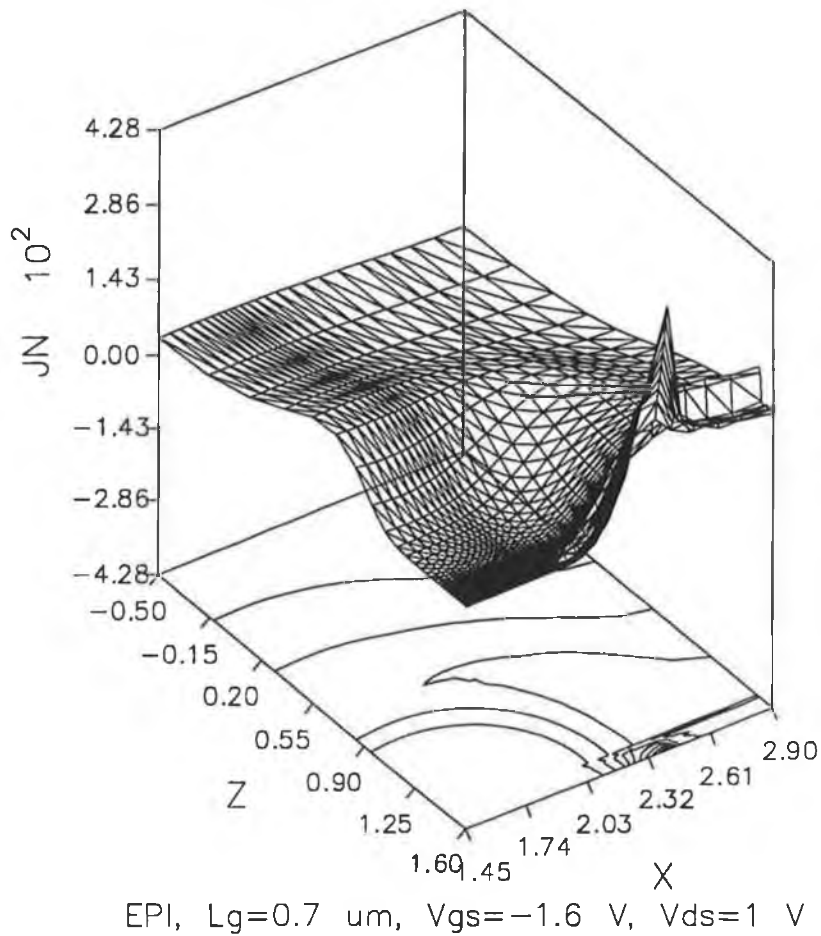

Figure 3.23: Electron current density distribution (in A/cm^2) at $V_{GS} = -1.6$ V and $V_{DS} = 1$ V ($I_D = 0.27$ mA) for the 0.7 μm gate-length epitaxial MESFET (see caption of Fig. 3.21).

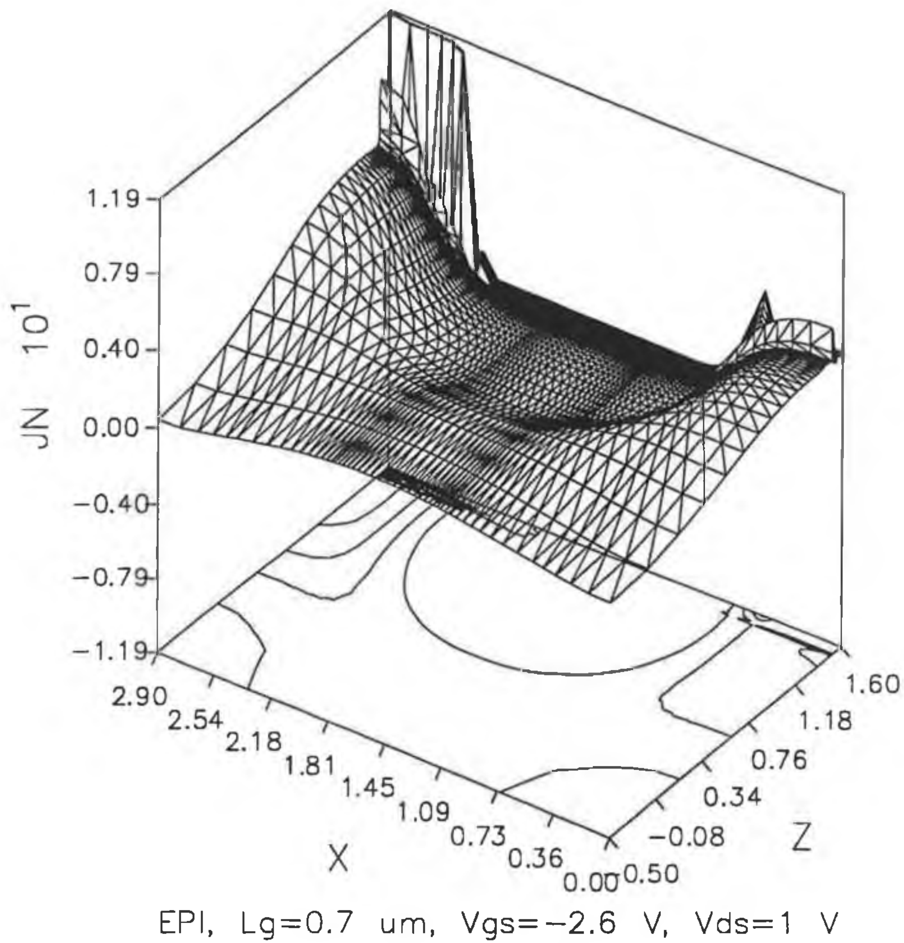

Figure 3.24: Electron current density distribution (in A/cm^2) at $I_D = 5$ μA ($V_{GS} = -2.6$ V, $V_{DS} = 1$ V) for the 0.7 μm gate-length EPI MESFET. High levels of current density at non-contact boundaries indicate that the Neumann boundary conditions are violated (contacts are deposited on the $x - y$ surface at $z = 1.6$ μm with the source metal going from x=0 μm to x=0.5 μm, the gate metal going from x=1.1 μm to x=1.8 μm, and the drain metal going from x=2.4 μm to x=2.9 μm).

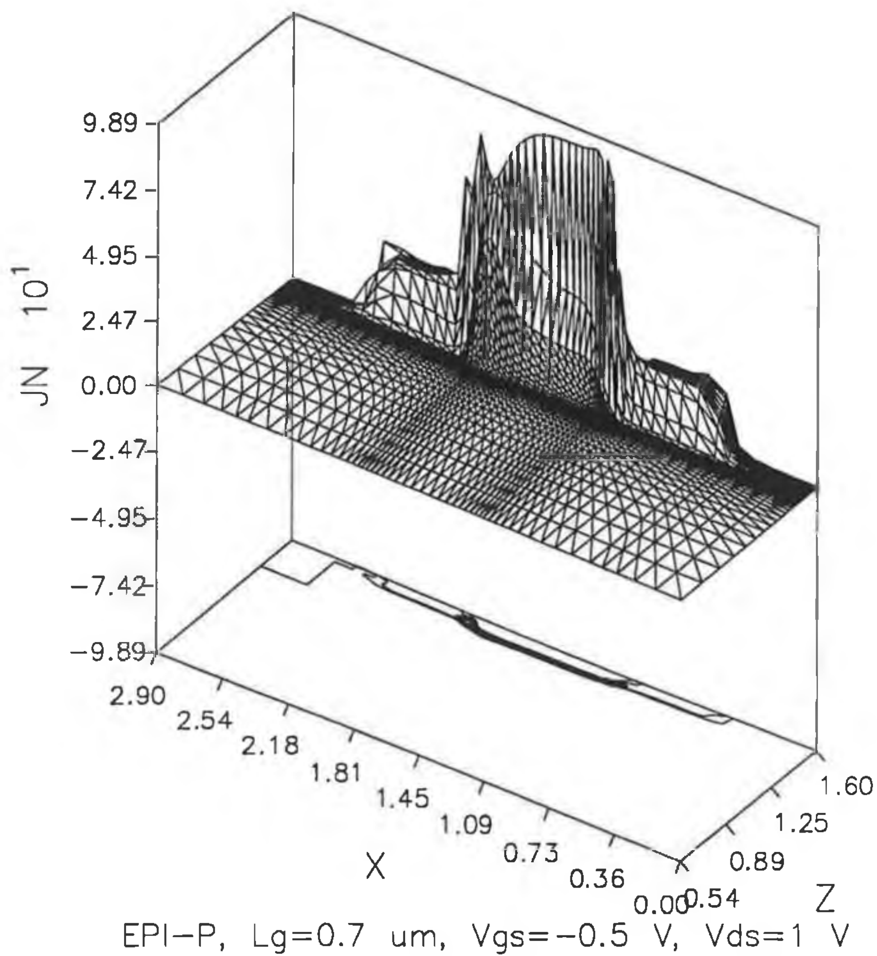

Figure 3.25: Electron current density distribution (in A/cm^2) at $I_D = 5\ \mu$A ($V_{GS} = -0.5$ V, $V_{DS} = 1$ V) for the 0.7 μm gate-length EPI-P MESFET. The electron current is well confined within the simulated structure (contacts are deposited on the $x-y$ surface at $z = 1.6\ \mu$m with the source metal going from x=0 μm to x=0.5 μm, the gate metal going from x=1.1 μm to x=1.8 μm, and the drain metal going from x=2.4 μm to x=2.9 μm).

Chapter 4

Stress and piezoelectric charge in GaAs MESFETs

The main objective of this work is to investigate the influence of stress induced piezoelectric charge on the performance of GaAs MESFETs. It is well known that different technological processes induce stresses in the semiconductor and it seems that the most pronounced effect is produced by dielectric overlayers [16]. Depending on the technique used for its preparation, the dielectric layer may be under significant stress. The stressed dielectric generally imparts a much lower stress to the underlying GaAs substrate, but the stress in the substrate is intensified locally in the vicinity of openings in the dielectric layer, such as the areas where the contacts are deposited. Due to the lack of centrosymmetry of the GaAs crystal lattice, GaAs is a piezoelectric material. Thus, the induced stress in the GaAs substrate gives rise to a piezoelectric charge that causes shifts in the MESFET electrical characteristics. The charge is especially high under the edges of the gate metal strip. It is also high under the source and drain metal edges, but the source and drain regions are highly doped and the final effect of the piezoelectric charge in these regions is of relatively minor importance to the electrical characteristics of MESFETs.

We shall first present a numerical approach to the derivation of the stress and piezoelectric charge. Later a simple analytical approach will be given and the results of the two methods will be compared.

4.1 Numerical approach

To calculate the equilibrium displacements, stresses and strains of a stressed MESFET structure we shall apply linear elasticity theory, assuming that all

introduced deformations are small enough for the theory to be valid. We shall also suppose that the GaAs crystal is elastically isotropic, although it is clear from the acoustic wave speeds in different crystallographic directions that GaAs is not perfectly isotropic [50]. Furthermore we assume that the width of the gate is much longer than its length (the length meaning the source-to-drain spacing, approximately), so that mechanical analysis can be performed in two dimensions.

4.1.1 Linear elasticity notation

Before the Finite Element Method (FEM) for calculation of stresses is presented it is necessary to introduce several important relations from linear elasticity theory [71]. The generalized Hooke's law expressed in matrix notation for the three-dimensional case

$$\boldsymbol{\sigma} = \boldsymbol{D}\boldsymbol{\varepsilon} \tag{4.1}$$

relates six components of the stress tensor $\boldsymbol{\sigma}$ with six components of the strain tensor $\boldsymbol{\varepsilon}$. For a homogeneous, isotropic and elastic material the number of independent elastic constants reduces to three

$$\begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{xz} \\ \sigma_{xy} \end{bmatrix} = \begin{bmatrix} d_{11} & d_{12} & d_{12} & 0 & 0 & 0 \\ d_{12} & d_{11} & d_{12} & 0 & 0 & 0 \\ d_{12} & d_{12} & d_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & d_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & d_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & d_{44} \end{bmatrix} \begin{bmatrix} \varepsilon_{x} \\ \varepsilon_{y} \\ \varepsilon_{z} \\ \gamma_{yz} \\ \gamma_{xz} \\ \gamma_{xy} \end{bmatrix}. \tag{4.2}$$

So, the compliance matrix $\boldsymbol{D}$ is symmetrical and has only three different components, namely

$$\boldsymbol{D} = \frac{E(1-\nu)}{(1+\nu)(1-2\nu)} \begin{bmatrix} 1 & \frac{\nu}{1-\nu} & \frac{\nu}{1-\nu} & 0 & 0 & 0 \\ \frac{\nu}{1-\nu} & 1 & \frac{\nu}{1-\nu} & 0 & 0 & 0 \\ \frac{\nu}{1-\nu} & \frac{\nu}{1-\nu} & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1-2\nu}{2(1-\nu)} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1-2\nu}{2(1-\nu)} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1-2\nu}{2(1-\nu)} \end{bmatrix} \tag{4.3}$$

where E is Young's modulus and ν is Poisson's ratio.

We can also express $\boldsymbol{\varepsilon}$ as

$$\boldsymbol{\varepsilon} = \boldsymbol{C\sigma} \tag{4.4}$$

where $\boldsymbol{C}$=$\boldsymbol{D}^{-1}$, i.e. the inverse matrix of the matrix $\boldsymbol{D}$. The matrix $\boldsymbol{C}$ has the same form as the matrix $\boldsymbol{D}$

$$\boldsymbol{C} = \frac{1}{E}\begin{bmatrix} 1 & -\nu & -\nu & 0 & 0 & 0 \\ -\nu & 1 & -\nu & 0 & 0 & 0 \\ -\nu & -\nu & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 2(1+\nu) & 0 & 0 \\ 0 & 0 & 0 & 0 & 2(1+\nu) & 0 \\ 0 & 0 & 0 & 0 & 0 & 2(1+\nu) \end{bmatrix}. \tag{4.5}$$

The components of the strain tensor can be obtained from

$$\begin{bmatrix} \varepsilon_x \\ \varepsilon_y \\ \varepsilon_z \\ \gamma_{yz} \\ \gamma_{xz} \\ \gamma_{xy} \end{bmatrix} = \begin{bmatrix} \partial u/\partial x \\ \partial v/\partial y \\ \partial w/\partial z \\ \partial v/\partial z + \partial w/\partial y \\ \partial u/\partial z + \partial w/\partial x \\ \partial u/\partial y + \partial v/\partial x \end{bmatrix} \tag{4.6}$$

where u, v and w are the components of the displacement in the x, y and z directions respectively.

In the case of a body that has one dimension longer than the other two dimensions and when the loading does not change along this direction, the three-dimensional problem may be reduced to the two-dimensional plane strain problem. If the coordinate system is chosen as in Fig. 4.1, i.e. the longest dimension is along the y axis (the positive y axis going into the paper), Hooke's law (4.2) can be rewritten as

$$\boldsymbol{\sigma} = \boldsymbol{D\varepsilon} \tag{4.7}$$

$$\begin{bmatrix} \sigma_{xx} \\ \sigma_{zz} \\ \sigma_{xz} \end{bmatrix} = \frac{E(1-\nu)}{(1+\nu)(1-2\nu)}\begin{bmatrix} 1 & \frac{\nu}{1-\nu} & 0 \\ \frac{\nu}{1-\nu} & 1 & 0 \\ 0 & 0 & \frac{1-2\nu}{2(1-\nu)} \end{bmatrix}\begin{bmatrix} \varepsilon_x \\ \varepsilon_z \\ \gamma_{xz} \end{bmatrix}. \tag{4.8}$$

Note that the shear strain components γ_{xy} and γ_{yz} are zero by definition as well as the normal strain component ε_y, but the normal stress component $\sigma_{yy} = \nu(\sigma_{xx} + \sigma_{zz})$ in order to satisfy the condition $\varepsilon_y = 0$. That can easily be checked by expressing $\boldsymbol{\varepsilon}$ in terms of $\boldsymbol{\sigma}$

$$\boldsymbol{\varepsilon} = \boldsymbol{C\sigma} \tag{4.9}$$

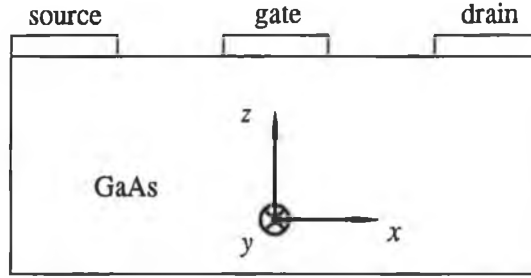

Figure 4.1: Schematic structure of a MESFET and the gate coordinate system (the y axis going into the paper).

$$\begin{bmatrix} \varepsilon_x \\ \varepsilon_y \\ \varepsilon_z \\ \gamma_{yz} \\ \gamma_{xz} \\ \gamma_{xy} \end{bmatrix} = \frac{1}{E} \begin{bmatrix} 1 & -\nu & -\nu & 0 & 0 & 0 \\ -\nu & 1 & -\nu & 0 & 0 & 0 \\ -\nu & -\nu & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 2(1+\nu) & 0 & 0 \\ 0 & 0 & 0 & 0 & 2(1+\nu) & 0 \\ 0 & 0 & 0 & 0 & 0 & 2(1+\nu) \end{bmatrix} \begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{xz} \\ \sigma_{xy} \end{bmatrix} \tag{4.10}$$

where $\boldsymbol{C}$ is written for the 3D problem. From (4.10) and $\gamma_{xy} = \gamma_{yz} = 0$, we can furthermore deduce that the shear stress components σ_{xy} and σ_{yz} are zero as well.

The strain-displacement relation (4.6) reduces to

$$\boldsymbol{\varepsilon} = \boldsymbol{L}\boldsymbol{u} \tag{4.11}$$

$$\begin{bmatrix} \varepsilon_x \\ \varepsilon_z \\ \gamma_{xz} \end{bmatrix} = \begin{bmatrix} \partial/\partial x & 0 \\ 0 & \partial/\partial z \\ \partial/\partial z & \partial/\partial x \end{bmatrix} \begin{bmatrix} u \\ w \end{bmatrix} \tag{4.12}$$

$$= \begin{bmatrix} \partial u/\partial x \\ \partial w/\partial z \\ \partial u/\partial z + \partial w/\partial x \end{bmatrix} \tag{4.13}$$

where $\boldsymbol{L}$ represents the differential operator

$$\boldsymbol{L} = \begin{bmatrix} \partial/\partial x & 0 \\ 0 & \partial/\partial z \\ \partial/\partial z & \partial/\partial x \end{bmatrix}. \tag{4.14}$$

4.1.2 Piezoelectric charge derivation

Suppose for the moment that the stress field in the GaAs substrate is known. To be able to model piezoelectric effects, which are known to be orientation

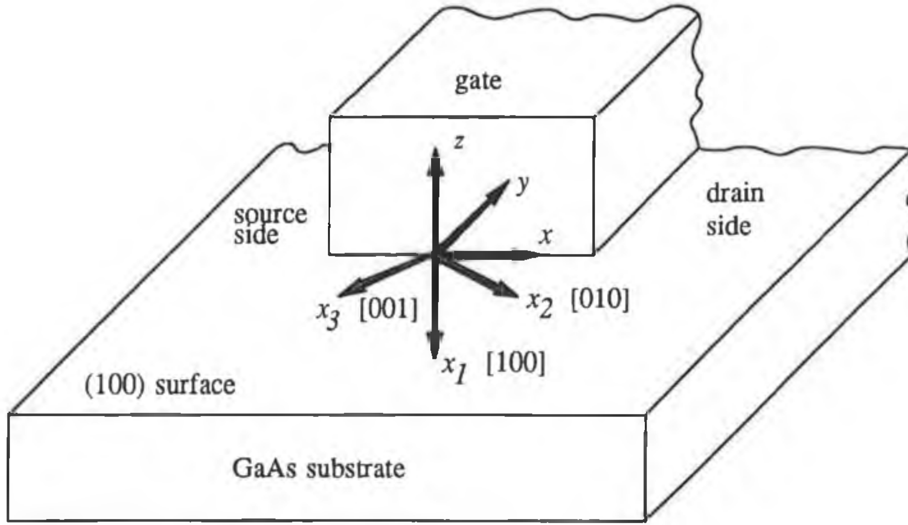

Figure 4.2: Gate (x,y,z) and crystallographic (x_1,x_2,x_3) coordinate systems. The gate is deposited on the (100) crystallographic surface. The axes x, y, x_2 and x_3 lie in the same plane. The axes z and x_1 are collinear, but they point in opposite directions.

dependent [15]-[24], it is necessary to introduce two coordinate systems and establish a suitable relation between them. Thus we shall use the gate coordinate system and the crystallographic coordinate system to model the stress in the GaAs substrate.

The gate coordinate system, shown in Fig. 4.1, is associated with the geometry of the device electrodes. The x axis extends along the source-to-drain direction, the z axis is perpendicular to the gate-substrate interface and the y axis is parallel to the "long" edges of the gate, with positive y being directed into the page. The solution for the stress field will be obtained with respect to this coordinate system.

The crystallographic coordinate system, depicted in Fig. 4.2, is used because the piezoelectric properties of GaAs are related to the crystallographic axes. This means that the stress field calculated in the gate coordinate system has to be transformed into the crystallographic coordinate system, and then the induced polarization can be determined. As the electrical characterization of a MESFET is performed in the gate coordinate system, the polarization vector has to be transformed back into the gate coordinate system, and finally the piezoelectric charge has to be deduced from the polarization vector.

The crystallographic axes x_1, x_2, and x_3 are associated with the main

directions of the unit cell [50]. The origin of the unit cell is taken to be at a group-III atom, i.e. the Ga atom. The As atom is situated at $(a_0/4, a_0/4, a_0/4)$, i.e. in the [111] direction[1], where a_0 represents the length of a side of the GaAs unit cell. The crystallographic x_1 axis is collinear with the gate z axis, but it points in the opposite direction. The axes x, y, x_2 and x_3 all lie in the same plane. The unit cell of the crystal is rotated about the x_1 axis through an angle α. The angle α is zero if the x and x_2 axes are coaxial. When the rotation is clockwise as viewed from the positive z axis, the angle is taken as positive. For an angle α equal to $\pi/4$ the source-to-drain direction or the x axis lies along the $[01\bar{1}]$ crystallographic direction and the long edges of the gate metal lie along the [011] direction; such a FET is called the [011] FET.

For the purpose of transformation from the gate to crystallographic coordinates, following the line of derivation of the piezoelectric charge in [22], the stress is given as a second rank tensor. In the gate coordinate system the stress tensor $[\boldsymbol{\sigma}]$ is

$$[\boldsymbol{\sigma}] = \begin{bmatrix} \sigma_{xx} & 0 & \sigma_{xz} \\ 0 & \sigma_{yy} & 0 \\ \sigma_{xz} & 0 & \sigma_{zz} \end{bmatrix} \tag{4.15}$$

where brackets in "$[\boldsymbol{\sigma}]$" denote the tensor representation of the stress; otherwise, we use the notation "$\boldsymbol{\sigma}$" without brackets when we mean the stress in vector form, as in (4.2). The stress components σ_{xy} and σ_{yz} have been omitted because they are proportional to the strain components γ_{xy} and γ_{yz} which are zero by definition of the plane strain problem. Note also that

$$\sigma_{yy} = \nu(\sigma_{xx} + \sigma_{zz}) \tag{4.16}$$

to satisfy the plane strain condition $\varepsilon_y = 0$.

The stress tensor $[\boldsymbol{\sigma}]$ transforms into the crystallographic stress tensor $[\boldsymbol{\sigma}^*]$ through

$$[\boldsymbol{\sigma}^*] = \boldsymbol{\beta}[\boldsymbol{\sigma}]\boldsymbol{\beta}^T \tag{4.17}$$

where $\boldsymbol{\beta}$ is the rotation matrix

$$\boldsymbol{\beta} = \begin{bmatrix} 0 & 0 & -1 \\ \cos\alpha & -\sin\alpha & 0 \\ -\sin\alpha & -\cos\alpha & 0 \end{bmatrix}. \tag{4.18}$$

[1]There are four equivalent < 111 > directions and the corresponding four equivalent {111} faces, i.e. the (111), $(1\bar{1}\bar{1})$, $(\bar{1}1\bar{1})$ and $(\bar{1}\bar{1}1)$ faces that consist of only Ga atoms and correspond to the directions of bonds that the Ga atom placed at the origin forms with the closest As atoms. The other four faces, namely the $(\bar{1}\bar{1}\bar{1})$, $(11\bar{1})$, $(1\bar{1}1)$ and $(\bar{1}11)$ contain only As atoms.

After multiplications in (4.17) we get the stress components in the crystallographic coordinate system expressed in terms of the stress components in the gate coordinate system σ_{xx}, σ_{zz} and σ_{xz}

$$[\sigma^*] = \begin{bmatrix} \sigma_{zz} & -\sigma_{xz}\cos\alpha & \sigma_{xz}\sin\alpha \\ -\sigma_{xz}\cos\alpha & \sigma_{xx}\cos^2\alpha + \sigma_{yy}\sin^2\alpha & (-\sigma_{xx}+\sigma_{yy})\sin\alpha\cos\alpha \\ \sigma_{xz}\sin\alpha & (-\sigma_{xx}+\sigma_{yy})\sin\alpha\cos\alpha & \sigma_{xx}\sin^2\alpha + \sigma_{yy}\cos^2\alpha \end{bmatrix} \tag{4.19}$$

which can also be written in vector form as

$$\sigma^* = \begin{bmatrix} \sigma_{11} \\ \sigma_{22} \\ \sigma_{33} \\ \sigma_{23} \\ \sigma_{13} \\ \sigma_{12} \end{bmatrix} = \begin{bmatrix} \sigma_{zz} \\ \sigma_{xx}\cos^2\alpha + \sigma_{yy}\sin^2\alpha \\ \sigma_{xx}\sin^2\alpha + \sigma_{yy}\cos^2\alpha \\ (-\sigma_{xx}+\sigma_{yy})\sin\alpha\cos\alpha \\ \sigma_{xz}\sin\alpha \\ -\sigma_{xz}\cos\alpha \end{bmatrix}. \tag{4.20}$$

The transformation from tensor to vector notation has been done by keeping in mind the same order of coordinates as in (4.2), i.e. the notation and order of variables given by Voigt [72] has been adopted.

The components of the polarization vector $\boldsymbol{P}^*$ in crystallographic coordinates can now be determined from [57, 73]

$$\boldsymbol{P}^* = \boldsymbol{d}\boldsymbol{\sigma}^* \tag{4.21}$$

where $\boldsymbol{d}$ is the piezoelectric tensor given in matrix notation as

$$\boldsymbol{d} = \begin{bmatrix} 0 & 0 & 0 & d_{14} & 0 & 0 \\ 0 & 0 & 0 & 0 & d_{14} & 0 \\ 0 & 0 & 0 & 0 & 0 & d_{14} \end{bmatrix} \tag{4.22}$$

where $d_{14} = -2.69 \cdot 10^{-12}$ C/N is the piezoelectric constant for GaAs [9]. It is worth noting from the structure of the piezoelectric tensor $\boldsymbol{d}$ that the stress components in the main crystallographic directions can not induce any polarization in the GaAs crystal. The sign of d_{14} is negative if the Ga atom is situated at the origin of the GaAs unit cell and if it has a bond with the As atom lying in the [111] direction [70].

The components of the polarization vector $\boldsymbol{P}^*$ are

$$\boldsymbol{P}^* = \begin{bmatrix} P_1 \\ P_2 \\ P_3 \end{bmatrix} = d_{14} \begin{bmatrix} (-\sigma_{xx}+\sigma_{yy})\sin\alpha\cos\alpha \\ \sigma_{xz}\sin\alpha \\ -\sigma_{xz}\cos\alpha \end{bmatrix}. \tag{4.23}$$

Finally, it is necessary to transform the crystallographic polarization vector into the gate coordinate system, and this is performed by

$$\boldsymbol{P} = \beta^T \boldsymbol{P}^* . \tag{4.24}$$

After straightforward calculations we obtain

$$\boldsymbol{P} = \begin{bmatrix} P_x \\ P_y \\ P_z \end{bmatrix} = \begin{bmatrix} 2d_{14}\sigma_{xz}\sin\alpha\cos\alpha \\ d_{14}\sigma_{xz}(-\sin^2\alpha+\cos^2\alpha) \\ -d_{14}\sin\alpha\cos\alpha[(\nu-1)\sigma_{xx}+\nu\sigma_{zz}] \end{bmatrix} \tag{4.25}$$

where we used (4.16).

The induced polarization $\boldsymbol{P}$ may be considered as being a result of the piezoelectric charge density per unit volume ρ_{pz} which can be calculated from

$$\rho_{pz} = -\nabla\cdot\boldsymbol{P} \tag{4.26}$$

$$= -\frac{\partial}{\partial x}P_x - \frac{\partial}{\partial y}P_y - \frac{\partial}{\partial z}P_z. \tag{4.27}$$

After the derivation indicated in (4.27) the charge density induced by the piezoelectric polarization becomes

$$\rho_{pz} = d_{14}\sin(2\alpha)\frac{\partial}{\partial z}\left[-\frac{1}{2}(1-\nu)\sigma_{xx}+(1+\frac{\nu}{2})\sigma_{zz}\right]. \tag{4.28}$$

In derivation of (4.28) we used the fact that there is no change of σ_{xz} in the out-of-plane direction and the momentum balance equation [71]

$$\frac{\partial\sigma_{zz}}{\partial z}+\frac{\partial\sigma_{xz}}{\partial x}=0. \tag{4.29}$$

It is worth noting that for the [011] FET the angle $\alpha = \pi/4$ and the term $\sin(2\alpha) = +1$, while in the case of the $[01\bar{1}]$ FET, i.e. the FET rotated though an angle of $\pi/2$, the angle $\alpha = -\pi/4$ and the term $\sin(2\alpha) = -1$, giving the charge of opposite sign and equal magnitude, as has been observed experimentally [17, 19]. A reversal of sign of the piezoelectric charge is also introduced if the stress in the dielectric changes its character, i.e. a dielectric under tension induces a charge of opposite sign to the charge induced by the dielectric in compression, which has also been noticed in the experimental work [19, 23].

To calculate the piezoelectric charge density from the known distribution of stresses, we have to determine the first derivative of σ_{xx} and σ_{zz} with respect to the z axis. The procedure will be explained after we see how the FEM technique is applied in solving the stress distribution in the strained MESFET structure.

4.1.3 Finite element method

So far we have defined the stress-strain and strain-displacement relations. To calculate the equilibrium displacements, strains and stresses of a solid body

constrained to deform in plane strain under prescribed load the following equilibrium conditions are taken into account

$$\frac{\partial \sigma_{xx}}{\partial x} + \frac{\partial \sigma_{xz}}{\partial z} + F_x = 0 \quad (4.30)$$

$$\frac{\partial \sigma_{xz}}{\partial x} + \frac{\partial \sigma_{zz}}{\partial z} + F_z = 0 \quad (4.31)$$

where F_x and F_z are the components of the body force $\boldsymbol{F}$ in the x and z directions respectively. The equilibrium conditions can be expressed in matrix notation as

$$\boldsymbol{L}^T \boldsymbol{\sigma} = -\boldsymbol{F} \quad (4.32)$$

and after substitutions $\boldsymbol{\sigma}=\boldsymbol{D}\boldsymbol{\varepsilon}$ and $\boldsymbol{\varepsilon} = \boldsymbol{L}\boldsymbol{u}$ we get

$$\boldsymbol{L}^T \boldsymbol{D} \boldsymbol{L} \boldsymbol{u} = -\boldsymbol{F} \quad (4.33)$$

which is a set of simultaneous partial differential equations in the displacements u and w. Once this system has been solved, the stresses and strains may be recovered by means of (4.8) and (4.13).

The equilibrium stresses will be determined over the domain shown in Fig. 4.3. Only one half of the MESFET structure is taken into account because of the symmetry associated with the problem. The lower left corner has no degrees of freedom, the bottom edge is allowed to deform only in the x direction, while the left edge can deform only in the z direction. The stress is introduced into the structure either by specifying the uniform displacement $\boldsymbol{u}$ at the right edge of the simulation region or by defining the force $\vec{F_l}$ parallel to the x axis that acts at the point where the gate, dielectric and substrate meet. If the dielectric film is under tension, it exerts a compressive stress in the region just below the gate. Such a case is modelled by the force $\vec{F_l}$ acting in the $-x$ direction or by specifying the positive uniform displacement $\boldsymbol{u}$ at the right boundary.

The state of equilibrium is determined by the application of the finite element method (FEM) [74]. Firstly the domain is divided into rectangular elements. The mesh of elements is very fine in the metal and dielectric layer, on the surface of the substrate and in the substrate around the gate corner. This fine mesh ensures that the high gradients of stresses are properly taken into account. Elsewhere the mesh is gradually coarsened to keep the number of nodes acceptably small for the numerical calculation. A typical mesh consists of 10000 nodes.

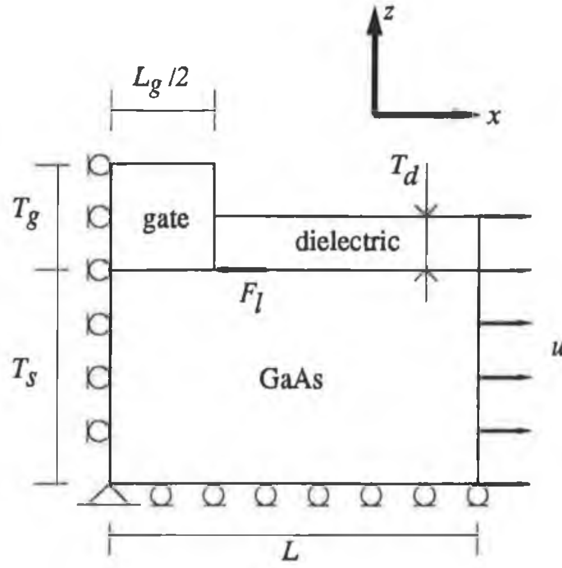

Figure 4.3: Schematic structure of a MESFET used for stress analysis. Two different sources of stress can be defined as boundary conditions: 1) uniform displacement $\boldsymbol{u}$ at the right edge of the simulated structure or 2) force $\vec{F}_l$ acting at the point common to the gate, dielectric and substrate.

Over each element the displacement is approximated by four bilinear shape functions [74, 75]. The displacement at each node has two components or two degrees of freedom, if the node is not restrained by boundary conditions. Thus, generally the nodal values of the displacement for the element e are represented by a vector $\boldsymbol{a}^e$

$$\boldsymbol{a}^e = \begin{bmatrix} u_i \\ w_i \\ u_j \\ w_j \\ u_k \\ w_k \\ u_l \\ w_l \end{bmatrix} \tag{4.34}$$

and the matrix of the shape functions is

$$\boldsymbol{N} = \begin{bmatrix} N_i & 0 & N_j & 0 & N_k & 0 & N_l & 0 \\ 0 & N_i & 0 & N_j & 0 & N_k & 0 & N_l \end{bmatrix} \tag{4.35}$$

where the indices i, j, k and l correspond to four nodes of an element. Over an element the displacements are approximated by

$$\boldsymbol{u} \approx \hat{\boldsymbol{u}} = \boldsymbol{N}\boldsymbol{a}^e \tag{4.36}$$

$$= \begin{bmatrix} N_i u_i + N_j u_j + N_k u_k + N_l u_l \\ N_i w_i + N_j w_j + N_k w_k + N_l w_l \end{bmatrix}. \tag{4.37}$$

Instead of solving the system of differential equations (4.33) the principle of minimising the total potential energy Π is applied, because this method is more appropriate for the application of the finite element method and the solution satisfies both the generalized Hooke's law and the equilibrium conditions [74, 76]. The total potential energy Π is the sum of the strain energy U

$$U = \frac{1}{2}\iint \boldsymbol{\sigma}^T \boldsymbol{\varepsilon} dxdz \tag{4.38}$$

and the work W done by the external loads

$$W = -\boldsymbol{a}^{eT}\boldsymbol{F}. \tag{4.39}$$

Using (4.8) and (4.13) the strain energy of an element becomes

$$\begin{aligned} U^e &= \frac{1}{2}\iint (\boldsymbol{DL\hat{u}})^T(\boldsymbol{L\hat{u}})dxdz && (4.40)\\ &= \frac{1}{2}\boldsymbol{a}^{eT}\left\{\iint (\boldsymbol{LN})^T\boldsymbol{D}(\boldsymbol{LN})dxdz\right\}\boldsymbol{a}^e && (4.41)\\ &= \frac{1}{2}\boldsymbol{a}^{eT}\left\{\iint \boldsymbol{B}^T\boldsymbol{DB}dxdz\right\}\boldsymbol{a}^e && (4.42)\\ & && (4.43)\end{aligned}$$

where $\boldsymbol{B}=\boldsymbol{LN}$ and the use has been made of the fact that $\boldsymbol{D} = \boldsymbol{D}^T$. The total potential energy Π is a quadratic function in $\boldsymbol{a}^e$

$$\Pi = \frac{1}{2}\boldsymbol{a}^{eT}\boldsymbol{K}^e\boldsymbol{a}^e - \boldsymbol{a}^{eT}\boldsymbol{F} \tag{4.44}$$

and in elastic situations it has a minimum. By simple differentiation we get the variation of Π

$$\delta\Pi = \delta\boldsymbol{a}^{eT}(\boldsymbol{K}^e\boldsymbol{a}^e - \boldsymbol{F}). \tag{4.45}$$

The principle expressed in (4.45) is that the equilibrium in mechanical systems can be achieved by the minimization of the total potential energy Π and that the stationary solution ($\delta\Pi = 0$) has to satisfy

$$\boldsymbol{K}^e\boldsymbol{a}^e - \boldsymbol{F} = 0. \tag{4.46}$$

The element stiffness matrix $\boldsymbol{K}^e$ is built up from 2×2 submatrices, each submatrix containing contributions to the element matrix due to both degrees of freedom at nodes i and j

$$\boldsymbol{K}^e_{ij} = \iint \boldsymbol{B}_i^T\boldsymbol{DB}_j dxdz. \tag{4.47}$$

The calculation of the integral (4.47) is performed numerically using the four-point quadrature rule [74, 75]. Once the system stiffness matrix has been assembled adding contributions from all elements, the solution for displacements in equilibrium can be easily obtained from (4.46).

The program that performs all the necessary steps for calculation of the stress field in the structure depicted in Fig. 4.3 is written in FORTRAN. The usage of the NAG FEM library [75] of the FORTRAN functions has made the production of the code very effective and simplified the testing stage of the final code.

4.1.4 Outline of the numerical procedure

The extraction of the piezoelectric charge is divided into two steps: the calculation of the stresses by the FEM method and the interpolation procedure.

To initiate the stress calculation the following data have to be defined: geometry of the simulated region (nodal coordinates and the list of nodes for each element), mechanical parameters (Young's modulus and Poisson's ratio for each material), nodal constraints, nodal loads, the angle α that defines the relation between the gate and crystallographic coordinate system, and the piezoelectric constant.

When specifying the simulation region several precautions pertaining to the geometry have been taken into account:

1. The thickness T_s of the GaAs substrate is at least ten times the gate thickness T_g (see Fig. 4.3).
2. The length L of the GaAs substrate is at least ten times the length $L_g/2$.
3. The mesh in the x direction is very fine ($\Delta x = 0.01$ μm) around the gate/dielectric edge and the mesh in the z direction is very fine ($\Delta z = 0.01$ μm) in the gate and dielectric regions as well as in the substrate up to the depth of 0.2 μm, which is at least twice the active channel thickness.

A typical mesh consists of approximately 10^4 nodes.

The results of the FEM analysis are the displacements at the nodal points and the stresses σ_{xx}, σ_{zz} and σ_{xz} at the quadrature points of each element. Additionaly, the values of the function $f(x, z)$

$$f(x,z) = d_{14}\sin(2\alpha)\left[-\frac{1}{2}(1-\nu)\sigma_{xx} + (1+\frac{\nu}{2})\sigma_{zz}\right] \tag{4.48}$$

are calculated at the quadrature points of each element.

The extraction of the piezoelectric charge ρ_{pz} is done at the interpolation stage of the numerical procedure by

$$\rho_{pz} = \frac{\partial}{\partial z}[f(x,z)]. \tag{4.49}$$

The reason why an interpolation has to be used is the following. The stresses calculated by the FEM method are obtained at the quadrature points of each element. As the derivatives of the bilinear functions used to approximate displacements over an element do not possess inter-element continuity, the stress field is discontinuous at the nodal points. Furthermore, in the FEM method involving a numerical integration over elements such as the quadrilateral isoparametric elements used here, the best sampling points are the integration points, i.e. the quadrature points [77]. The nodes, which are the most useful output locations, appear to be the worst sampling points. Although reasons for this phenomenon are not immediately apparent, it is well known that interpolation functions tend to behave badly near the extremities of the interpolation region, i.e. near the boundaries of elements. To counteract this problem the following procedure has been adopted. Firstly, the stresses are averaged over each element and this value has been taken as the stress value at every node of an element, and then a second averaging is performed over different elements sharing the same node, i.e. the final nodal stress value is calculated as the average stress in the elements sharing the node.

The second averaging is a common practice [74, 77], but the first averaging where the stress is approximated by a constant function over the element raises suspicions because this procedure seems to be oversimplified. Thus, a different procedure has been tested. The stress over an element has been approximated by bilinear functions passing through the stress values at quadrature points and the nodal values have been calculated by extrapolation. Finally, an averaging over the elements sharing the same node has been done as in the first interpolation procedure.

The results of these two interpolation procedures have been surprisingly similar. Apart from the surface of the GaAs substrate, the difference was completely negligible. On the surface, and only around the region close to the gate/dielectric edge, the bilinear interpolation resulted in slightly higher values of the piezoelectric charge. It has been decided to adopt the first interpolation procedure for two reasons: 1) the influence of the piezoelectric charge

on the surface of the substrate around the gate edge is negligible because of the Schottky barrier depletion region, and 2) there is no way to guess which procedure is physically more sound.

Once the nodal values of stresses are calculated, the stress distribution has been approximated by bilinear functions over each element and the piezoelectric charge has been obtained by calculating the first derivative in the z direction as indicated in (4.49).

Note that the mesh used in the FEM method and subsequent interpolation procedure differs from the mesh used in the device simulator. As a consequence, the piezoelectric charge has been calculated at the nodal coordinates pertaining to the mesh used in the device simulator. Once the piezoelectric charge distribution is calculated, the doping profile is updated in such a way that positive piezoelectric charge is added to the donor concentration and negative charge is added to the acceptor concentration of the corresponding node.

4.2 Analytical approach

The underlying analytical stress analysis and the derivation of piezoelectric charge are similar to that presented by Kirkby *et al.* [78] and Asbeck *et al.* [18].

The schematic structure of a GaAs FET which will be analysed is shown in Fig. 4.4. The FET is considered to be very wide, so that the stress distribution is effectively two-dimensional. In the approximation that GaAs is considered elastically isotropic the stress produced by the gate metal can be neglected. If the dielectric is under tension, for the coordinate system in Fig. 4.4 the nonzero components of the stress tensor at the point P inside the substrate are

$$\sigma_{xx} = -\frac{2}{\pi}F_l\left(\frac{x_1^3}{r_1^4} - \frac{x_2^3}{r_2^4}\right) \quad (4.50)$$

$$\sigma_{zz} = -\frac{2}{\pi}F_l\left(\frac{x_1 z^2}{r_1^4} - \frac{x_2 z^2}{r_2^4}\right) \quad (4.51)$$

$$\sigma_{xz} = \frac{2}{\pi}F_l\left(\frac{x_1^2 z}{r_1^4} - \frac{x_2^2 z}{r_2^4}\right) \quad (4.52)$$

where F_l is the force per unit length that is used to model the reaction of the stressed dielectric deposited on the GaAs substrate. If the origin of the coordinate system is chosen in such a way that it is on the surface of the substrate and at the middle of the gate, the points at the edges of the dielectric

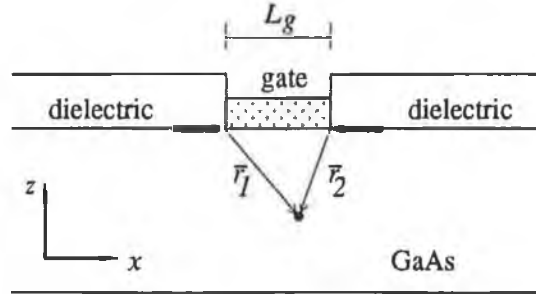

Figure 4.4: Schematic structure of a MESFET showing the coordinate system used (the y axis going into the paper). The dielectric layer is under tension and the stress exerted on the GaAs substrate is modelled by forces acting towards the centre of the gate.

window have the coordinates $(-L_g/2,0)$ and $(L_g/2,0)$. The vectors $\vec{r_1}$ and $\vec{r_2}$ pointing from the points at the edges of the dielectric window towards the point P with the coordinates (x,z) are

$$\vec{r_1} = x_1\vec{\imath} + z\vec{k} = (x + L_g/2)\vec{\imath} + z\vec{k} \quad (4.53)$$

$$\vec{r_2} = x_2\vec{\imath} + z\vec{k} = (x - L_g/2)\vec{\imath} + z\vec{k} \quad (4.54)$$

where $\vec{\imath}$ and $\vec{k}$ are the unit vectors in the direction of the x and z axes, respectively. Note that within the substrate $z \leq 0$.

When a window is opened in the dielectric, the edge of the window exerts a force on the GaAs substrate, parallel to the surface of the substrate. If the dielectric is under tension, the force acts in the direction towards the centre of the gate producing a compressive stress just under the gate. The force $\vec{F_l}$ at the right gate edge is

$$\vec{F_l} = -F_l\vec{\imath} \quad (4.55)$$

and

$$F_l = \sigma_d T_d \quad (4.56)$$

where σ_d is the dielectric stress and T_d is the dielectric thickness. If the stress σ_d is positive, the dielectric is under tension, the region just below the gate is under compression and the force $\vec{F_l}$ acts in the direction opposite to the x axis direction. The force at the left gate edge has the sign opposite to the sign of the force at the right gate edge.

It is necessary to note that neither the gate metal nor the dielectric have actually been taken into consideration when calculating the stress distribution in the substrate and as a result the calculated stresses have singularities at

the edges of the dielectric layer. In practice such factors as the finite dielectric thickness, the gate metal and plastic deformations will limit the stresses to finite values.

If we consider a FET processed on a (100) substrate and with such an orientation that its longest dimension is in the $[01\bar{1}]$ direction, i.e. the $[01\bar{1}]$ FET (which is the case originally discussed in [18]), the piezoelectrically induced polarization vector is

$$\boldsymbol{P} = \begin{bmatrix} P_x \\ P_y \\ P_z \end{bmatrix} = \begin{bmatrix} -d_{14}\sigma_{xz} \\ 0 \\ -\frac{d_{14}}{2}(\sigma_{xx} - \sigma_{yy}) \end{bmatrix} \tag{4.57}$$

and the corresponding piezoelectric charge density is

$$\rho_{pz} = -\nabla \cdot \boldsymbol{P} \tag{4.58}$$

$$= -\frac{\partial}{\partial x}P_x - \frac{\partial}{\partial z}P_z \tag{4.59}$$

$$= -\gamma_b F_l \left(\frac{x_1 z(x_1^2 - \beta z^2)}{r_1^6} - \frac{x_2 z(x_2^2 - \beta z^2)}{r_2^6} \right) \tag{4.60}$$

where $\gamma_b = (2/\pi)d_{14}(4+\nu)$ and $\beta = (2+\nu)/(4+\nu)$.

Note that (4.57) is actually a special case of (4.25) for $\alpha = -\pi/4$. In the case of the [011] FET, the angle $\alpha = \pi/4$ and the piezoelectric charge will acquire opposite sign, as well as the components of the polarization vector (4.57).

4.3 Comparisons and discussions

In this section a comparison between the numerical and analytical approach is given together with the results for different load models used to introduce the stress into the GaAs substrate. The accuracy of the numerical method is estimated. The advantages and disadvantages of the methods are pointed out.

Additionally, a brief discussion on the level of knowledge about the dielectric stress has been presented.

4.3.1 On the dielectric stress

It seems appropriate to address first of all the question of what is the current level of knowledge about the stress caused by depositing a dielectric film on a GaAs substrate.

Kirkby *et al.* [78] measured the radius of curvature of the GaAs substrate to deduce the stress in the dielectric film. The dielectric film used was rf plasma-deposited SiO_2/Si_3N_4. Its properties varied depending on the deposition conditions, but it was always under considerable compression on cooling to room temperature. The curvature measurements showed that the dielectric stress was $-5 \cdot 10^8$ N/m^2 and -10^9 N/m^2 for two typical sets of deposition conditions. No mention has been made about the relative concentration of SiO_2 in the SiO_2/Si_3N_4 film, but as the stress obtained by measurements compared with the calculated value of $2.5 \cdot 10^8$ N/m^2 for the thermal mismatch stress of SiO_2 on GaAs when cooling from 500° C to room temperature, it can be supposed that the relative SiO_2 concentration was high.

Ohnishi *et al.* [19] confirmed by X-ray diffraction measurements that SiO_2 and Si_3N_4 films imposed opposite stresses on GaAs; the SiO_2 film was in compression with a magnitude of about mid 10^8 N/m^2 and the Si_3N_4 film in tenssion with a magnitude of about 10^8 N/m^2. The threshold voltage measurements showed opposite threshold voltage shifts for the SiO_2 and Si_3N_4 films with smaller threshold voltage shifts obtained for the Si_3N_4 film. In both cases the orientation dependence was almost eliminated when the dielectric thickness was reduced to zero. This fact suggests that the stress caused by the WSi_x gate is negligibly small.

The work by Ohnishi *et al.*, in attributing the opposite threshold voltage shifts to opposite signs of the stresses in the dielectric films used, has certainly clarified the source of apparently inconsistent results.

However, it is necessary to mention that although the tensile stress in the SiO_2 dielectric on GaAs is consistent with the results published under the framework of "orientation effects in GaAs MESFETs" [15, 20], the SiO_2 layers have been deposited on GaAs with average stresses ranging from $+10^8$ N/m^2 (tensile) to -10^8 N/m^2 (compressive) depending on the deposition conditions [79]. The case of the stress in the Si_3N_4 films produces similar inconsistencies. Although this film is found to be under tension when evaporated onto the GaAs substrate [19], with all the results in the field of "orientation effects in GaAs MESFETs" being in accordance with this [14, 17, 18, 80, 81], it has been also reported to be under compression of approximately $-2 \cdot 10^8$ N/m^2 [82].

4.3.2 Accuracy of the numerical method

The accuracy of the numerical procedure for derivation of piezoelectric charge can be verified by comparing the results obtained by the analytical approach and the results obtained by the application of the finite element method when both dielectric and gate metal are excluded from the simulation.

The 0.7 μm gate-length EPI-P MESFET has been taken as a reference for the comparison.

Two forces parallel to the substrate surface acting on the points at the edges of the dielectric window in such a way that the points are displaced towards the middle of the dielectric window are used to model the tensile stress in the dielectric exerted on GaAs. The absolute value of the force is $|\vec{F}_l| = 40$ N/m, which corresponds to the tensile dielectric stress $\sigma_d = 2 \cdot 10^8$ N/m^2 and the dielectric thickness $T_d = 0.2$ μm. The mechanical constants for GaAs are: Young's modulus $E = 8.53 \cdot 10^{10}$ N/m^2 and Poisson's ratio $\nu = 0.31$ [9]. The MESFET analysed is the $[01\bar{1}]$ MESFET, which means that the source-to-drain direction is in the [011] direction.

The stresses σ_{xx} and σ_{zz} obtained by the analytical method are shown in Figs. 4.5 and 4.6, respectively, and the piezoelectric charge ρ_{pz} is depicted in Fig. 4.7.

As it is difficult to compare two-dimensional graphs, it was decided to plot the stress σ_{xx} down the middle of the gate (at $x = 1.45$ μm) and down the right boundary of the simulated region[2] (at $x = 2.9$ μm) obtained by the analytical and FEM method (see Fig. 4.8). As it can be noticed a very good agreement has been obtained for both stresses.

Fig. 4.9 shows the piezoelectric charge down the middle of the gate obtained by both methods. It can be noticed that the charge is underestimated, but the shape and the position of the maximum charge are correct. The error is probably due to both the finite mesh size and the interpolation procedure. Considering the stress σ_{xx} down the middle of the gate, the difference between

[2]The right boundary, unless it is explicitely stated otherwise, means the right boundary of the simulated region used in the EVEREST simulator, i.e. it is 2.7, 2.9, 3.2 and 4.2 μm long for the 0.5, 0.7, 1.0 and 2.0 μm gate-length MESFETs, respectively. The right boundary used in the stress calculation is actually 3.85, 4.95, 6.6 and 12.1 μm long for the aforementioned gate lengths, respectively. In other words, the simulated region in EVEREST in the x direction is [0,2.7], [0,2.9], [0,3.2] and [0,4.2] μm and in the stress calculation it is [1.35,3.85], [1.45,4.95], [1.6,6.6] and [2.1,12.1] μm for the 0.5, 0.7, 1.0 and 2.0 μm gate-length MESFETs, respectively, i.e. in the stress calculation only one half of the MESFET on the drain side is simulated appealing to symmetry to avail of the overall solution. The simulated region in the z direction is from $z = 1.6$ μm to $z = -0.5$ μm in all cases.

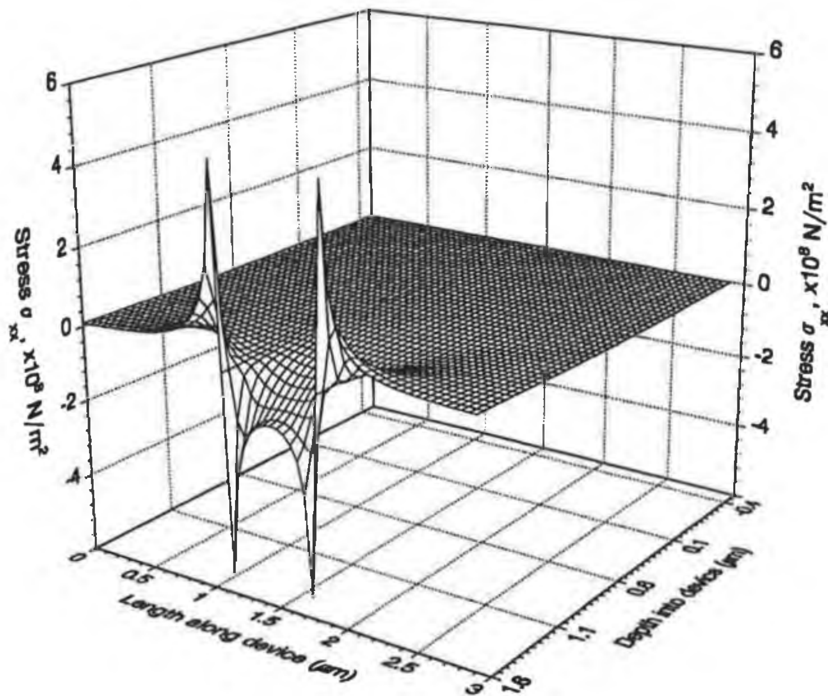

Figure 4.5: Stress σ_{xx} calculated by the analytical method for the 0.7 μm EPI-P MESFET. The gate metal is deposited on the x-y surface at z=1.6 μm between the points x=1.1 μm and x=1.8 μm (the x axis is denoted as 'Length along device', the z axis is denoted as 'Depth into device', and the y axis is not shown on the graph).

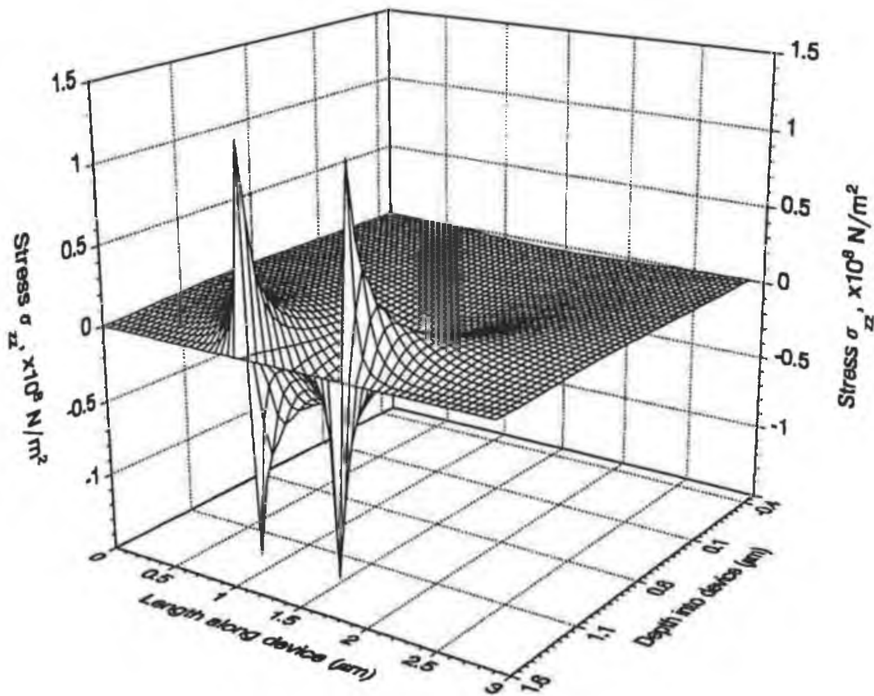

Figure 4.6: Stress σ_{zz} calculated by the analytical method for the 0.7 μm EPI-P MESFET. The gate metal is deposited on the x-y surface at z=1.6 μm between the points x=1.1 μm and x=1.8 μm (the x axis is denoted as 'Length along device', the z axis is denoted as 'Depth into device', and the y axis is not shown on the graph).

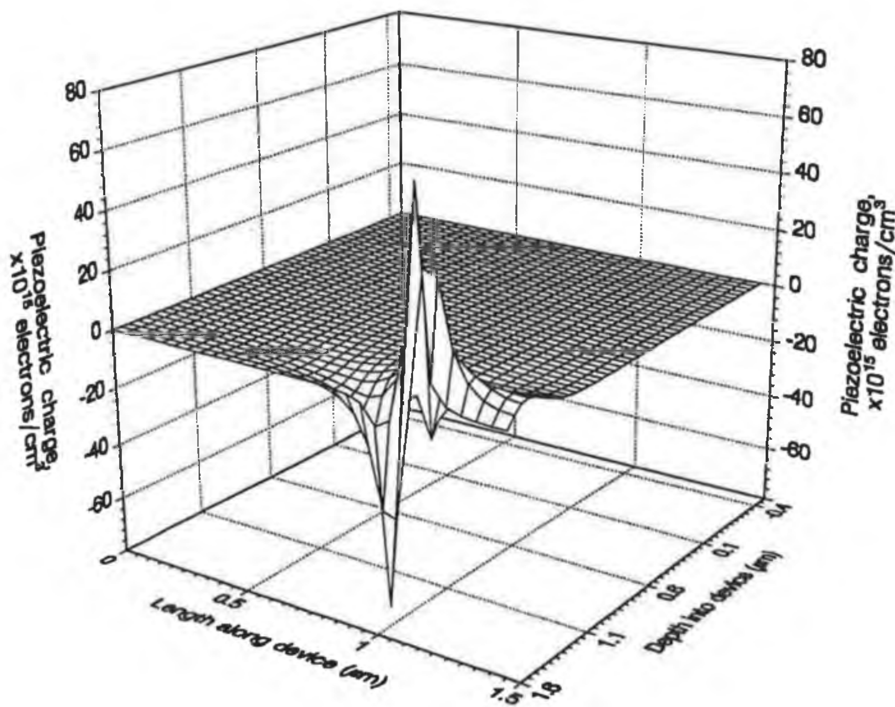

Figure 4.7: Piezoelectric charge ρ_{pz} calculated by the analytical method for the 0.7 μm EPI-P MESFET. Only one half of the simulated region is shown (the source side, from $x = 0$ to $x = 1.45$ μm) because the charge is symmetric around the gate centre. The gate metal is deposited on the x-y surface at z=1.6 μm between the points x=1.1 μm and x=1.8 μm (the x axis is denoted as 'Length along device', the z axis is denoted as 'Depth into device', and the y axis is not shown on the graph).

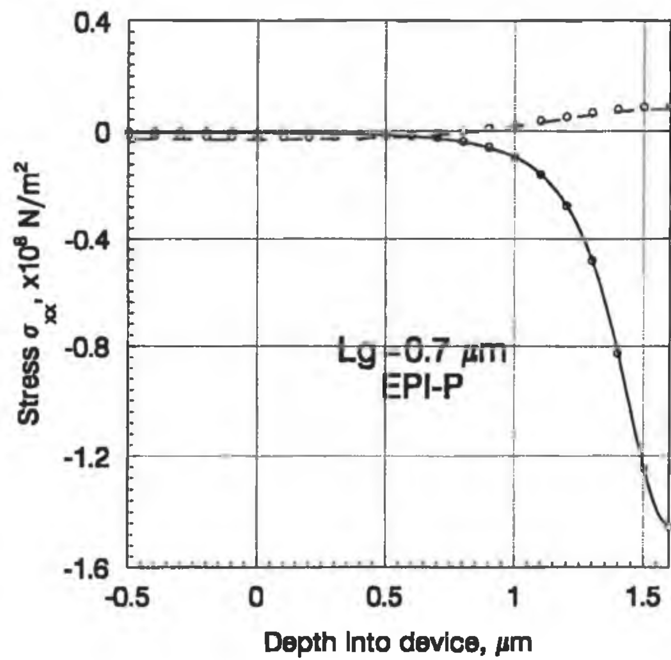

Figure 4.8: Stress σ_{xx} calculated by the analytical and FEM method for the 0.7 μm EPI-P MESFET down the middle of the gate (full line) and down the right boundary of the simulated region (dashed line), $x = 1.45$ μm and $x = 2.9$ μm respectively. Circles represent the analytical results and lines show the results of the FEM method.

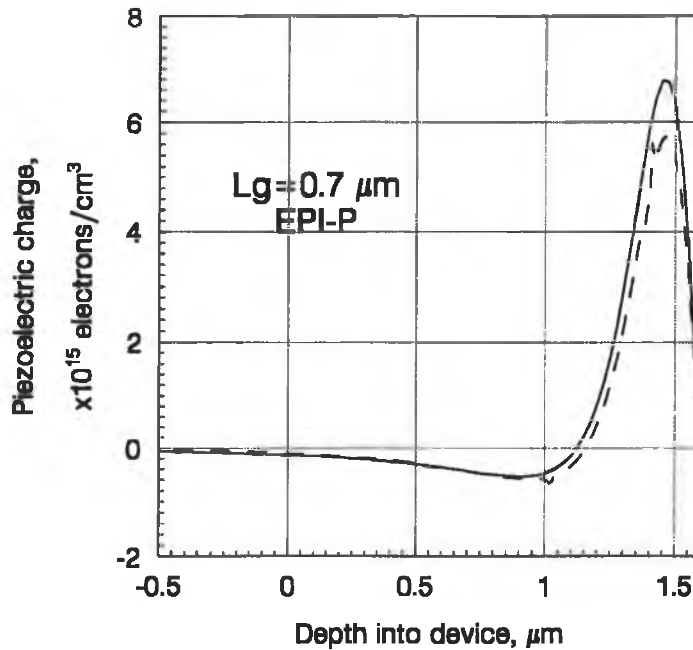

Figure 4.9: Piezoelectric charge ρ_{pz} calculated by the analytical (full line) and FEM (dashed line) method for the 0.7 μm EPI-P MESFET down the middle of the gate (at $x = 1.45$ μm).

the FEM and analytical method was less than 1%, while the maximum charge down the middle of the gate obtained by the FEM method was 20% smaller than the charge obtained by the analytical method. Thus, we may conclude that the error is mainly introduced in the interpolation stage when calculating the piezoelectric charge.

After adding the calculated piezoelectric charge to the doping profile of the reference MESFET the device simulation has been performed. The piezoelectric charge used to update the doping profile of the reference MESFET has been calculated in the following ways:

1. Analytical method.
2. FEM method.
3. FEM method and scaled upwards by a factor K=1.2 .
4. FEM method and scaled upwards by a factor K=1.25 .

The threshold voltages obtained are shown in Table 4.1. The values for

Method	σ_d (N/m^2)	V_{th} (V)	ΔV_{th} (mV)
analytical	$2 \cdot 10^8$	-0.751	-196
FEM*1.25	$2 \cdot 10^8$	-0.745	-190
FEM*1.2	$2 \cdot 10^8$	-0.736	-181
FEM	$2 \cdot 10^8$	-0.708	-153
reference	0	-0.555	0
FEM	$-2 \cdot 10^8$	-0.440	115
FEM*1.2	$-2 \cdot 10^8$	-0.421	134
FEM*1.25	$-2 \cdot 10^8$	-0.415	140
analytical	$-2 \cdot 10^8$	-0.411	144

Table 4.1: Threshold voltages for the 0.7 μm gate-length EPI-P MESFET used as the reference. The piezoelectric charges used to update the doping profile of the reference MESFET have been calculated by different methods, as is shown in the table.

both tensile ($\sigma_d = 2 \cdot 10^8$ N/m^2) and compressive ($\sigma_d = -2 \cdot 10^8$ N/m^2) stress in the dielectric are shown.

From the results shown in Table 4.1 it can be noticed that the threshold voltage shifts for the analytical method and the FEM method when the piezoelectric charge is multiplied by 1.25 are very close in value (the error is 3.1% for the tensile dielectric stress and 2.8% for the compressive dielectric stress, if the threshold voltage shift obtained by the analytical method is used as the reference). Thus, we conclude that the finite element method and subsequent interpolation procedure yield a piezoelectric charge that is underestimated approximately 25%.

The accuracy of the FEM method has been estimated upon the effect of the calculated piezoelectric charge on the threshold voltage of the 0.7 μm gate-length EPI-P MESFET. However, it is necessary to check whether the error of the FEM method is an 'intrinsic' property of the method or if it also varies with gate length.

To do so, the EPI-P MESFETs with gate lengths of 0.5, 1.0 and 2.0 μm have been simulated for both tensile and compressive stress in the dielectric film. The piezoelectric charge has been calculated by the four methods, as in the case of the 0.7 μm EPI-P MESFET. Fig. 4.10 shows calculated threshold voltages. Note a good agreement between the threshold voltages obtained by the analytical method and the FEM method when the charge is multiplied by 1.25 for all four gate lengths.

It should be noted that it has not been tried to compare the maximum stresses and piezoelectric charges, that appear around the gate edges, because

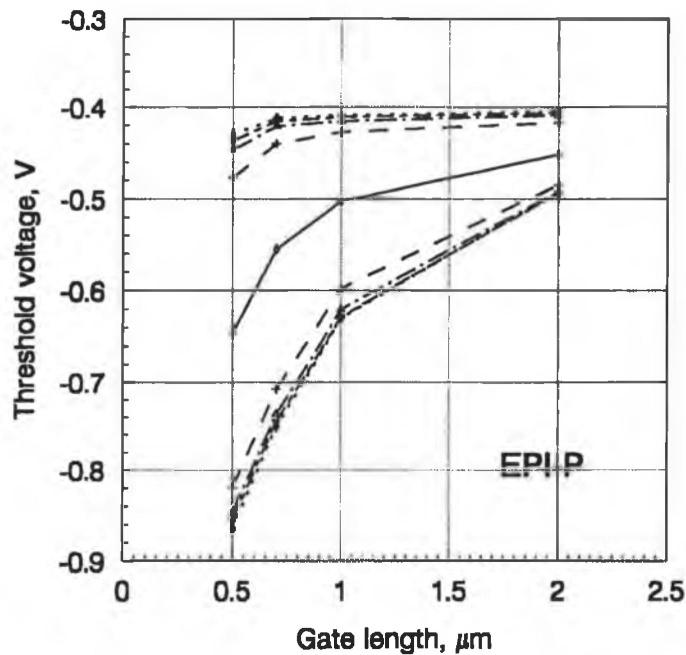

Figure 4.10: Dependence of the threshold voltage on the gate length for the EPI-P simulations. The threshold voltage vs. gate length for the reference simulations is represented by full line. The following methods have been used to update the doping profile of the reference MESFETs: FEM method (dashed line), FEM and charge multiplied by 1.2 (dash-dot line), FEM and charge multiplied by 1.25 (long-dash/short-dash line), and analytical method (dots). The threshold voltages above the reference case (full line) have been obtained for compressive stress in the dielectric ($\sigma_d = -2 \cdot 10^8$ N/m^2) and the threshold voltages below the reference line have been obtained for tensile stress in the dielectric ($\sigma_d = 2 \cdot 10^8$ N/m^2).

these values strongly depend on the mesh size used. It is also worth noting that the same dependence exists for the analytical method as well as for the FEM method, because the maxima do not appear at the gate edge nodes, but at the nodes on the GaAs surface closest to the gate edges. Furthermore, the value of the piezoelectric charge peaks around the gate edges is not of major importance, because the relative contribution of the piezoelectric charge peaks to the charge of the active channel is small.

Finally, it is necessary to mention that the accuracy of the FEM method has been estimated by using the results of the analytical method as a reference, because the analytical method is correct from the mathematical point of view under assumptions used. However, it does not mean that the analytical method is completely physically correct. Actually, its validity is satisfied only outside the region of radius of approximately two dielectric thicknesses around the gate edges [23, 79], i.e. the validity is violated around the gate edges as a consequence of not including the dielectric layer in the calculation of the stress fields.

4.3.3 Influence of the gate and dielectric

The value of the analytical method for the calculation of stresses in GaAs and the resulting piezoelectric charge lies in its simplicity. However, neither the gate metal nor dielectric are taken into account when calculating stresses in the GaAs substrate.

To demonstrate the influence of the gate metal and dielectric layer two more simulations have been performed. The reference model is again the 0.7 μm gate-length EPI-P MESFET. Firstly the stress fields have been calculated for the structure consisting of the gate metal deposited on the GaAs substrate (gate metal thickness being $T_g = 0.2$ μm) and then the 0.2 μm thick dielectric layer has been added for the second simulation. The same load of $|\vec{F}_l| = 40$ N/m (corresponding to $\sigma_d = 2 \cdot 10^8$ N/m^2 and $T_d = 0.2$ μm) has been used in both cases. This load and the same reference MESFET have been used in the previous section where the structure consisting of only GaAs has been analysed. The mechanical parameters for all three materials are presented in Table 4.2.

Figs. 4.11, 4.12 and 4.13 show the σ_{xx} stress for the GaAs, metal/GaAs and metal/dielectric/GaAs structures, respectively, and Figs. 4.14, 4.15 and 4.16 show the piezoelectric charge for the same cases, respectively. All results

	E (N/m^2)	ν
GaAs	$8.53 \cdot 10^{10}$	0.31
WSi_x	$6.21 \cdot 10^{11}$	0.30
Si_3N_4	$3.10 \cdot 10^{11}$	0.30

Table 4.2: Mechanical parameters Young's modulus E and Poisson's ratio ν for GaAs [9], WSi_x used as metal and Si_3N_4 used as dielectric [83].

have been calculated by applying the FEM method.

When only the GaAs substrate is taken into account, the positive peak of the σ_{xx} stress has the same magnitude of $16 \cdot 10^8$ N/m^2 as the negative peak. The negative peak appears below the gate, indicating the compressive stress produced by the dielectric in tension, and the positive peak appears just outside the gate. Thus, the ratio between the positive and negative stress peaks is $16 \cdot 10^8 / -16 \cdot 10^8$. In the case of the metal/GaAs structure the ratio is $3 \cdot 10^8 / -4.5 \cdot 10^8$ and in the case of the metal/dielectric/GaAs structure the ratio is $2.4 \cdot 10^8 / -2.5 \cdot 10^8$.

It can be noticed that an average stress of $2 \cdot 10^8$ N/m^2 in the dielectric produces 8 times higher peak of the σ_{xx} stress in the case of the GaAs structure alone. Adding the metal layer has reduced the σ_{xx} peaks and also produced unsymmetric peaks, the magnitude of the peak under the gate being 50% higher than the positive peak. When the dielectric film is also taken into account the magnitudes of the peaks are further reduced. The difference in magnitudes between the positive and negative peak has been reduced as well.

A very similar situation appears for the peaks in the piezoelectric charge distribution, except that the negative peak of the σ_{xx} stress results in the positive peak of the piezoelectric charge. The ratio between the maximum negative and maximum positive peak is $-4 \cdot 10^{17} / 4 \cdot 10^{17}$ in the case of the GaAs structure, $-1.2 \cdot 10^{17} / 1.5 \cdot 10^{17}$ in the case of the metal/GaAs structure and $-7.6 \cdot 10^{16} / 8.2 \cdot 10^{16}$ in the case of the metal/dielectric/GaAs structure.

Thus, we conclude that the inclusion of both the gate metal and dielectric in the calculation of stress distributions results in approximately 6 times lower levels of the maximum stresses and approximately 5 times lower levels of the maximum piezoelectric charges in the GaAs substrate.

Finally, the threshold voltages have been estimated for the 0.5, 0.7, 1.0 and 2.0 μm gate-length EPI-P MESFETs. The piezoelectric charge has been calculated for the three aforementioned structures with both the tensile and compressive stress in the dielectric. The results are shown in Fig. 4.17.

Lg=0.7 μm, EPI-P

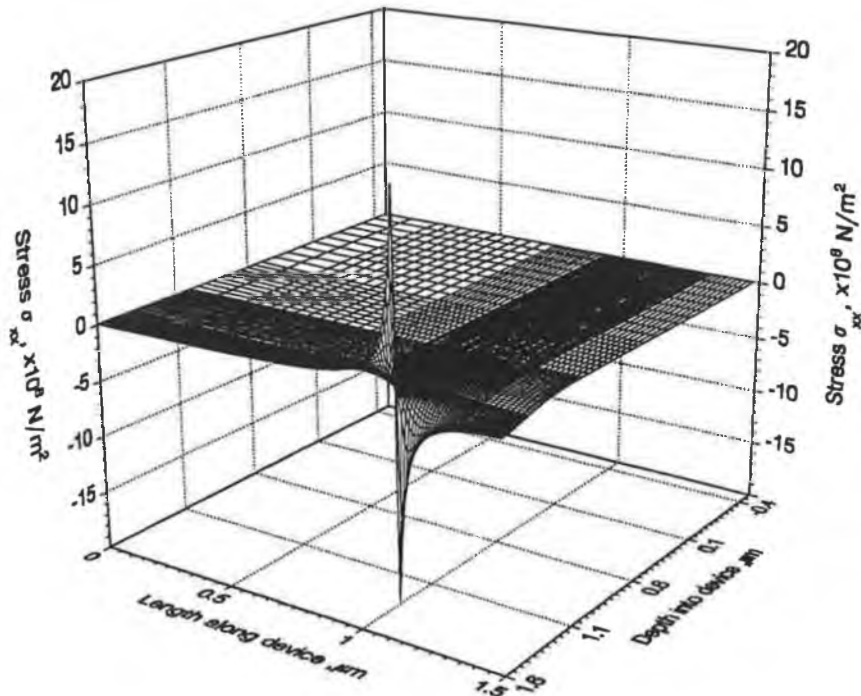

Figure 4.11: Stress σ_{xx} calculated by the FEM method for the 0.7 μm EPI-P MESFET for the GaAs structure, i.e. no dielectric and no metal gate. Only one half of the simulated region is shown (the source side, from x = 0 to x = 1.45 μm) because the stress is symmetric around the gate centre. The gate metal is deposited on the x-y surface at z=1.6 μm between the points x=1.1 μm and x=1.8 μm (the x axis is denoted as 'Length along device', the z axis is denoted as 'Depth into device', and the y axis is not shown on the graph).

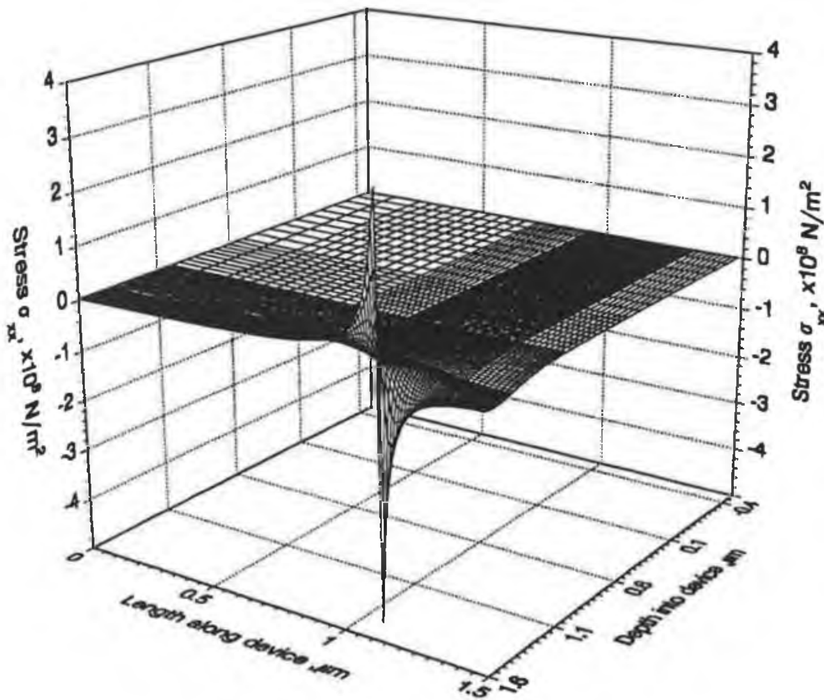

Figure 4.12: Stress σ_{xx} calculated by the FEM method for the 0.7 μm EPI-P MESFET for the metal/GaAs structure, i.e. no dielectric. Only one half of the simulated region is shown (the source side, from $x = 0$ to $x = 1.45$ μm) because the stress is symmetric around the gate centre. The gate metal is deposited on the x-y surface at z=1.6 μm between the points x=1.1 μm and x=1.8 μm (the x axis is denoted as 'Length along device', the z axis is denoted as 'Depth into device', and the y axis is not shown on the graph).

Lg=0.7 μm, EPI-P

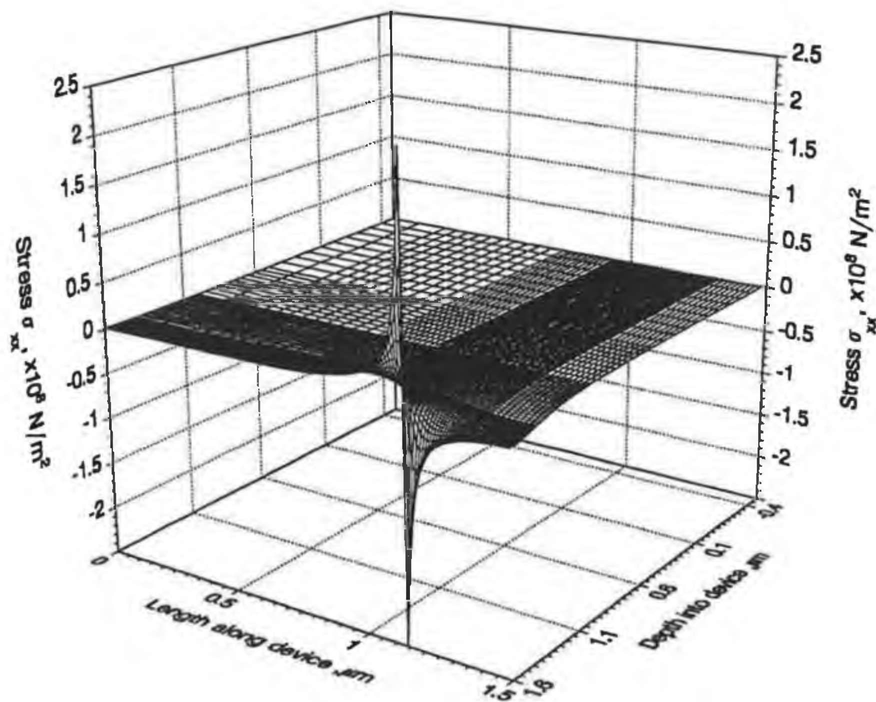

Figure 4.13: Stress σ_{xx} calculated by the FEM method for the 0.7 μm EPI-P MESFET for the metal/dielectric/GaAs structure. Only one half of the simulated region is shown (the source side, from x = 0 to x = 1.45 μm) because the stress is symmetric around the gate centre. The gate metal is deposited on the x-y surface at z=1.6 μm between the points x=1.1 μm and x=1.8 μm (the x axis is denoted as 'Length along device', the z axis is denoted as 'Depth into device', and the y axis is not shown on the graph).

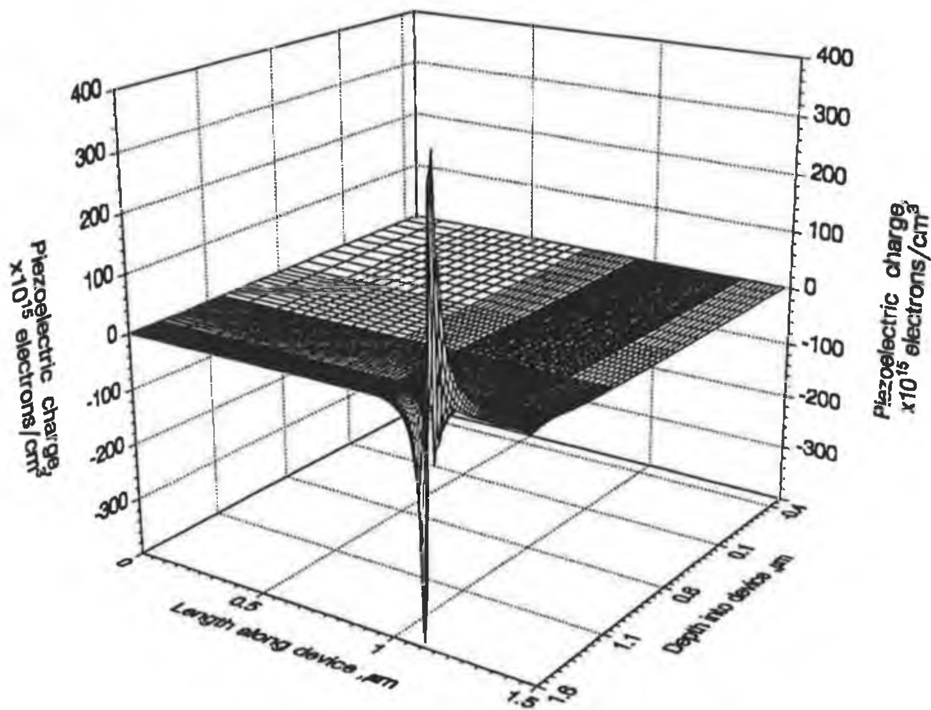

Figure 4.14: Piezoelectric charge ρ_{pz} calculated by the FEM method for the 0.7 μm EPI-P MESFET for the GaAs structure. Only one half of the simulated region is shown (the source side, from $x = 0$ to $x = 1.45$ μm) because the charge is symmetric around the gate centre. The gate metal is deposited on the x-y surface at z=1.6 μm between the points x=1.1 μm and x=1.8 μm (the x axis is denoted as 'Length along device', the z axis is denoted as 'Depth into device', and the y axis is not shown on the graph).

Lg=0.7 μm, EPI-P

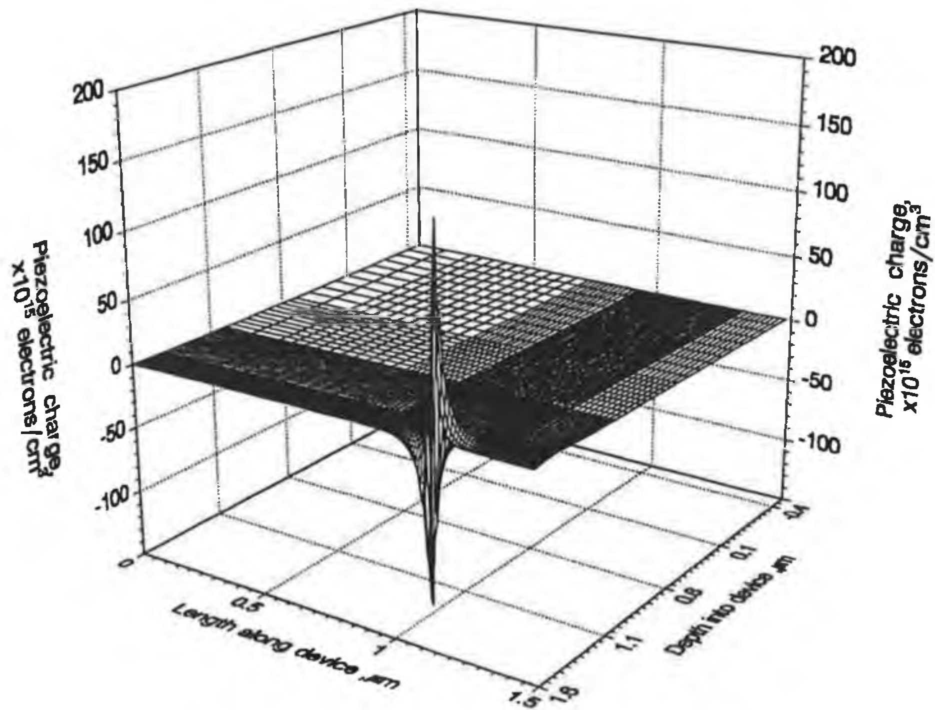

Figure 4.15: Piezoelectric charge ρ_{pz} calculated by the FEM method for the 0.7 μm EPI-P MESFET for the metal/GaAs structure. Only one half of the simulated region is shown (the source side, from $x = 0$ to $x = 1.45$ μm) because the charge is symmetric around the gate centre. The gate metal is deposited on the x-y surface at z=1.6 μm between the points x=1.1 μm and x=1.8 μm (the x axis is denoted as 'Length along device', the z axis is denoted as 'Depth into device', and the y axis is not shown on the graph).

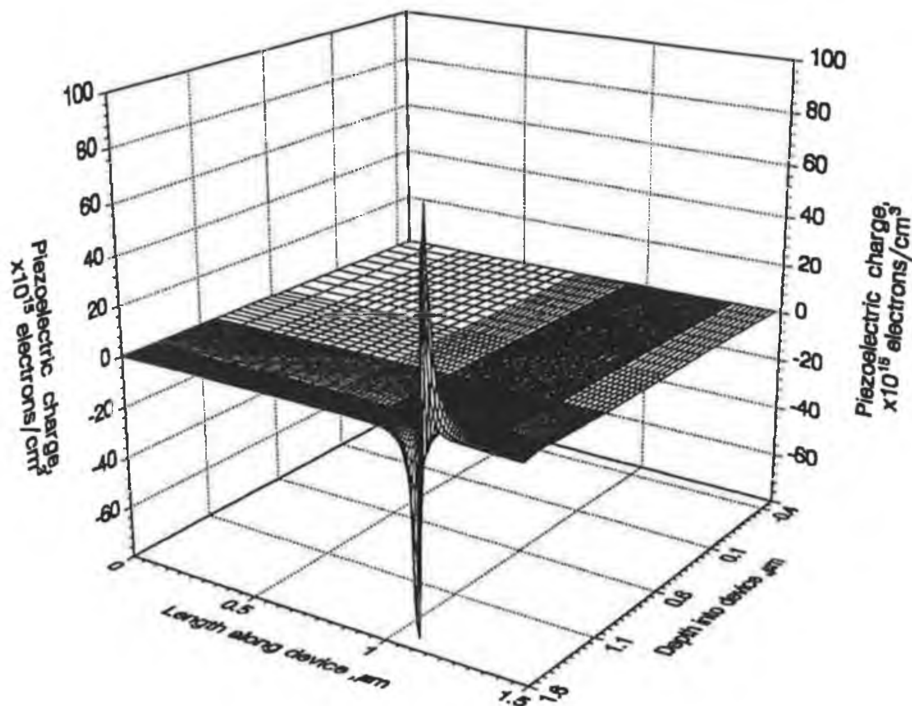

Figure 4.16: Piezoelectric charge ρ_{pz} calculated by the FEM method for the 0.7 μm EPI-P MESFET for the metal/dielectric/GaAs structure. Only one half of the simulated region is shown (the source side, from $x = 0$ to $x = 1.45$ μm) because the charge is symmetric around the gate centre. The gate metal is deposited on the x-y surface at z=1.6 μm between the points x=1.1 μm and x=1.8 μm (the x axis is denoted as 'Length along device', the z axis is denoted as 'Depth into device', and the y axis is not shown on the graph).

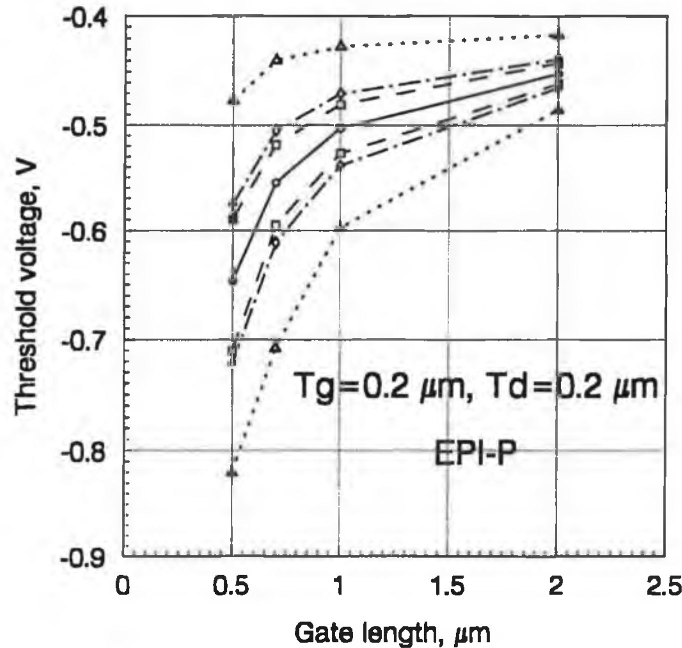

Figure 4.17: Dependence of the threshold voltage on the gate length for the EPI-P simulations. The piezoelectric charge has been calculated for the GaAs (unscaled piezoelectric charge) (dots), metal/GaAs (dash-dot line) and metal/dielectric/GaAs (dashed line) structures with both the tensile and compressive stress in the dielectric. The threshold voltages above the reference case (full line) have been obtained for compressive stress in the dielectric ($\sigma_d = -2 \cdot 10^8$ N/m^2) and the threshold voltages below the reference line have been obtained for tensile stress in the dielectric ($\sigma_d = 2 \cdot 10^8$ N/m^2).

When inspecting the maximum positive and negative piezoelectric charges, it was noticed that they did not depend on the gate length. The main difference among the piezoelectric charges for differing gate lengths was in the region down the middle of the gate. Fig. 4.18 demonstrates the piezoelectric charge down the middle of the gate obtained for the metal/dielectric/GaAs structure for the 0.5, 0.7, 1.0 and 2.0 μm gate-length EPI-P MESFETs.

A note should be made on the idea of using maximum stress and charge values for comparison although it has been already mentioned that the maximum values of stresses depend on the mesh size. The comparisons performed above are meaningful in the sense that the same mesh has been used for all stress and charge calculations.

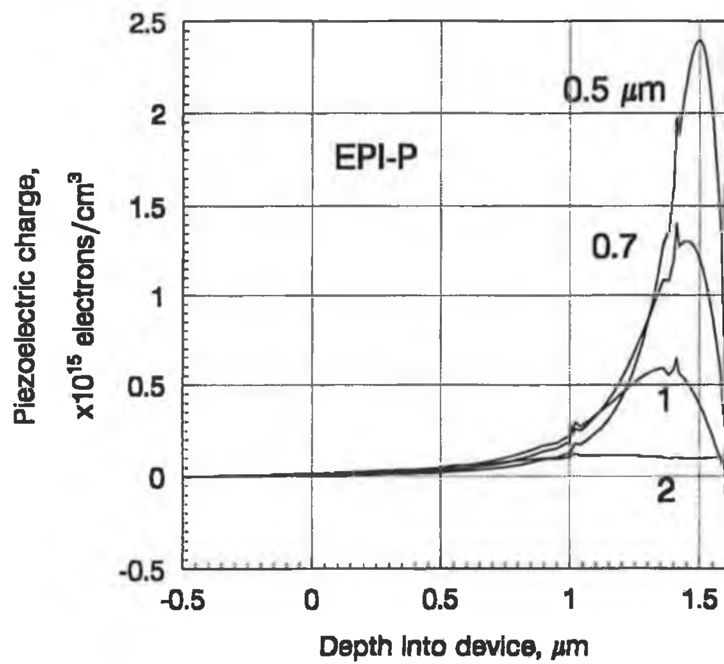

Figure 4.18: Piezoelectric charge ρ_{pz} down the middle of the gate calculated by the FEM method (metal/dielectric/GaAs structure) for the 0.5, 0.7, 1.0 and 2.0 μm gate-length EPI-P MESFETs.

4.3.4 Comparison of different load models

Up to now two horizontal forces acting at the edges of the dielectric opening have been used to model the stress produced by the dielectric layer deposited on the GaAs substrate. The magnitude of the forces is

$$|F_l| = |\sigma_d| T_d \tag{4.61}$$

where T_d is the dielectric thickness and σ_d is an average stress in the dielectric. The model is simple and physically reasonable. The physicality of the model is justified by the fact that σ_d can be estimated by measuring the curvature of the dielectric layer deposited on the substrate. The principle of neglecting the gate metal when estimating the magnitude of the load is also justified because experiments clearly show that the influence of the gate metal is of minor importance [16, 19]. This model will be called the force model or the F_l model.

Another way of introducing the stress into the GaAs substrate is to define a uniform displacement $\boldsymbol{u}$ at the right edge of the simulated region used in the stress analysis (see Fig. 4.3). This type of load represents a good physical representation of the stresses exerted on the GaAs substrate by externally applied loads [21, 22, 23, 24]. In this case there is no direct way of relating the magnitude of the uniform displacement at the right edge to the average dielectric stress obtained by the substrate curvature measurements. This model will be called the uniform displacement model or the $\boldsymbol{u}$ model.

While the inclusion of the force model into the FEM program is straightforward, the uniform displacement model is implemented in two steps. The first step consists of applying the Payne-Irons method [75] on (4.46)

$$\boldsymbol{K}^e \boldsymbol{a}^e = \boldsymbol{F} \tag{4.62}$$

in such a way that the displacement of the nodes at the right boundary (see Fig. 4.3) are all equal. The Payne-Irons method is a simple way of imposing Dirichlet type conditions, i.e. the nodal displacements, without incurring the cost of reordering and right-hand side modifications. Once the solution for the displacements $\boldsymbol{a}^e$ is obtained and the stress and strain fields are calculated, the strain ε_x at the right boundary of the simulated region used in the FEM calculation is scanned and all results are multiplied by the number that gives the strain $\varepsilon_x = 0.001$ at the right boundary. Thus, by means of the aforementioned first step, the uniform displacement at the right boundary is ensured,

while the second step produces a well defined elongation of the structure in the x direction that might be used as a basis of comparison among different gate length MESFETs.

Note that the multiplication of all results by a fixed number is valid from the solution point of view due to the fact that the stress problem, as presented here, is a linear elasticity problem.

Figs. 4.19 and 4.20 show the σ_{xx} stress distribution of the 0.7 μm gate-length EPI-P MESFET obtained by the application of the force model and the uniform displacement model, respectively, for the metal/dielectric/GaAs structure.

Note that the far-field stress for the force model tends to zero, while the uniform displacement model produces a high far-field stress. Furthermore, the stress caused by the uniform displacement model is tensile in the whole GaAs substrate. As the piezoelectric charge is proportional to the gradient of the stress (see Eq. (4.28)), the difference in the absolute values of stresses does not represent a real obstacle. To compare the two load models the stress distribution for both load models down the middle of the gate is shown in Fig. 4.21.

For the force model the total change of stress from the top of the structure ($z = 1.6$ μm) to the bottom ($z = -0.5$ μm) is $|\Delta\sigma_{xx}| = 0.226 \cdot 10^8$ N/m^2, while the stress change for the uniform displacement model is $|\Delta\sigma_{xx}| = 0.347 \cdot 10^8$ N/m^2.

The ratio between the $|\Delta\sigma_{xx}|$ value for the force model and the $|\Delta\sigma_{xx}|$ value for the uniform displacement model is 0.65 down the middle of the gate and 0.38 at the right boundary of the simulated region.

To be able to compare the load models, the piezoelectric charge obtained by the uniform displacement model has been multiplied by 0.65, which is equivalent to the reduction of the strain or displacements defined at the right boundary to 65% of the initial value. As a result $|\Delta\sigma_{xx}|$ obtained by the uniform displacement model has been reduced to $0.226 \cdot 10^8$ N/m^2, i.e. the value obtained by the force model down the middle of the gate. This operation is physically correct due to the fact that the stress problem presented here is a linear elasticity problem. Then, the EVEREST simulator is invoked to extract the threshold voltage.

The same procedure has been repeated for the 0.5, 1.0 and 2.0 gate-length EPI-P MESFETs for both tensile and compressive dielectric stress (compres-

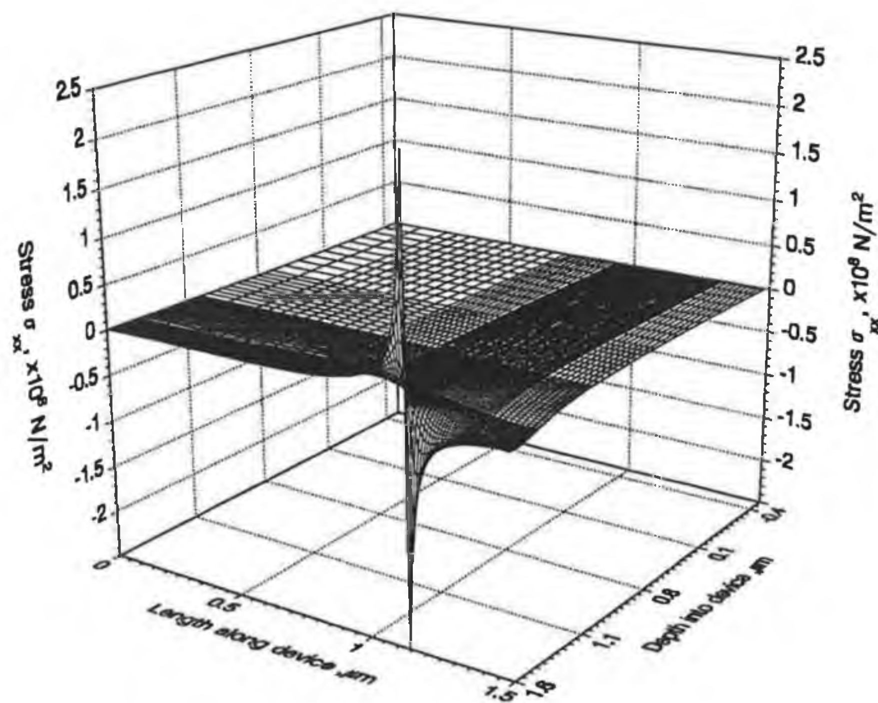

Figure 4.19: Stress σ_{xx} calculated by the FEM method for the 0.7 μm EPI-P MESFET for the metal/dielectric/GaAs structure obtained by the application of the force model ($|F_l|$ = 40 N/m). Only one half of the simulated region is shown (the source side, from x = 0 to x = 1.45 μm) because the stress is symmetric around the gate centre. The gate metal is deposited on the x-y surface at z=1.6 μm between the points x=1.1 μm and x=1.8 μm (the x axis is denoted as 'Length along device', the z axis is denoted as 'Depth into device', and the y axis is not shown on the graph).

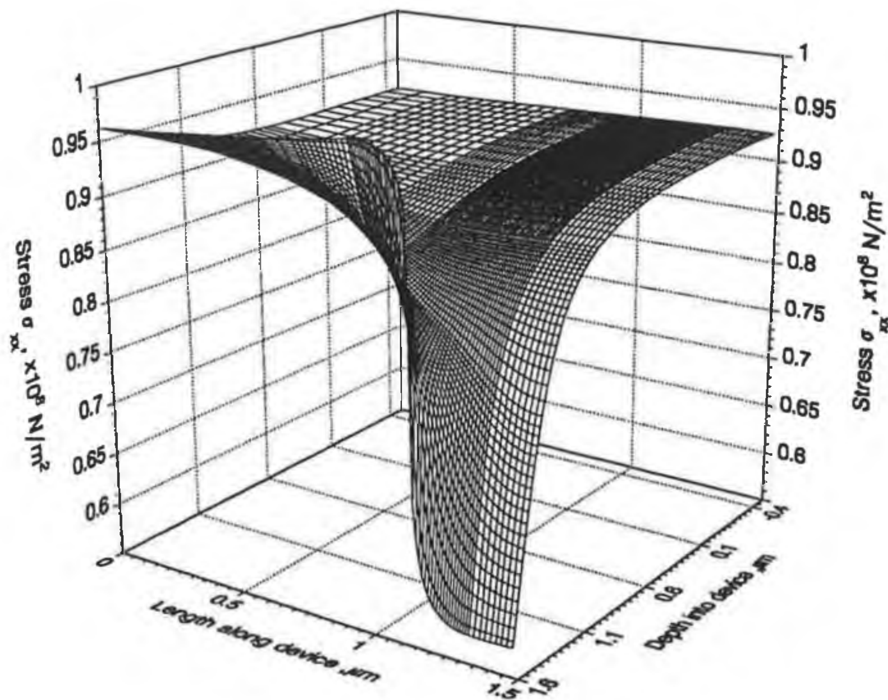

Figure 4.20: Stress σ_{xx} calculated by the FEM method for the 0.7 μm EPI-P MESFET for the metal/dielectric/GaAs structure obtained by the application of the uniform displacement model ($\varepsilon_x = 0.001$). Only one half of the simulated region is shown (the source side, from $x = 0$ to $x = 1.45$ μm) because the stress is symmetric around the gate centre. The gate metal is deposited on the x-y surface at z=1.6 μm between the points x=1.1 μm and x=1.8 μm (the x axis is denoted as 'Length along device', the z axis is denoted as 'Depth into device', and the y axis is not shown on the graph).

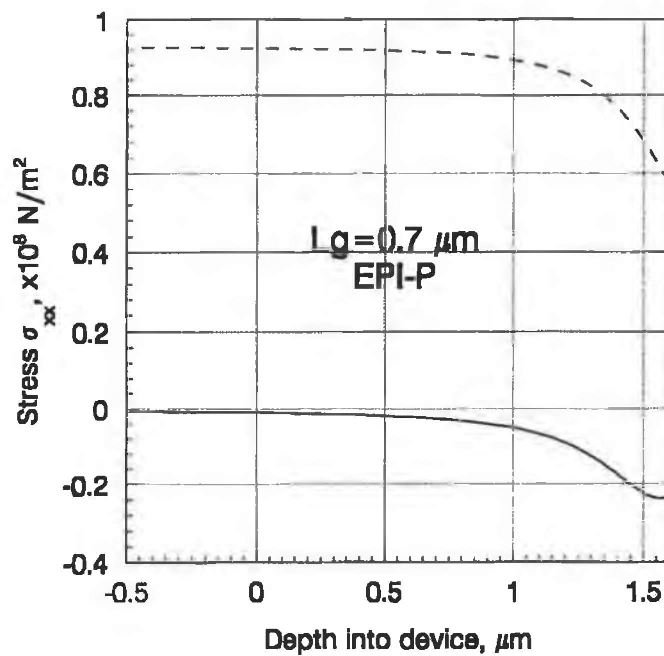

Figure 4.21: Stress σ_{xx} for the 0.7 μm EPI-P MESFET down the middle of the gate (at $x = 1.45$ μm) calculated by applying the force model (full line) and the uniform displacement model (dashed line).

L_g (μm)	0.5	0.7	1.0	2.0
constant	0.882	0.650	0.493	0.473

Table 4.3: The multiplying constants used to reduce the $|\Delta\sigma_{xx}|$ value obtained by the uniform displacement model to the value obtained by the force model. These constants are actually used to multiply the piezoelectric charge obtained by the uniform displacement model.

sive dielectric stress is simulated by defining a negative displacement $\boldsymbol{u}$ at the right boundary of the simulated region used in the stress analysis). The constants used to reduce the $|\Delta\sigma_{xx}|$ value obtained by the uniform displacement model to the value obtained by the force model are shown in Table 4.3.

The threshold voltages obtained are shown in Fig. 4.22. It can be noticed that the threshold voltage shifts resulting from the uniform displacement model are lower. If we wanted to reproduce the same $|\Delta\sigma_{xx}|$ down the right boundary of the simulated region, we would have to use the following multiplying constants: 0.15, 0.38, 0.48 and 0.51 for the gate lengths 0.5, 0.7, 1.0 and 2.0 μm, respectively. Comparing these constants with the constants given in Table 4.3 it might be supposed that the threshold voltage shifts would be even lower for the gate lengths 0.5 and 0.7 μm.

The reason for obtaining lower threshold voltage shifts by the uniform displacement model becomes obvious after inspecting the charge down the middle of the gate obtained by the two load models (see Fig. 4.23). As the charge inside the active channel, from $z = 1.6$ μm to $z = 1.5$ μm, is screened by the heavy donor doping of $N_D = 2.3 \cdot 10^{17}$ cm^{-3}, higher piezoelectric charge at the active channel/substrate boundary will result in larger threshold voltage shift. Although $|\Delta\sigma_{xx}|$ is the same for both load models, the piezoelectric charge obtained by the uniform displacement model reaches maximum closer to the surface, but at the channel/substrate interface its value is lower.

In conclusion, the use of the force load model is strongly recommended for a number of reasons:

1. The magnitude of the forces used to model the stress produced by the dielectric overlayer can be estimated by measuring the dielectric thickness and the average dielectric stress, thus ensuring the physicality of the simulation.

2. The accuracy of the force model implemented into the FEM method can be estimated by comparison with the analytical method in the case when

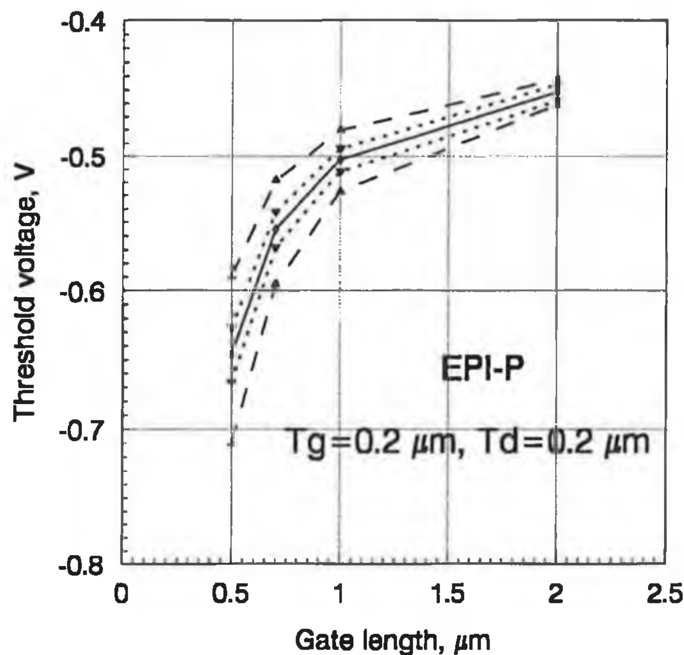

Figure 4.22: Dependence of the threshold voltage on the gate length for the EPI-P simulations. The values for the reference simulation (full line), the force model (dashed line) and the scaled uniform displacement model (dotted line) are shown. The multiplying constants used to scale the piezoelectric charge of the uniform displacement model are given in Table 4.3. The piezoelectric charge has been calculated for the metal/dielectric/GaAs structures with both the tensile and compressive stress in the dielectric. The threshold voltages above the reference case (full line) have been obtained for compressive stress in the dielectric ($\sigma_d = -2 \cdot 10^8$ N/m^2) and the threshold voltages below the reference line have been obtained for tensile stress in the dielectric ($\sigma_d = 2 \cdot 10^8$ N/m^2).

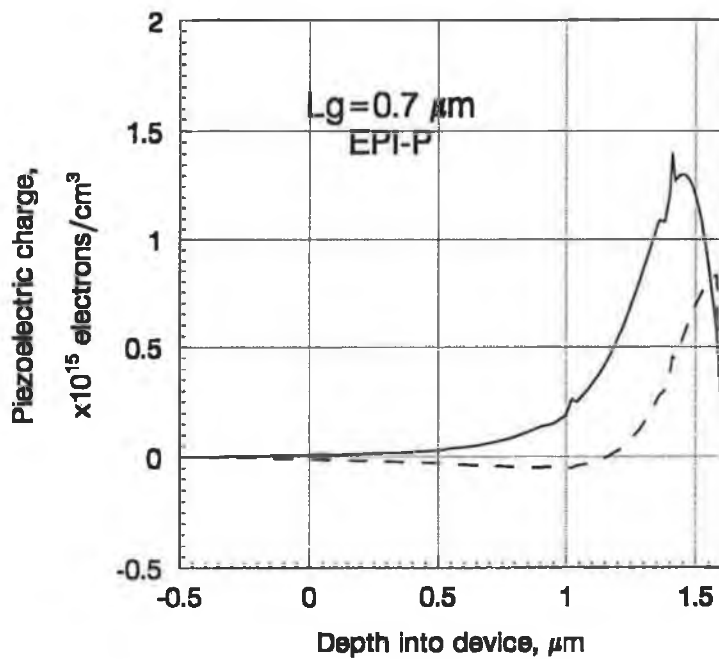

Figure 4.23: Piezoelectric charge ρ_{pz} down the middle of the gate calculated by the FEM method (metal/dielectric/GaAs structure) for the 0.7 μm gate-length EPI-P MESFET: force model (full line) and uniform displacement model (dashed line). The $|\Delta\sigma_{xx}|$ value is the same for both load models, i.e. the piezoelectric charge obtained by the uniform displacement model is multiplied by 0.65.

only GaAs substrate is taken into account.

3. It is not clear how to relate the measured average dielectric stress to the uniform displacement load model.

The fact that in [23] a good agreement was found between the experimental results with externally applied load and the simulated results with the uniform displacement model confirms that the uniform displacement model accurately models the externally applied load and, what is even more important, as the uniform displacement model is a good representation of the externally applied load, it indirectly confirms that the coupled system of electrical and mechanical quantities may be solved in a decoupled form, as it is done in [23, 24] and in this work.

When considering the analytical method, the main disadvantage is the inability to include the dielectric layer into the calculation of the stress distributions. This problem makes the results unreliable within the region of radius of two dielectric thicknesses around the gate edges. For a typical dielectric thickness of 0.2 μm, this region extends into the depth of 0.4 μm which is much more than the usual active channel thickness of 0.1 μm. This problem is easily overcome by the FEM method.

When considering high stress peaks that appear when the force load model is applied (see Fig. 4.19), it should be noted that in practice plastic deformation limits the stresses to finite values.

Chapter 5

Electrical characteristics

In this chapter the electrical characteristics of epitaxial and ion-implanted MESFETs are discussed. The influence of varying gate length, substrate doping and stress-induced piezoelectric charge on transfer characteristics, transconductance, threshold voltage, subthreshold current slope and output resistance is presented. The explanations for underlying physical mechanisms are given as well.

There are a number of reasons why the aforementioned electrical characteristics are discussed. The threshold voltage is important to both digital- and analogue-design engineers. While an analogue-design engineer is relatively tolerant towards the value of the threshold voltage, a digital-design engineer not only requires a well defined value of the threshold voltage, but also requires a standard deviation of a threshold voltage on the order of 25 mV or less for LSI and VLSI ICs. In GaAs IC design the rule that all MESFET gates on a wafer must run in the same direction [8] is a consequence of orientation effects or stress-induced piezoelectric charge. Closely related to the theshold voltage is the subthreshold current slope which is an indicator of the effectiveness of the device's switch-off mechanism. A lower value of subthreshold current slope indicates that a MESFET can be switched from the logic state '1' to the logic state '0' with a smaller change of input voltage. This characteristic also influences the noise margin of digital ICs. The transconductance is important for an analogue-design engineer because it defines the small-signal voltage gain of the electronic circuit, while a digital-design engineer is concerned with the value of transconductance because it defines the capability of a MESFET to drive the next stage. Knowledge of the transfer characteristic is crucial because it actually contains all this information, i.e. the threshold voltage, subthreshold current slope and transconductance. Furthermore, for an analogue-design

engineer the shape of the transfer characteristic is important by itself because it shows whether an efficient frequency mixer or frequency multiplier can be built, or it may indicate possible problems with intermodulation and higher harmonics of input signals. Finally, a low output resistance represents a sink for the drain current and it is reflected as decreased capability of driving the next stage or reduced voltage gain.

When the piezoelectric charge is included in the device simulation, unless it is explicitly said otherwise, the stress simulation is performed for the metal/dielectric/GaAs structure with a gate metal thickness $T_g = 0.2$ μm. The stress imparted to the GaAs substrate is modelled by the force load model: the intrinsic dielectric stress is tensile $\sigma_d = 2 \cdot 10^8$ N/m^2 and the dielectric thickness is $T_d = 0.2$ μm. The piezoelectric charge is calculated for the $[01\bar{1}]$ MESFET. Such a definition of the MESFET orientation and load produces compressive stress under the gate and the piezoelectric charge under the gate is predominantly positive.

It must be noted that few of the references that present experimental data give thorough information about the MESFET geometry, doping profile and electrical characteristics necessary for the device simulation and subsequent comparison of results. As such a situation has rendered the quantitative comparison unmanageable, the qualitative comparison with an accent on the correct trends for varying simulation parameters has become the main working tool. The references concerned with the topic discussed are abundantly cited throughout this chapter.

When considering the published experimental data, the references should be divided into two categories:

- Experiments on 'hot' MESFETs [15]-[20]: contrary to what the word 'hot' suggests, these experiments are conducted at the room temperature. The word 'hot' is used to emphasize that the stress had been introduced to the device via the cooling stage after the gate metal and dielectric layer have been evaporated onto the GaAs substrate.

- Experiments with externally applied load [21]-[24].

Although both types of experiments clearly show the piezoelectric nature of the shifts in electrical characteristics, there is a remarkable difference in the interpretation of the physical mechanisms that occur, as will be shown. Where

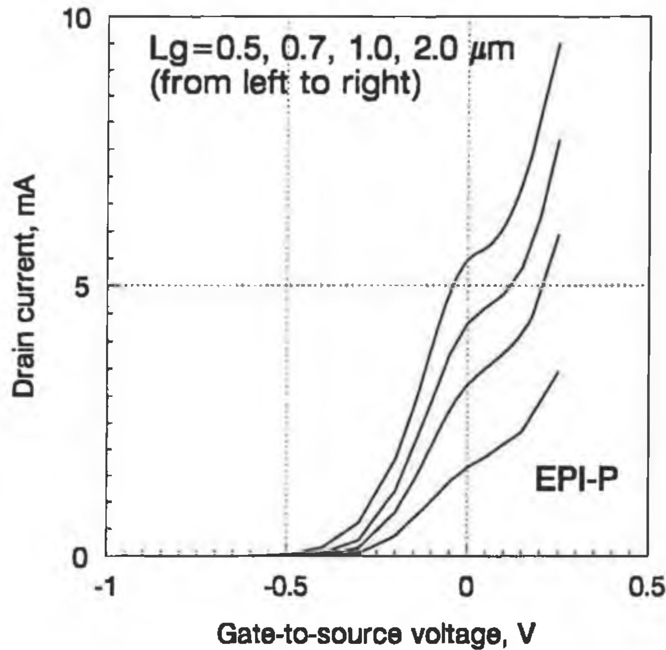

Figure 5.1: Transfer characteristics for the EPI-P simulations at $V_{DS} = 1$ V. The EPI-P simulations have been performed with $N_A = 5 \cdot 10^{15}$ cm^{-3}.

there is a conflict between experimental data, the results obtained for the 'hot' MESFETs are to be considered more reliable.

When considering the numerical stress simulation [23, 24] in relation to experiments, it is necessary to say that unless extreme care is taken over the physical interpretation of the results, the simulation results lead to incorrect conclusions.

5.1 Transfer characteristics

The transfer characteristics for the 0.5, 0.7, 1.0 and 2.0 μm gate-length EPI-P MESFETs are shown in Fig. 5.1 (compare with the characteristics given in Fig. 3.19 where the drain current is given in logarithmic scale). The linear plot of the drain current reveals kinks in the transfer characteristics around $V_{GS} = 0$ V.

To make sure that the kinks are not a consequence of numerical instabilities of the device simulator, the calculation of the transfer characteristics for the 0.5 and 1.0 μm gate-length EPI-P MESFETs has been repeated with the step $\Delta V_{GS} = 10$ mV in the V_{GS} range from -0.15 V to 0.18 V (Fig. 5.2). It can be

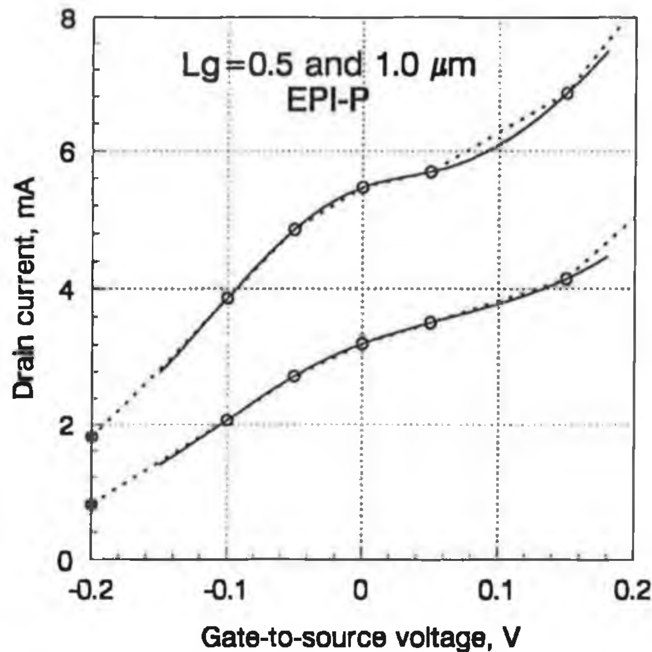

Figure 5.2: Transfer characteristics for the 0.5 and 1.0 μm gate-length EPI-P simulations at $V_{DS} = 1$ V (enlargement of the Fig. 5.1 around $V_{GS} = 0$ V).

seen that the change of I_D is smooth around $V_{GS} = 0$ V.

On the other hand, the transfer characteristics for the ION-P MESFETs show no noticeable evidence of such kinks (Fig. 5.3).

It should be noted that all these characteristics are given for the reference cases, i.e. no piezoelectric charge has been taken into account. It can be speculated that the reason for the appearance of kinks might be related to the different doping profiles of epitaxial and ion-implanted MESFETs and consequently, to the way electrons are confined within the channel. The problem of kinks will be readdressed later in this section.

Fig. 5.4 presents the influence of the piezoelectric charge on the EPI-P transfer characteristics. The piezoelectric charge is calculated by the FEM method using the force load model. The shift of the transfer characteristics towards more negative V_{GS} voltages is a result of predominantly positive induced charge under the gate. The positive piezoeletric charge under the gate attracts electrons from the bulk of GaAs and consequently increases the substrate current. If the piezoelectric charge under the gate is predominantly negative, the transfer characteristics are shifted towards more positive V_{GS} voltages with respect to the characteristics for the reference EPI-P simulations (Fig. 5.5).

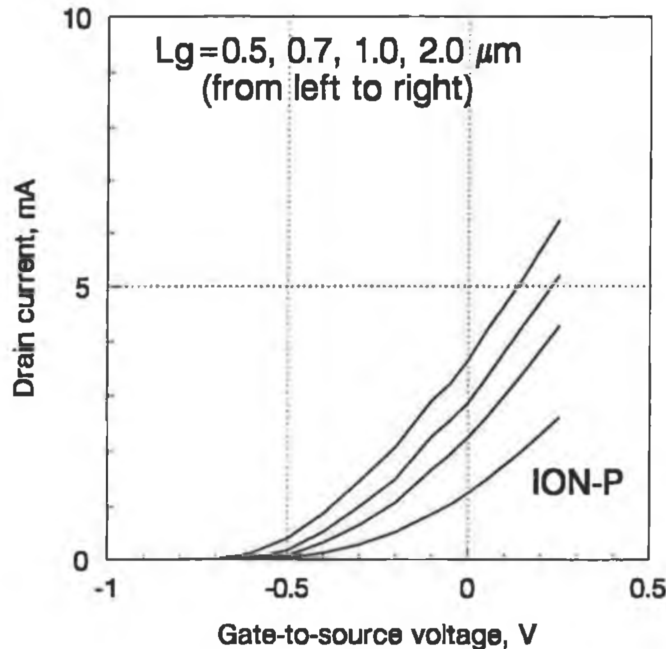

Figure 5.3: Transfer characteristics for the ION-P simulations at $V_{DS} = 1$ V. The ION-P simulations have been performed with $N_A = 5 \cdot 10^{15}$ cm^{-3}.

A predominantly positive piezoelectric charge under the gate appears in the $[01\bar{1}]$ orientated MESFETs (the orientation used throughout this study) if the dielectric stress is tensile ($\sigma_d > 0$), i.e. if the region under the gate is under compression. Equivalently, the charge under the gate is also mostly positive for the [011] MESFETs when the dielectric stress is compressive.

A very similar impact of the piezoelectric charge on the transfer characteristics of the ION-P MESFETs has been obtained (the graphs are not shown as they essentially add no more information to what has already been said).

To readdress the problem of kinks in the transfer characteristics it is necessary to establish two facts: 1) the transfer characteristics of epitaxial MESFETs show more pronounced kinks than the characteristics of the ion-implanted MESFETs, 2) the kink form varies with gate length. From the first fact it can be concluded that the doping profile at the active channel/substrate interface plays a significant role in determing the magnitude of the kink. It is apparently the existence of an abrupt change of the donor concentration when going from the active channel into the substrate that pronounces the appearance of kinks.

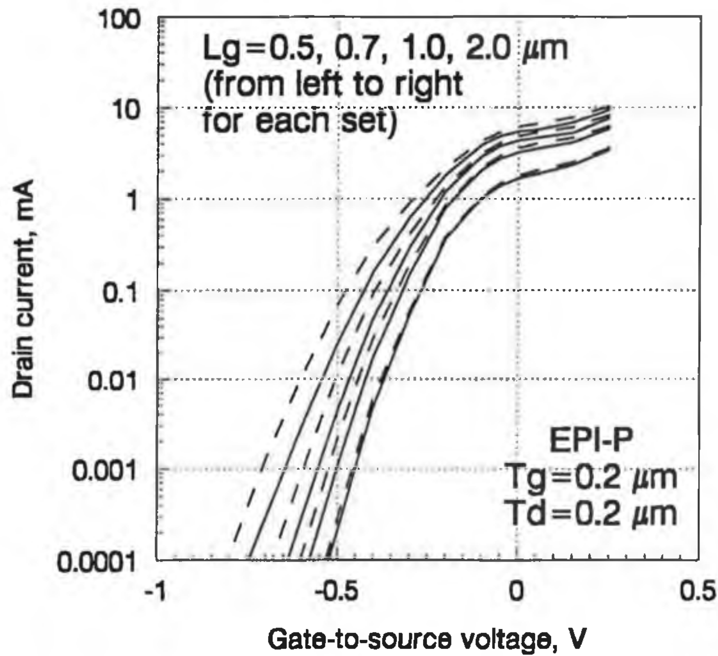

Figure 5.4: Transfer characteristics for the EPI-P simulations at V_{DS} = 1 V: reference case (full line), predominantly positive piezoelectric charge under the gate (dashed line).

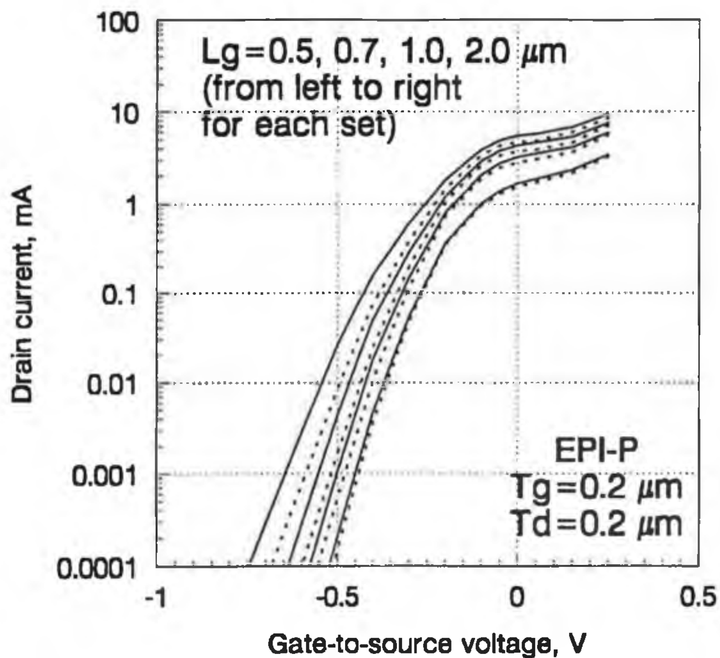

Figure 5.5: Transfer characteristics for the EPI-P simulations at V_{DS} = 1 V: reference case (full line), predominantly negative piezoelectric charge under the gate (dotted line).

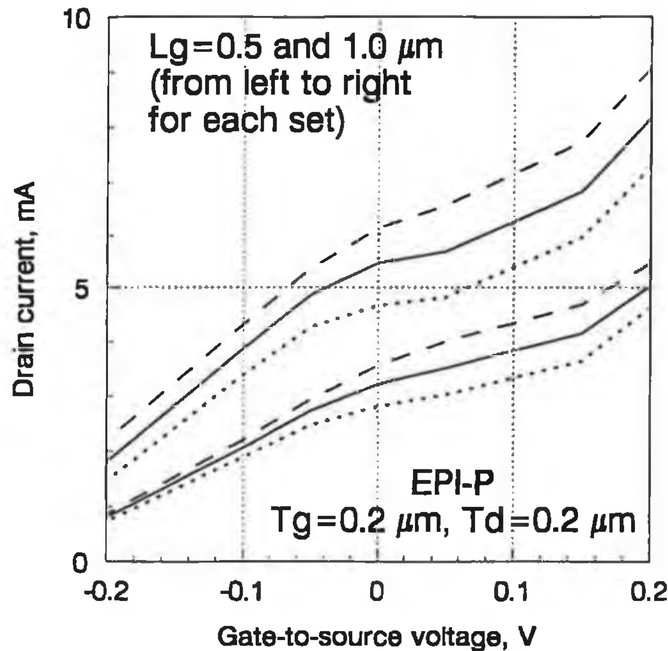

Figure 5.6: Transfer characteristics for the 0.5 μm (top set) and 1.0 μm (bottom set) gate-length EPI-P simulations at V_{DS} = 1 V: reference case (full line), predominantly positive piezoelectric charge (dashed line) and predominantly negative piezoelectric charge (dotted line) under the gate.

A confirmation for this conclusion is given in Figs. 5.6 and 5.7 which show enlargements of the transfer characteristics around V_{GS} = 0 V for the EPI-P and ION-P MESFETs respectively. Each figure presents the transfer characteristics for the 0.5 and 1.0 μm gate-length MESFETs. Apart from the transfer characteristics for the reference cases, i.e. no piezoelectric charge taken into account, the transfer characteristics for the predominantly positive and predominantly negative piezoelectric charge under the gate have been added.

Fig. 5.6 clearly demonstrates that the kink is less pronounced for the predominently positive piezoelectric charge which conforms with the aforementioned line of reasoning, which states that predominently positive piezoelectric charge effectively reduces the abruptness of the doping profile at the active channel/substrate interface. Equivalently, mostly negative piezoelectric charge below the gate reduces the ability of electrons to penetrate into the substrate, increases the confinement of electrons and effectively accentuates the abruptness of the doping profile at the interface. The transfer characteristics for the ION-P MESFETs (see Fig. 5.7) show the same pattern although less pronounced.

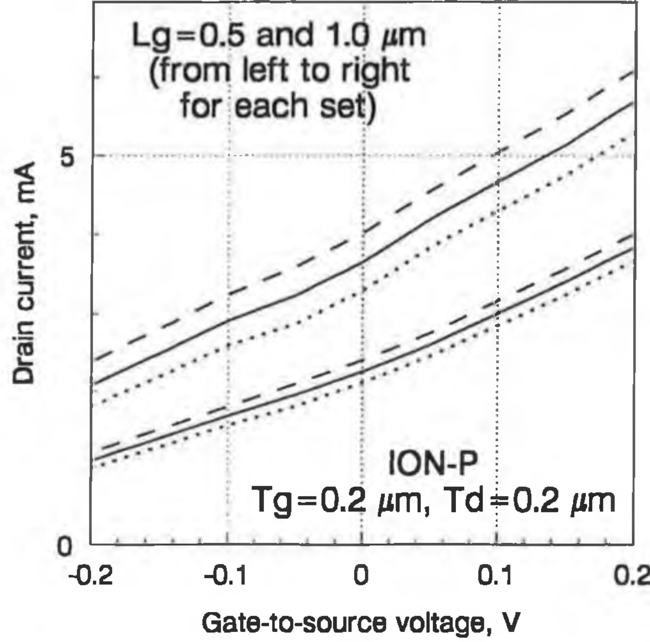

Figure 5.7: Transfer characteristics for the 0.5 μm (top set) and 1.0 μm (bottom set) gate-length ION-P simulations at $V_{DS} = 1$ V: reference case (full line), predominantly positive piezoelectric charge (dashed line) and predominantly negative piezoelectric charge (dotted line) under the gate.

The second fact, variations of the kink shape with varying gate lengths, suggests that the effective resistance of the electron path also influences the shape of kinks. The kink in the transfer characteristic for the 0.5 μm gate-length EPI-P MESFET is sharper and occurs over a smaller V_{GS} range than the kink for e.g. the 1 μm gate-length MESFET, indicating that longer gate lengths smooth the kink effect (see Fig. 5.2).

However, although all this reasoning has clarified the circumstances under which kinks are more probable to appear, it has not actually revealed their source. In an attempt to find out the physical mechanism that produces kinks, it is convenient to approximate the drain current by

$$|\vec{I_D}| \doteq qSn\mu_n|\vec{E}| \tag{5.1}$$

where q is the electronic charge, S is the effective area, n is the electron concentration, μ_n is the electron mobility and $\vec{E}$ is the electric field. The electron concentration, electron mobility and electric field should be considered here as average quantites. The effective area S is the product of the gate width (the longest gate dimension, being 250 μm for the epitaxial MESFETs) and the effective channel thickness. The effective channel thickness is the active

channel thickness (0.1 μm for the EPI MESFETs), minus the thickness of the gate depletion region, plus the effective depth of electron penetration into the substrate.

When the gate-to-source voltage changes from a positive value ($V_{GS} > 0$) towards the threshold voltage, the following actions take place:

1. the thickness of the gate depletion region increases reducing the effective channel thickness;

2. the electron concentration decreases in the channel;

3. electrons are pushed into the substrate, thus increasing the effective channel thickness;

4. electrons pushed into the substrate have higher impurity dependent mobility due to lower doping concentration (see Eq. (3.54));

5. the final value of the electron mobility in the active channel as well as in the substrate is determined by the value of the electric field (see Eq. (3.55));

6. the electric field changes in such a way that the basic semiconductor equations (3.19)–(3.23) are satisfied.

In general, when the gate-to-source voltage decreases, the mechanisms that reduce the current prevail. However, when approaching the kink region some of the aforementioned mechanisms tend to keep the drain current at a constant level (see Fig. 5.2), causing the kink effect.

The following mechanism had been singled out as a possible explanation for the kink: if a substantial number of electrons is pushed into the substrate, the decrease of the effective channel thickness and overall electron concentration may be counteracted by increased electron mobility of the electrons pushed into the substrate.

To test this hypothesis, the impurity-dependent mobility model has been disabled and the impurity-dependent electron mobility has been set to a constant value of $\mu_n^I = 5316$ cm^2/V·s in the whole simulation region. This value is the value of μ_n^I in the active channel when the impurity-dependent mobility model is used. If the hypothesis is correct, the drain current for $V_{GS} = 0.25$ V (the most positive V_{GS} voltage used in the previous simulations) has to be very similar to the value obtained by the impurity-dependent mobility because most

of the electrons are in the active channel for the positive gate-to-source voltage. When decreasing the gate-to-source voltage, no kink effect is to appear.

The simulation has shown not only the kink effect, but the drain currents were almost the same (the difference being in the fifth significant digit) as the currents obtained with the impurity-dependent mobility model.

Thus, the hypothesis has become an erroneous theory. This simulation has also shown that the electrons which ultimately determine the value of current, i.e. the electrons in the narrowest current filament, whether they are in the channel or in the substrate, travel at the saturation velocity rendering the value of the impurity dependent mobility unimportant. It has also been learned that the source of the kink effect is hidden either in the dependence of the effective channel thickness or(and) electron concentration on V_{GS}.

Finally, after it had been decided to leave the problem open, the plot of output characteristics of the 0.7 μm gate-length EPI-P MESFET had shown very interesting features (see Figs. 5.8 and 5.9). At drain-to-source voltage $V_{DS} = 0.2$ V the drain current for $V_{GS} = 0$ V is higher than the drain current at $V_{GS} = 0.1$ V. The transfer characteristic has been recalculated for $V_{DS} = 0.2$ V for V_{GS} in the range from -0.2 V to 0.2 V (see Fig. 5.10) and the aforementioned region of negative gradient of I_D has appeared, as well as an explanation for the underlying physical mechanism. Firstly, for low drain-to-source voltages most electrons have velocities below the peak velocity because of small electric field (see Fig. 3.4) and secondly, for higher drain-to-source voltages, as it has been demonstrated in the previous simulation for $V_{DS} = 1$ V and $\mu_n^I = 5316$ cm^2/V·s in the whole simulation region, the electrons that determine the ultimate value of current travel at the saturation velocity. Thus, between these two regions there is a transition region where the negative differential mobility may be pronounced, as it is the case for the transfer characteristic at $V_{DS} = 0.2$ V in this simulation.

A MESFET structure, depending on physical and geometrical parameters and applied bias, exhibits a variety of operational modes, i.e. Gunn-effect oscillation, stable negative resistance mode and normal FET mode with saturating I_D versus V_{DS} curves [28, 31, 84, 85, 86, 87].

The results on the analysis of the stability criteria of GaAs MESFETs [28] show that the formation of the Gunn domain and consequent oscillations is very likely for MESFETs with a channel thicknesses of approximately 1 μm. MESFETs having thinner channels are more likely to operate in the stable

negative resistance (SNR) or normal FET operation mode. The MESFETs operating in the SNR mode exhibit an overshoot of the drain current for $V_{GS} = 0$ V and that happens only if the total number of carriers in the narrow channel is sufficient enough [28, 86, 87]. Thus, not only the channel thickness, but also the channel doping defines the operation mode of a MESFET.

A MESFET that normally operates in the SNR mode at $V_{GS} = 0$ V gradually changes its mode of operation into a normal FET mode as the reverse gate bias is increased. This is so because the residual channel thickness becomes smaller and the number of electrons in the channel decreases. The analysis presented in [28] furthermore shows that a MESFET with a longer gate tends to show SNR rather than instability, and a normal FET operation rather than SNR. Finally, the 2D simulation presented in the same paper has demonstrated that when the substrate is included in the simulation, although a Gunn domain is formed beneath the gate, electrons penetrate into the substrate and the size of the domain is reduced compared to that in the MESFET simulated without the substrate. As a consequence, the I_D overshoot found in the SNR mode does not occur.

The criteria for Gunn domain formation given in [28] suggest that the epitaxial MESFETs analysed in this study (the channel doping-channel thickness product of $2.3 \cdot 10^{12}$ cm^{-2}) is likely to exhibit the normal FET operation mode or SNR.

It is interesting to note that circumstances under which the kink effect is more probable to occur, described on the previous pages, correspond to findings given in [28], i.e. that the effect is less pronounced for the long gate MESFETs and that the confinement of electrons in the channel is of crucial importance.

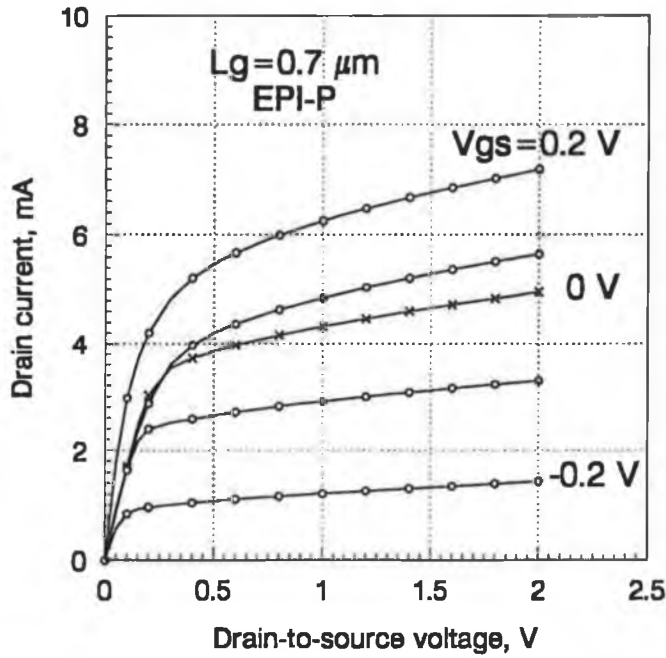

Figure 5.8: Output characteristics for the 0.7 μm gate-length EPI-P MESFET.

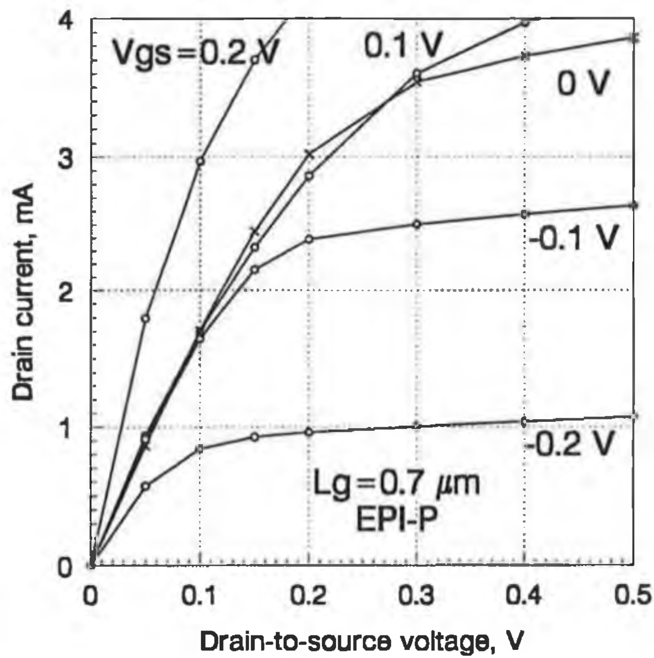

Figure 5.9: Enlargement of the output characteristics for the 0.7 μm gate-length EPI-P MESFET.

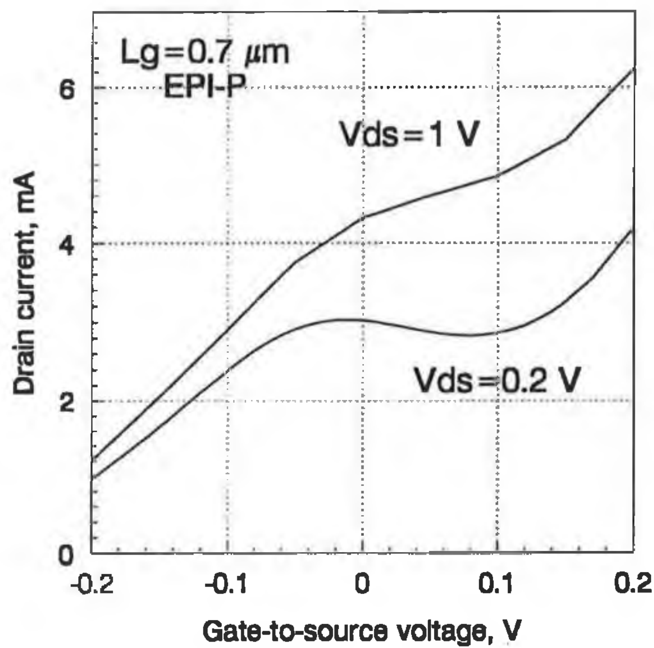

Figure 5.10: Transfer characteristics for the 0.7 μm gate-length EPI-P MESFET at $V_{DS} = 0.2$ and 1 V.

5.2 Transconductance

The transconductance is calculated here as the drain current change ΔI_D per unit change of the gate-to-source voltage ΔV_{GS} at $V_{GS} = 0$ V[1] and $V_{DS} = 1$ V

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{\Delta V_{GS} = -50 \text{ mV at } V_{GS} = 0 \text{ V and } V_{DS} = 1 \text{ V}} \tag{5.2}$$

where $\Delta V_{GS} = -50$ mV indicates that the drain currents used to calculate ΔI_D are determined at $V_{GS} = 0$ V and $V_{GS} = -0.05$ V. The transconductance is measured in A/V.

It is very interesting to note that while the transconductance of the EPI-P MESFETs is substantially affected by the inclusion of the piezoelectric charge (see Fig. 5.11), the transconductance of the ION-P MESFETs is practically not influenced by the piezoelectric charge (see Fig. 5.12), although the drain current I_D at $V_{GS} = 0$ V is changed when the piezoelectric charge is included for both the EPI-P and ION-P MESFETs (see the transfer characteristics for the EPI-P and ION-P MESFETs in Figs. 5.6 and 5.7, respectively).

An increase of the transconductance with reduced gate lengths is expected and physically reasonable for the following reasons. It has been already shown in Sections 3.5 and 3.6 that the effective resistance of the electron path through the substrate influences the drain current for V_{GS} around the threshold voltage. Fig. 3.21 demonstrates that in the case of the 0.7 μm gate-length EPI MESFET ('EPI' indicating the low substrate doping $N_A = 5 \cdot 10^{13}$ cm^{-3}), practically no current flows through the channel even for a relatively high current of $I_D = 1.56$ mA at $V_{GS} = -1$ V. In the case of the 0.7 μm gate-length EPI-P MESFET ('EPI-P' indicating the high substrate doping $N_A = 5 \cdot 10^{15}$ cm^{-3}) even at a current of $I_D = 5$ μA at $V_{GS} = -0.5$ V, i.e. a current very close to $I_D = 1$ μA used to define the threshold voltage, the major portion of current still flows through the channel, while the contribution of the substrate current is of relatively minor importance (see Fig. 3.25).

Figs. 5.13, 5.14 and 5.15 show the electron current distribution of the 0.7 μm gate-length EPI-P MESFET at V_{GS} =0.15, 0.0 and -0.2 V, respectively. Although it can be noticed that the relative contribution of the substrate

[1]Quite generally, the transconductance g_m can be defined and calculated for any V_{GS} higher than the threshold voltage.

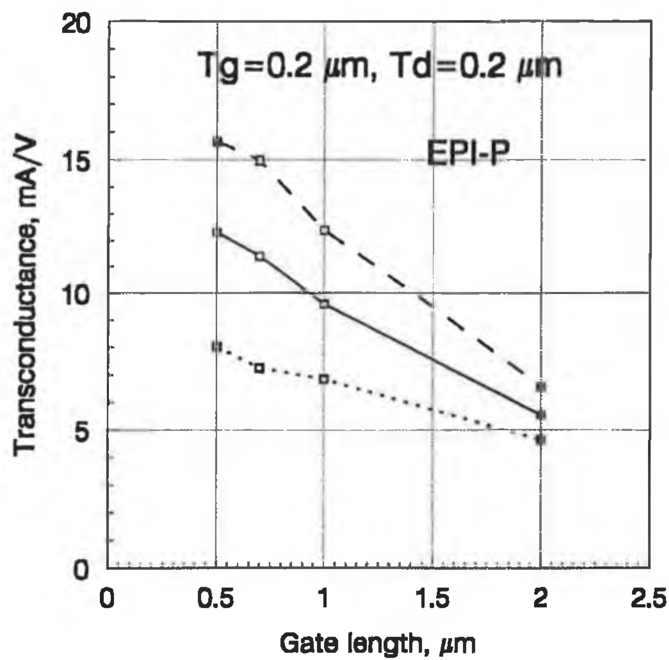

Figure 5.11: Dependence of the transconductance on the gate length for the EPI-P simulations. The transconductance values above the reference case (full line) have been obtained for predominantly positive piezoelectric charge (dashed line), while the values below the reference case have been obtained for predominantly negative piezoelectric charge (dotted line) under the gate.

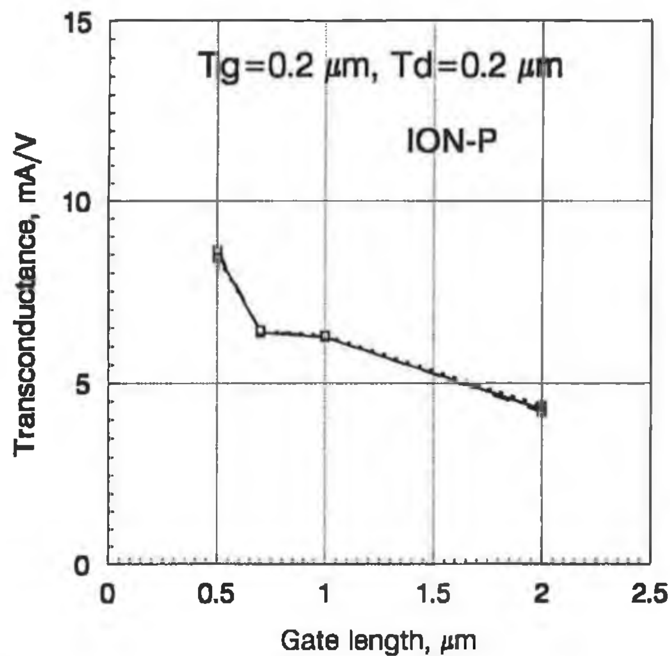

Figure 5.12: Dependence of the transconductance on the gate length for the ION-P simulations. The transconductance values for the simulations where the piezoelectric charge has been taken into account only slightly differ from the transconductance values for the reference case (full line): predominantly positive piezoelectric charge (dashed line) and predominantly negative piezoelectric charge under the gate (dotted line). The value of the transconductance for the 0.7 μm gate-length MESFET, which is lower than it might be expected from the rate of increase of transconductance as gate length reduces, is a result of the kink in the transfer characteristic (see Fig. 5.3).

current[2] to the whole current increases with reduced gate-to-source voltage, it is always of relatively minor importance, even for V_{GS} around the threshold voltage (see Fig. 3.25). This discussion indicates that electrons are well confined within the active channel region. Thus, it can be concluded that the main reason why an increase of the transconductance is observed for reduced gate lengths is the reduction of an effective resistance of the electron path through the active channel. The effect is analogous to the reduction of the effective resistance experienced by electrons going through the substrate in the case of MESFETs with low substrate doping (EPI and ION simulations).

It is worth noting that a similar effect, i.e. the shift of the current characteristics towards more positive input voltage, can be seen in the I–V curve of the pn diode when the lengths of the cathode and anode regions increase.

It is also worth remembering that the primary manifestation of reduced gate lengths is an increase of the drain current for the same gate-to-source voltage and the increase of the transconductance is just a consequence.

Up to now only the characteristics for the EPI-P and ION-P MESFETs have been presented because these characteristics are unconditionally accurate from the mathematical point of view. In Chapter 3 the accuracy of the ION and EPI simulations has been discussed and it has been concluded that the drain current, once it falls below 0.5 mA, tends to be inaccurate because the simulation region is not large enough and the Neumann boundary conditions become violated. As the transconductance is estimated at $V_{GS} = 0$ V, it is possible to calculate the transconductance accurately because the drain currents at $V_{GS} = 0$ V are above the level of 0.5 mA.

Thus, Fig. 5.16 shows the transfer characteristics for both the EPI and EPI-P sets of simulations. It should be noted that the currents for V_{GS} around $V_{GS} = 0$ V are higher in the case of the EPI MESFETs due to the additional current path through the substrate. At the same time the effectiveness of the switch-off mechanism for the EPI MESFETs has been reduced because of the decreased control of the gate electrode over the electrons pushed into the substrate (the decreased control being the consequence of increased spatial separation between the gate and electrons), but this mechanism actually takes

[2]The grid used in the simulations of the EPI and EPI-P MESFETs is very fine in the substrate at the active channel/substrate interface. For this reason the electron current that flows through the substrate appears darker on the current distribution plots. Thus, it is very simple to distinguish relative contribution of the substrate current from the current through the active channel.

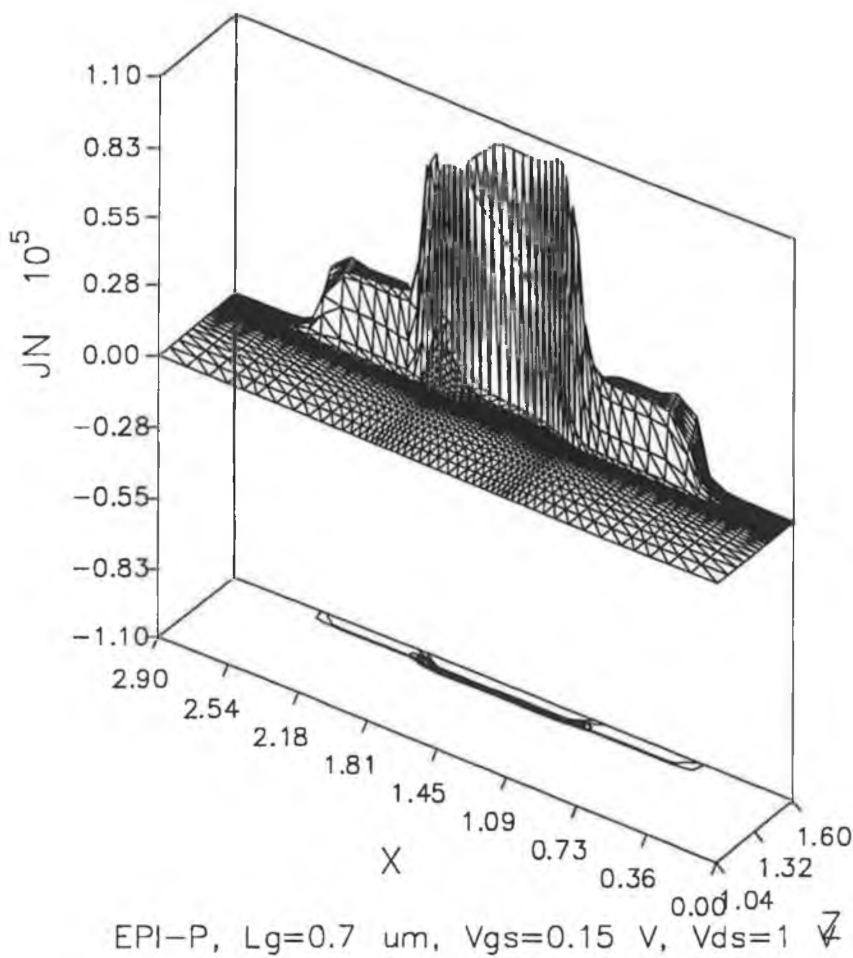

Figure 5.13: Electron current density distribution (in A/cm^2) at I_D = 5.32 mA (V_{GS} = 0.15 V, V_{DS} = 1 V) for the 0.7 μm gate-length EPI-P MESFET. The electron current is well confined within the simulated structure (contacts are deposited on the $x - y$ surface at z = 1.6 μm with the source metal going from x=0 μm to x=0.5 μm, the gate metal going from x=1.1 μm to x=1.8 μm and the drain metal going from x=2.4 μm to x=2.9 μm).

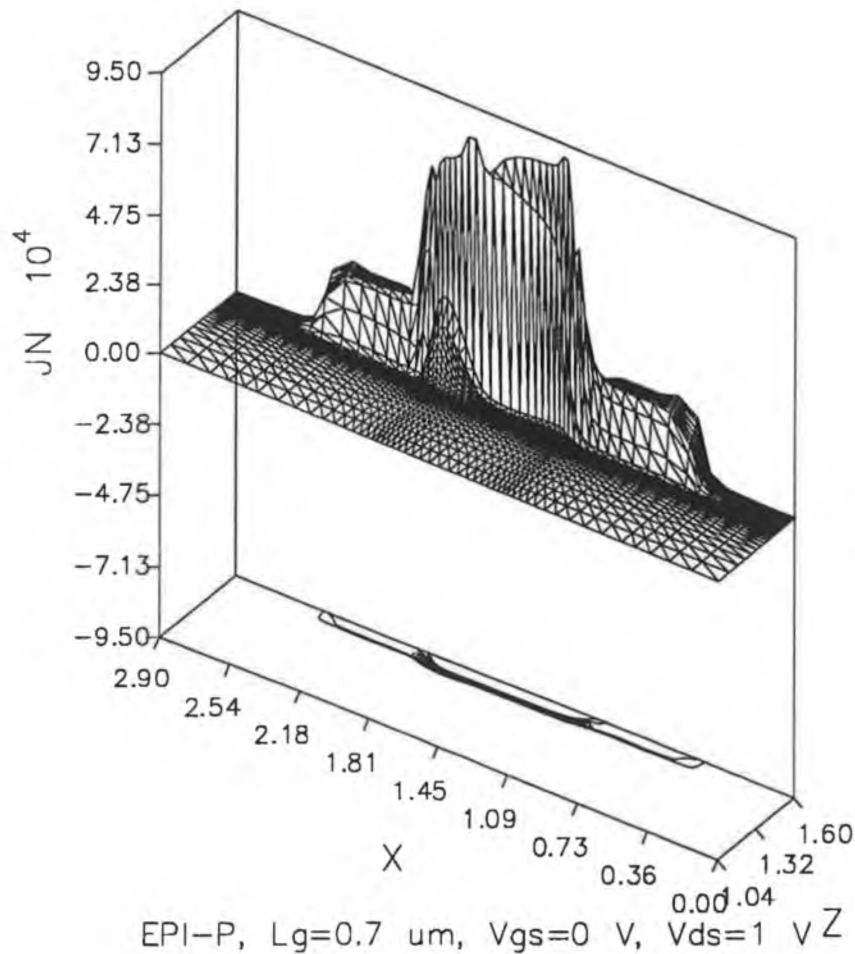

Figure 5.14: Electron current density distribution (in A/cm^2) at $I_D = 4.32$ mA ($V_{GS} = 0$ V, $V_{DS} = 1$ V) for the 0.7 μm gate-length EPI-P MESFET (contacts are deposited on the $x - y$ surface at $z = 1.6$ μm with the source metal going from x=0 μm to x=0.5 μm, the gate metal going from x=1.1 μm to x=1.8 μm and the drain metal going from x=2.4 μm to x=2.9 μm).

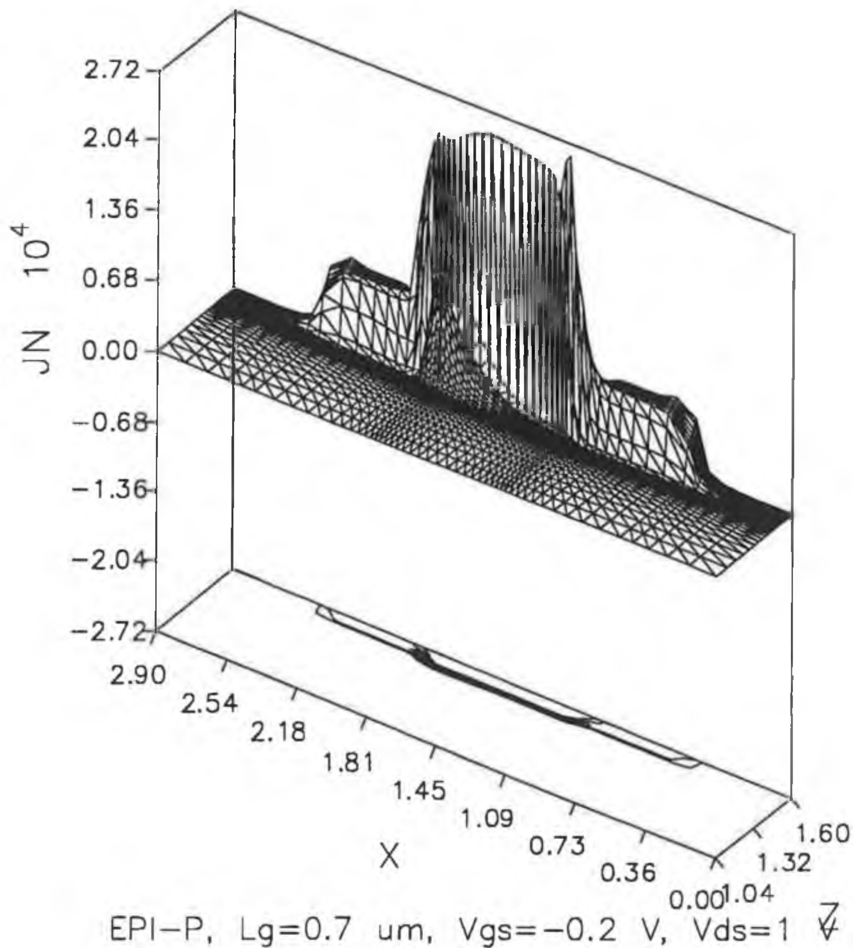

Figure 5.15: Electron current density distribution (in A/cm^2) at I_D = 1.21 mA (V_{GS} = −0.2 V, V_{DS} = 1 V) for the 0.7 μm gate-length EPI-P MESFET (contacts are deposited on the $x - y$ surface at z = 1.6 μm with the source metal going from x=0 μm to x=0.5 μm, the gate metal going from x=1.1 μm to x=1.8 μm and the drain metal going from x=2.4 μm to x=2.9 μm).

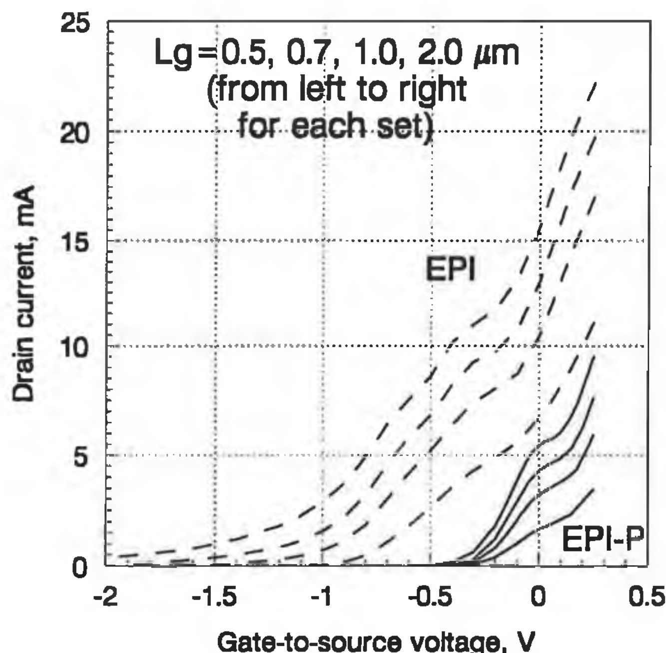

Figure 5.16: Linear plot of the EPI and EPI-P transfer characteristics for $V_{DS} = 1$ V. The EPI simulations have been performed with $N_A = 5 \cdot 10^{13}$ cm^{-3} (dashed line) and the EPI-P simulations with $5 \cdot 10^{15}$cm^{-3} (full line). The currents for the EPI simulations below 0.5 mA tend to be underestimated, but in the linear plot this is not so important because the currents below 0.5 mA are hardly distinctive and finally, even currents an order of magnitude lower do not substantially deviate from the 'real' value (see Fig. 3.19).

place for V_{GS} away from $V_{GS} = 0$ V. At $V_{GS} = 0$ V the transconductance for the EPI MESETs is higher than the transconductance for the EPI-P MESFETs (Fig. 5.17). It should be noted that the main reason why the transconductance values are lower for the EPI-P simulations is the very pronounced kink effect around $V_{GS} = 0$ V. The kink effect also appears on the transfer characteristics for the EPI MESFETs, but at negative V_{GS} voltages, i.e. away from the point where the transconductance is calculated.

The transfer characteristics for the ION and ION-P simulations are shown in Fig. 5.18 in linear scale, and the corresponding transconductance values are shown in Fig. 5.19. The transconductance of the ION-P MESFETs exhibits anomalous behaviour for devices with $L_g \leq 0.7$ μm. When compared to the trends exhibited by the longer gate length devices (namely the 1 μm and 2 μm MESFETs), one can see that g_m is significantly influenced by the kink

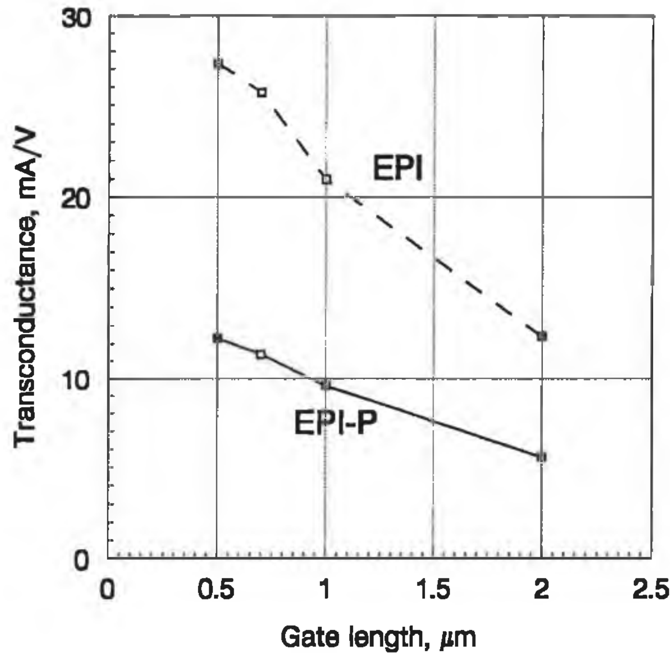

Figure 5.17: Dependence of the transconductance on the gate length for the EPI (dashed line) and EPI-P (full line) simulations.

effect. Note that in the case of the EPI-P MESFETs, where the kink effect is more pronounced, a much smoother change of transconductance as a function of gate length is observed.

To estimate the influence of the piezoelectric charge on the transconductance for the EPI and ION simulations, the simulations for the 0.7 μm gate-length EPI and ION MESFETs with predominantly positive and predominantly negative piezoelectric charge have been also done. The load conditions and the simulated structure were the same as those used to obtain the transconductance values for the EPI-P (see Fig. 5.11) and ION-P (see Fig. 5.12) MESFETs. The piezoelectric charge has resulted in a change of transconductance of +/-2% for the EPI MESFET and +/-2.7% for the ion MESFET.

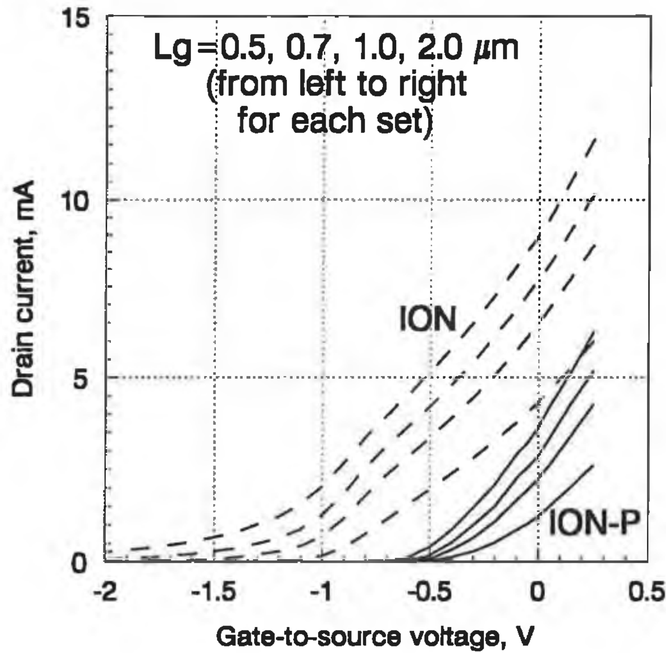

Figure 5.18: Linear plot of the ION and ION-P transfer characteristics for V_{DS} = 1 V. The ION simulations have been performed with $N_A = 5 \cdot 10^{13}$ cm^{-3} (dashed line) and the ION-P simulations with $5 \cdot 10^{15}$cm^{-3} (full line). For the accuracy of the ION simulations see the caption of Fig. 5.16 and Fig. 3.16.

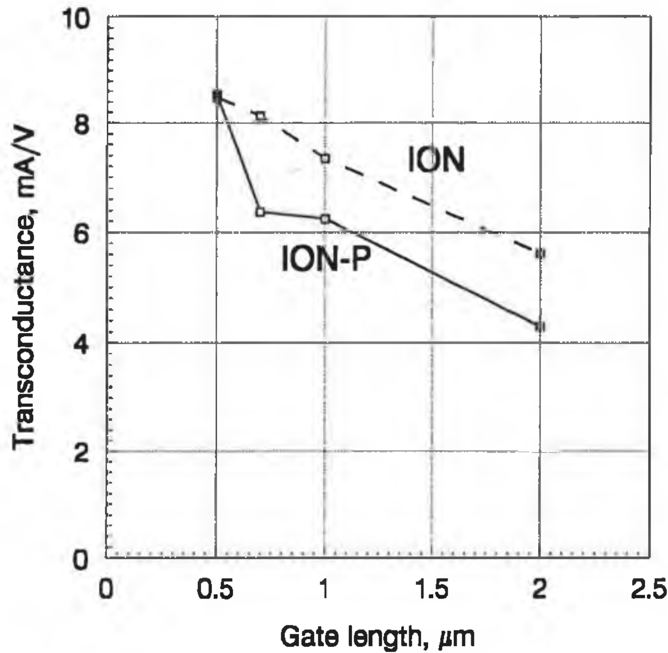

Figure 5.19: Dependence of the transconductance on the gate length for the ION (dashed line) and ION-P (full line) simulations.

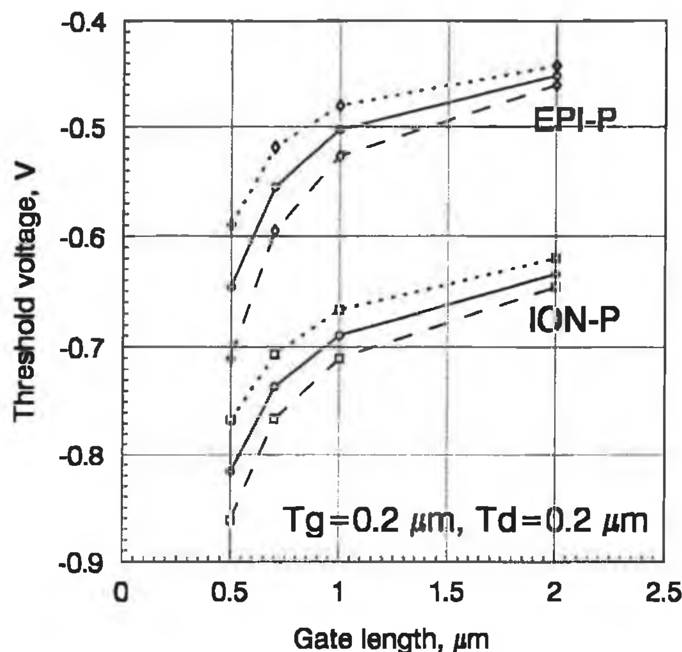

Figure 5.20: Dependence of the threshold voltage on the gate length for the EPI-P and ION-P simulations with and without the piezoelectric charge included. The threshold voltages below the reference case (full line) have been obtained for predominantly positive piezoelectric charge (dashed line) and the threshold voltages above the reference line have been obtained for predominantly negative piezoelectric charge (dotted line) under the gate.

5.3 Threshold voltage

The threshold voltage has already been treated quite extensively and the discussions from the previous sections about the current conduction mechanisms at low drain currents are directly applicable.

Fig. 5.20 shows the threshold voltage for the reference EPI-P and ION-P simulations along with the threshold voltages obtained when the piezoelectric charge is included into the doping profile. It can be seen that the impact of predominantly negative piezoelectric charge under the gate is to reduce threshold voltage variations with the gate length due to improved electron confinement. Fig. 5.21 shows the corresponding threshold voltage shifts. It is worth noting that the relative contribution of piezoelectric charge to the charge of ionized donors below the gate increases with reduced gate lengths (see Fig. 4.18) and so does the threshold voltage shift.

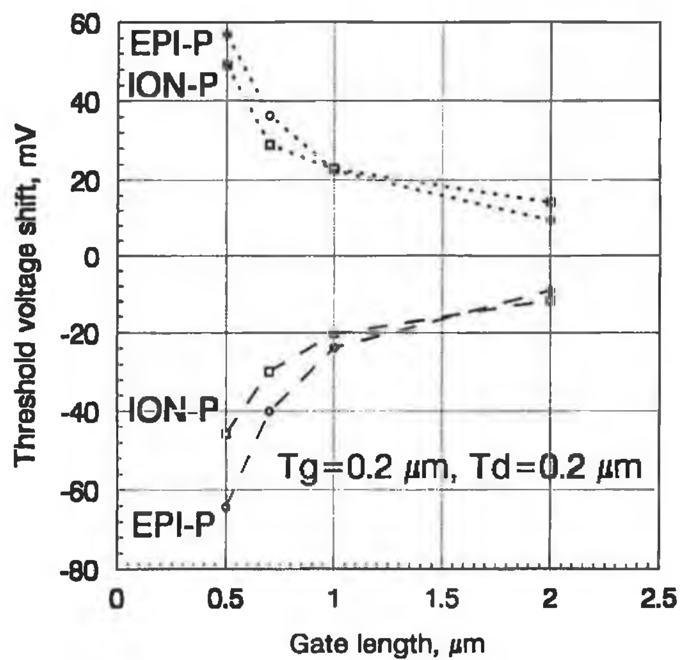

Figure 5.21: Dependence of the threshold voltage shift on the gate length for the EPI-P and ION-P simulations. The negative threshold voltage shifts have been obtained for predominantly positive piezoelectric charge (dashed line) and the positive threshold voltages have been obtained for predominantly negative piezoelectric charge (dotted line) under the gate.

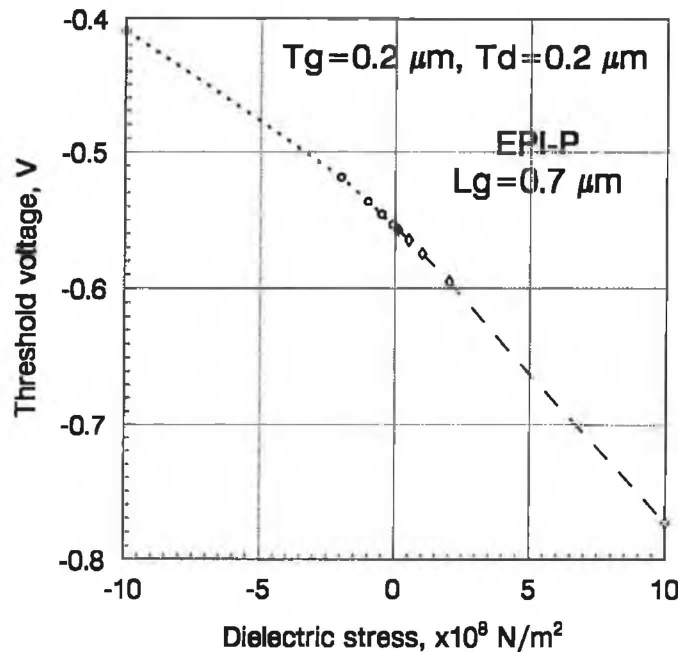

Figure 5.22: Dependence of the threshold voltage on the dielectric stress for the 0.7 μm gate-length EPI-P simulations. The threshold voltages have been obtained for predominantly positive (dashed line) and predominantly negative (dotted line) piezoelectric charge under the gate.

5.3.1 Influence of intrinsic dielectric stress

The dependence of the threshold voltage on the value of dielectric stress for the 0.7 μm gate-length EPI-P MESFET is shown in Fig. 5.22. Although the dependence is obviously linear for small values of the dielectric stress, it can be noticed that the positive threshold voltage shift tends to saturate for higher values of the compressive dielectric stress, i.e. for higher values of negative dielectric stress. On the other hand, for negative threshold voltage shifts such a tendency does not occur. The effect has been experimentally observed by Yokoyama *et al.* [15], Asbeck *et al.* [18], Ohnishi *et al.* [19] and Onodera *et al.* [20], and obtained by the numerical device simulation by McNally *et al.* [24] as well.

It should be noted that when magnitude of the dielectric stress is decreased by a factor of two, the value of the piezoelectric charge is decreased by the same factor of two at every node in the simulation region. On the other hand, if the dielectric thickness is decreased by a factor of two, it can be expected that,

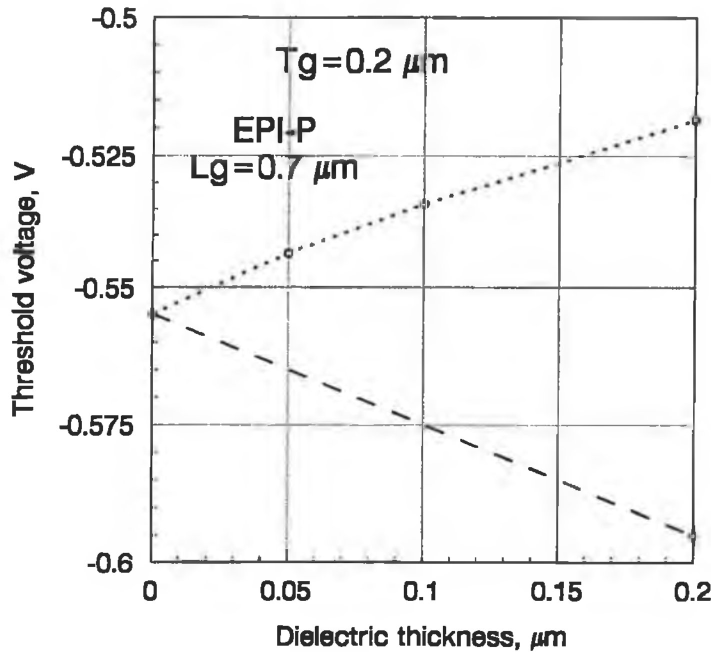

Figure 5.23: Dependence of the threshold voltage on the dielectric thickness for the 0.7 μm gate-length EPI-P simulations. The threshold voltages have been obtained for predominantly positive (dashed line) and predominantly negative (dotted line) piezoelectric charge under the gate. In the case of predominantly positive piezoelectric charge the V_{th} vs. T_d dependence is linearly interpolated between the case for $T_d = 0$ and $T_d = 0.2$ μm because the V_{th} vs. T_d dependence for predominantly negative piezoelectric charge does not substantially deviate from the linear characteristic.

although the magnitude of the forces used to model the stress is the same as the one obtained by reducing the dielectric stress by two (see Eq. (4.61)), the piezoelectric charge is not uniformly scaled at every node because the simulation structure has changed. Fig. 5.23 shows the dependence of the threshold voltage on the dielectric thickness. When the values of threshold voltages obtained by halving the dielectric thickness and by halving the magnitude of the dielectric stress have been compared, it has been found that the reduction of the dielectric thickness resulted in a 2 mV lower threshold voltage shift, indicating that the shape of the piezoelectric charge has been only slightly influenced by the change of the simulation structure (the threshold voltage shift obtained by halving the dielectric stress was 18 mV).

5.3.2 Physicality of numerical stress simulation

When considering the dependence of the threshold voltage shift on dielectric thickness, one gets a slightly confusing picture from the literature, a problem that seeks clarification. A strong dependence of the threshold voltage shift with varying dielectric thickness is in accord with the experimental evidence given by Asbeck *et al.* [18], Ohnishi *et al.* [19] and Onodera *et al.* [20]. The same sources also confirm that the threshold voltage tends to saturation when the piezoelectric charge induces the positive threshold voltage shift. In the case of the negative threshold voltage shift, such a saturation of the threshold voltage does not take place.

On the other hand, the numerical simulation in [24] offers a confusing picture of the same effect for the following reason. The dielectric stress imparted to the GaAs substrate has been modelled by the uniform displacement load model. An increase of the uniform displacement at the right boundary has a qualitatively similar effect to an increase of the dielectric stress in the force load model. The results obtained by varying the uniform displacement are in good agreement with the results presented in [18, 19, 20] and in this study. However, when the dielectric thickness has been varied, the threshold voltage shift of -200 mV for the dielectric thickness $T_d = 666$ Å becomes approximately -50 mV for $T_d = 1000$ Å (although it should be actually more negative) and it even becomes positive for $T_d = 2000$ Å. Thus, such a result contradicts even the results presented in the paper itself.

The experimental work [21], where the externally applied load has been used to induce the stress in the GaAs substrate, is related to the previous problem because the same type of load is used. This work suggests that the main source of the stress imparted to the GaAs substrate is the gate metal, which is in contrast with the experimental evidence obtained for the 'hot' MESFETs [16]-[20], i.e. the measurements conducted on MESFETs without applying external load, but measuring the threshold voltages of MESFETs produced with differing dielectric thicknesses or measuring the threshold voltages of MESFETs by thinning the dielectric layer down to zero.

These two works, [21] and [24], raise questions about:

1. the physicality of the experiments with externally applied load;
2. the applicability of the uniform displacement load model;
3. the physicality of the numerical stress simulation in general.

When speaking about the first topic, there are four papers reporting the experiments with an externally applied load: Kanamori *et al.* [21], McNally *et al.* [22], Ramirez *et al.* [23] and McNally *et al.* [24]. All four papers undoubtedly show that it is the piezoelectrically induced charge that causes the shift of electrical characteristics by obtaining opposite signs for threshold voltage shifts for the $[01\bar{1}]$ and [011] MESFETs. The papers [22, 23, 24] furthermore confirm that stresses of opposite signs change the polarity of the threshold voltage shift. Finally, the papers [21, 24] predict increased threshold voltage shifts for reduced gate lengths.

If the theoretical work is considered, the papers [23, 24] successfully match the experimental results and the results of numerical simulations for the opposite stress signs and two perpendicular orientations of MESFETs. Furthermore, the paper [24] also presents good agreement between the simulation and experiment for varying gate lengths. It should be noted that in both of these papers a 2D numerical stress simulation has been used. When considering electrical characterisation, a simple 1D analysis used in [23] has been changed over to a 2D numerical simulation in [24].

Thus, the experiments with externally applied load and the uniform displacement model, as the background for the numerical simulation, confirm their usefulness by matching experimental data and simulation results for varying gate lengths, opposite dielectric stresses and two perpendicular MESFET orientations. However, other important points seem to escape the reach of the aforementioned methods. The experimental results presented in [21] indicate that the gate metal is the major source of stress in the MESFET structure. The other three papers that present experimental results with externally applied load [22, 23, 24] do not deal with this problem, but the results of numerical simulations presented in [24] confirm the experiment [21]. Secondly, inconsistent numerical results regarding the influence of the load and dielectric thickness on the threshold voltage shift presented in [24] furthermore show that neither this type of experiment nor the uniform displacement model are generally acceptable methods.

The reason why the experiment with externally applied load suggests that the gate metal is a major source of stress, in contrast to the experiments on the 'hot' MESFETs where the dielectric thickness has been varied [16]-[20] and which have observed that the residual threshold voltage shift after thinning the dielectric stress down to zero is very small, is not quite clear. The same state-

ment can be paraphrased by stating that it is not clear why mathematically correct and physically sound numerical stress simulations produce results in discrepancy with the results obtained for the 'hot' MESFETs.

However, it is evident [16]-[20] that the initial stress of the gate metal introduced while evaporating the metal on the GaAs surface is very successfully relaxed in the cooling phase, an effect that obviously does not take place in the case of the initial stress of the dielectric layer.

Thus, to conclude the discussion on the physicality of the experiments with externally applied load, it is necessary to say that although such experiments clearly demonstrate the piezoelectric nature of the threshold voltage shifts, they also show a lack of ability to interprete accurately finer points of the same effect.

Much has already been said about the second topic, namely the uniform displacement model introduced by Ramirez *et al.* [23] and used by McNally *et al.* [24], and a brief recapitulation on the applicability of the uniform displacement load model follows. The most important aspect of this model is that it accurately models the stress produced in the experiments with externally applied load and consequently, the fact that good agreement between the experiment and model has been found in [23, 24] means that the coupled system of the basic semiconductor equations and stress equations can be successfully simulated in a decoupled form. Otherwise, the piezoelectric charge should have been recalculated during the solution process of the basic semiconductor equations each time the new electric field had been calculated. That would pose a major problem as the mesh used in the stress simulation does not suit the requirements of the mesh used in the device simulation. The negative aspect of the uniform displacement load model is that it necessarily attracts the same problems that appear in the experiments performed with externally applied load. The second negative aspect of the uniform displacement model is a lack of correspondence between the measured values of the dielectric stress and the uniform displacement (or uniform strain) that has to be defined at the right boundary of the simulation region, as it has been already explained in Section 4.3.4. This problem represents a serious disadvantage in the case when the influence of varying gate lengths has to be estimated.

When considering the third topic, the physicality of the numerical stress simulation in general, there are two points to be discussed:

1. Is there a physical load model that can be related to the measured values

of the dielectric stress?

2. The influence of the gate metal on the stress fields and the physicality of numerical simulations when the influence of the intrinsic dielectric stress has to be estimated.

It is suggested throughout this study that the force load model be used instead of the uniform displacement load model because the former directly takes into account both the dielectric stress and the dielectric thickness as two major parameters that influence the stress imparted to the GaAs substrate. The force model, in conjunction with the derivation of analytical expressions for the stress fields, is presented in [88], then used in [78] to explain the photoelastic waveguiding effect, and finally used by Asbeck *et al.* [18] to derive the piezoelectric charge in MESFETs. To derive analytical expressions of stress fields it is necessary to use a simple geometrical structure. Thus, neither the influence of the gate metal nor the dielectric layer have been included. However, when the force model is used in the FEM stress analysis, both of these layers are properly taken into account. The main objection to the force model, namely that the model is not valid in a region of radius equal to twice the dielectric thicknesses around the gate edges, does not apply when the model is used in the FEM stress analysis. However, the application of the force model does result in very high stress and piezoelectric charge peaks around the edges of the dielectric opening, which is not entirely physical as plastic deformation would actually smooth the stress peaks.

To assess the influence of the charge peaks a number of simulations have been performed for the 0.7 μm gate-length EPI-P and ION-P MESFETs. For each MESFET three additional simulations have been performed with the peaks of the piezoelectric charge limited by the following rules:

1. $\rho_{pz} \leq 10^{16}$ cm^{-3} to assess the influence of the positive charge peaks;

2. $\rho_{pz} \geq -10^{16}$ cm^{-3} to assess the influence of the negative charge peaks;

3. $|\rho_{pz}| \leq 10^{16}$ cm^{-3} to assess the influence of both polarities of the charge peaks.

The limiting value of 10^{16} cm^{-3} is chosen because this value is approximately 20 times lower than the donor concentration in the active channel ($N_D = 2.3 \cdot 10^{17}$ cm^{-3}), which means that what is left of the peak is screened by donors in the

channel and consequently, does not significantly affect electrical characteristics of the MESFETs. If the charge stored in the peaks does influence electrical characteristics, then the values of the characteristics obtained from the simulations with restrained piezoelectric charge have to differ from the values obtained with charge peaks fully taken into account.

The influence of the charge peaks has been checked at $V_{GS} = 0$ V and at the threshold voltage. In all three cases for the EPI-P MESFET the drain current at $V_{GS} = 0$ V has changed less than 0.3% compared with the value obtained with the charge peaks taken into account, and the threshold voltage has changed less than 0.8 mV, i.e. less than 2% of the threshold voltage shift obtained with the charge peaks taken into account[3]. In the case of the ION-P MESFET, the drain current at $V_{GS} = 0$ V changed less than 0.2% and the threshold voltage changed less than 0.48 mV, i.e. less than 1.6% of the threshold voltage shift obtained with the charge peaks taken into account.

Thus, it has been shown that the influence of the charge peaks is almost negligible and at the same time it has been confirmed that it is the piezoelectric charge in the substrate at the substrate/active channel interface that has the largest impact on electrical characteristics.

Although it is clear that the dielectric stress can be properly modelled by the force load model, the question of the feasibility of accurate numerical simulation from the physical point of view still remains open.

Actually, the fact that the results of the externally applied load in [21], the results of the numerical simulations in [24] and the results presented in this study (see Fig. 4.17) all show that the metal layer has a dominant influence on the threshold voltage shift is not inconsistent from the mechanical engineering point of view.

The real source of the problem is obviously the difference in the relaxation of the initial stress of the metal and dielectric layer when a MESFET is cooled down to room temperature. The fact that the residual threshold voltage shift is almost negligible after the dielectric is completely etched away and the fact

[3]To calculate the threshold voltage, the gate-to-source voltage has been varied in steps of 0.1 V. After a suitable 0.1 V wide range of V_{GS} has been found, the simulation has been repeated by dividing this range into steps of 10 mV, and finally a third simulation has been performed for steps of 1 mV. The maximum difference between the threshold voltages determined by the 0.1 V range and 10 mV range was approximately 30 mV, while the maximum difference in the threshold voltage between the second and third simulation was less than 0.3 mV. If the difference in V_{th} by reducing the step from 10 mV to 1 mV is less than 0.3 mV, we may suppose that the accuracy of the threshold voltage obtained for the V_{GS} step of 1 mV is better than 0.1 mV.

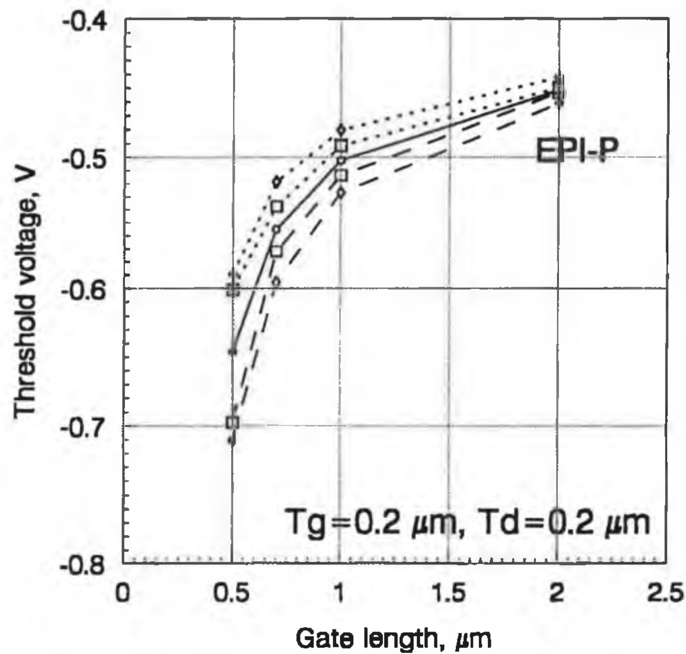

Figure 5.24: Dependence of the threshold voltage on the gate length for the EPI-P simulations for the metal/dielectric/GaAs (diamonds) and dielectric/GaAs (squares) structure. The threshold voltages above the reference case (full line) have been obtained for predominantly positive piezoelectric charge (dashed line) and the threshold voltages below the reference line have been obtained for predominantly negative piezoelectric charge (dotted line) under the gate.

that the etching process (being a low-temperature treatment) is not likely to change the stress distribution mean that physically sound results may be expected from the numerical simulations when only the dielectric layer on top of the GaAs substrate is considered. Such simulations have been performed for the EPI-P MESFETs. The resulting threshold voltages are shown in Fig. 5.24 and the corresponding threshold voltage shifts are shown in Fig. 5.25 along with the results for the metal/dielectric/GaAs structure. The threshold voltage shifts for the dielectric/GaAs structure are lower than the threshold voltage shifts for the metal/dielectric/GaAs structure, but the difference decreases for shorter gate lengths, with a tendency of the threshold voltage shift for the dielectric/GaAs structure to become even larger than the threshold voltage shift for the metal/dielectric/GaAs structure for the gate lengths below 0.5 μm.

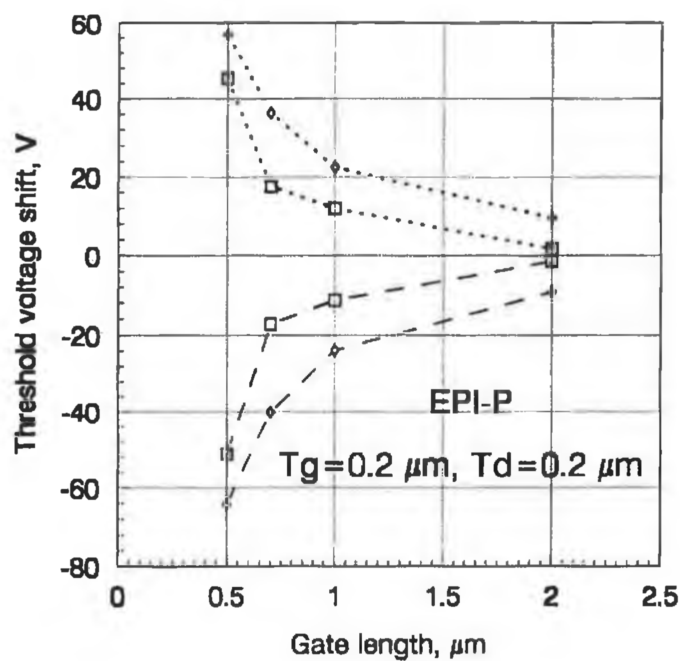

Figure 5.25: Dependence of the threshold voltage shift on the gate length for the EPI-P simulations for the metal/dielectric/GaAs (diamonds) and dielectric/GaAs (squares) structure. The negative threshold voltage shifts have been obtained for predominantly positive piezoelectric charge (dashed line) and the positive threshold voltages have been obtained for predominantly negative piezoelectric charge (dotted line) under the gate.

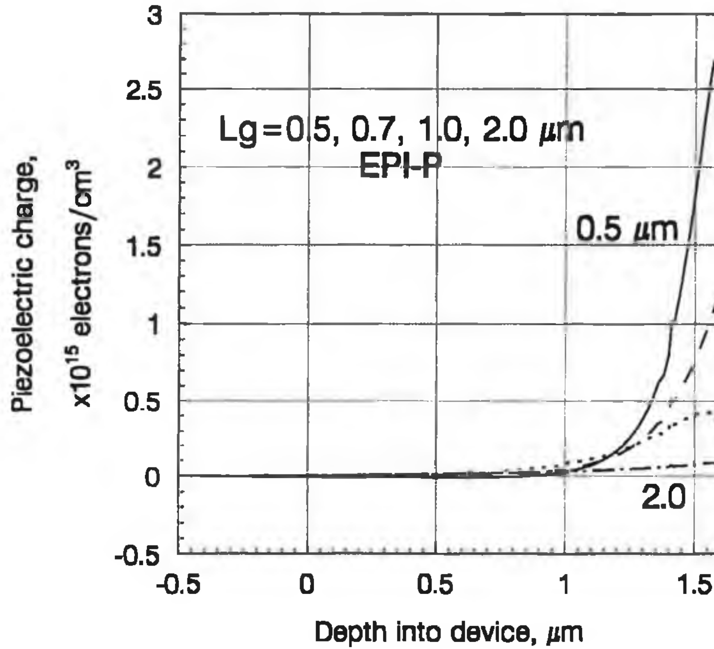

Figure 5.26: Piezoelectric charge ρ_{pz} down the middle of the gate calculated by the FEM method (dielectric/GaAs structure) for the 0.5, 0.7, 1.0 and 2.0 μm gate-length EPI-P MESFETs.

The piezoelectric charge down the middle of the gate is shown in Fig. 5.26 and the piezoelectric charge distribution for the 0.7 μm gate-length EPI-P MESFET is shown in Fig. 5.27. When the piezoelectric charge distribution down the middle of the gate obtained for the dielectric/GaAs structure is compared with the charge distribution for the metal/dielectric/GaAs structure (see Fig. 4.18), it can be seen that in the former case the charge is closer to the surface of the GaAs substrate. Although the maximum piezoelectric charge down the middle of the gate is similar, the charge concentration at the active channel/substrate interface is lower and the penetration of the piezoelectric charge into the substrate is shallower in the case of the dielectric/GaAs structure, and this is the main source of difference in the threshold voltage shift between the dielectric/GaAs and metal/dielectric/GaAs structures.

It has been seen that the transfer characteristics and transconductance suffered proportionally the same change as the threshold voltage shift, thus the graphs for these characteristics obtained for the dielectric/GaAs structure are not shown as they essentially bring no more information and the same is the case of the results for the ION-P MESFETs.

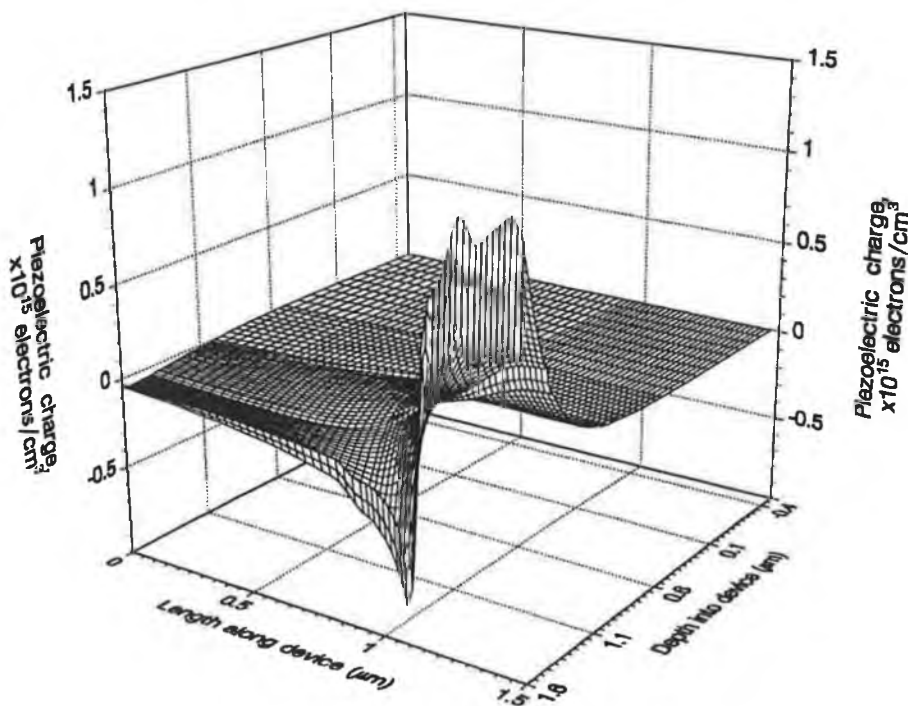

Figure 5.27: Piezoelectric charge ρ_{pz} calculated by the FEM method for the 0.7 μm EPI-P MESFET for the dielectric/GaAs structure. Only one half of the simulated region is shown (the source side, from x = 0 to x = 1.45 μm) because the charge distribution is symmetric around the gate centre. The gate metal is deposited on the x-y surface at z=1.6 μm between the points x=1.1 μm and x=1.8 μm (the x axis is denoted as 'Length along device', the z axis is denoted as 'Depth into device', and the y axis is not shown on the graph).

Although the idea of taking into account only the dielectric layer and neglecting the metal gate may at first glance seem to be reasonable, this is actually not the case for the following reason. Even if the intrinsic stress in the metal layer is completely relaxed in the cooling stage, the stress distribution in GaAs at room temperature is affected by the presence of the metal layer. Thus, as there is a difference in the threshold voltage shifts between the metal/dielectric/GaAs and dielectric/GaAs structures, it is necessary to assume that the results obtained for the metal/dielectric/GaAs structure are more reliable. Furthermore, the difference in the threshold voltage shifts actually indicates the relative influence of the metal and dielectric layers on the stress distribution in GaAs and not the source of stress as it has been suggested in [21].

At this stage the experiment with externally applied load and the uniform displacement model have to be revisited. The application of both methods results in completely incorrect results when the dielectric thickness is $T_d = 0$ because none of these methods models the stress source correctly, i.e. even if $T_d = 0$ both methods result in substantial threshold voltage shift, qualitatively similar to the threshold voltage shift obtained for the metal/GaAs structure discussed in this study (see Fig. 4.17), due to the presence of two materials with different mechanical parameters E and ν.

Thus, the results obtained by experiments with externally applied load are misleading because the source of stress can not be modelled by externally applied load and the same conclusion applies to the numerical stress simulation with the uniform displacement load model.

To close the discussion on the feasibility of physically correct numerical simulation of the influence of the intrinsic dielectric stress on the threshold voltage shift, we propose that the stress be modelled by the force load model applied to the metal/dielectric/GaAs structure. The fact that chemistry and physics of the relaxation of the initial dielectric stress are not exactly known presents no problem, because the dielectric stress can be measured at room temperature as well as the dielectric thickness, so that all data needed for the force model are available.

5.3.3 SiO_2 as dielectric

There is an aspect of the piezoelectrically induced threshold voltage shift that has not been treated by numerical simulation. The experimental evidence in

	E (N/m^2)	ν
GaAs	$8.53 \cdot 10^{10}$	0.31
WSi_x	$6.21 \cdot 10^{11}$	0.30
Si_3N_4	$3.10 \cdot 10^{11}$	0.30
SiO_2	$7.10 \cdot 10^{10}$	0.17

Table 5.1: Mechanical parameters Young's modulus E and Poisson's ratio ν for GaAs [9], WSi_x used as metal, Si_3N_4 and SiO_2 used as dielectrics [83].

metal/dielectric/GaAs		
ΔV_{th} (mV)	Si_3N_4	SiO_2
'positive'	36	43
reference	0	0
'negative'	-40	-48
dielectric/GaAs		
ΔV_{th} (mV)	Si_3N_4	SiO_2
'positive'	18	40
reference	0	0
'negative'	-17	-44

Table 5.2: Influence of the dielectric material on the threshold voltage shift for the 0.7 μm gate-length EPI-P MESFET for the metal/dielectric/GaAs and dielectric/GaAs structures: 'positive' denotes predominantly positive charge below the gate and 'negative' denotes predominantly negative charge below the gate.

[19] shows that the magnitudes of threshold voltage shifts are greater when a SiO_2 dielectric layer is used instead of a Si_3N_4 layer. In the same paper the SiO_2 stress is estimated to be approximately $5 \cdot 10^8$ N/m^2 and approximately 10^8 N/m^2 for Si_3N_4 and this is the reason why the threshold voltage shifts are higher when SiO_2 is used as dielectric. However, it is certainly interesting to know how the threshold voltage changes if the same dielectric stress is applied to the structure with different dielectric materials used. Table 5.1 presents the mechanical parameters for GaAs, WSi_x (WSi_x being the gate metal used in the experiments), Si_3N_4 and SiO_2.

Table 5.2 shows the threshold voltage shifts for the 0.7 μm gate-length EPI-P MESFET for the metal/dielectric/GaAs and dielectric/GaAs structures. It is interesting to note that SiO_2 produces higher threshold voltage shifts for both simulation structures, but the difference between SiO_2 and Si_3N_4 is much larger in the case of the dielectric/GaAs structure.

Thus, we conclude that the threshold voltage shifts are higher when the SiO_2 dielectric is used not only because the intrinsic stress of the SiO_2 layer is

L_g (μm)	0.5	0.7	1.0	2.0
EPI	-4.9	-3.6	-2.5	-1.5
ION	-5.0	-3.5	-2.3	-1.8

Table 5.3: Estimated threshold voltage (in Volts) for the EPI and ION MESFETs as a function of the gate length.

bigger, but also because the difference in the mechanical parameters between SiO_2 and Si_3N_4 pronounces this difference.

5.3.4 EPI and ION MESFETs

To conclude the discussion on the threshold voltage, the estimated values of the threshold voltages for the EPI and ION simulations, i.e. the simulations with the low substrate doping $N_A = 5 \cdot 10^{13}$ cm^{-3}, are presented in Table 5.3. The threshold voltages are estimated by extrapolating the current by the line that passes through the point $I_D = 0.5$ mA and has the same inclination as the calculated current at this point on the logarithmic plot of the current.

The estimated threshold voltage shifts with the piezoelectric charge included for the 0.7 μm gate-length MESFETs are -180 mV and 160 mV for the EPI MESFET and -260 mV and +350 mV for the ION MESFET with predominantly positive and predominantly negative piezoelectric charge under the gate, respectively for each MESFET. The piezoelectric charge has been calculated for the metal/dielectric/GaAs structure. The values of the threshold voltage shifts are approximately 4 to 5 times higher than the corresponding values for the EPI-P and ION-P MESFETs (see Fig. 5.21).

5.4 Subthreshold current slope

Subthreshold current slope (STS) is a good indicator of the effectiveness of the switch-off mechanism of MESFETs. Higher values of STS indicate that the slope of current with respect to applied voltage V_{GS} decreases and consequently, that a larger V_{GS} change is necessary to achieve the same change of the drain current, i.e. the switch-off mechanism becomes less effective.

Except for the results with externally applied load and numerical simulations presented in [24], there is no experimental evidence of the influence of piezoelectric charge on STS. However, by simple physical reasoning it can be concluded that the same mechanisms that improve the confinement of electrons will also reduce the STS value. Thus, the STS values for the EPI-P and ION-P simulations will inevitably be smaller than the values for the EPI and ION simulations, respectively. A confirmation of this statement can be found in Figs. 3.19 and 3.16.

Following the same idea, it can be supposed that mostly negative piezoelectric charge under the gate also reduces the STS value. Fig. 5.28 confirms this line of reasoning in the case of the EPI-P simulations. Note also that the STS value increases with reducing gate length, indicating decreased control of the gate electrode over electrons in the channel and substrate. The variation of STS with the piezoelectric charge taken into account is relatively small.

On the other hand, the STS values for the ION-P simulations show an unusual character (see Fig. 5.29). For the reference case (no piezoelectric charge taken into account), when the gate length decreases from 2 μm to 1 μm, the STS value decreases as well, indicating improved switch-off mechanism for the 1 μm gate-length MESFET. This is in contrast to the variation of STS with the gate length found in the EPI-P MESFETs. At the same time, the variation of the threshold voltage with the gate length for the ION-P MESFETs is consistent with the physical picture, i.e. a more negative threshold voltage (the case of the 1 μm MESFET) suggests that the electron confinement is worse and as a result the STS value should increase. This effect also occurs when the piezoelectric charge is taken into account. The mostly negative piezoelectric charge under the gate, although it should normally produce better confinement and lower the value of STS, actually results in higher values of STS. It goes without saying that in the full picture, the complex interaction of regions of positive and negative piezoelectric charge with the ion-implanted donors may and will produce unexpected effects.

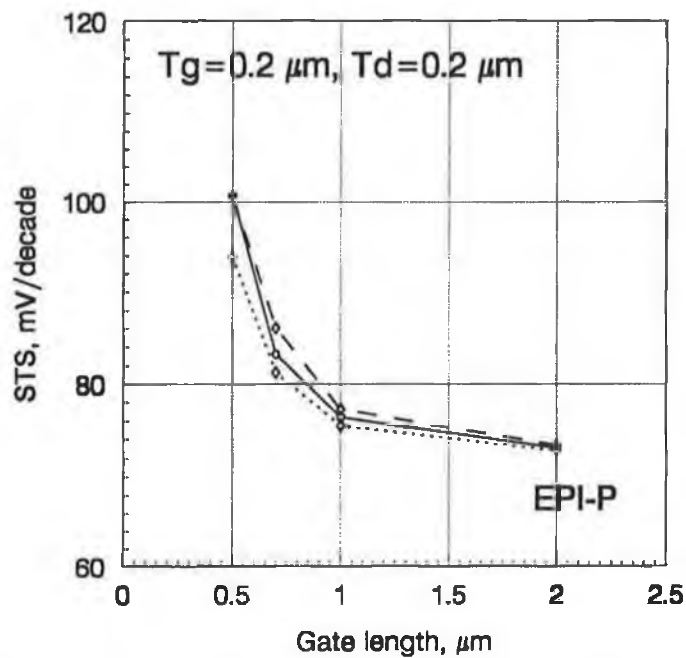

Figure 5.28: Dependence of the subthreshold current slope on the gate length for the EPI-P simulations with and without the piezoelectric charge included: reference case (full line), predominantly positive piezoelectric charge (dashed line) and predominantly negative piezoelectric charge (dotted line) under the gate.

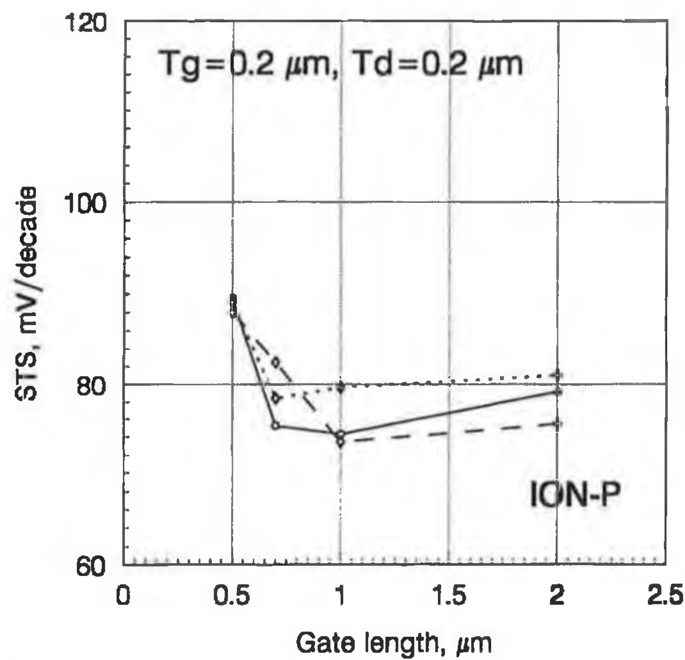

Figure 5.29: Dependence of the subthreshold current slope on the gate length for the ION-P simulations with and without the piezoelectric charge included: reference case (full line), predominantly positive piezoelectric charge (dashed line) and predominantly negative piezoelectric charge (dotted line) under the gate.

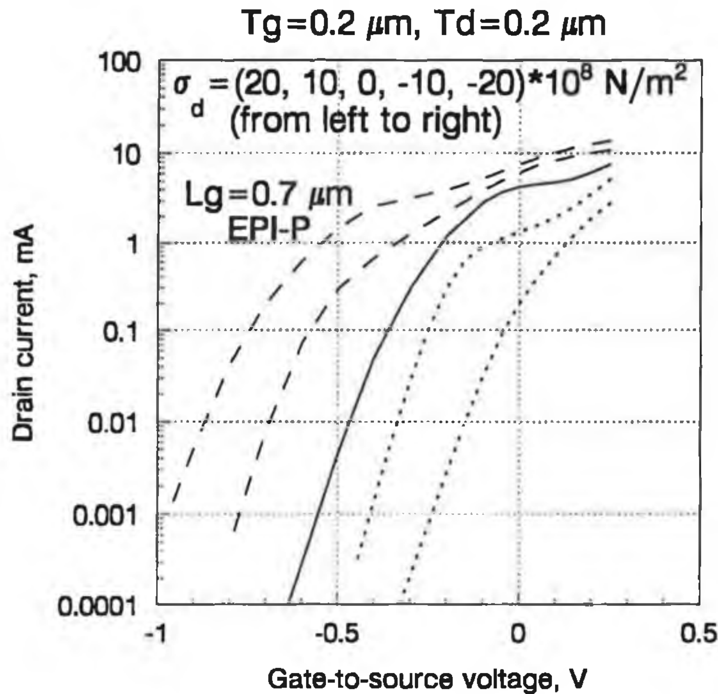

Figure 5.30: Transfer characteristics for the 0.7 μm gate-length EPI-P MESFET at V_{DS} = 1 V: reference case (full line), predominantly positive piezoelectric charge obtained with $\sigma_d > 0$ (dashed line) and predominantly negative piezoelectric charge obtained with $\sigma_d < 0$ (dotted line) under the gate.

To expand on this topic, another aspect of the same problem is presented in Fig. 5.30. If the 0.7 μm gate-length EPI-P MESFET, one that behaves in accordance with the physical expectations, is subjected to 5 and 10 times higher dielectric stress than the stress used to obtain the STS values from Fig. 5.28, the following interesting features become visible when predominantly negative piezoelectric charge is induced under the gate:

1. Higher stress results in higher piezoelectric charge densities and higher threshold voltage shifts (consistent with the theory);

2. Higher stress ($-20 \cdot 10^8$ N/m^2) results in STS = 88.0 mV/decade, while a stress of $-10 \cdot 10^8$ N/m^2 results in STS = 71.6 mV/decade (inconsistent with expectations at a first glance).

When the transfer characteristics are inspected, it becomes apparent that the magnitude of the piezoelectric charge in the case of the higher stress is such that the piezoelectric charge not only slightly modulates the current, but it actually screens the donor charge in the active channel and changes the

drain current by increasing the effective resistance of the electron path. Furthermore, although negative charge below the gate would normally increase electron confinement, when it is on the order of magnitude of the donor concentration, by reducing the donor concentration in the channel the shape of the active channel doping profile is smoothed and the confinement of electrons is consequently deteriorated.

Because of this smoothing effect, the kink that is still apparent in the transfer characteristic for the predominantly negative charge under the gate obtained with $\sigma_d = -10 \cdot 10^8$ N/m^2 disappears from the characteristic obtained with $\sigma_d = -20 \cdot 10^8$ N/m^2 (see Fig. 5.31). The net doping $N_D - N_A$ for $\sigma_d = -20 \cdot 10^8$ N/m^2 is shown in Fig. 5.32 and Fig. 5.33 displays $N_D - N_A$ for $\sigma_d = -2 \cdot 10^8$ N/m^2. The charge peaks above $|2 \cdot 10^{16}|$ cm^{-3} are cut out from the plot to make the change of the donor concentration in the channel more visible[4].

The transfer characteristics for mostly positive charge under the gate also show interesting features. The characteristic obtained with $\sigma_d = 10 \cdot 10^8$ N/m^2 is nicely smoothed without an apparent kink, in accordance with the results presented in Fig. 5.6 where it can be seen that higher positive piezoelectric charge under the gate smooths the kink more effectively. However, a piezoelectric charge density of magnitude twice as great is obtained with $\sigma_d = 20 \cdot 10^8$ N/m^2 and produces another kink in the transfer characteristic around $V_{GS} = -0.4$ V (see Fig. 5.34).

[4]To estimate the influence of the piezoelectric charge peaks for $\sigma_d = -20 \cdot 10^8$ N/m^2, which is a load 10 times higher than the load normally used throughout this chapter, a simulation has been performed with the piezoelectric charge peaks limited by $|\rho_{pz}| \leq 2 \cdot 10^{16}$ cm^{-3}. The difference in the threshold voltage shift with the piezoelectric charge peaks fully taken into account and the limited piezoelectric charge is 35 mV, i.e. V_{th} with the limited piezoelectric charge is 11% lower than the threshold voltage shift obtained with the charge peaks taken into account.

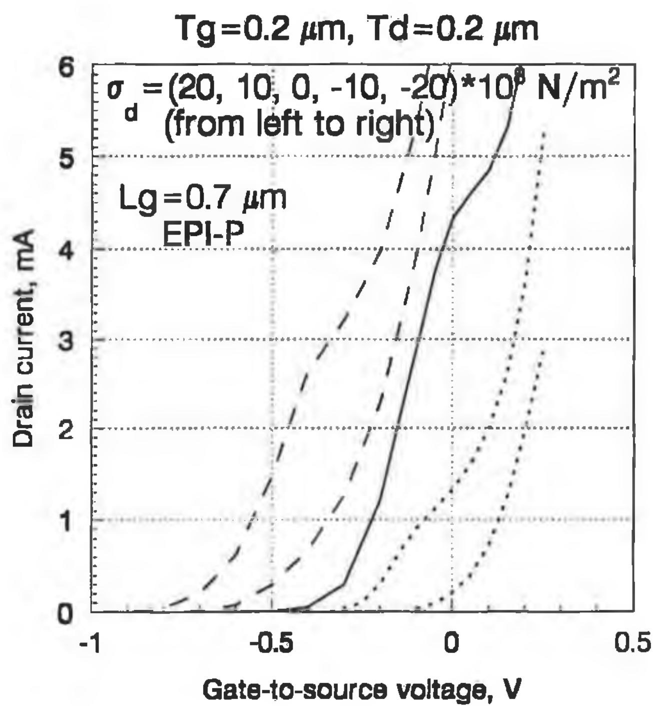

Figure 5.31: Transfer characteristics for the 0.7 μm gate-length EPI-P MESFET at V_{DS} = 1 V: reference case (full line), predominantly positive piezoelectric charge obtained with $\sigma_d > 0$ (dashed line) and predominantly negative piezoelectric charge obtained with $\sigma_d < 0$ (dotted line) under the gate.

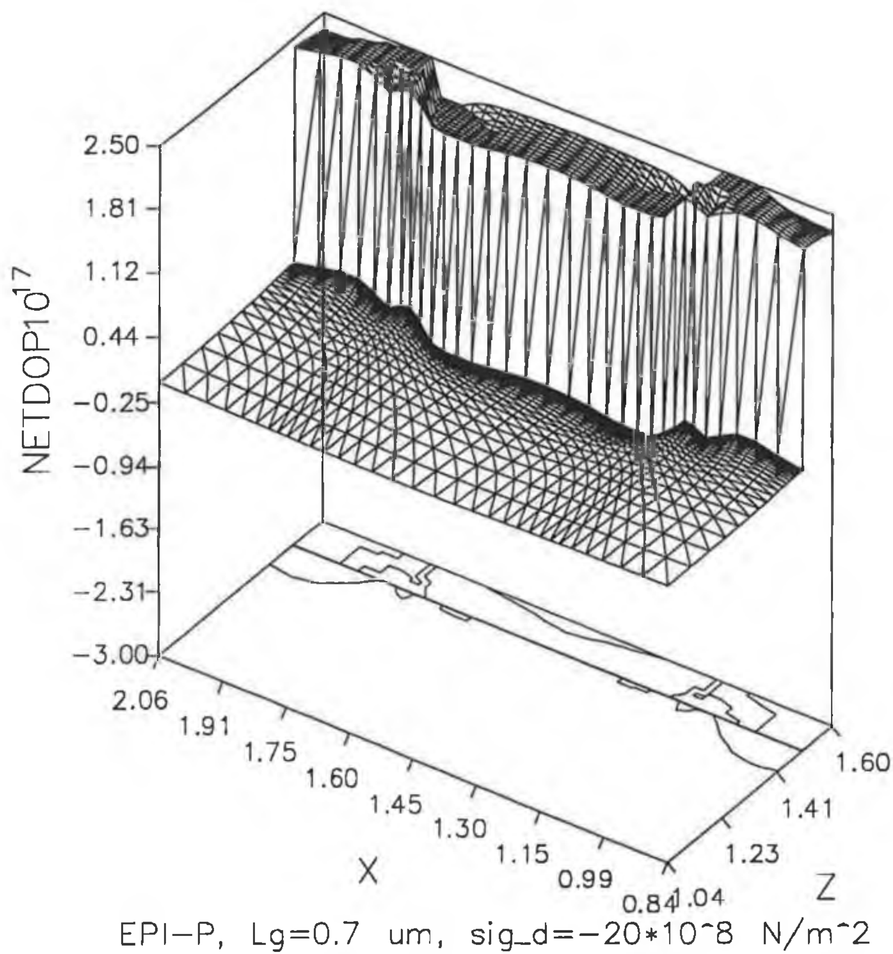

Figure 5.32: Net doping $N_D - N_A$ for the 0.7 μm gate-length EPI-P MESFET for $\sigma_d = -20 \cdot 10^8$ N/m^2 (contacts are deposited on the $x-y$ surface at $z = 1.6$ μm with the source metal going from x=0 μm to x=0.5 μm, the gate metal going from x=1.1 μm to x=1.8 μm and the drain metal going from x=2.4 μm to x=2.9 μm).

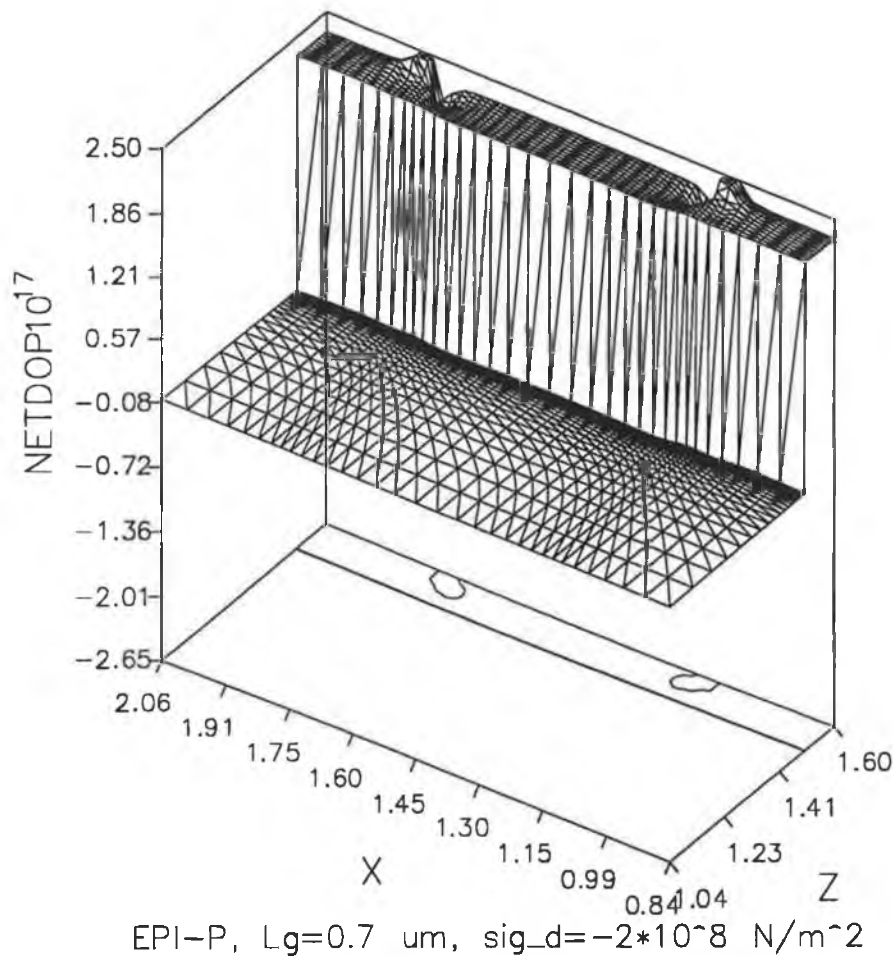

Figure 5.33: Net doping $N_D - N_A$ for the 0.7 μm gate-length EPI-P MESFET for $\sigma_d = -2 \cdot 10^8$ N/m^2 (contacts are deposited on the $x-y$ surface at $z = 1.6$ μm with the source metal going from x=0 μm to x=0.5 μm, the gate metal going from x=1.1 μm to x=1.8 μm and the drain metal going from x=2.4 μm to x=2.9 μm).

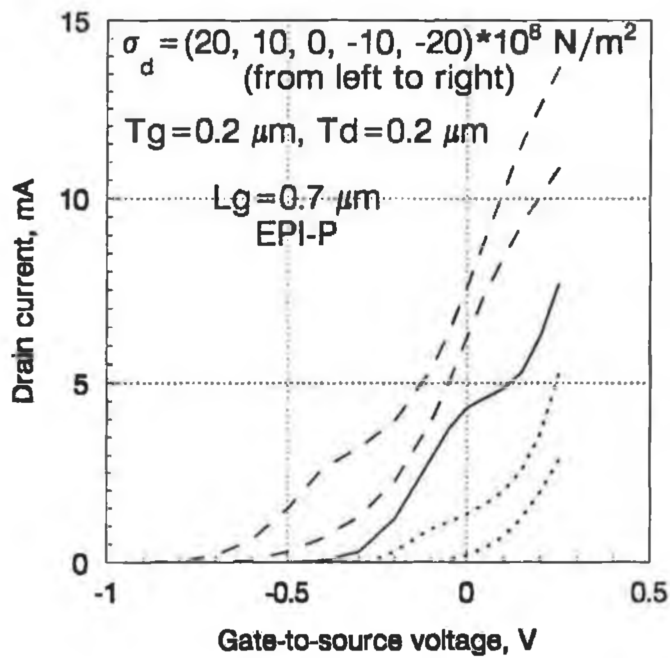

Figure 5.34: Transfer characteristics for the 0.7 μm gate-length EPI-P MESFET at $V_{DS} = 1$ V: reference case (full line), predominantly positive piezoelectric charge obtained with $\sigma_d > 0$ (dashed line) and predominantly negative piezoelectric charge obtained with $\sigma_d < 0$ (dotted line) under the gate.

5.5 Output resistance

The last characteristic that is going to be discussed is the output resistance r_o. It is defined as

$$\frac{1}{r_o} = \left.\frac{\Delta I_D}{\Delta V_{DS}}\right| \Delta V_{DS} = 50 \text{ mV at } V_{GS} = 0 \text{ V and } V_{DS} = 1 \text{ V} \tag{5.3}$$

Fig. 5.35 shows the output resistance for the epitaxial and ion-implanted MESFETs. The output resistance increases with increasing gate length in accordance with experimental evidence, e.g. [3, 89]. For gate bias $V_{GS} = 0$ the drain current saturates around $V_{DS} = 0.3$ V (see Fig. 5.8) because electrons that determine the drain current have acquired the saturation velocity. Any further small increase of the drain current with increasing V_{DS} is due to the increased substrate current (see Figs. 5.36 and 5.37). Note a substantial improvement of the output resistance for the EPI-P and ION-P MESFETs which is due to better electron confinement. It is also interesting to note that the output resistance is higher for the ion-implanted MESFETs as opposed to the epitaxial MESFETs, which is unexpected because the tail of the ion-implanted profile suggests that the electron confinement and consequently the output resistance should be worse when compared to the epitaxial MESFETs.

When the currents in Figs. 5.36 and 5.37 are compared, it can be seen that for a change of drain-to-source voltage $\Delta V_{DS} = 1$ V the maximum current at $z = 1.51$ μm (i.e. 0.09 μm from the surface - inside the channel) increases 16%, the current at $z = 1.5$ μm (0.1 μm from the surface = the channel/substrate interface) increases 73%, and the current at $z = 1.49$ μm (0.11 μm from the surface - inside the substrate) increases 300%, clearly indicating that the substrate current is responsible for the increase of the drain current in the saturation region.

Improvement of the output resistance can be observed as a lower slope of the drain currents in the saturation region (see Figs. 5.38 and 5.39). It is interesting to note that higher substrate doping of $N_A = 5 \cdot 10^{15}$ cm^{-3} has decreased the drain current less in the case of the ion-implanted MESFETs. This observation is in accord with the aforementioned higher output resistance of the ion-implanted MESFETs. Although unexpected, it appears that the tail of the ion-implanted profile makes the ion-implanted MESFETs less susceptible to variations of V_{DS} in the saturation region. The same figures also demonstrate the influence of the piezoelectric charge. It is expected that predominantly positive piezoelectric charge, by means of a reduction of electron confinement

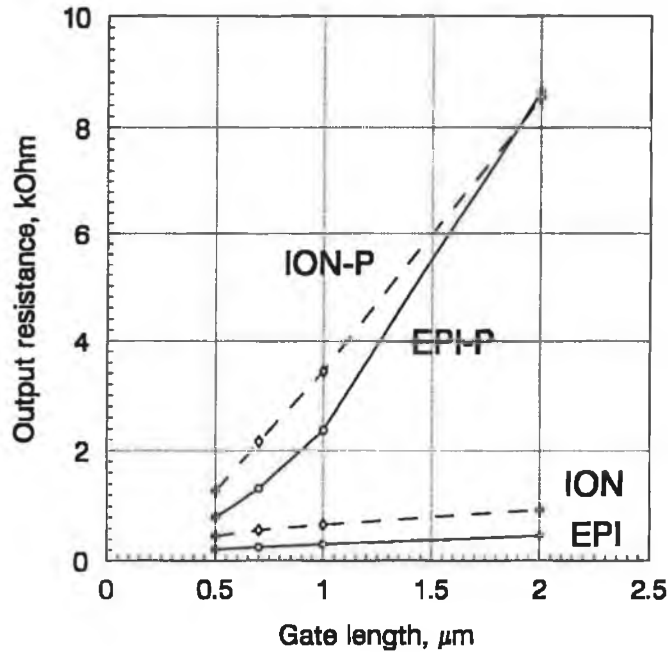

Figure 5.35: Output resistance of the epitaxial (full line) and ion-implanted (dashed line) MESFETs.

and an increase of drain current also reduces the output resistance. The output resistance of the ION-P MESFETs conforms to this theory (see Fig. 5.41), but the EPI-P MESFETs show the opposite character(see Fig. 5.40).

It has been already seen throughout this study that simple physical pictures about the processes governing the operation of GaAs MESFETs do not necessarily offer correct explanations for the complex interactions of the physical mechanisms involved. For the time being the problem of unexpected influence of the piezoelectric charge on the output resistance of epitaxial MESFETs still remains unanswered.

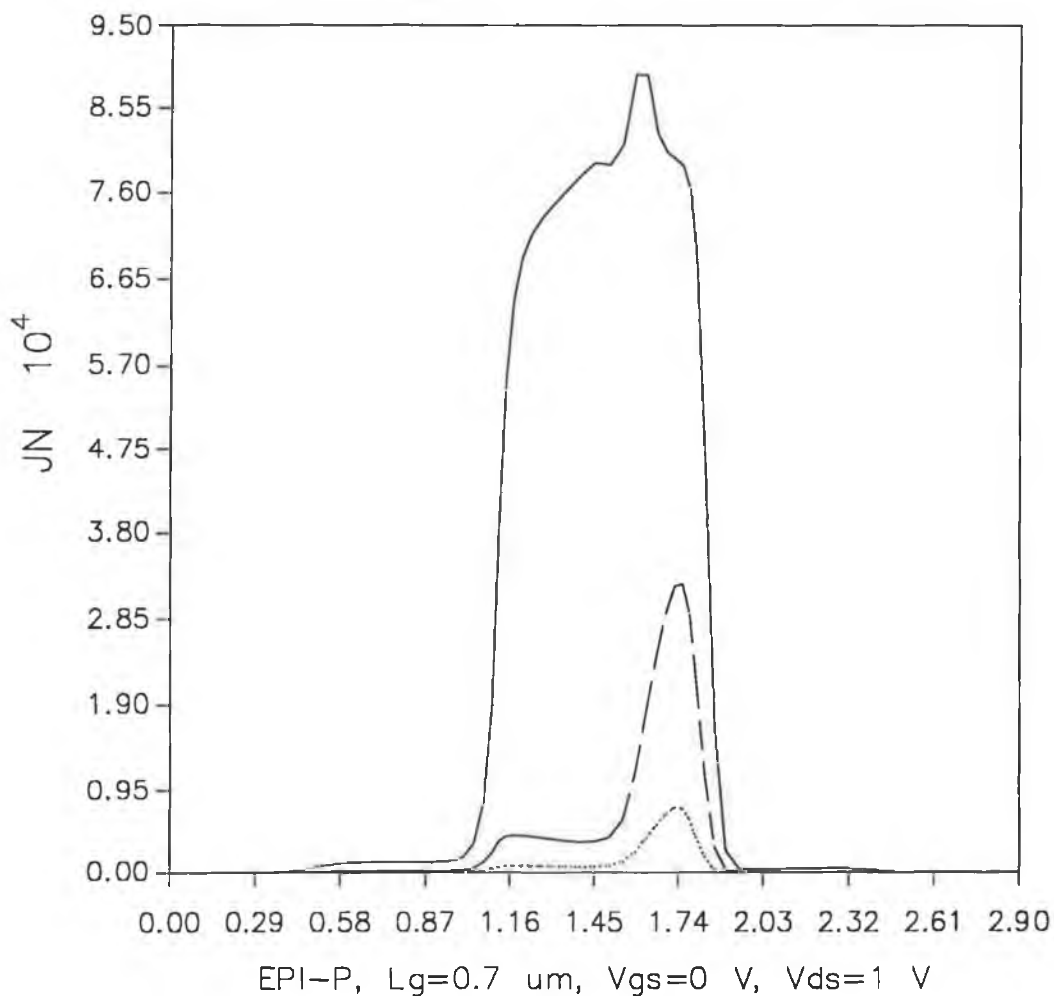

Figure 5.36: Electron current density distribution (in A/cm^2) for $V_{GS} = 0$ V and $V_{DS} = 1$ V at depth $z = 1.51$, 1.50 and 1.49 μm, i.e. 0.09 μm (full line), 0.1 μm (dashed line) and 0.11 μm (dotted line) from the surface. The channel thickness is 0.1 μm. The horizontal axis in the graph is the x axis (the source metal is going from $x = 0$ μm to $x = 0.5$ μm, the gate metal is going from $x = 1.1$ μm to $x = 1.8$ μm and the drain metal is going from $x = 2.4$ μm to $x = 2.9$ μm).

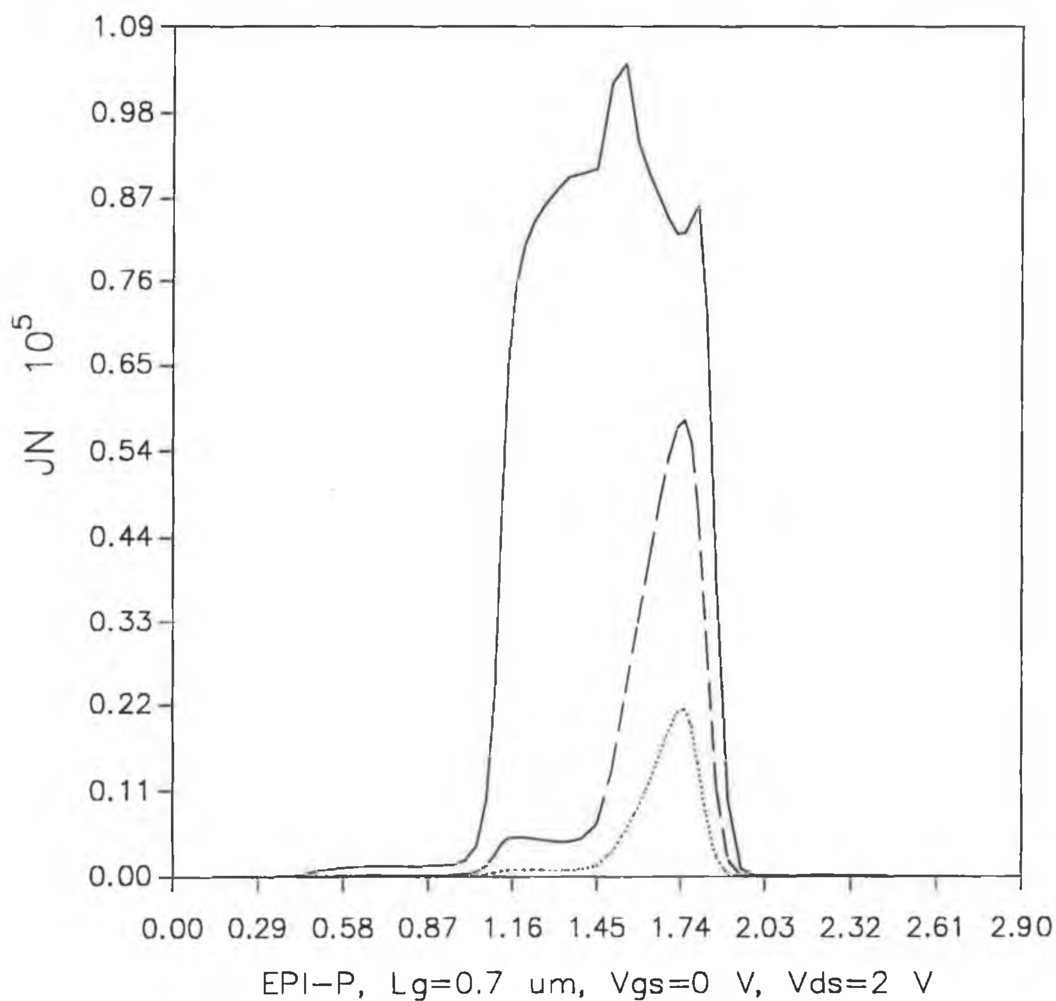

Figure 5.37: Electron current density distribution (in A/cm^2) for $V_{GS} = 0$ V and $V_{DS} = 2$ V at depth $z = 1.51$, 1.50 and 1.49 μm, i.e. 0.09 (full line), 0.1 (dashed line) and 0.11 μm (dotted line) from the surface. The channel thickness is 0.1 μm. Compare with Fig. 5.36. The horizontal axis in the graph is the x axis (the source metal is going from $x = 0$ μm to $x = 0.5$ μm, the gate metal is going from $x = 1.1$ μm to $x = 1.8$ μm and the drain metal is going from $x = 2.4$ μm to $x = 2.9$ μm).

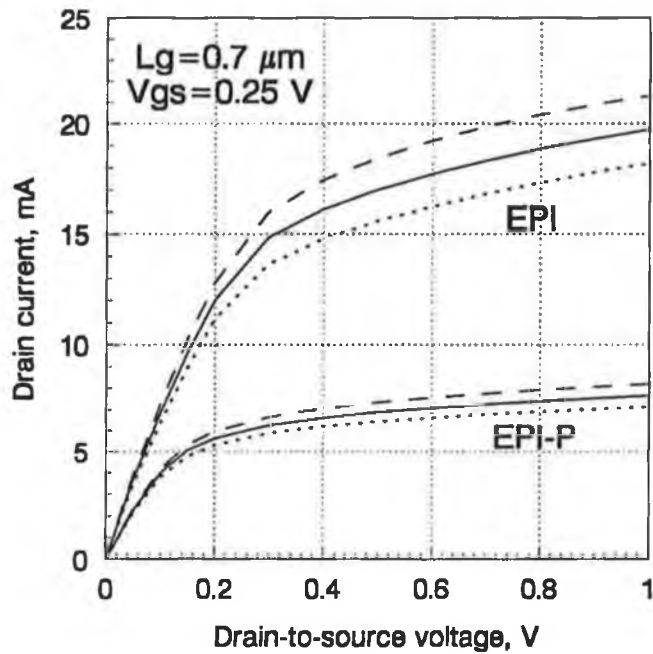

Figure 5.38: Output characteristics for the 0.7 μm gate-length EPI and EPI-P MESFETs at V_{GS} = 0.25 V: reference case(full line), predominantly positive (dashed line) and predominantly negative (dotted line) piezoelectric charge under the gate.

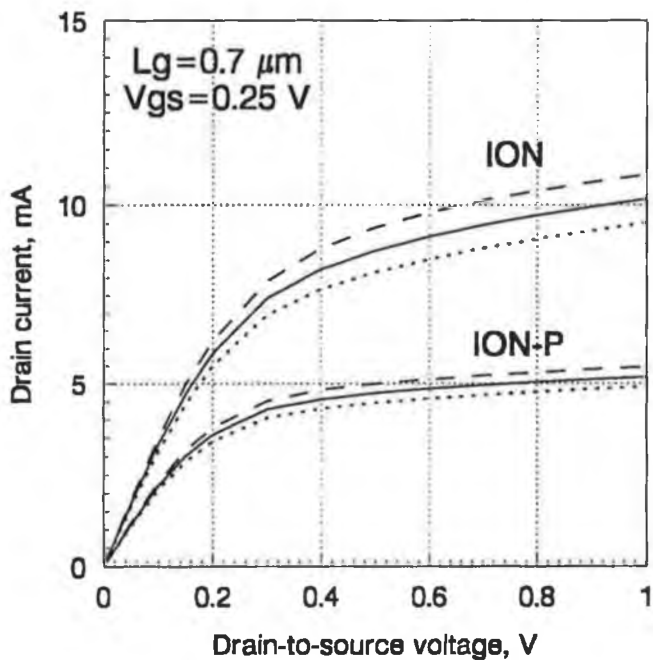

Figure 5.39: Output characteristics for the 0.7 μm gate-length ION and ION-P MESFETs at V_{GS} = 0.25 V: reference case(full line), predominantly positive (dashed line) and predominantly negative (dotted line) piezoelectric charge under the gate.

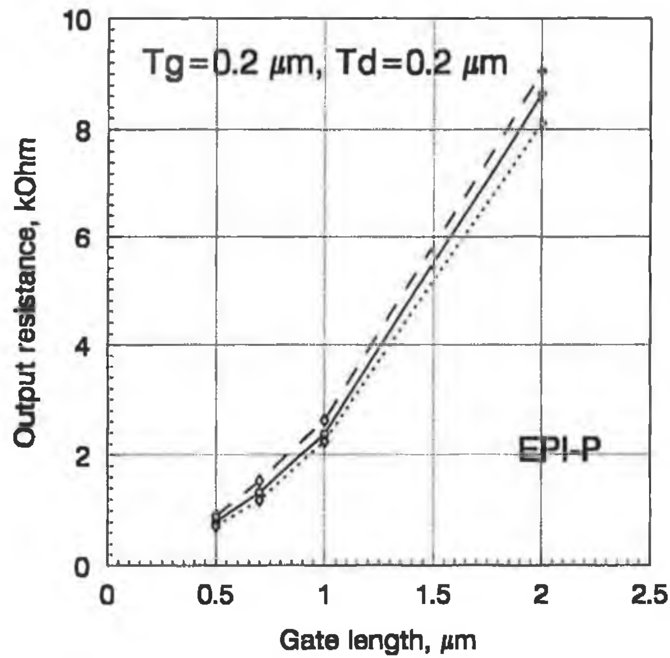

Figure 5.40: Output resistance of the EPI-P MESFETs with piezoelectric charge taken into account: reference simulation (full line), predominantly positive piezoelectric charge (dashed line) and predominantly negative piezoelectric charge (dotted line).

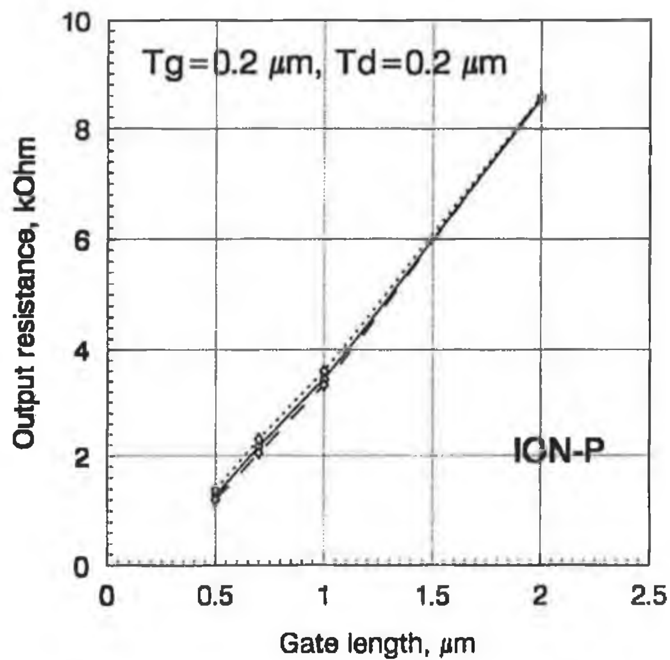

Figure 5.41: Output resistance of the EPI-P MESFETs with piezoelectric charge taken into account: reference simulation (full line), predominantly positive piezoelectric charge (dashed line) and predominantly negative piezoelectric charge (dotted line).

Si_3N_4			
orientation	T_d (μm)	V_{th} (V)	ΔV_{th} (V)
[011]	1.0	0.10	0.21
[011]	0.5	-0.06	0.05
	0	-0.11	0.00
$[01\bar{1}]$	0.5	-0.16	-0.05
$[01\bar{1}]$	1.0	-0.48	-0.37
SiO_2			
orientation	T_d (μm)	V_{th} (V)	ΔV_{th} (V)
$[01\bar{1}]$	1.2	0.2	0.3
$[01\bar{1}]$	0.6	0.1	0.2
	0	-0.1	0.0
[011]	0.6	-0.7	-0.6
[011]	1.2	-1.4	-1.3

Table 5.4: Dependence of the threshold voltage and the threshold voltage shift on the dielectric thickness and dielectric material (Si_3N_4 and SiO_2) for the 0.7 μm gate-length ion-implanted MESFET [19].

5.6 Experiments versus simulations

It has been already mentioned that a comprehensive comparison between the simulations performed in this study and the published experimental data [14]–[20] is not possible because of the lack of geometrical and doping characteristics of the MESFETs used in experiments and because only the influence of the piezoelectric charge on the threshold voltage has been reported, i.e. the transfer characteristics, output characteristics, transconductance, subthreshold current slope and output resistance are not reported.

Two papers published by the same group of authors shall be discussed [19, 20], first of all to compare the respective experiments and secondly, to demonstrate the severity of piezoelectric effects in real MESFET devices.

Table 5.4 shows the threshold voltages for the 0.7 μm gate-length ion-implanted MESFET discussed in [19]. The dielectric material and the dielectric thickness are varied. Table 5.5 shows the threshold voltages for the 0.7 μm gate-length ion-implanted MESFET with SiO_2 used as dielectric. Only the results for the $[01\bar{1}]$ orientation are presented in [20].

There are a number of points worth noting:

1. Si_3N_4 and SiO_2 introduce opposite threshold voltage shifts for the same MESFET orientation.

SiO_2			
orientation	T_d (μm)	V_{th} (V)	ΔV_{th} (V)
[01$\bar{1}$]	1.2	0.15	0.60
[01$\bar{1}$]	0.6	0.0	0.45
[01$\bar{1}$]	0.3	-0.15	0.30
	0	-0.45	0.00

Table 5.5: Dependence of the threshold voltage and the threshold voltage shift on the dielectric thickness (SiO_2) for the 0.7 μm gate-length ion-implanted MESFET [20].

2. Threshold voltage shift is lower when Si_3N_4 is used as dielectric.

3. The results for SiO_2 in Table 5.4 show that saturation occurs for the positive threshold voltage shifts.

4. When comparing the results for SiO_2 from Tables 5.4 and 5.5 it can be seen that the positive threshold voltage shifts for the same dielectric thicknesses presented in [20] are twice as high as the threshold voltage shifts in [19], although the same technological process has been used to evaporate the SiO_2 dielectric in both experiments as well as the same ion-implantation process.

5. The difference in the threshold voltage between the [01$\bar{1}$] and [011] orientations is 1.6 V for SiO_2 with $T_d = 1.2$ μm, and it is 0.5 V for Si_3N_4 with $T_d = 1$ μm (Table 5.4).

Firstly, we conclude that the influence of the stress induced piezoelectric charge is very pronounced. Secondly, the MESFETs produced by the same technological processes show a remarkable spread of the threshold voltage shift, making the comparison between experiments and simulations even more complicated.

The threshold voltage shift obtained in this study by the simulations of the 0.7 μm gate-length ION-P MESFET is $+/-$ 30 mV (see Fig. 5.21) and a rough approximation for the 0.7 μm gate-length ION MESFET presented in Section 5.3.4 suggests that the threshold voltage shift is $+/-$ 300 mV for the dielectric stress $\sigma_d = +/- 2 \cdot 10^8$ N/m^2, dielectric thickness $T_d = 0.2$ μm and Si_3N_4 used as dielectric.

As there is no mention of any procedure undertaken to enhance the electron confinement in the ion-implanted MESFETs reported in [19, 20], the approxi-

mation of the threshold voltage shift for the ION MESFET shall be used for comparison.

The results for SiO_2 presented in Tables 5.4 and 5.5 are used for comparison because Table 5.2 presented in this study suggests that the difference between the results obtained with SiO_2 and Si_3N_4 is approximately 20%, which is much less than the uncertainty in the dielectric stress. The work [19] suggests that the intrinsic dielectric stress of SiO_2 is about mid 10^8 N/m^2. Furthermore, whatever is the dielectric stress obtained in [19], the one obtained by the same group of authors in [20] is 2 to 3 times larger.

The difference in the dielectric thickness is taken into account by scaling downwards by a factor of 3 the threshold voltage shift obtained for $T_d = 0.6$ μm in Table 5.4 and by a factor of 1.5 the V_{th} shift obtained for $T_d = 0.3$ μm in Table 5.5. These scalings give ΔV_{th} of +70 mV and −200 mV for the results in Table 5.4 and +200 mV for the results in Table 5.5.

Considering the uncertainty in the estimated dielectric stress for the case of the 0.7 μm gate-length ION MESFET presented in this study, the threshold voltage shifts of $+/-$ 300 mV calculated here compare very well with the scaled threshold voltage shifts of +70 (+200) mV and −200 mV obtained in the experiments [19, 20].

Chapter 6

Conclusion

The goals of this study are to contribute to the methodology involved in applying numerical electronic device simulation, and specifically, the application of this methodology to the study of piezoelectric effects in GaAs MESFETs.

To fulfil these goals a 3D numerical simulation package EVEREST has been enhanced by the introduction of models for GaAs device physics. Firstly, the Schottky barrier model or rectifying contact model has been added to the simulator to allow simulations of MESFETs. Then, GaAs specific models for the energy gap, the effective electron and hole concentrations, the intrinsic concentration and the intrinsic Fermi level have been defined as well as the electron mobility models. When considering the fact that both the Schottky barrier model and the field-dependent mobility model are very demanding from the numerical point of view (the former model because of huge gradients of potential and quasi-Fermi level and the latter because of negative differential mobility), the EVEREST simulator has proved to be very robust and a valuable tool for analysis of GaAs MESFETs.

To verify the applicability of the numerical device simulation, an ion-implanted MESFET has been simulated and the results have been compared with experimental data. The disagreement obtained has been attributed to the dependence of the electric field on the magnitude of the electric field instead of on the projection of the electric field on the direction of the current flow. When the projection of the electric field has been used as the driving force that defines the electron mobility, good agreement between simulation and experiments has been obtained. In the iterative process of matching the results of simulation and experiment the low-field mobility and critical electric field have been varied. It has been seen that relatively high differences in the electron velocity characteristics result in relatively small differences in the

drain currents.

Furthermore, a discussion on the GaAs electron velocity models has been presented where it has been shown that various authors, using completely different electron velocity models, have successfully matched the same experimental results. Such a situation has triggerred the conclusion that the simulation of GaAs MESFETs may be regarded as an art as well as a science!

To conclude the chapter on GaAs MESFET simulation, epitaxial and ion-implanted MESFETs with differing gate lengths have been analysed. The accuracy of simulations has been discussed from the mathematical and physical point of view.

When considering the second major goal, the study of piezoelectric effects in GaAs MESFETs, the work has been divided into two parts. Firstly, the numerical stress simulation and derivation of the resulting piezoelectric charge distributions have been described, and secondly, the influence of piezoelectric charge on electrical characteristics of GaAs MESFETs has been discussed.

The finite-element method has been used as the backbone of the numerical stress simulation. Due to the existence of an analytical solution for the stress fields inside the GaAs substrate for the structure consisting of the GaAs substrate only, the accuracy of the method has been estimated. It has been found that the error in the calculation of the stress fields is relatively small compared to the error introduced in the derivation of the piezoelectric charge. By comparing the impact of analytically and numerically calculated piezoelectric charge on the threshold voltage of epitaxial MESFETs, it has been estimated that the numerical procedure underestimates the piezoelectric charge by approximately 25%. The source of error has been attributed to the finite mesh size and the interpolation procedure used to derive the piezoelectric charge from the calculated values of stress fields. Although the error is relatively large, it has been found that it does not depend on the gate length, thus making the method reliable when the influence of the varying gate length has to be estimated.

Furthermore, the force load model and the uniform displacement model have been discussed. It has been concluded that there is no clear method of relating the average dielectric stress to the uniform displacement model. However, it has been pointed out that the uniform displacement model is a good approximation of the stress produced by an experimental application of an external load. Thus, a good agreement found between the experiments

with externally applied load and the results obtained by the application of the uniform displacement model, proves that the coupled system of electrical and mechanical quantities may be solved in a decoupled form.

Before the influence of piezoelectric charge is discussed the impact of the high acceptor substrate doping is reviewed. A highly doped *p*-type layer below the channel substantially reduces variations of the threshold voltage shift with gate length, improves the subthreshold current slope, decreases the saturation current and increases the output resistance. Except for a reduced current in the saturation region, all other changes are desired. The transconductance of the ion-implanted MESFETs has not been substantially affected. However, in the case of epitaxial MESFETs a highly doped *p*-type layer also enhances the kink effect by improving the confinement of electrons within the channel and by pronouncing the effect of negative differential mobility.

When considering the piezoelectric charge, an emphasis has been put on depicting a physically correct simulation model for the analysis of stress fields and resulting piezoelectric charge distributions in the GaAs substrate. The force load model applied on the metal/dielectric/GaAs structure is suggested as a good mathematical representation of the physical processes involved. The use of this model is advocated because it can be easily related to the measurable quantities that describe the dielectric stress, and furthermore the metal/dielectric/GaAs structure should be preferred because all three materials influence the stress distribution in the GaAs substrate.

The impact of the piezoelectric charge can be observed as a modulation of the doping profile in the substrate just below the gate. Predominantly negative piezoelectric charge under the gate enhances electron confinement just like an increased acceptor concentration in the substrate, and predominantly positive piezoelectric charge has the opposite effect. It has been shown that higher *p*-type doping in the substrate reduces the variations of electrical characteristics caused by piezoelectric charge as well as the variations caused by varying gate length, and the introduction of a *p*-type layer below the channel is suggested as an effective method for improvement of the uniformity of electrical characteristics as well as a method for reduction of the impact of piezoelectric charge.

Comparison between experimental data and simulation results has shown firstly, that the influence of piezoelectric charge on the threshold voltage shift in real MESFETs is huge and secondly, that the stress produced by depositing

the dielectric layer is hard to control even when the same processing technology is used.

The conclusion is that, although predominantly negative piezoelectric charge can be used to improve electrical characteristics of GaAs MESFETs, to allow more flexibility in the design of GaAs ICs it is necessary to reduce the impact of piezoelectric charge either by using highly doped p-type substrate (or burried p-layer) or by depositing the gate electrode in the $< 001 >$ directions. Improvement of electrical characteristics by intentional introduction of piezoelectric charge can not be recommended because the magnitude of the dielectric stress is difficult to control.

For future work, there are two topics that seem to be worth investigating. Firstly, the influence of piezoelectric charge on the gate-to-source and gate-to-drain capacitance would be an interesting area of research because these two quantities would enable a design engineer to make preliminary judgments about the ultimate performance potential of GaAs MESFETs. Secondly, experimental work is needed to determine first of all the magnitude and then the possibility of uniform control of the stress produced by the dielectric layer.

Bibliography

[1] C. A. Mead, "Schottky barrier gate field effect transistor," *Proc. IEEE*, vol. 54, no. 2, pp. 307–308, 1966.

[2] M. Feng, J. Laskar, J. Kruse, and R. Neidhard, "Ultra low-noise performance of 0.15-micron gate GaAs MESFET's made by direct ion implantation for low-cost MMIC's applications," *IEEE Microwave and Guided Wave Lett.*, vol. 2, no. 5, pp. 194–195, 1992.

[3] K. Yamasaki, N. Kato, and M. Hirayama, "Below 10 ps/gate operation with buried p-layer SAINT FETs," *Electronics Lett.*, vol. 20, no. 25/26, pp. 1029–1031, 1984.

[4] M. Hirayama, M. Togashi, N. Kato, M. Suzuki, Y. Matsuoka, and Y. Kawasaki, "A GaAs 16-kbit static RAM using dislocation-free crystal," *IEEE Trans. Electron Devices*, vol. ED-33, no. 1, pp. 104–110, 1986.

[5] R. B. Brown, M. Upton, A. Chandna, T. R. Huff, T. N. Mudge, and R. E. Oettel, "Gallium-arsenide process evaluation based on a RISC microprocessor example," *IEEE J. Solid-state Circuits*, vol. 28, no. 10, pp. 1030–1037, 1993.

[6] D. L. Lile, "Metal-insulator-GaAs structures," in *Gallium Arsenide*, Eds. M. J. Howes and D. V. Morgan, New York: Wiley, 1985.

[7] J. R. Chelikowsky and M. L. Cohen, "Nonlocal pseudopotential calculations for the electronic structure of eleven diamond and zinc-blende semiconductors," *Phys. Rev. B*, vol. 14, no. 2, pp. 556–582, 1976.

[8] S. I. Long and S. E. Butner, *Gallium arsenide digital integrated circuit design*, New York: McGraw-Hill, 1990.

[9] S. Adachi, "GaAs, AlAs, and $AL_xGa_{1-x}As$: Material parameters for use in research and device applications," *J. Appl. Phys.*, vol. 58, no. 3, pp. R1–R29, 1985.

[10] H. Nagai, "Anisotropic bending during epitaxial-growth of mixed-crystals on GaAs substrate," *J. Appl. Phys.*, vol. 43, no. 10, p. 4254, 1972.

[11] G. H. Oleson, M. S. Abrahms, and T. J. Zamerowski, "Asymmetric cracking in III-V compounds," *J. Electrochem. Soc.*, vol. 121, no. 12, pp. 1650–1656, 1974.

[12] H. Booyens, J. S. Vermaak, and G. R. Proto, "Asymmetric deformation of GaAs single-crystals," *J. Appl. Phys.*, vol. 49, no. 11, pp. 5435–5440, 1978.

[13] Y. Tarui, Y. Komiya, and Y. Harada, "Preferential etching and etched profile of GaAs," *J. Electrochem. Soc.*, vol. 118, pp. 118–122, 1971.

[14] C. P. Lee, R. Zucca, and B. M. Welch, "Orientation effect on planar GaAs Schottky barrier field effect transistors," *Appl. Phys. Lett.*, vol. 37, no. 1, pp. 311–313, 1980.

[15] N. Yokoyama, H. Onodera, T. Ohnishi, and A. Shibatomi, "Orientation effect of self-aligned source/drain planar GaAs Schottky barrier field-effect transistors," *Appl. Phys. Lett.*, vol. 42, no. 3, pp. 270–271, 1983.

[16] R. A. Sadler and L. F. Eastman, "Orientation effect reduction through capless annealing of self-aligned planar GaAs Schottky barrier field-effect transistors," *Appl. Phys. Lett.*, vol. 43, no. 9, pp. 865–867, 1983.

[17] M. F. Chang, C. P. Lee, P. M. Asbeck, R. P. Vahrenkamp, and C. G. Kirkpatrick, "Role of the piezoelectric effect in device uniformity of GaAs integrated circuits," *Appl. Phys. Lett.*, vol. 45, no. 3, pp. 279–281, 1984.

[18] P. M. Asbeck, C. P. Lee, and M. F. Chang, "Piezoelectric effects in GaAs FETs and their role in orientation-dependent device characteristics," *IEEE Trans. Electron Devices*, vol. ED-31, no. 10, pp. 1377–1380, 1984.

[19] T. Ohnishi, T. Onodera, N. Yokoyama, and H. Nishi, "Comparison of the orientation effect of SiO_2- and Si_3N_4-encapsulated GaAs MESFET's," *IEEE Electron Device Lett.*, vol. EDL-6, no. 4, pp. 172–174, 1985.

[20] T. Onodera, T. Ohnishi, N. Yokoyama, and H. Nishi, "Improvement in GaAs MESFET performance due to piezoelectric effect," *IEEE Trans. Electron Devices*, vol. ED-32, no. 11, pp. 2314–2318, 1985.

[21] M. Kanamori, H. Ono, T. Furutsuka, and J. Matsui, "External stress effect on GaAs MESFET characteristics," *IEEE Electron Device Lett.*, vol. EDL-8, no. 5, pp. 228–230, 1987.

[22] P. J. McNally, L. S. Cooper, and J. J. Rosenberg, "Investigation of stress effects on the direct current characteristics of GaAs metal-semiconductor field-effect transistors through the use of externally applied loads," *Appl. Phys. Lett.*, vol. 52, no. 21, pp. 1800–1802, 1988.

[23] J. C. Ramirez, P. J. McNally, L. S. Cooper, J. J. Rosenberg, L. B. Freund, and T. N. Jackson, "Development and experimental verification of a two-dimensional numerical model of piezoelectrically induced threshold voltage shifts in GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. ED-35, no. 8, pp. 1232–1240, 1988.

[24] P. J. McNally, J. J. Rosenberg, T. N. Jackson, and J. C. Ramirez, "Modelling and experimental analysis of the impact of process induced stress on the electrical performance of GaAs MESFETs," *Solid-State Electron.*, vol. 36, no. 11, pp. 1597–1612, 1993.

[25] W. Shockley, "A unipolar field-effect transistor," *Proc. IRE*, vol. 40, no. 11, pp. 1365–1376, 1952.

[26] J. J. Barnes and R. J. Lomax, "Two-dimensional finite element simulation of semiconductor devices," *Electronics Lett.*, vol. 10, no. 16, pp. 341–343, 1974.

[27] J. J. Barnes, R. J. Lomax, and G. I. Haddad, "Finite-element simulation of GaAs MESFET's with lateral doping profiles and submicron gates," *IEEE Trans. Electron Devices*, vol. ED-23, no. 9, pp. 1042–1048, 1976.

[28] K. Yamaguchi, S. Asai, and H. Kodera, "Two-dimensional numerical analysis of stability criteria of GaAs FETs," *IEEE Trans. Electron Devices*, vol. ED-23, no. 12, pp. 1283–1290, 1976.

[29] J. J. Barnes and R. J. Lomax, "Finite-element methods in semiconductor device simulation," *IEEE Trans. Electron Devices*, vol. ED-24, no. 8, pp. 1082–1089, 1977.

[30] H. L. Grubin and T. M. McHugh, "Hot electron transport effects in field effect transistors," *Solid-State Electron.*, vol. 21, no. 1, pp. 69–73, 1978.

[31] H. L. Grubin, J. K. Ferry, and K. R. Gleason, "Spontaneous oscillations in gallium arsenide field effect transistors," *Solid-State Electron.*, vol. 23, no. 2, pp. 157–172, 1980.

[32] S. E. Laux, "Two-dimensional simulation of gallium-arsenide MESFETs using the finite-element method," Ph.D. Dissertation, University of Michigan, 1981.

[33] C. M. Snowden, M. J. Howes, and D. V. Morgan, "Large-signal modeling of GaAs MESFET operation," *IEEE Trans. Electron Devices*, vol. ED-30, no. 12, pp. 1817–1824, 1983.

[34] P. R. H. Riemenschneider and K. L. Wang, "A finite-element program for modeling transient phenomena in GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. ED-30, no. 9, pp. 1142–1150, 1983.

[35] M. Tomizawa, K. Yokoyama, A. Yoshii, and T. Sudo, "Two-dimensional device simulator for gate-level characterization," *Solid-State Electron.*, vol. 25, no. 9, pp. 913–916, 1982.

[36] M. Hirose, Y. Yoshida, and N. Toyoda, "An improved two-dimensional simulation model (MEGA) for GaAs MESFET applicable to LSI design," *IEEE Trans. Comp. Aided Design*, vol. CAD-7, no. 2, pp. 225–230, 1988.

[37] R. W. Hockney and R. A. Warriner, "Two-dimensional particle models in semiconductor-device analysis," *Electronics Lett.*, vol. 10, no. 23, pp. 484–486, 1974.

[38] R. A. Warriner, "Computer simulation of gallium arsenide field effect transistors using Monte-Carlo methods," *Solid-State and Electron Devices*, vol. 1, no. 4, pp. 105–110, 1977.

[39] C. Moglestue and S. J. Beard, "A particle model simulation of field effect transistors," *Proc. NASECODE I Conf.*, pp 232–236, Dublin: Boole Press, 1979.

[40] C. Moglestue, "A Monte-Carlo particle model study of the influence of the doping profiles on the characteristics of field-effect transistors," *Proc. NASECODE II Conf.*, pp. 244–249, Dublin: Boole Press, 1981.

[41] J. F. Pone, R. C. Castagne, J. P. Courat, and C. Arnodo, "Two-dimensional particle modeling of submicrometer gate GaAs FET's near pinchoff," *IEEE Trans. Electron Devices*, vol. ED-29, no. 8, pp. 1244–1255, 1982.

[42] A. Yoshii, M. Tomizawa, and K. Yokoyama, "Accurate modeling for submicrometer-gate Si and GaAs MESFET's using two-dimensional particle simulation," *IEEE Trans. Electron Devices*, vol. ED-30, no. 10, pp. 1376–1380, 1983.

[43] B. Carnez, A. Cappy, A. Kaszynski, E. Constant, and G. Salmer, "Modelling of a submicrometer gate field-effect transistor including effects of non-stationary electron dynamics," *J. Appl. Phys.*, vol. 51, no. 1, pp. 784–790, 1980.

[44] R. K. Cook and J. Frey, "Two-dimensional numerical simulation of energy transport effects in Si and GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. ED-29, no. 6, pp. 970–977, 1982.

[45] J. A. Higgins and D. N. Pattanayak, "A numerical approach to modelling the ultra short gate MESFET," *IEEE Trans. Electron Devices*, vol. ED-29, no. 2, pp. 179–183, 1982.

[46] S. Yoganathan and S. K. Banerjee, "A new decoupled algorithm for non-stationary transient simulations of GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. 39, no. 7, pp. 1578–1587, 1992.

[47] S. Selberherr, *Analysis and simulation of semiconductor devices*, Wien: Springer-Verlag, 1984.

[48] C. Greenough, C. J. Fitzsimons, and R. F. Fowler, "Software for modelling semiconductor devices in three dimensions," *Report RAL-91-042*, Rutherford Appleton Laboratory, UK, April 1991.

[49] S. J. Polak, C. Den Heijer, W. H. A. Schilders, and P. Markowich, "Semiconductor device modelling from the numerical point of view," *Int. J. Num. Meth. Eng.*, vol. 24, pp. 763–838, 1987.

[50] J. S. Blakemore, "Semiconducting and other major properties of gallium arsenide," *J. Appl. Phys.*, vol. 53, no. 10, pp. R123–R181, 1982.

[51] W. van Roosbroeck, "Theory of the flow of electrons and holes in germanium and other semiconductors," *Bell System Technical Journal*, vol. 29, no. 4, pp. 560–607, 1950.

[52] T. J. Maloney and J. Frey, "Transient and steady-state electron transport properties of GaAs and InP," *J. Appl. Phys.*, vol. 48, no. 2, pp. 781–787, 1977.

[53] J. T. Lue, "Theory of Schottky barrier heights of amorphous MIS solar cells," *Solid-State Electron.*, vol. 25, no. 9, pp. 869–874, 1982.

[54] A. P. Gnädinger and H. E. Talley, "Quantum mechanical calculations of the carrier distribution and the thickness of the inversion layer of a MOS field-effect transistor," *Solid-State Electron.*, vol. 13, no. 9, pp. 1301–1309, 1970.

[55] C. R. Crowell and M. Beguwala, "Recombination velocity effects on current diffusion and IMREF in Schottky barriers," *Solid-State Electron.*, vol. 4, no. 11, pp. 1149–1157, 1971.

[56] W. L. Engl, H. K. Dirks, and B. Meinerzhagen, "Device modeling," *Proc. IEEE*, vol. 71, no. 1, pp. 10–33, 1983.

[57] Landolt-Börnstein, *New series*, Ed. K.-H. Hellwege, vol. 11 (1979) and 17a (1982), and Ed. O. Madelung, vol. 22a (1987), Berlin: Springer-Verlag.

[58] D. S. Newman, D. K. Ferry, and J. R. Sites, "Measurement and simulation of GaAs FET's under electron beam irradiation," *IEEE Trans. Electron Devices*, vol. ED-30, no. 7, pp. 849–855, 1983.

[59] G. D. Alley, " High-voltage two-dimensional simulations of permeable base transistors," *IEEE Trans. Electron Devices*, vol. ED-30, no. 1, pp. 52–60, 1983.

[60] A. S. Grove, *Physics and technology of semiconductor devices*, New York: Wiley, 1967.

[61] S. M. Sze, *Physics of semiconductor devices*, New York: Wiley, 1969.

[62] R. C. Weast and M. J. Astle, *CRC handbook of chemistry and physics*, Boca Raton, Florida: CRC Press, 1981.

[63] C. Hilsum, "Simple empirical relationship between mobility and carrier concentration," *Electron.Lett.*, vol. 10, no. 12, pp. 259–260, 1974.

[64] J. G. Ruch and W. Fawcett, "Temperature dependence of the transport properties of gallium arsenide determined by a Monte Carlo method," *J. Appl. Phys.*, vol. 41, no. 9, pp. 3843–3849, 1970.

[65] D. L. Rode and S. Knight, "Electron transport in GaAs," *Phys. Rev. B*, vol. 3, no. 8, pp. 2534–2541, 1971.

[66] N. Uchitomi, M. Nagaoka, K. Shimada, T. Mizoguchi, and N. Toyoda, "Characterization of reactively sputtered WN_X film as gate metal for self-alignment GaAs metal-semiconductor field effect transistors," *J. Vac. Sci. Technol. B*, vol. 4, no. 6, pp.1392–1397, 1986.

[67] K. Yamasaki and M. Hirayama, "Determination of effective saturation velocity in n^+ self-aligned GaAs MESFET's with submicrometer gate lengths," *IEEE Trans. Electron devices*, vol. ED-33, no. 11, pp. 1652–1658, 1986.

[68] Y.-K. Feng, "New $v(E)$ relationship for GaAs," *Electron. Lett.*, vol. 21, no. 10, pp. 453–454, 1985.

[69] H. Z. Fardi and R. E. Hayes, "Modeling submicrometer GaAs MESFET's using PISCES with an apparent gate-length-dependent velocity-field relation," *IEEE Trans. Electron Devices*, vol. ED-39, no. 7, pp. 1778–1780, 1992.

[70] G. Arlt and P. Quadflieg, "Piezoelectricity in III-V compounds with a phenomenological analysis of the piezoelectric effect," *Phys. Stat. Sol.*, vol. 25, pp. 323–330, 1968.

[71] S. P. Timoshenko and J. N. Goodier, *Theory of elasticity*, 3rd ed., Singapore: McGraw-Hill, 1982.

[72] W. Voigt, *Lehrbuch der Kristallphysik*, Leipzig: Teubner, 1928.

[73] J. F. Nye, *Physical properties of crystals*, Oxford: Clarendon Press, 1957.

[74] O. C. Zienkiewicz, *The finite element method*, 3rd ed., New York: McGraw-Hill, 1977.

[75] C. Greenough and K. Robinson, *Finite element library*, Didcot, Oxfordshire, England: Science and Engineering Research Council, 1981.

[76] I. H. Shames, *Introduction to solid mechanics*, 2nd ed., New Jersey: Prentice-Hall, 1989.

[77] E. Hinton and J. S. Campbell, "Local and global smoothing of discontinuous finite element functions using a least squares method," *Int. J. Num. Meth. Eng.*, vol. 8, pp. 461–480, 1974.

[78] P. A. Kirkby, P. R. Selway, and L. D. Westbrook, "Photoelastic waveguides and their effect on stripe-geometry GaAs/GaAlAs lasers," *J. Appl. Phys.*, vol. 50, no. 7, pp. 4567–4579, 1979.

[79] H.Booyens, G. R. Proto, and J. H. Basson, "Strain effects associated with $Si0_2$ layers evaporated onto GaAs," *J. Appl. Phys.*, vol. 54, no. 10, pp. 5779–5784, 1983.

[80] K. L. McLaughlin and M. S. Birrittella, "Preferential diffusion and orientation effects of Schottky-barrier GaAs field-effect transistors," *Appl. Phys. Lett.*, vol. 44, no. 2, pp.252–254, 1984.

[81] K. Yamasaki, K. Asai, and K. Kurumada, "GaAs LSI-directed MESFETs with self-aligned implantation for n^+-layer technology (SAINT)," *IEEE Trans. Electron Devices*, vol. ED-29, no. 11, pp. 1772–1777, 1982.

[82] C. Blaauw, "Stress in chemical-vapor-deposited SiO_2 and plasma-SiN_x films on GaAs and Si," *J. Appl. Phys.*, vol. 54, no. 9, pp. 5064–5068, 1983.

[83] M. F. Ashby and D. R. H. Jones, *Engineering Materials I, International Series on Materials Science and Technology*, vol. 34, New York: Pergamon, 1980.

[84] T. Wada and J. Frey, "Physical basis of short-channel MESFET operation," *IEEE J. Solid-State Circuits*, vol. SC-14, no. 2, pp. 398–412, 1979.

[85] P. Bonjour, R. Castagne, J. F. Pone, J. P. Courat, G. Bert, G. Nuzillat and M. Peltier, "Saturation mechanism in 1 μm gate GaAs FET with

channel-substrate interfacial barrier," *IEEE Trans. Electron Devices*, vol. ED-27, pp. 1019, 1980.

[86] W. R. Curtice and Y.-H. Yun, "A temperature model for the GaAs MESFET," *IEEE Trans. Electron Device*, vol. ED-28, no. 8, pp. 954–962, 1981.

[87] K. Yokoyama, M. Tomizawa, T. Takada, and A. Yoshii, "Anomalous gate-to-drain capacitance characteristics of GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. ED-30, no. 6, pp. 719–721, 1983.

[88] I. A. Blech and E. S. Meieran, "Enhanced X-ray diffraction from substrate crystals containing discontinuous surface films," *J. Appl. Phys.*, vol. 38, no. 7, pp. 2913–2919, 1967.

[89] J. Sone and Y. Takayama, "A small-signal analytical theory for GaAs field-effect transistors at large drain voltages," *IEEE Trans. Electron Devices*, Vol. ED-25, no. 3, pp. 329–337, 1978.