Mapping of Mechanical, Thermomechanical and Wire-Bond Strain Fields in Packaged Si Integrated Circuits Using Synchrotron White Beam X-Ray Topography

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Abstract—Thermal processing steps used during the production of packaged integrated circuits can lead to severe thermomechanical stresses. In addition, the process of bonding wires to contact pads can also lead to strain field generation. A feasibility study using the application of white beam synchrotron x-ray topography to packaged erasable programmable read-only memory (EPROM) Si integrated circuits (ICs) has been undertaken in order to produce maps of the strain fields induced by such processing steps. This technique provides depth-resolved mapping with spatial resolutions currently in the region of 5–10 μ m throughout the entire mapping volume. Furthermore, the use of different experimental geometries allows the user to nondestructively probe the strain fields present at the wafer surface right through to the back side.

Index Terms—High resolution, nondestructive evaluation, packaged integrated circuits, strain fields, synchrotron x-ray topography.

I. INTRODUCTION

URRENT and future electronic equipment technologies require smaller and thinner packaged integrated circuits (ICs). These trends toward miniaturization are themselves imposing ever-tighter constraints in IC packaging, whose rôle is now considered a vital factor in the development of electronic system concepts [1]. The process of fabricating a complete packaged integrated circuit is a complex one, involving the thermal processing of many materials of differing thermal expansion coefficients, e.g., moulding compounds, the die itself, die attach glue and die pad [2], [3]. Mismatches in these coefficients can lead to the build-up of thermomechanical

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strain. These process-induced stresses can produce cracks in the packaging and any consequent moisture leakage could lead to corrosion and eventual IC failure [4]. Another source of strain fields is due to the bonding of wires to the die itself [5], [6]. Weak bonds could be detected through a monitoring of variations in these strain fields, and this could be used to predict the location of bonds, which may lift off their pads. Elevated temperature steps used for solder reflow can also lead to package cracking and subsequent IC failure [7]. Other studies have shown that device parametric deviations (e.g., saturation drain current, $I_{\rm DSAT}$, in NMOS and PMOS transistors) are attributable to biaxial stresses resulting from the plastic packaging process [8].

For all of the above, an effective means of nondestructive analysis is required. Current approaches include

- a) finite element modeling (FEM) [9];
- b) the positioning of miniature strain gauges especially using piezoresistive stress sensors [10]–[15];
- c) scanning acoustic microscopy, in either C-mode or (scanning laser acoustic microscopy) SLAM-mode [16], [17];
- d) using Moiré interferometry [18]-[22];
- e) photoelastic techniques [23]–[26].

Each of these techniques possesses considerable merits and demerits, though naturally they are all useful for soliciting vital information about the state of strain in IC packages. FEM techniques can provide useful predictive models. On-chip piezoresistive stress sensors are useful in the study of thermal cycling and consequent stress-induced reliability concerns [10]. Such sensors are often used in a rosette configuration [11]-[13]. In one study [11] IC cards were subjected to bending and twisting conditions and stresses of the order of 25-100 MPa were observed under various conditions. However, the chief drawback is that such sensors are useful mainly for stress analysis near the surface of the die [12]-[14] and depth resolution of stresses is not easily achieved [13]. In the case of scanning acoustic microscopy the resolution is dependent on frequency (typically 10-100MHz) and hence on depth [16], [17]. Moiré interferometry [18]–[20] and indeed microscopic Moiré interferometry [22] has been used successfully to provide contour maps of in-plane displacement fields with high sensitivity and high spatial resolution. For example, the Moiré fringes observed in [18] corresponded to deformations of the order of 0.4 μ m, which, for

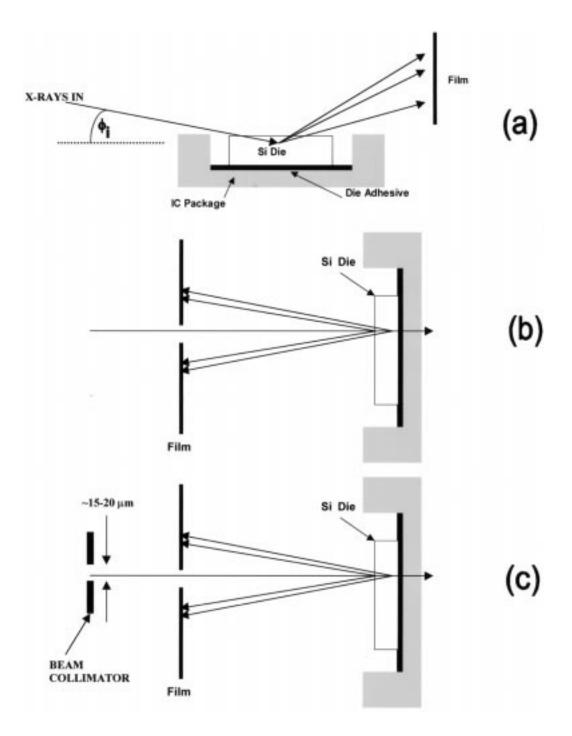


Fig. 1. (a) Schematic details of the grazing incidence diffraction topography (GIDT) geometry, (b) the large area back reflection topography (LA-BRT) geometry, where two reflections are shown on the film, and (c) the back reflection section topography (BRST) geometry, where the same two reflection as in (b) are shown.

the package structures studied, correspond to observed strains of the order of 10^{-3} . Photoelastic response, and in particular infrared photoelasticity has been used to provide quantitative information on the directions and magnitudes of stresses in Si structures [23], [26]. Resolutions are as great as a few tens of nanometers [24], [25]; however this technique relies on the interpretation of the presence of interference fringes and does not allow for a ready visualization of the locations of strain fields and their distributions.

Synchrotron s-ray topography (SXRT) in the grazing incidence diffraction (GID) or back reflection (BRT) geometries

can address some of the drawbacks of the aforementioned techniques and can be usefully used as a complementary analysis tool. SXRT is a genuinely nondestructive technique in that the wafers do not have to be cleaved, and the three-dimensional (3-D) strain fields right through from wafer top-side to back-side can be mapped *in situ*, providing the user with "real" stress evaluation for his/her device structures [27], [28]. The user can vary the depth of penetration through the diffracting Si die and obtain spatial resolutions in the $5{\text -}10~\mu{\rm m}$ range.

The strain fields imposed on the silicon by the adjacent IC packaging materials may be significant enough to be visible via

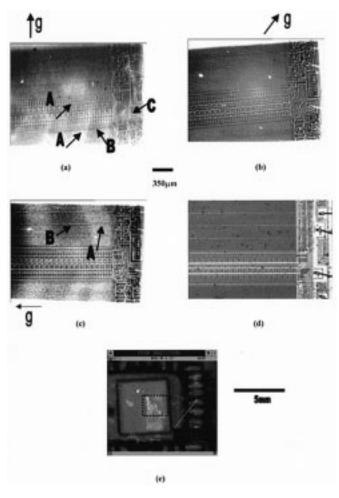


Fig. 2. LA-BRT images for a packaged IC (a) 311 reflection [$t_p=242~\mu{\rm m}$], (b) 620 reflection [$t_p=27~\mu{\rm m}$], (c) 822 reflection [$t_p=62~\mu{\rm m}$], (d) optical micrograph, and (e) scanning acoustic microscopy image of the same EPROM. Diffraction vectors \vec{g} are shown for the topographic images.

orientational contrast (see for example pp. 230 et seq. in [28]). Suppose that the crystal is placed in an x-ray beam of divergence $\Delta \phi$ so that the Bragg reflection from a particular set of lattice planes is obtained for one or more characteristic reflections. If we then examine the diffracted beam as a function of position in a perfect parallel-sided crystal, we would expect to find a uniform field of view in a projection topograph. However, should the crystal contain an imperfect region, e.g., a strained region, misorientated with respect to the otherwise perfect crystal, a contrast between the two regions will be observed if the misorientation exceeds $\Delta \phi$. Since the divergence of synchrotron beams is extremely low (in this study the vertical beam divergence is \sim 0.06 mrad, which is 10–100 times smaller than typical angular shifts observed here) then this contrast mechanism can be activated in many ordinary situations. This implies a limit on the magnitude of strain, which can be observed, will be of the order of 0.06×10^{-3} , or 6×10^{-5} , which is more sensitive than typical Moiré interferometry, for example. The other contrast mechanism, extinction contrast, is even more sensitive to strain (or Si displacement) by up to many orders of magnitude, as discussed in [28Chapter 8]. Thus at worst, a sensitivity to strains of magnitude $>6 \times 10^{-5}$ is expected. One drawback should be noted at this stage—it is very difficult to determine the sign of

TABLE I BACK REFLECTION TOPOGRAPHY RELATIVE NUMBER OF X-RAY PHOTONS ABSORBED BY THE RECORDING FILM (N_{abs}) and X-Ray Penetration Depth (t_p) for Topographs

Reflection Index	λ	N_{abs}	t _p
hkl	(nm)	(relative arbitrary units)	(μ m)
311	0.296	0.28	_
933	0.099	1.00	106
12 4 4	0.074	0.55	242
15 5 5	0.059	0.07	364
620	0.163	1.00	27
12 4 0	0.083	0.07	201
822	0.1217	1.00	62

[&]quot;N/S" indicates "not significant"

Shaded area = does not propagate to recording film

the stain fields which produce contrast on the recording films. More information on the technique is provided in the next section.

II. EXPERIMENTAL

SXRT is a nondestructive technique, which can provide detailed information on the defect distribution in crystals. This imaging technique is based on the difference in reflecting power between perfect and distorted parts of a crystal. It is also sensitive to strain fields because contrast produced by misorientated lattice planes is observed in the topographs made with the continuous spectrum of synchrotron radiation. SXRT is predominantly used for the study of dislocations, planar defects, stacking faults, domain walls in ferromagnetic materials, growth defects, or large precipitates [27]–[29].

The measurements were performed at the Hamburger Synchrotronstrahlungslabor at the Deutsches Elektronen-Synchrotron (HASYLAB am DESY), Hamburg, Germany, utilizing the continuous spectrum of synchrotron radiation from the DORIS III storage ring bending magnet. The ring operates at positron energies of 4.45 GeV and at typical currents of 80–150 mA. The Bragg pattern of topographs was recorded either on a Kodak type SR or on a Kodak High-Resolution SO-343 Professional film having an emulsion grain size of about 0.05 μm .

Three topography techniques were employed in this study:

- 1) grazing incidence diffraction topography (GIDT);
- 2) large area back reflection topography (LA-BRT);
- 3) back reflection section topography (BRST).

These techniques are illustrated in Fig. 1(a)–(c). In GIDT, the x-rays impinge on the surface [see Fig. 1(a)] at an angle $\phi_i > \phi_C$ (the critical angle for total external reflection) [30].

By varying ϕ_i and using a judicious choice of reflections one can examine large areas of the diffracting crystals from depths of < 100 nm to > 100 μ m. In LA-BRT, the x-rays arrive normal to the crystal surface ($\phi_i = 90^\circ$), i.e., a Bragg geometry is used [31]. For the BRST experiments, the geometry is similar to LA-BRT, except that the beam is now collimated to a thin ribbon whose height is 15–20 μ m [32]. Reflections recorded on the film will now contain information on strain, dislocation, etc. distribution through a thin slice of the crystal near the surface.

The x-ray beam (approximately 4 mm wide) is incident on the surface at an incidence angle ϕ_i . Bragg reflection occurs and is described by the familiar Braggs' Law

$$2d_{hkl}\sin\theta_B = n\lambda\tag{1}$$

where

 d_{hkl} interplanar spacing;

 λ wavelength of the diffracted radiation;

 θ_B Bragg angle;

n integer.

Since this is a white beam experiment, the crystal, containing a variety of lattice planes at fixed spacings d_{hkl} , will reflect out particular wavelengths given by (1), assuming such reflections are not structure factor forbidden. This pattern of spots is recorded on the x-ray films and each spot itself is a topograph. Thus the user has simultaneous access to a variety of reflections on an individual recording film each corresponding to a set of diffracting planes, x-ray wavelengths and hence penetration depths. Since the divergence of the beam is small (e.g., 0.06 mrad full width at half maximum (FWHM) at HASYLAB), close inspection of these reveal details of the strain fields in the diffracting silicon.

Varying the wavelength of the diffracted radiation by varying the angle of incidence allows the user to alter the depth of penetration of the x-rays, thus producing a depth-resolved map of the strain fields in the packaged Si IC. In this study, various reflections were used in order to obtain a useful range of penetration depths.

III. THEORETICAL ANALYSIS

The kinematical approximation of x-ray diffraction is considered appropriate, and the effective penetration depth of the x-rays within the contributing volume is determined by this approach [33]. This kinematical penetration depth, t_p (measured perpendicular to the surface), at which the intensity of the outgoing reflected beam has dropped to e^{-1} that of the incident beam due to absorption is given by [33]

$$t_p = \frac{1}{\mu(\lambda) \left(\frac{1}{\sin \phi_i} + \frac{1}{\sin \phi_f}\right)}; \qquad \phi_i, \, \phi_f \gg \phi_C \quad (2)$$

where

 $\mu(\lambda)$ wavelength-dependent linear absorption coefficient;

 ϕ_i incidence angle;

 ϕ_f exit angle;

 ϕ_C critical angle of total reflection measured from the wafer surface.

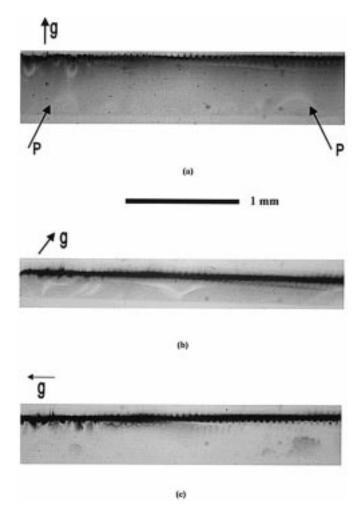


Fig. 3. BRST images for the same packaged IC a) 311 reflection [$t_p=242~\mu$ m], (b) 620 reflection [$t_p=27~\mu$ m], and (c) 822 reflection [$t_p=62~\mu$ m]. Diffraction vectors \vec{g} are shown. The top surface of the silicon is uppermost in these images.

Equation (2) is suitable for most cases but fails if ϕ_i , $\phi_f \leq \phi_C$.

Since a white beam is used in these experiments, the x-ray topographs typically consist of overlapping images formed by several harmonics. From the topographic films one records the integrated intensity (exposure), rather than the contributing harmonics. However, the relative intensities of the harmonics in each topograph can be calculated [27], [31], [33], [34]. The results of these calculations are shown in Table I for the 311, 620, and 822 reflections from the (100) surface of silicon used in this study.

The SXRT analysis was carried out on six 2764 8Kx8 EPROMs. The clear optical opening was removed by submersion of the package in a fuming sulphuric acid solution at a temperature of ~150 °C. Care was taken to ensure that the integrity of the package structure was maintained and that the metallization on the die was not attacked. An alternative method is to remove the encapsulation by mechanical means. This was also attempted, though it often resulted in mechanical damage, which could be observed in the topographs. Experience has taught us that chemical removal methods are preferable. This particular IC was chosen, as there is no moulding layer present on the chip surface. This is recognized as a drawback in the

Reflection Index	Wavelength	Grazing Angle	t _p
hkl	(nm)	(φ _i)	(µm)
620	0.059	4.5°	86
620	0.042	0.60	38

TABLE II GRAZING INCIDENCE DIFFRACTION TOPOGRAPHY X-RAY PENETRATION DEPTHS (t_p)

method currently, as x-rays impinging directly on packaging materials produce a high fluorescence background, which "washes out" any images obtained.

IV. RESULTS

Qualitative data on the strain fields are obtained as shown in the large area back reflection topographic maps of Fig. 2(a)–(c). An optical micrograph of the same region is shown in Fig. 2(d). Fig. 2(a) is a nominal 311 LA-BRT topograph of the IC with a nominal $t_p \approx 4.3 \ \mu \mathrm{m}$. However, while this reflection is nominally 311, the fundamental component of radiation ($\lambda = 0.296$ nm, see Table I) will be severely attenuated through the air on the way to the film. Hence it is assumed that the largest contribution to this image is from the two most significant harmonics, i.e., 933 and 12 4 4. For these two cases $t_p = 106$ μ m and 242 μ m, respectively. Any contribution smaller than 5% is considered insignificant and is not included in Table I. Note also that this image is blurred, possibly due to the relatively large intermixing of the 933 and 12 4 4 harmonics. The strain fields near the top surface are visible as the dense circuitry due to the strains imposed on this region by the circuit overlayers. Note also that there is a distinct variation in background contrast, varying from white (neighborhood of arrows A) to black (neighborhood of arrow B). This contrast is presumably due to the varying strain field within the entire Si substrate due to the packaging process, e.g., die adhesive nonuniformities, warpage of the die, etc. The penetration depth attributed to the 12 4 4 harmonic is large enough to visualise strain fields through to the backside of this wafer. In addition, one can also clearly discern the strain fields due to the bonding, as regions of enhanced contrast (black) directly under the wire bonds, e.g., see arrow C. For comparison an optical micrograph and a scanning acoustic microscopy (SAM) image of the same IC are shown in Fig. 2(d) and (e), respectively. The dotted box in Fig. 2(e) indicates the region imaged using SXRT. The white areas are voided areas of die attach and account for approximately 20% of the overall die area. Within the region examined by SXRT strain fields due to this voiding and other strain contributions are easily seen, yet the resolution is ca. two orders of magnitude better than in the SAM image.

In Fig. 2(b) $t_p = 27 \mu \text{m}$ for this 620 LA-BRT, and all harmonic contributions are well below 5%. In this case a smaller volume of silicon is contributing to the image and we can now examine the presence of strain fields to a much smaller depth. The circuitry strain fields are easily seen and so also are the bonding strain fields. However, the longer-range strain field

variation appears to be absent from this topograph. A careful inspection of the $\{620\}$ family of topographs revealed this to be the case in all their occurrences. Therefore it appears that these longer-range strain fields are either below the threshold of resolution ($\epsilon \geq 6 \times 10^{-5}$ for the F-1 topography beamline at HASYLAB since the beam divergence is ≈ 0.06 mrad) at depths approaching 27 μ m, or indeed are at depths within the crystal of $>\!27$ μ m. The latter is the most probable situation, as the most likely source of strain nonuniformity is at the back side of the silicon at the die-adhesive interface.

Fig. 2(c) is an 822 LA-BRT for the same sample wherein $t_p=62~\mu\mathrm{m}$. The circuit and bonding strain fields are still visible. However, there is now strong contrast from a slowly varying strain field similar in nature to those of Fig. 2(a). In this case the contrast is stronger and the respective positions of the white and black regions are altered (see, e.g., Arrows A and B), since this image is more sensitive to strain variations at angles \approx 14° away from the 620 direction (i.e., 822). Once again it is probable that the slowly varying black-and-white contrast of Fig. 2(c) is due to strains which exist at depths between 27 μ m and 62 μ m, since this phenomenon was not observed for the 620 reflection and is most likely obscured by the strain fields on the back side of the wafer in the 311 LA-BRT.

Three BRSTs are shown in Fig. 3(a)–(c). These are the BRST images for the 311 ($t_p = 242~\mu\mathrm{m}$), 620 ($t_p = 27~\mu\mathrm{m}$) and 822 ($t_p = 62 \mu \text{m}$) reflections, respectively. The 311 BRST of Fig. 3(a) exhibits reasonably uniform resolution of details throughout the entire depth of the wafer. This is to be expected since the 12 4 4 harmonic contributes significantly for t_p up to 242 μ m, which is approximately equal to the sample thickness $(\approx 250 \ \mu \text{m})$. Circuit strain imparted to the underlying Si is seen on the upper surface. Note also that there are looped strain structures emanating from the backside of the wafer, which are presumably due to backside adhesion problems (Arrows P). Much less detail is seen in the 620 BRST of Fig. 3(b), since the penetration depth is much smaller (27 μ m) and this upper region is overexposed. Note also that one can still see strain images throughout the entire depth of the sample. This apparent contradiction is easily explained. The kinematical penetration depth is defined as the depth at which the intensity of the reflected beam has dropped to e^{-1} that of the incident beam due to absorption [33], [34]. The 12 4 0 harmonic represents a significant contribution of overall intensity (7.3%, Table I) because the upper region is overexposed, and has an attributed $t_p = 201$ μ m. This harmonic will contribute to imaging deeper layers of the sample and this is readily apparent on this image. However, for the 822 BRST of Fig. 3(c) only the fundamental component contributes and $t_p=62~\mu\mathrm{m}$. Thus, the majority of x-ray energy is deposited in this \approx 60–100 μ m upper region and excellent detail of the strain fields due to the overlying circuitry is visible. In this case, the backside of the wafer is barely visible, since no other harmonic contributes significantly and little of the x-ray energy reaches that region. It is worth noting that the BRSTs of Fig. 3(a)–(c) are similar to the transmission section topographs of similar silicon wafers with integrated circuits reported in [35]. In [35] the strain field contrast was compared with the calculated map of radial strain field near and below an oxide edge. The topographic image can be explained qualitatively with the

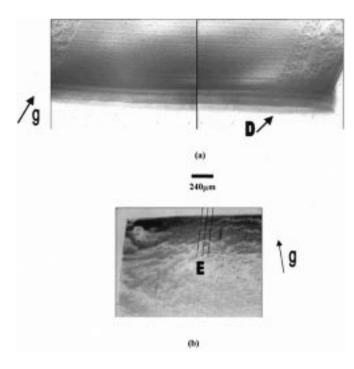


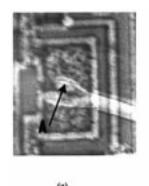
Fig. 4. GIDT images for various incidence angles: (a) $\phi_i=4.5^\circ$ [$t_p=86~\mu$ m] and (b) $\phi_i=0.6^\circ$ [$t_p=38~\mu$ m]. Diffraction vectors \vec{g} are shown.

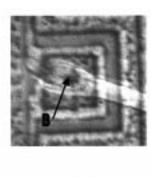
aid of an orientational contrast resulting from misorientated lattice planes.

GIDT topography was also carried out on these samples and penetration depths are given in Table II. The incidence angle was relatively large (0.6° and 4.5°) in order to avoid hitting the lip on the package and thus provide incident x-rays on the silicon itself. Typical topographs are shown in Fig. 4(a)–(b). One of the sources of observed strain is revealed in Fig. 4(a). The geometry allows one to see the front edge of the chip in addition to surface circuitry and bond strains. A slowly varying strain field is also seen and the contrast is particularly strong close to arrow D. There is a local warpage of the chip at this location. This straightforward correlation between die warpage and strain fields is only possible using SXRT.

In the low angle GIDT ($\phi_i=0.6^\circ$) of Fig. 4(b) the strain fields due to the adhesive, circuitry and bonding have almost disappeared (though some circuit detail is still present, parallel to lines E), leaving a mottled diffraction image. One thing is clear—only the silicon can diffract the x-rays and the image is still visible, implying that the x-rays have accessed the near surface region. However, it is possible that severe scattering in the protective oxide layer on the chip surface is dispersing the low angle incident and diffracted photons. Since Bragg reflections are observed it is also clear that total external reflection has not occurred at the dielectric protection (e.g., the critical angle for 13 keV x-rays on SiO₂ is $\phi_C \approx 0.2^\circ$, and for this experiment $\phi_i > 0.2^\circ$!). The ensuing image reveals that there are many strain inhomogeneities in the dielectric cap, though a more precise interpretation of the image is difficult.

Fig. 5(a) and (b) show two 620 BRTs, where particular attention is paid to the strain fields directly under two wedge bonds. These are enlargements of Fig. 2(b). The strain fields under these bonds differ dramatically from each other (see ar-





(b)

Fig. 5. 620 LA-BRT images [$t_p=27~\mu\mathrm{m}$]—strain fields under two wedge bonds (a) and (b). Enlargement of the bonds seen in Fig. 2(b).

rows A and B). The strain field in the Si under the bond pad, indicated by arrow A, runs in a line along the wedge bond. However, the strain field, indicated by arrow B, is spherically distributed under the bond. The strain fields due to the wedge bonding result in a localized enhancement of x-ray intensity directly under the metal bonds and thus are not attributable to stresses arising from the curing of the die attach materials or other process-induced stresses. Note also the defect generation in the silicon directly under the bonding pads themselves.

V. CONCLUSION

Synchrotron x-ray Topography is an extremely adaptable quality evaluation tool for semiconductor IC process development. In this study, SXRT has been used in large area and section back reflection and grazing incidence modes to provide depth-resolved diffraction images of strain fields in simple packaged integrated circuits. Details including backside adhesive strain, bonding strain, circuit overlayer strain and dielectric cap strain fields have been observed. Many problems remain and these include improved incidence angle control, a reduction of fluorescence background radiation due to the package moulding compounds, and a comparison with device performance and yield. The possibility of using these techniques as process evaluation tools has been established, and in the future could be used as a comparative tool or screening technique. It is reasonable to assume, however, that fabrication facilities will not be in a position to establish synchrotron sources to provide such screening, and as such, SXRT is more suited to process research and development.

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REFERENCES

- [1] I. Anjoh, A. Nishimura, and S. Eguchi, "Advanced IC packaging for the future applications," *IEEE Trans. Electron Devices*, vol. 45, pp. 743–752, Mar. 1998.
- [2] O. Slattery, T. Hayes, W. Lawton, G. Kelly, C. Lydon, and C. O'Mathuna, "Methods of analyzing thermomechanical stress in plastic ICs," *J. Mat. Proc. Technol.*, vol. 54, no. 1–4, pp. 199–204, 1995.
- [3] M. Amagai and E. Kawasaki, "Chip surface damage induced by internal stress of lead-on-chip (LOC) packages," in *Proc. Mat. Res. Soc. Symp.*, vol. 338, 1994, pp. 185–193.

- [4] L. T. Nguyen, S. R. Gee, M. R. Johnson, H. E. Grimm, H. Berardi, and R. L. Walberg, "Effects of die coatings, mold compounds, and test conditions on temperature cycling failures," *IEEE Trans. Comp., Packag. Manufact. Technol. A*, vol. 18, pp. 15–22, Mar. 1995.
- [5] D. A. Leonhardt, "Ultrafine pitch gold ball bonding," Semicond. Int., vol. 19, no. 5, pp. 311–318, 1996.
- [6] R. Pantaleon, J. Sanchez-Mendoza, and M. Mena, "Rationalization of gold ball bond shear strengths," in *Proc. Electron. Comp. Technol. Conf.*, Washington, DC, May 1–4, 1994, pp. 733–740.
- [7] S. K. Groothuis and K. G. Heinen, "Mold compounds: Linking materials science and IC package reliability," in *Proc. Mat. Res. Soc. Symp.*, vol. 390, 1995, pp. 77–88.
- [8] H. Ali, "Stress-induced parametric shift in plastic packaged devies," IEEE Trans. Comp., Packag., Manufact. Technol. B, vol. 20, pp. 458–462, Nov. 1997.
- [9] S. Liu and Y. Mei, "Behavior of delaminated plastic IC packages subject to encapsulation cooling, moisture absorption and wave soldering," *IEEE Trans. Comp., Packag., Manufact. Technol. A*, vol. 18, pp. 634–645, Sept. 1995.
- [10] Z. Qian and C. P. Yeh, "Preliminary in process stress analysis of flip chip assemblies during thermal cycling," in *Proc. Thermo-Mech. Characterization Evolving Packag. Mater. Structures*, 1998 ASME Int. Mech. Eng. Congr. Expo. New York, NY, Nov. 15–20, 1998, pp. 101–106.
- [11] J. Songliang, Z. Haoying, and L. Yanbin, "Study and application of piezoresistive stress test chip for IC packages," *Chinese J. Semiconduc*tors, vol. 19, no. 11, pp. 811–817, 1998.
- [12] J. C. Suhling, R. C. Jaeger, S. T. Lin, R. J. Moral, Y. Zou, E. Suhir, M. Shiratori, Y.C. Lee, and G. Subbarayan, "Advances in electronic packaging," in *Proc. Pacific Rim/ASME Int. Intersoc. Electron. Photon. Packag. Conf. INTERPack'97*, vol. 2, Kohala Coast, HI, June 15–19, 1997, pp. 1741–1750.
- [13] R. C. Jaeger, J. C. Suhling, K. M. Liechti, and S. Liu, "Advances in stress test chips," in *Proc. Applicat. Experimental Mech. Electron. Packag.* '97, ASME Int. Mech. Eng. Congr. Expo., Dallas, TX, Nov. 16–21, 1997, pp. 1–5
- [14] H. C. J. M. Vangestel, A. Bossche, and J. R. Mollinger, "On-chip piezoresistive stress measurement in 3 directions," *Sens. Actuators A*, vol. 27, no. 1–3, pp. 801–807, 1991.
- [15] H. Miura, M. Kitano, A. Nishimura, and S. Kawai, "Thermal stress measurements in silicon chips encapsulated in IC plastic packages under temperature cycling," in *Proc. 1992 Joint ASME/JSME Conf. Electron. Packag.* Milpitas, CA, Apr. 9–12, 1992, vol. 2, pp. 957–963.
- [16] P. Yalamanchili, A. Christou, S. Martell, and C. Rust, "C-SAM sounds the warning for IC packaging defects," *IEEE Circuits Devices Mag.*, vol. 10, pp. 36–41, Apr. 1994.
- [17] R. Tilgner, P. Alpern, J. Baumann, G. Pfannschnidt, and O. Selig, "Changing states of delamination between molding compound and chip surface: A challenge for scanning acoustic microscopy," *IEEE Trans. Comp., Packag., Manufact. Technol. B*, vol. 17, pp. 442–448, Aug. 1994.
- [18] J. Wang, W. Ren, D. Zou, and S. Lin, "Effect of cleaning and noncleaning situations on the reliability of flip-chip packages," *IEEE Trans. Comp.*, *Packag., Manufact. Technol.*, vol. 22, pp. 221–228, June 1999.
- [19] D. Zou, M. Lu, L. Shi, J. Wang, S. Liu, and Y. Guo, "Moiré interferometer, an effective tool in electronic packaging, concept and applications," *Int. J. Microcirc. Electron. Packag.*, vol. 22, no. 3, pp. 212–220, 1999.
- [20] A. S. Voloshin, P. H. Tsao, and R. A. Pearson, "In situ evaluation of residual stresses in an organic die-attach adhesive," J. Electron. Packag., vol. 120, no. 3, pp. 314–318, 1998.
- [21] S. Liu, J. Zhu, D. Zou, and J. Benson, "Study of delaminated plastic packages by high temperature Moiré and finite element method," *IEEE Trans. Comp., Packag., Manufact. Technol. A*, vol. 20, pp. 505–512, Dec. 1007
- [22] B. Han, Y. Guo, C. K. Lim, and D. Calekta, "Verification of numerical models used in microelectronics packaging design by interferometric displacement measurement methods," *J. Electron. Packag.*, vol. 118, no. 3, pp. 157–163, 1996.
- [23] H. J. Peng, S. P. Wong, W. F. Lau, N. Ke, and S. Zhao, "Measurement of bonding stress in silicon high power device structures by infrared photoelasticity method," in *Proc. Mat. Rel. Microelectron. IX Symp.*, Apr. 6–8, 1999, pp. 303–308.
- [24] T. Y. Chen and C. H. Lin, "Whole-field digital measurement of principal stress directions in photoelasticity," *Opt. Lasers Eng.*, vol. 30, pp. 527–537, 1998.
- [25] K. Ramesh and S. K. Mangal, "Data acquisition techniques in digital photoelasticity: A review," Opt. Lasers Eng., vol. 30, pp. 53–75, 1998.

- [26] H. J. Peng and S. N. Zhao, "Infrared photoelastic research of sintering stress in silicon thyristor," *J. Inf. Millim. Waves*, vol. 17, no. 1, pp. 42–47, 1998
- [27] T. Tuomi, K. Naukkarinen, and P. Rabe, "Use of synchrotron radiation in x-ray diffraction topography," *Phys. Stat. Sol.* (A), vol. 25, pp. 93–106, 1974.
- [28] D. K. Bowen and B. K. Tanner, High Resolution X-Ray Diffractometry and Topography. London, U.K.: Taylor & Francis, 1998.
- [29] M. Sauvage-Simkin, "X-ray topography and related techniques using synchrotron radiation," in *Synchrotron Radiation Research*, H. Winick and S. Doniach, Eds. New York: Plenum, 1982, pp. 179–204.
- [30] D. V. Novikov, M. Ohler, R. Köhler, and G. Materlik, "Observation of defects in crystal surface layers by grazing-incidence diffraction x-ray topography." J. Phys. D: Applicat. Phys., vol. 28, pp. A84–A87, 1995.
- topography," *J. Phys D: Applicat. Phys.*, vol. 28, pp. A84–A87, 1995. [31] M. Hart, "Synchrotron radiation—Its application to high-speed, high-resolution x-ray diffraction topography," *J. Appl. Cryst.*, vol. 8, pp. 436–444, 1975.
- [32] K. Wieteska, W. Wierzchowski, and W. Graeff, "Interference effects in Bragg-case synchrotron section topography of elastically bent crystals," *Il Nuovo Cimento D*, vol. 19D, no. 2–4, pp. 227–232, 1997.
- [33] G. D. Yao, M. Dudley, and J. Wu, "Synchrotron white beam topographic imaging in grazing Bragg-Laue geometries," *J. X-Ray Sci. Technol.*, vol. 2, pp. 195–213, 1990.
- [34] R. Rantamäki, T. Tuomi, P. J. McNally, J. Curley, and A. Danilewsky, "Grazing incidence synchrotron x-ray topography as a tool for denuded zone studies of silicon wafers," *J. X-Ray Sci. Technol.*, vol. 8, pp. 159–169, 1998.
- [35] M. Karilahti, T. Tuomi, M. Taskinen, J. Tulkki, H. Lipsanen, and P. McNally, "Synchrotron x-ray topographic study of strain in silicon wafers with integrated circuits," *Il Nuovo Cimento*, vol. 19D, no. 2–4, pp. 181–184, 1997.

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