A Simple One-Dimensional Model for the Explanation and Analysis of GaAs MESFET Behavior

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Abstract—The explanation of GaAs metal–semiconductor field-effect transistor (MESFET) operation often involves the use of simplistic analytical formulas, which serve to obscure the more subtle physics of device action. We consider here a simple one-dimensional (1-D) model for GaAs MESFET's, which avoids more confusing numerical modeling schemes, yet still facilitates an analysis of the physical functionality of the device. The model takes into account current saturation due to either velocity saturation or channel pinch-off, the modulation of effective gate length, and the series resistance of the regions beyond the gate. The results of the model have been compared to experimental data readily obtained from the literature, and the agreement has been shown to be good.

Index Terms—Gallium arsenide (GaAs) modeling, I–V characteristics, metal–semiconductor field-effect transistor (MESFET).

I. INTRODUCTION

A COMMON approach to one-dimensionl (1-D) metal–semiconductor field-effect transistor (MESFET) modeling is to use device technological parameters to define some characteristic values as a function of the gate-to-source voltage and to include it in an empirical expression which describes the drain current over the entire range of applied voltages [1]–[5]. In the model presented here, we have reduced the reliance on empirical fitting schemes, and appealed to a physical model to account for device modeling. The drain current is calculated in the linear region by taking into account the dependence of the effective gate length on the applied gate-to-source voltages once the saturation velocity has been reached at the drain side of the channel. The saturation region is modeled through a calculation of the voltage drop across this region. This approach allows one to evaluate the drain current after velocity saturation has been reached and before pinch-off of the channel has come into force. After pinch-off, the current is approximated by the current that has the same slope with respect to the drain-to-source voltage as the last current value calculated before pinch-off.

II. THE 1-D MODEL

The model is based on the gradual channel approximation [6], which states that the thickness of the depletion region

at every point y along the gate may be found by using conventional 1-D equations for the Schottky barrier. This approximation is valid when the derivative of the electric field with respect to the coordinate along the channel is much smaller than the derivative of the electric field in the depletion region with respect to the coordinate perpendicular to the channel. We also assume that the conducting channel is neutral and that the space-charge region between the gate and the channel is totally depleted. The boundary between the channel and the depletion region is assumed to be sharp (in fact, the transition region width is of the order of three Debye lengths [1]). For simplicity, we consider uniform n-type doping in the channel.

The electron drift velocity is modeled by

$$v(y) = \frac{\mu_o E(y)}{1 + \dfrac{E(y)}{E_S}} \tag{1}$$

where μ_o is the low-field electron mobility, when the electric field $E(y)$ along the channel is smaller than the saturation electric field E_s. This represents one of the few empirical approaches in the analysis, as full access to such data requires the use of techniques such as Monte Carlo simulation [7].

The model can be made even more sophisticated by including the effects of impurity concentration on electron drift velocity. The model used here is outlined in [8] and is given by

$$\mu_o = \mu_{\min, n} + \frac{\mu_{\max, n}(T/300)^{-\beta_n}}{[1 + (N_a + N_d)/N_{ref, n}]^{\alpha_n}}. \tag{1'}$$

Typical values are given by $\mu_{\min, n} = 1500$ cm^2/V·s, $\mu_{\max, n} = 6400$ cm^2/V·s, $T = $ temperature in Kelvins $= 300$ K, $\beta_n = 1$, $N_{ref, n} = 1.426 \times 10^{17}$ cm^{-3}, $\alpha_n = 0.5385$, $N_{d(a)} = $ donor (acceptor) concentration in cm^{-3}. This extra level of complication (empirical in nature) is typically omitted initially, and is considered to be a second-order effect. The student can refine his/her initial model through incorporation of (1') in later exercises. For the purposes of the following discussion it will also be omitted.

The drift velocity saturates at $E(y) = E_s$ and is given by
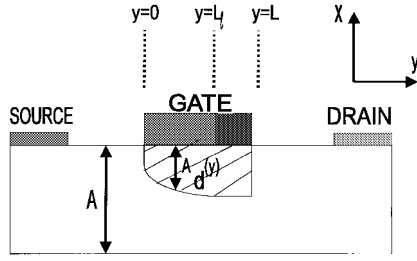
$$v_{\text{sat}} = \frac{\mu_o E_S}{2}. \tag{2}$$

Fig. 1. A schematic representation of the GaAs MESFET structure used in this study. The coordinate system and relevant device dimensions are shown.

III. LINEAR MODE OPERATION

In the case where the longitudinal electric field everywhere in the channel is smaller than the velocity saturation field E_s, the drain-to-source current along the channel is given by

$$I_D(y) = qN_dW[A - A_d(y)]v(y) \qquad (3)$$

where q is the electron charge, N_d is the donor concentration in the channel, W is the gate width, A is the full channel thickness, and $v(y)$ is the drift velocity at position y. This is analogous to the statement that $I_D(y) = WQ_n v$, where $Q_n = $ total mobile charge and v is the velocity of mobile charge; or, in other words, current density $j(y) = qn_n v$, where n_n is the total mobile charge density. The depletion-layer thickness $A_d(y)$ under the Schottky gate can be found from the solution of Poisson's equation [6] and it is equal to

$$A_d(y) = A\left(\frac{V_{bi} - V_G + V(y)}{V_{po}}\right)^{1/2} \qquad (4)$$

where V_{bi} is the built-in voltage of the Schottky barrier, V_G is the gate voltage, and $V(y)$ is the potential along the channel. The pinch-off voltage V_{po} is given by

$$V_{po} = \frac{qN_dA^2}{2\varepsilon} \qquad (5)$$

where ε is the dielectric constant of GaAs. A schematic representation of the MESFET is given in Fig. 1, where the coordinate system and relevant device dimensions are shown.

Substituting (1) and (4) into (3) we obtain

$$I_D(y) = qN_dWA\left[1 - \left(\frac{V_{bi} - V_G + V(y)}{V_{po}}\right)^{1/2}\right]\frac{\mu_o E(y)}{1 + \frac{E(y)}{E_S}}. \qquad (6)$$

Keeping in mind that $|E(y)| = |dV/dy|$ and that the current is constant along the channel, we integrate (6) from the source side of the gate $(y = 0)$ to the drain side of the gate $(y = L)$.

After some rearrangement we obtain

$$I_D = \frac{qN_dWA\mu_o}{L}$$
$$\cdot \frac{V_D - \frac{2}{3V_{po}^{1/2}}[(V_{bi} - V_G + V)^{3/2} - (V_{bi} - V_G)^{3/2}]}{1 + \frac{V_D}{E_S L}} \qquad (7)$$

where we assume that the potential at the source side of the gate $V(0) = 0$. The potential at the drain side of the gate $V(L)$ is equal to the drain voltage V_D.

As (6) is valid everywhere in the channel, we can evaluate it at $y = L$ to give

$$I_D = qN_dWA\left[1 - \left(\frac{V_{bi} - V_G + V_D}{V_{po}}\right)^{1/2}\right]\frac{\mu_o E(L)}{1 + \frac{E(L)}{E_S}}. \qquad (8)$$

Eliminating I_D from (7) and (8) we can find the electric field $E(L)$ for the given voltages V_G and V_D in a closed form. In this way, we can simply check whether the MESFET still operates in the linear mode, i.e., whether $E(L)$ is smaller than E_s. If $E(L) < E_s$, the current can be calculated either from (7) or (8).

IV. SATURATION-MODE OPERATION

After the electric field at the drain side of the gate has reached E_s, any further increase of the drain voltage causes the point at which velocity saturation occurs to move toward the source side of the gate. Let us define this point as $y = L_\ell = L - L_s$, where L_s is the width of the saturation region. Equation (6) is still valid in the linear region under the gate $(y = 0$ to $y = L_\ell)$. Integrating this equation from $y = 0$ to $y = L_\ell$ we obtain (9) (shown at the bottom of this page), and evaluating (6) at $y = L_\ell$ we obtain

$$I_D = qN_dWA\left[1 - \left(\frac{V_{bi} - V_G + V_{D,\ell}}{V_{po}}\right)^{1/2}\right]\frac{\mu_o E_S}{2} \qquad (10)$$

where $V_{D,\ell}$ represents the voltage drop across the linear region, which is related to the applied drain voltage through

$$V_D = V_{D,\ell} + \Delta V \qquad (11)$$

and ΔV is the voltage drop across the saturation region $(y = L_\ell$ to $y = L)$.

$$I_D = \frac{qN_dWA\mu_o}{L - L_S} \cdot \frac{\left(V_{D,\ell} - \frac{2}{3V_{po}^{1/2}}\right)[(V_{bi} - V_G + V_{D,\ell})^{3/2} - (V_{bi} - V_G)^{3/2}]}{1 + \frac{V_{D,\ell}}{E_S(L - L_S)}} \qquad (9)$$

The relationship between the saturation region L_s, and the voltage ΔV has been examined elsewhere—the examination of this would in itself be a useful class assignment—and is given by [9]

$$\Delta V = \frac{2AE_S}{\pi} \sinh\left(\frac{\pi}{2} \cdot \frac{L_S}{A}\right). \tag{12}$$

Eliminating I_D from (9) and (10), and substituting (11) and (12) into the resulting equation, we can find L_s or ΔV. There is no closed-form solution for L_s. After ΔV and L_s are found iteratively, either (9) or (10) may be used to obtain the current in saturation.

The influence of the resistance R_s of the region from the source contact to the source side of the gate, and the resistance R_d of the drain region outside the gate is included through

$$V_{GS} = V_G + I_D R_S \tag{13}$$
$$V_{DS} = V_D + I_D(R_S + R_d) \tag{14}$$

where V_{GS} and V_{DS} represent the gate-to-source and drain-to-source voltages, respectively. It is obviously necessary to implement an iterative technique to obtain currents for given values of V_{GS} and V_{DS}.

V. DIGRESSION

The gate V_G should be smaller than the built-in voltage V_{bi} of the Schottky barrier. Otherwise, the gate current becomes substantial and the I_D–V_{DS} characteristics collapse. The current in the linear mode will be positive if

$$V_G - V_{th} > V_D$$

where $V_{th} = V_{bi} - V_{po}$ is the threshold voltage. If $V_G - V_{th} = V_D$, the depletion layer width is equal to the full channel height A and the channel is pinched off. At the onset of pinch-off of the channel, according to the gradual channel approximation, the current saturates and remains constant even if the drain voltage increases. This also means that the output resistance, $\partial V_{DS}/\partial I_D$, reaches infinity above pinch-off.

Because of the low-saturation electric field E_s, the current for a GaAs MESFET, whose gate length $L_G \approx 1$ μm for example, saturates initially due to velocity saturation. If the drain voltage increases above this point, the pinch-off mechanism comes into force. The use of the constant current approximation after pinch-off does not appear to be the best choice. We suggest approximating the current above pinch-off with the current which possesses the same slope with respect to V_{DS} as the last current value calculated prior to pinch-off.

Finally, it has been assumed that no electrons penetrate the substrate. This is, in fact, an effect which is certainly known to be pronounced at higher fields unless some precautions (e.g., a heterostructure buffer layer or buried p-layer) have been undertaken. An increase of the drain current in the saturation region is partially attributed to this effect [10].

TABLE I
THE DEVICE PARAMETERS USED IN [11]

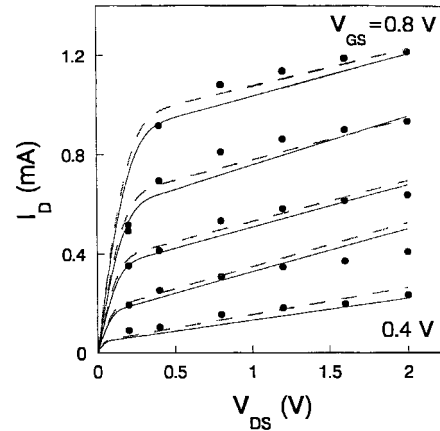|	
Doping concentration, N_d	7.24×10^{16} cm^{-3}
Gate length, L_G	0.7μm
Gate height, A	0.1μm
Gate width, W	20μm
Low-field mobility, μ_o	2500 cm^2/Vs
Saturation velocity, v_{sat}	1.3×10^7 cm/s
Schottky barrier height, V_{bi}	0.72V
Source resistance, R_s	50Ω
Drain Resistance, R_d	50Ω

Fig. 2. The results of the model for $V_{bi} = 0.81$ V and different values of μ_o (solid line: $\mu_o = 4000$ cm^2/V $\cdot$ s, dashed line: $\mu_o = 4500$ cm^2/V $\cdot$ s, circles: experimental data). Other parameters as per Table I.

VI. RESULTS

The results of the model have been compared to experimental data which are readily accessible to students in the literature. As an example, a comparison is made with [11]. The device parameters used therein are outlined in Table I.

The value of $V_{bi} = 0.72$ V does not allow calculation of the current for $V_{GS} = 0.8$ V, because V_{GS} should be smaller than the Schottky-barrier height. Thus in the following calculations we used $V_{bi} = 0.81$ V, in accordance with experimentally determined values of V_{bi}, which are usually in the region 0.8–0.9 V for n-type GaAs due to Fermi-level pinning [12]. Furthermore, we tested different values of μ_o because $\mu_o = 2500$ cm^2/V $\cdot$ s is a fairly low estimation when compared to the long-sample low-field mobility (7500 cm^2/V $\cdot$ s at $T = 300$ K). We used $\mu_o = 4000$ cm^2/V $\cdot$ s and $\mu_o = 4500$ cm^2/V $\cdot$ s (see Fig. 2). As mentioned in [11], the nominal gate length was actually 1 μm. Thus we tried the following parameters: $L_G = 1$ μm, $V_{bi} = 0.81$ V, $\mu_o = 7500$ cm^2/V $\cdot$ s (see Fig. 3). We also compared the model with experimental data given in [2]. The device parameters used in this reference are shown in Table II. The experimental
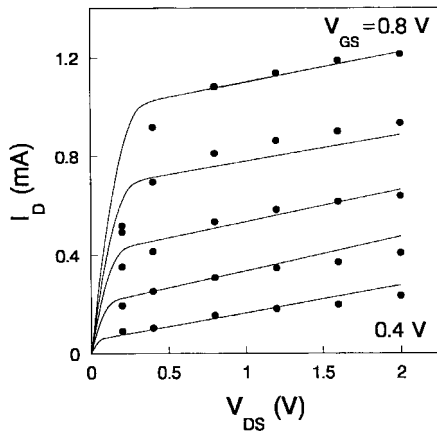
Fig. 3. The results of the model for $L_G = 1~\mu$m, $V_{bi} = 0.81$ V, and $\mu_o = 7500$ cm^2/V $\cdot$ s (solid line: model, circles: experiment). Other parameters as per Table I.

TABLE II
THE DEVICE PARAMETERS USED IN [2] *

Doping concentration, N_d	6.5×10^{16} cm^{-3}
Gate length, L_G	1μm
Gate height, A	0.34μm
Gate width, W	500μm
Low-field mobility, μ_o	4500 cm^2/Vs
Saturation velocity, v_{sat}	1.2×10^7 cm/s
Schotthy barrier height, V_{bi}	0.75V
Source resistance, R_s	6.5Ω
Drain Resistance, R_d	11.3Ω

* The channel thickness A has been determined from a pinch-off voltage $V_{po} = 5.3$ V.
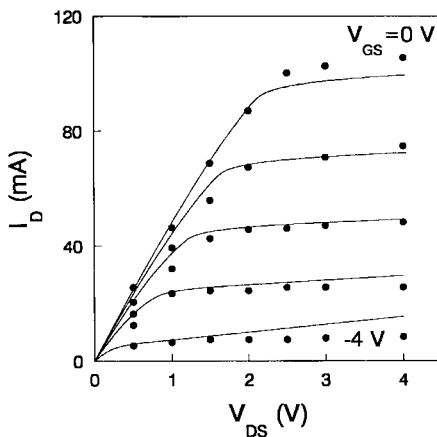

Fig. 4. Comparison of experimental data with the model for device parameters given in Table II (solid line: model, circles: experiment).

data and the results of our model are good, and are shown in Fig. 4. However, it can be seen that the current saturates slightly more smoothly than predicted by the model.

The agreement with experiment is very reasonable, given the gross simplifications concomitant with 1-D modeling. Although the model is probably not useful for devices with $L_G < 1~\mu$m, it still serves as a useful learning and pedagogical exercise for the student. Indeed, the shortcomings of this model are used as a springboard for further investigation of submicrometer L_G modeling, including the efficacy of numerical modeling, short-channel effects, etc. It should also be noted that complete MESFET models are given in PSpice®, are described in [12] and [13], and can also be used for comparison with the physical model developed here.

VII. CONCLUSION

We have described a new 1-D physical model to allow advanced students gain an insight into the more subtle aspects of GaAs MESFET behavior. The model takes into account current saturation due to either velocity saturation or channel pinch-off, the modulation of the effective gate length for operation in the linear region, and the series resistance of the regions beyond the gate. The results of the model have been compared to available experimental data, and agreement has been shown to be good for devices with $L_G \to 1~\mu$m. One of the major advantages of this model is that confusing numerical schemes in the calculation of I–V characteristics have been avoided. A further exercise could engage the student in observing/explaining the eventual breakdown of the model for submicrometer L_G devices. This can be used as a motivation for the necessity of performing intensive two- and three-dimensional modeling for such devices.

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