Analysis of the impact of dislocation distribution on the breakdown voltage of GaAs-based power varactor diodes

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A synchrotron x-ray topography analysis of the impact of the distribution of defects/dislocations on the electrical performance of GaAs power varactor diodes was carried out. Diodes fabricated on or near Liquid Encapsulated Czochralski cellular dislocation networks in the substrate, which are also known to be rich in As precipitates near these cell walls, were observed to have reduced breakdown voltages (V_{BR}). This is consistent with the possibility that the presence of space-charge cylinders surrounding these dislocations gives rise to reduced V_{BR} if they thread a p-n junction; it is also in accord with the possibility that the As precipitates themselves can act as sites for local field enhancement, thus promoting premature avalanche breakdown. © *1996 American Institute of Physics.* [S0021-8979(96)08411-3]

I. INTRODUCTION

GaAs power varactor diodes are utilized in advanced ultrahigh frequency circuitry. In typical usage, arrays or stacks of such diodes are arranged to be biased by modest dc voltages and to be in series rf-wise in order to handle high rf powers and peak voltages. It is therefore crucial to ensure a uniform operating breakdown voltage (V_{BR}) for these devices. A typical figure for V_{BR} would be of the order of many tens of volts, e.g., 40 V. However, a common problem is that many diodes fabricated in such a stack do not meet the required breakdown specifications.

It is well known that the presence of dislocations in semiconductor devices has a deleterious impact on their performance, yield and reliability. Recent studies have shown that these effects manifest themselves in differing guises for a wide variety of devices, e.g., dislocations can reduce the current gain in AlGaAs/GaAs heterojunction bipolor transistors (HBTs),[1] and heteroepitaxial solar cells have low efficiencies due to misfit and thermally induced dislocations acting as recombination centers.[2–4]

This article reports on the use of synchrotron x-ray topography (SXRT) to analyze the defect/dislocation distributions within wafer substrates and their correlation with substandard performance of GaAs power varactor diodes.

II. EXPERIMENT

X-ray topography (XRT) is a nondestructive technique which can provide a map of the defect distribution in crystals.[5–10] The technique is based on the difference in reflecting power between perfect and distorted parts of a crystal. It is sensitive to strain fields extending over more than several micrometers and therefore XRT is mainly used for the study of dislocations, planar defects, stacking faults, domain walls in ferroelectric and magnetic materials, growth defects or large precipitates.

Two main experimental setups were used:

(a) *Large Area Topography*

This is a common technique, described in Refs. 6 and 10, and provides for an improvement over Lang topography[7] in that the traversal stage can be eliminated. When a single crystal is immersed in a white x-ray beam a number of lattice planes (hkl) select out of the continuous spectrum the proper wavelengths to be reflected according to Bragg's law

$$2d_{hkl}\cdot\sin\,\theta_B = n\lambda, \tag{1}$$

where d_{hkl} is the interplanar spacing of (hkl) lattice planes, θ_B is the Bragg angle, and n is an integer. A beam diffracted in a direction $2\theta_B$ with respect to the incident beam has a spectrum of wavelengths λ, $\lambda/2$, $\lambda/3$, etc, corresponding to diffraction lattice planes (hkl), ($2h2k2l$), ($3h3k3l$), etc. The fundamental reflection hkl or its harmonics may, however, be structure factor forbidden. This is the well-known Laue method. However, due to the low divergence of the synchrotron radiation beam, each spot of this particular Laue pattern is itself a high-resolution topograph.[6]

(b) *Section Topography*

An arrangement similar to that for large area topography is used, only in this case the incoming beam is collimated into a narrow ribbon by a slit typically 10–15 μm in width. A set of Laue case section topograph images of sample cross sections are produced as previously described and, provided that the Bragg angle is not too small, the image gives detailed information about the energy flow within the crystal and direct depth information on the defects present in a particular crystal slice.[10]

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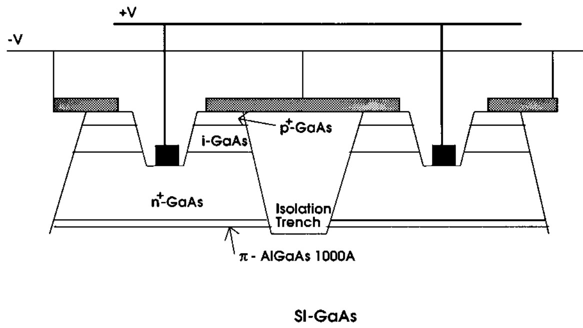


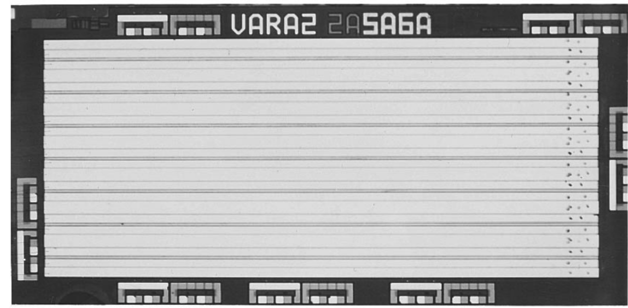
FIG. 1. Structure of varactor power diodes used in this study. The n^+-GaAs layer is 2.5 μm thick with $n=5\times10^{18}$ cm^{-3}, the nominally i-GaAs layer is 2.5 μm thick and $n=10^{16}$ cm^{-3}. The p^+-GaAs layer is 0.15 μm thick with $p=5\times10^{18}$ cm^{-3}.

The measurements were performed at HASYLAB-DESY, Hamburg, Germany (Hamburger Synchrotronstrahlungslabor am Deutschen Elektronen-Synchrotron), utilizing the continuous spectrum of synchrotron radiation from the DORIS storage ring bending magnet. The ring operated at a positron energy of 4.45 GeV and at typical currents of 50–100 mA. The aforementioned Laue pattern of topographs was recorded either on a Kodak type R or on a Kodak high-resolution professional x-ray film having an emulsion grain size of about 0.05 μm. Both the section and large area modes were employed in producing the topographs. In section topography, the beam was limited by a horizontal slit having a width of 15 μm. The surface of the wafer made an angle of 63.5° with the beam. In large area topography, the beam was limited by a rectangular slit of ~4 mm×4 mm and the wafer surface was set perpendicular to the beam. This relatively small area also eliminated unwanted fluorescence from the GaAs when excited by the beam. As noted earlier, both methods used transmission geometry, i.e., the diffracted beam passed through the wafer.

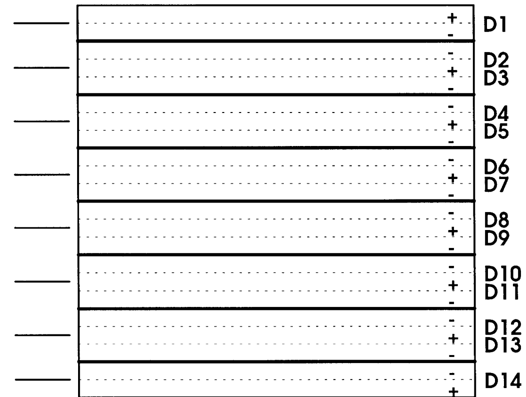
III. RESULTS AND DISCUSSION

The structure of the diodes examined is shown in Fig. 1. The dimensions of each diode were 6300 μm×100 μm and each chip consisted of a stack of 14 of these p-i-n varactor diodes. The nominal wafer thickness was 600 μm, though approximately 200 μm was removed from the bottom surface to facilitate good defect visibility in the XRTs (GaAs is relatively highly absorbent of x radiation). Care was taken to reduce the possibility of introducing unwanted stresses into the diode arrays. Samples were mounted onto a holder using soft wax, which ensured that they were neither bent nor stressed. This eliminates the possibility of induced defect generation. A photograph of the chip is shown in Fig. 2(a) and the numbering system for each diode is shown in Fig. 2(b). The section topographs (ST) were taken in such a position as to cut a slice across the middle of each chip.

The breakdown criterion was considered to be the reverse voltage (V_{BR}) required to produce a current of 50 μA through the diode. This was an arbitrary choice, but the concern was with the relative performance of each diode on a chip. The measurements were performed on a Tektronix 576 curve tracer. The electrical data for a typical chip are shown in Fig. 3 which is correlated with the XRT data as follows.



(a)



(b)

FIG. 2. (a) Micrograph of a chip containing a stack of 14 diodes. (b) Numbering system used for each diode stack. The black markers on the left-hand side of the figure locate the center of each p-n diode stack and should be used in conjunction with Fig. 4.

From Figure 3 it is seen that diodes D1 and D5 appear damaged, displaying no diode action. However, diodes in the range D2–D8 showed 10 V$\leq V_{BR}\leq$15 V with individual values considerably scattered. Diode D9 performed very badly with $V_{BR}\leq$1.2 V and nonstandard behavior. Diodes D10–

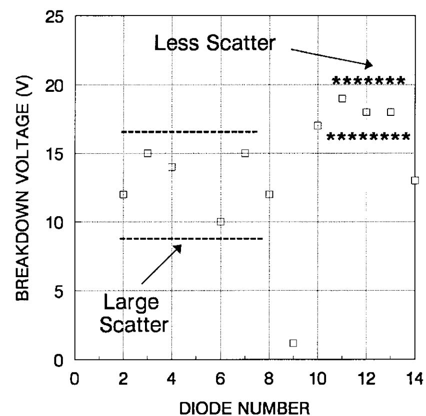


FIG. 3. Breakdown voltage performance for a typical chip containing an array of 14 diodes. The diode numbers refer to positions on the chip as outlined in Fig. 2(a).

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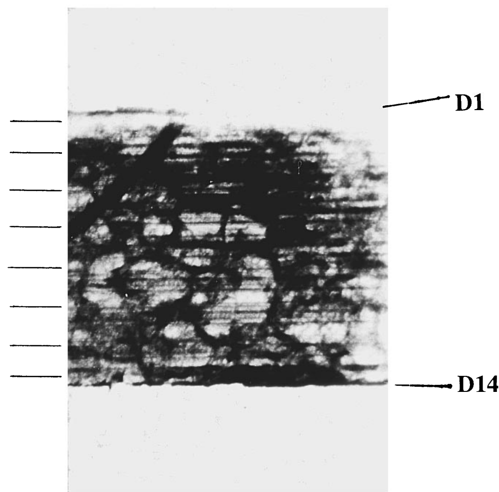

FIG. 4. A $\overline{2}\overline{2}8$ large area topograph for the diode array. Dimensions for this topograph are approximately 3 mm×3 mm. The location of selected diodes are indicated for clarity, in addition to black markers on the left-hand side of the topograph which correspond to positions indicated in Fig. 2(b).

D13 showed higher values 17 V$\leqslant V_{BR} \leqslant$19 V and also displayed a reduced scatter in performance. The final device, D14, deteriorated with $V_{BR} \approx$13 V.

The $\overline{2}\overline{2}8$ large area topograph for this sample is shown in Fig. 4 and has several features. A large dislocation line on the left-hand side of the topograph runs in an arc from D6 to D2 approximately. There is a large concentration of defects and cellular networks covering diodes D2–D7, while a smaller concentration covers D9–D13. The liquid encapsulated Czochralski (LEC) substrates have typical etch pit densities of the order of 10^4 cm^{-2}. It can be seen from Fig. 4 that one cannot distinguish individual dislocations, but rather, one can observe the strain fields due to macroscopic distributions of defects/dislocations under the device metallization. As discussed in Ref. 10, the detectability limit for individual dislocations is of the order of 10^4–10^5 cm^{-2}, which is in accordance with observations in this study. It is also clear from Fig. 4 that the number of dislocations (though not individually resolvable) under diodes D2–D7 is at least an order of magnitude greater than the above figure, and far greater in number that those under diodes D10–D13, for example. The inferior performance (lower V_{BR}, higher scatter in V_{BR}) of diodes D2–D7 correlates well with the high dislocation density and could also be attributable to the presence of the dislocation line. The lower dislocation density covering D10–D13 is in accord with their improved performance. In addition, the low V_{BR} of D14 correlates with the presence of a large defect/dislocation density region at this location (approximately bottom centre of topograph). The topograph does not appear to provide explanations for the terrible performances of D1, D5 (these two diodes displayed ohmic behavior) or D9, whose defects may lie outside the crystal, for example, in the quality of the metal-semiconductor ohmic contacts.

A somewhat underexposed section topograph, $\overline{1}1\overline{1}$ reflection through the center of the stack and perpendicular to the long axis of the chip, is displayed in Fig. 5. The large majority of the strain, defects, and damage appear clearly located in the top surface region where device processing takes place. This region extends approximately 110 μm into the substrate and indicates the very substantial impact that device processing has on semiconductor crystal quality and, hence, on electrical behavior. Such impact is confirmed by Fig. 4. Visible on the $\overline{2}\overline{2}8$ large area topograph in Fig. 4 is the metallization. Stresses imposed on the crystal by the metal overlayer are greatly enhanced at metal edges[10] and these are easily detected on the XRT.

In both topographs numerous cellular regions are seen which are indicative of a LEC substrate. The dislocations tend to be concentrated in and around the cellular walls with the central regions tending to be more dislocation free. Near diodes D2–D7, the cells tend to fuse into each other producing one region of very high dislocation density (the threshold of visibility in an XRT is typically 10^4–10^5 defects per cm^2). The origin of these cellular dislocation networks is little understood though recent advances have been made by Schlossmacher *et al.*[11] The authors noted that the most prominent dislocation types were the 30° and 60° type, with only around 10% being screw type. Precipitates, primarily of excess As dissolved in the GaAs matrix, appear at points where these dislocations change their glide planes. Most (60%–70%) of the dislocations were on {111} glide planes in

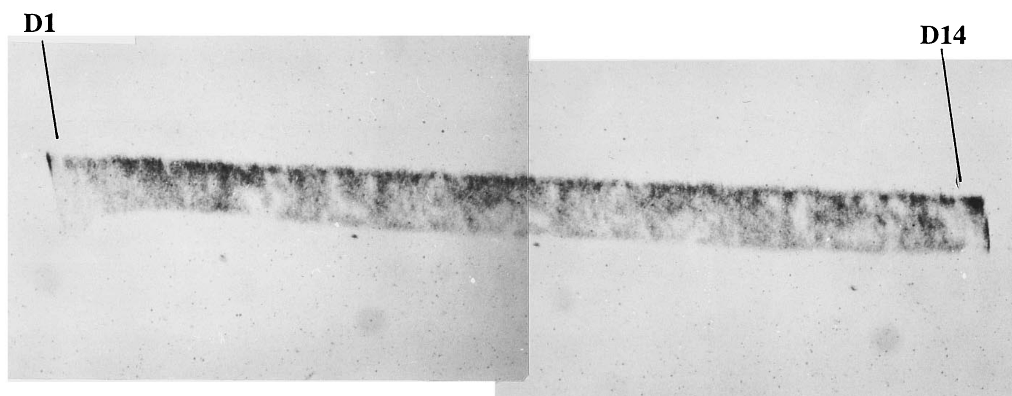

FIG. 5. A $\overline{1}1\overline{1}$ section topograph for the diode array taken along the center of the stack perpendicular to the long axis of the chip and therefore through each device.

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a glissile configuration while only 20%–30% were sessile (i.e., lying on a {111} plane with Burgers vector **b** lying on another {111} plane) or had climbed out of their glide planes. A complicated interaction of dislocation climb and reactions between intersecting glide systems produces the sessile dislocations and obstacles for dislocation movement which are necessary for the buildup of the cellular structure. It is assumed that the sources of these dislocations appear at or near the crystal edges during LEC growth, though there is currently little knowledge available about either the nature of these sources or their formation.

The proximity of these dislocation/precipitation cells to the various diodes correlates well with V_{BR} degradation. Little work has been carried out on the effects of the cells on breakdown in GaAs devices. However, a recent analysis by Beam *et al.*[12] on InP diode structures suggests similar breakdown mechanisms to the GaAs structures studied here. It is suggested that the presence of space-charge cylinders induced by strain fields around the dislocations (see, for example, Refs. 13–15) could impact on reverse bias minority carrier transport. If these dislocations and their cellular networks thread a *p-n* junction, the resulting space-charge region could transport more current than the surrounding high-resistivity inversion layer. An increase in reverse leakage current (namely a degradation of the diode) would be expected in regions of high dislocation density. This is in accord with the observations, wherein a correlation was found to exist between reverse leakage current density (J_0) and relative dislocation densities (N_{DIS}). Such a correlation is supportive of the above hypothesis, because J_0 is a function of minority-carrier lifetime, τ, in the space-charge region[2,16] and is dependent on N_{DIS} as follows:

$$J_0 \propto \frac{1}{\tau} \propto N_{DIS}. \tag{2}$$

For example, in the diode array topographed in Fig. 4, given regions where N_{DIS} was relatively *high* (i.e., diodes D2–D7), the average J_0 was measured as 0.42 mA/cm^2. However, in the region where N_{DIS} was relatively *low* (i.e., diodes D10–D12) the average J_0 was 0.20 mA/cm^2.

Furthermore, following Ref. 12, a degraded V_{BR} at regions of high precipitate concentration would be expected and, thus, near regions of high cellular network density. Queisser[17] found that precipitates can act as sites for local field enhancement and can promote premature avalanche breakdown of *p-n* junctions under reverse bias.

IV. CONCLUSIONS

A study was carried out on the impact of crystalline defects/dislocations on the electrical performance of GaAs power varactor diodes. The breakdown voltages of diodes in a linear stack of 14 were compared to the crystal defect distribution across the chip as revealed by synchrotron x-ray topographs. Strong correlation was observed between the presence of dislocations in the semiconductor and V_{BR} behavior. Diodes fabricated on or near LEC cellular dislocation networks, which also are known to be rich in As precipitates near the cell walls, were observed to have reduced and widely scattered breakdown voltages. This is consistent with the presence of space-charge cylinders surrounding such dislocations giving rise to reduced V_{BR} if they thread a *p-n* junction; it is also in accord with the possibility that the precipitates themselves can act as sites for local field enhancement, thus promoting premature avalanche breakdown.

This study suggests that mechanical crystal quality is the major determinant of both device performance and production yield for these devices. Enhancement of both performance and production yield for these devices would appear achievable by: (i) the development of device processing techniques which preserve crystal quality and new device designs and topographies which facilitate such techniques, for example, by reduction in the number of fabrication levels and (ii) the use of better quality, i.e., lower defect density, wafer start material. This study also demonstrates the ability of SXRT to operate as an effective industrial quality control tool in the production of semiconductor devices.

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