# Design of a <br> Switched Reluctance Machine Drive for Automotive Applications 

By

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A thesis presented for the award of MASTER OF ENGINEERING

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## Declaration

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Abstract<br>Design of a Switched Reluctance Machine<br>Drive for Automotive Applications

## Anthony Murphy

Automotive electrical systems are currently 12 Vdc supplied from an engine driven alternator. In an effort to meet electrical system demands of the future this voltage will be increased to a 42 Vdc standard.

Operating at this increased voltage level will facilitate numerous electronic systems to be incorporated into the vehicle in order to improve safety, increase fuel efficiency and reduce emissions. As part of the initiative the starter and alternator will be integrated into a single unit. The 42 -volt bus will allow for a more powerful integrated starter alternator (ISA).

The switched reluctance motor (SRM) could be considered as a viable solution for implementing integrated starter alternator. The SRM is a low maintenance, low cost, rugged, brushless motor without permanent magnets. It has a rugged construction that is ideally suited for automotive applications with its harsh under-bonnet environment. It provides high torque and power relative to motor volume. The principal disadvantages of this type of motor include the motor design and control difficulties Modern motor design software and lower cost digital signal processing chips for motor control have overcome these difficulties.

This thesis discusses the automotive electrical systems, switched reluctance motors (SRM), converter configurations. The operation and the design of a 3.5 kW full bridge converter and its associated control circuitry to facilitate the SRM to operate in starter and alternator modes are described in detail.

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## Chapter 1 - Introduction

Energy efficiency has become increasingly important in the $21^{\text {st }}$ century due to the increased cost of fossil fuel resources combined with the need to reduce the levels of greenhouse gases. Combining the capabilities of an electric machine to act as a motor and a generator in a system significantly reduces the carbon footprint of that system by eliminating the need for an extra machine. In order to maximise the advantage of this system integration, the electrical machine must be very efficient and require drive circuitry of limited complexity while providing equal or better levels of efficiency.

In the automotive environment, the increase in fuel efficiency and the reduction in greenhouse gas emissions have become critically important issues. The reduction in the number of motors used, together with providing new opportunities to harness their regenerative capabilities, is an area under continuous investigation. The integrated starter-generator (ISG) is an immediate application for the electric machine to operate as a motor and a generator in the automotive environment. This has expanded into the area of mild hybrid through to a full hybrid electric vehicle (HEV) that provides varying degrees of propulsion assistance and regenerative braking.

Vehicles with an ISG and a 42 V electrical system are defined as a mild hybrid (Jones 2003). The ISG allows for start-stop mode of operation, where the engine can be shut down when the car is braking or stopped but when required it can be restarted quickly and cleanly. At start up the large motor allows the engine to spin up to operating speed before commencing the engine combustion process. It can also provide some levels of propulsion assistance and, when the car is slowing down, energy can be recovered through regenerative braking. All these capabilities contribute to improving the vehicle fuel efficiency and reducing emissions.

The HEV uses an internal combustion engine (ICE) together with batteries and electric motors as propulsion sources (Sreedhar 2006). The batteries and machine in this application can provide some or all vehicle propulsion capabilities and the motor also provides regenerative braking capabilities when the vehicle is slowing. The ICE that is currently fuelled by petroleum products (petrol, diesel, etc) is transitioning so that it can also operate with various forms of biofuels (bioethanol, biodiesel, etc) in order to reduce
the dependency on crude oil. The increasing popularity of hybrid vehicles, for example the Toyota Prius, together with the sharp increase in cost of petroleum in recent years has led to intense interest in the application of electric machines for the purpose of vehicle propulsion assistance and regenerative braking capabilities.

### 1.1 Motivation

The switched reluctance machine (SRM) is particularly suitable for use in automobiles (where there is a harsh environment of high temperature and vibration) as it has a rugged construction and is a brushless motor without permanent magnets (DiRenzo 2000). The SRM is one of the oldest electric motor designs having been used in industrial applications as far back as the 1830s. Despite its advantages, it has been largely unused for many years because of design and control difficulties.

The SRM has a very simple construction as shown in Figure 1.1(a). Only the stator has windings, while the rotor has no conductors or permanent magnets. The windings on two opposing stator poles are connected to create a single phase winding. Both the rotor and stator poles are salient in order for the machine to produce reluctance torque. A magnetic field is created when the stator phase-winding is energized and reluctance torque is produced by the movement of the rotor to its minimum reluctance position.


Figure 1.1: The SRM Layout

The saliency of both the stator and rotor poles creates non-linear magnetic characteristics which complicate the analysis and control of the SRM. The control problem arises because phase to phase switching of the drive current must be precisely synchronised with rotor position for optimal operation under motoring and generating conditions. Magnetic circuit analysis software has reduced the problems associated with SRM design, while the arrival of powerful, yet moderately priced, digital signal processors (DSP) has enabled the control to be addressed in a cost effective manner. These advances have fuelled a new interest in the SRM for a wide range of consumer and industrial applications.

The work presented in this thesis was undertaken as part of a larger research project entitled "Switched Reluctance Design for Automotive Applications". The project was carried out by three PEI Technologies (PEI) centres: the University of Limerick Analogue Centre (ULA), University College Dublin (UCD) centre and the Dublin City University (DCU) centre. The Dublin City University (DCU) centre was the principal investigator and had overall management responsibility for the project.

The DCU centre was responsible for selection and design of a prototype machine controller. This involved the selection and design of generic models for the SRM as a motor and as a generator, the simulation and implementation of closed-loop control of the SRM under motoring and generating conditions, and the design and construction of a suitable power converter for the SRM and the construction of a laboratory test apparatus. The key sections are illustrated in Figure 1.2.


Figure 1.2: Key project sections for the Switched Reluctance Design for Automotive Applications

The specific part discussed in this thesis is the design and construction of the power converter, the closed-loop current control strategy and the laboratory test apparatus. The main purpose of the power converter design and the control scheme for the SRM was to maximise efficiency when operating as a motor or a generator in low voltage, battery powered applications. The development of the converter is divided into five stages: converter selection, preliminary analysis, converter design, experimental setup and converter control implementation.

The converter is targeted for operation under the 42 V automotive specification in order to maximise the capabilities of automotive power semiconductors. In order to meet the additional requirements of future electrical systems the automotive industry has established a new 42 V voltage standard ( 42 V PowerNet) to replace the current 14 V system (Kassakian 1996) and (Kassakian 2000). Improvements in fuel economy and reduction in emissions are the main arguments for the introduction of the 42 V standard.

A number of converter topologies were reviewed, the details of which are discussed. The asymmetrical half bridge and full bridge converters were selected for preliminary analysis. The analysis includes the evaluation of a number of semiconductor devices to determine component efficiency, based on a range of operating conditions that are discussed in detail and to verify reverse recovery times. The full-bridge converter using synchronous rectifier operation proved to be the most efficient solution for both motoring and generation over a wide range of operation.

Configuring of semiconductors in parallel was central to the implementation of the fullbridge converter design and this required particular attention to power and thermal analysis, layout of the printed circuit board and the implementation of specific control strategies in order to achieve an efficient design operation. Discrete MOSFET semiconductors mounted in parallel significantly increase the current handling capability of the circuit but numerous design issues had to be addressed, including stray inductances, circuit layout and thermal coupling.

Control strategies were designed to coordinate the full-bridge circuit switching signals for both motoring and generating modes with synchronous rectifier capability, to
employ blanking time capability and to implement accurate proportional-integral pulse width modulated (PI-PWM) current control.

Two pieces of laboratory test apparatus were constructed as part of this project. The first apparatus consisted of the inductive load, the DSP evaluation board (to implement the switching and current control strategies), low voltage and high voltage power supplies to power the converter. It was constructed in order to evaluate the converter operation, to develop the switching strategies for motoring and generating and, from there, the development of the current control strategy. The second laboratory apparatus consisted of an SRM coupled with a load/drive machine and torque measurement system. This apparatus was constructed for the integration of the converter with the SRM control algorithms for motoring and generating.

The contribution of this work is to illustrate that this converter configuration together with the control strategy would improve the efficiency of the switched reluctance drive system operating in both motoring and generating conditions. This topology allows independent operation of each SRM phase to maximise control flexibility and to enable the converter to be applied to an SRM with any number of phases. The laboratory apparatus facilitates evaluation of SRM control strategies under motoring and generating conditions to further enhance this machine's application potential.

### 1.2 Overview of thesis

The fundamental principles of operation of the switched reluctance machine under motoring and generating conditions are discussed in Chapter 2. The essential concepts, modes of operation and benefits and limitations are presented for the machine. The mathematical model for torque production is investigated for both motoring and generating modes and a review of the dynamic operation of the machine under motoring and generating conditions is presented for the machine. The chapter also includes a historical review of the SRM.

Chapter 3 reviews a variety of converter topologies in order to determine the most suitable selection for this application. The converter topologies are classified according to a predominant feature and a description of operation and main advantages and
restrictions are then presented for each converter. The selection of the most suitable converter topologies for preliminary analysis is then presented.

The preliminary analysis of semiconductor components to determine the most efficient converter configuration is discussed in Chapter 4. The operating conditions are defined in order to set limits of converter operation and these include: SRM specifications, operating environment and electrical requirements. A detailed component power analysis to determine the most efficient semiconductor solution is then presented. The simulation analysis and electrical tests on the most efficient components to determine the final semiconductor selection together with the most suitable converter configuration are then examined.

Chapter 5 discusses the final converter design, including a review of the issues that needed to be addressed when implementing MOSFETs in parallel: the design of heatsinks, gate drive circuitry, the determination of the dc-link capacitor, bus bar configuration, the current sensing circuit and the specific printed circuit board layout considerations.

The experimental setup is described in Chapter 6. A description is given of the laboratory apparatus consisting of an SRM coupled with a load/drive machine and torque measurement system for the purpose of integrating the converter and the SRM control algorithms for motoring and generating operation. The laboratory apparatus to evaluate the converter under various load conditions and to implement the switching and current control strategies is then discussed. The key components in this apparatus include the inductive load, the DSP evaluation board and low voltage and high voltage power supplies. A detailed description is provided of the converter prototyping including the circuit board layout and the mechanical layout of the converter through to final assembly of the complete converter.

Chapter 7 describes the development and implementation of the current control strategy implemented with the converter. A detailed description is given of the converter switching sequence including experimental results. The current control strategy, including the implementation of the proportional integral controller, is outlined and experimental results presented to illustrate converter operation at low and high current.

Finally, a summary of the thesis, conclusions and suggestions for possible future research are given in chapter 8 .

## Chapter 2 - Operating principles and features of the SRM

In order to design a power converter for the SRM to operate as both a motor and a generator a detailed understanding of the machine is required. Knowledge of the dynamic modes of operation of the SRM as a motor and a generator is central in order to define the current and voltage waveforms applied to each machine phase. These waveforms are used to implement a detailed power analysis for each of the switching components in the converter. To understand the dynamic operation of the SRM, the fundamental principles of the machine are first discussed and this is followed by a detailed mathematical analysis. A historical review provides a chronological history of the SRM up to the present day.

### 2.1 Historical review

Developments in the switched reluctance machine can be divided into different periods and under specific categories. Early evolution in this machine would be defined as the period up to the 1960s and modern developments would be defined thereafter. The specific categories would include: the developments in the machine design from its early beginnings through to its present day configuration implemented as both a motor and a generator; the progress in converter design, the growth in control strategies for motoring, generating and sensorless control operation; and, finally, applications of the SRM both past and present and possibly in the future.

Early switched reluctance machines were known as "electromagnetic engines", due to the strong influence of steam engine design, and were some of the first machines developed in the 1830's and 1850's (Miller 2001). It began with the horseshoe electromagnet of William Sturgeon in 1824 and was improved upon by Joseph Henry in 1831. A model for the electromagnetic behaviour was initially developed by Rev. William Richie in 1833. It was not until John Hopkinson's work on magnetic circuits that the electric machine could be designed systematically. These early machine designs were largely by trial and error and some examples include machines by Rev. Nicholas Callan in the late 1830's, a number of his machines can still be seen in Saint Patrick's College, Maynooth [(Miller 2001) and (IEEE 2006)], the machines built for Charles

Wheatstone by William Healey in 1842, examples built by Taylor and others built by Davidson (Miller 2001). They all had very poor magnetic circuits due to the use of solid instead of laminated iron for the rotor and stator. They also had no means to recover the stored inductive energy and the pulsating forces yielded structural problems. These machines were superseded by the ring wound armature dc motor by Pacinotti (1864) and Gramme (1869) and the polyphase induction motor of Tesla (Keville 1994) that provided vastly superior performance.

The transition to the modern era of what is now termed the 'switched reluctance machine' occurred in the mid 1960s and it was brought about by four parallel advancements in industry: developments in power switching devices (thyristors and power transistors); the evolutions of microprocessors and digital circuitry to implement control algorithms; the development of high speed computers to analyse and design the machine using advanced programming languages; and, finally, the general expansion in the application of the machine and the control systems. According to (Miller 2001), some of the key features of modern reluctance machines and their drives were developed at Queen's College, Dundee, in the early 1960s, specifically in the area of motor design, electric switching circuits using thyristors and open-loop and closed-loop control.

In the late 1960s through the early 1970s, Prof. Byrne and his colleagues at University College Dublin published significant material on the influence of saturation to improve energy conversion efficiency of the machine [(Byrne 1973) and (Byrne 1976)] that was verified by [(Miller 1985) and (Stephenson 1989)]. They also did valuable original work on machines with low phase numbers (Byrne 1973), electronic drives with fewer power switches (Byrne 1985) and addressed the issue of current imbalance on machine performance (Devitt et al 1981). Burnice Bedford of the General Electric Company, USA, published two patents in 1972 describing all the key features of the modern SRM and the controlled switching circuits [(Bedford 1972a) and (Bedford 1972b)].

Around this period, Lawrenson and Stephenson at the University of Leeds, began work on the switched reluctance machine and their research efforts culminated in the landmark paper published in 1980 (Lawrenson 1980). It addressed the many design issues regarding number of poles, pole arcs and choice of phase numbers and described
the favourable static and dynamic performance of the machine in four quadrants when compared to an induction motor of equivalent size. This paper marked the beginning of renewed interest in the switched reluctance machine that continues to this day. Their research work lead to the formation of SR Drives Ltd. (bought out by Emerson in 1994) and produced about half the commercial applications for the machines in the early 1980s (Miller 2001). Since 1987 Professor Miller and his colleagues of the Speed Consortium at the University of Glasgow have made significant developments in the design and analysis of the SRM and developed a widely used CAD program called PC-SRD [(Miller 1990) and (Fuengwarodsakul 2005)].

Up until the 1930s, electronic switching between phases in electrical machines was controlled using a commutator (Miller 2001). Early electronic switching circuits consisted of mercury arc rectifiers or thyratrons but offered poor reliability at a high cost and this severely limited the application of these devices. The advent of thyristors and power transistors in the early 1960s allowed for the development of reliable (but still at a relatively high cost) electronics switching circuits to be developed for electrical machines. Dr. Cruickshank and his colleagues at Queens College, Dundee, developed some of the first switching circuits using thyristors for the SRM and also developed some of the fundamental switching techniques for these machines (Miller 2001).

Burnice Bedford of General Electric (GE) Company, USA, developed all the key features of the modern controlled electronic circuits for the SRM by exploiting new power semiconductors being developed by GE and the company's capability to manufacture a wide range of speciality motors. He initially developed the asymmetric half-bridge converter (Bedford 1972b) which was further refined and developed by Ray (Ray 1979) and Lawrence (Lawrence 1980). He also originally developed the split-dc converter (Bedford 1972a) that was further refined by Graseby Controls Ltd. UK (Miller 1993). Early work on the C-dump topology was implemented by Prof. J.V. Byrne (Byrne 1985) and further developed in detail by J.T. Bass (Bass 1987).

During the 1980s through the 1990s, significant developments took place in electronic switching circuits for the SRM due mainly to the advances in semiconductor technologies from the development and advances in microprocessor design. This led to greater power handling capabilities for the power transistor beginning with the bipolar
junction transistor (BJT) but more significantly the MOSFET and the IGBT. These devices allowed for forced commutation and current regulation using pulse-width modulation working at switching frequencies higher than was possible with the thyristors. Numerous topologies facilitating different circuit configurations and component count were realized during this period and up to the present day. Examples of these converters include: the R-dump converter (Krishnan 2001), the Sood converter (Sood 1992), the series resonant converter (Park 1992) and the full-bridge converter (Krishnamurthy 2005). A useful comparison of many different converter topologies are included in both (Vukosavic 1990) and (Barnes 1998). A detailed review of a number of converter topologies is presented in chapter three.

The development of microprocessors and microcontrollers and related digital circuits during the late 1970s and the early 1980s allowed for the implementation of complex control algorithms and ushered in a new era of control capability for the SRM (Chappell 1984). Reduction in the torque ripple that is inherent in SR motor operation was a key area that was targeted using these complex algorithms. A comprehensive review of the different control approaches to torque ripple reduction is provided by (Husain 2002).

Since the 1990s, the operation of the SRM as a generator has received considerable attention. Radun emphasised the need for closed loop control of the switched reluctance generator (SRG) when he discussed the instability of the open loop operation of the SRG with fixed turn-on and turn-off angles in an important paper from 1994 (Radun 1994). The SRG has been under investigation for application as an automotive starter/generator [(Kokernak 1999), (Mese 2000) and (Fahimi 2001)], wind power generation [(Torrey 1993) and (Cardenas 1995)] and various aero space applications [(MacMinn 1989), (Radun 1994), (Radun 1998) and (Cossar 2004). A thorough overview of the development of SRG control is provided by (Miller 2001) and (Torrey 2002).

In recent years, significant research has being directed towards the operation of the SRM without a position sensor. A number of different methods of indirectly estimating the rotor position have been proposed but they all make use of the inductance variation in one way or another. The aim of these 'sensorless' position estimation schemes is to
reduce system cost while also increasing system reliability. A detailed review of the various approaches is provided by both (Husain 1996) and (Ehsani 2002).

| Products | Company |
| :--- | :--- |
| Air-handler | A.O Smith |
| EV drives | Aisin Seiki |
| High-speed motors and controllers | AMC NEC/Densei |
| Commercial vacumm products | Ametek Lamb Electric |
| High speed centrifuge systems | Beckman Instruments |
| Electric doors | Besam A/b |
| Mining drives | British Jeffrey Diamond |
| Energy saving screw air compressor | CompAir Ltd. |
| Automotive cruise control | DANA Corp. |
| High air flow-rate hand-dryer | Dyson UK |
| 250kW low-speed drive | Elektro Magnetix Ltd |
| Washer drive | Emerson/SRDL |
| Pumps,HVAC motion control | Emotron A/b |
| Plotter drive | Hewlett-Packard |
| Several | Mavrik Motors |
| Train air conditioning | Normalair Garrett |
| Megatorque direct-drive | NSK Ltd |
| General purpose industrial drives | Oulton, Tasc Drives |
| Weaving machine servos | Picanol |
| Fork lift/pallet truck drive | Radio Energie |
| Starter/Generator for articulated vehicle | SR drives Ltd. |
| Mild hybrid-electric powertrain | SR drives Ltd. |
| $3 k W$ 12V belt-drive starter-generator | SR drives Ltd. |
| Industrial drives | Sicmemotori |
| VSR high pressure pumps | Weir Group Plc. |
|  |  |

Table 2.1: Switched reluctance applications

While a significant number of developments have occurred with the SRM over the past number of decades, it has yet to receive significant acceptance in industry. Some of the most popular applications for the SRM include the Maytag Neptune washing machine and vacuum cleaners by Ametek, LG and Dyson (Fiedler 2005). In addition Dyson introduced a new hand dryer in October 2006 that used a SRM operating at 100,000 rpm to generate a $180 \mathrm{~ms}^{-1}$ air flow-rate that is claimed to dry hands in 10s (Nathan 2006). A number of current and previous applications of the SRM are provided in Table 2.1 [(Krishnan 2001), (Miller 1993), (Miller 2002), (SR drives Ltd 2007a), (SR drives Ltd 2007b) and (Dyson UK 2007)].

### 2.2 Fundamentals

Electrical machines can be broadly defined into two categories by how they produce torque: either electromagnetically or by variable reluctance (DiRenzo 2000). With the first type, motion occurs due to the interaction of two mutually coupled magnetic fields, one generated by the stator and the other by the rotor. This produces electromagnetic torque, which tends to bring the magnetic fields into alignment. DC and induction motors operate on this principle. In the second type the motion is produced by variable reluctance in the air gap between the rotor and the stator. Switched reluctance machines fall into this second group.

The switched reluctance machine is an extremely simple electrical machine. The machine is doubly salient in that it has both salient rotor and stator poles made of magnetically soft, low loss steel laminations. The rotor pole does not contain magnets or windings, while the stator pole has windings on each pole, with one phase consisting of two diametrically opposite poles wound in series to form a single phase winding. Numerous combinations of phase, rotor pole and stator pole combinations are available to yield different SRM geometries. The phase winding and the cross section of a four phase, eight stator pole and six rotor pole arrangement of an $8 / 6$ four-phase SRM is illustrated in Figure 2.1 (a). A typical converter arrangement is shown in Figure 2.1 (b).


Figure 2.1: (a) Cross-section of an 8/6 four-phase SRM. (b) Classic converter.

Magnetic flux is generated when current flows in a phase winding and results in torque being produced due to the tendency of the rotor pole to align with the stator pole in order to yield a minimum reluctance path. In Figure 2.1 (a), the rotor and stator pole pairs, $R_{1}$ and $S_{1}$ illustrate an unaligned position and $R_{2}$ and $S_{2}$ illustrate the aligned position. The flux-linkage and therefore the phase inductance varies with rotor position where it is at the minimum value $\left(\mathrm{L}_{\mathrm{u}}\right)$ at the unaligned positions $\left(\theta_{1}\right.$ and $\left.\theta_{4}\right)$ and rises to a maximum value $\left(\mathrm{L}_{\mathrm{a}}\right)$ at the aligned positions $\left(\theta_{2}\right.$ and $\left.\theta_{3}\right)$ as illustrated in Figure 2.2. Physically, position $\theta_{1}$ corresponds to the start of overlap where the leading edge of the rotor pole is aligned with the leading edge of the stator pole and $\theta_{4}$ corresponds to the end of rotor and stator pole overlap.


Figure 2.2: The variation of idealised phase inductance with rotor position

The rotor angle at which the voltage is applied across the phase winding is called the turn-on angle and it is removed at the turn-on angle, while the difference in these angles is defined as the dwell angle or firing angle. The complete cycle from the start of one variation in inductance cycle until it repeats again is called the pole pitch. The region where the phase inductance remains constant is defined as a dead zone. The rotor speed at which the back-emf and the applied voltage across the phase winding are equal in magnitude is defined as the base speed.



Figure 2.3: The idealised phase inductance, current and torque for motoring operation

The SRM can operate either as a motor or as a generator depending on the range of rotor angles at which the voltage is applied to the phase winding. The machine's operation is independent of the direction of current in the phase windings but is a function of rotor position with respect to the energised phase. Accurate rotor position information is essential to ensure smooth operation of the SRM when motoring and generating. The term "switched reluctance" refers to the switching of sequential phase excitations that achieve the rotor rotation (Miller 2001).

Figure 2.3 shows the variation in idealised phase inductance and torque with rotor angle for a constant phase current. For motoring operation, the firing angles are selected so that current flows in the phase winding when the rotor and stator poles approach alignment which is when the phase inductance in increasing and this produces a positive motoring torque in the direction of rotation. The electrical energy consumed in the alignment of the rotor pole and stator pole pair is converted to mechanical energy in driving a load attached to the rotor shaft. For generating operation, the firing angles are selected so that the current flows in the phase winding immediately after the rotor and stator poles have passed alignment when the phase inductance is decreasing. The rotor produces negative or braking torque opposing the direction of rotation. Generating occurs when the mechanical energy expended by a prime mover in pulling the rotor pole away from the excited stator pole is converted to electrical energy.

To illustrate the fundamental operation of the SRM as a motor and as a generator, only motoring operation at low speed, and generating at the base speed, are discussed here. The SRM operation as a motor and a generator at other speeds is discussed in Section 2.3.

Under motoring operation it is clear that negative torque is undesirable. For this reason, the phase current must be reduced to zero before the $\theta_{3}-\theta_{4}$ interval when the poles are separating (The operation in the intervals $\theta_{1}-\theta_{2}$ and $\theta_{2}-\theta_{3}$ are discussed in the following paragraphs).Therefore, the ideal motoring current waveform should be a series of pulses where the position of the pulses coincides with the rising inductance interval. Thus, the ideal motoring torque waveform for a single-phase SRM has the shape shown in Figure 2.4.




Figure 2.4: The idealised phase inductance, current and torque for motoring operation

The inductance at the unaligned position $\left(\theta_{1}\right)$ tends to be a very small value resulting in the value of current in the phase winding increasing very quickly. The rectangular current waveform (current pulse) can then be approximated by chopping the current along $\theta_{1}-\theta_{2}$. To avoid production of negative torque the current must be reduced to zero before alignment at $\theta_{3}$ and this can be achieved by reversing the voltage across the phase before alignment.

As can be seen in Figure 2.4, the single-phase SRM produces regions of discontinuous torque. Continuous rotation of a single-phase machine relies on either the momentum of the machine when motoring or on the prime mover when generating. Similarly, the machine cannot start from every position, as at least two phases are required to guarantee starting and at least three phases are required to ensure starting direction (DiRenzo 2000). It is shown in Section 2.3 that the torque can only be produced in regions of increasing and decreasing inductance. Hence, no torque is produced in the 'dead zones' between $\theta_{2}$ and $\theta_{3}$ at the aligned position and in the unaligned position between $\theta_{4}$ and $\theta_{1}$.

To produce continuous positive motoring torque and to ensure self-starting capability from all positions, the full 360 degrees of rotation must have areas of increasing inductance so that appropriate placed current pulses produce continuous torque output. Figure 2.5 shows the idealised inductance, current and torque waveforms for the fourphase $8 / 4$ SRM of Figure 2.1. The energy conversion (torque production) that takes place in discrete cycles through the interaction of one rotor and stator pole pair is called a stroke. The number of strokes per revolution, $S$, is related to the rotor poles, $N_{R}$, and the number of phases, $P$, by $S=N_{R} P$. Hence, for the $8 / 6$ four-phase machine in Figure $2.1(\mathrm{a}), S=6(4)=24$.


Figure 2.5: The idealised phase inductance, current and torque waveforms for a fourphase 8/6 SRM under motoring conditions

Under generating operation, the ideal generator current should be a series of pulses where the position of the pulses coincides with the falling inductance interval as shown
in Figure 2.6. The rectangular current waveform can be approximated when the backemf and the applied voltage balance and the current stays constant until pole overlap ends. Current pulses must be applied at areas of decreasing inductance over the full 360 degrees of rotor rotation to produce continuous generating torque as illustrated in Figure 2.7.




Figure 2.6: The idealised phase inductance, current and torque for generating operation


Figure 2.7: The idealised phase inductance, current and torque waveforms for a fourphase 8/6 SRM under generating conditions

Like other motors, the machine torque is restricted by maximum allowed current, and the speed by the available bus voltage. The current must be maintained within a maximum allowable limit until the rotor reaches the base speed. At this speed the backemf of the machine is equal to the applied voltage to the phase winding and the current will not increase further. Above the base speed the back-emf continues to increase so the conduction angles can be enlarged to maintain constant power output. At very high speeds, when the conduction angle cannot be increased any further, the torque decays rapidly. The SRM can still operate at very high speed but only under light loads. The torque/speed characteristic for motoring in a particular direction is illustrated in Figure 2.8. The characteristic for generating in the same direction of rotation would be achieved by reflecting the waveform in the speed axis, while that for motoring and generating in the opposite direction is achieved by reflection in the torque axis.


Figure 2.8: Torque/speed characteristic of the SRM

The main benefits of the switched reluctance machine include:

- Simple construction in that only the stator poles have windings and the rotor has no windings or magnets but is constructed of steel laminates stacked on a shaft.
- Simplicity of the rotor construction which means that it is suitable for extremely high-speed operation as it has a low moment of inertia.
- Ease in cooling as the stators are located nearest the machines outer casing and only the stators have windings which are the main source of heat generation.
- Extremely robust machine primarily due to is simple construction and additionally due to the electrical independence of the phases, which enables the SRM to remain operational even with a failure of one of the phases.
- Lower maintenance requirements than a dc machine as the SRM is a brushless machine
- Good starting torque like a dc series motor as the torque is proportional to the square of the current (explained in Section 2.3).
- Power density equivalent to, or better than, induction machines but less than permanent magnet synchronous, and brushless dc, machines for speeds up to $20,000 \mathrm{rpm}$, while above this speed, power density is comparable to, or greater than, these other machines (Krishnan 2001).
- A number of sensorless position estimation schemes are possible using the principle that the phase inductance variation of the SRM is uniquely dependent on rotor position and the phase current. This allows the elimination of the position sensor to further improve reliability and reduce cost.
- Independence of torque with respect to current direction which means that the converter only needs to facilitate unidirectional current. Converter topologies can use less than two switches per phase, leading to a reduction in cost.

The main limitations of the switched reluctance machine include

- Complex control algorithms are required to eliminate the torque ripple produced due to the strong non-linear magnetic characteristics of the SRM.
- Radial magnetic forces that act on the stator structure during rotor shaft rotation produce acoustic noise levels higher than other machines. The noise can be reduced by using complex torque control strategies and through careful design of the SRM structure.
- Need for electronic commutation for its operation and fact that it cannot work directly from a dc or ac line. Additionally, a separate path must be provided for current in the phase winding to flow at the end of the commutation cycle. This requires additional components that contribute to the overall cost of the converter.
- Precise rotor position information is required in order to synchronise the excitation of the phase windings with rotor position in order to implement effective control strategies. The method of obtaining the position feedback information has a significant bearing on the complexity and the reliability of the SRM drive. If a position sensor is used it can have a significant effect on the reliability and robustness of the drive while sensorless position schemes contribute significantly to the complexity of the drive.


### 2.3 Mathematical Modeling of the SRM

Because each phase is identical and energised in sequence, the analysis is confined initially to a single phase. Firstly it is assumed that no saturation occurs and a linear approach is taken. Later, saturation is taken into account using non-linear analysis. The following discussion on linear and non-linear operations is from the analysis by (Miller 2001). The linear and nonlinear analysis discussed here for motoring can be applied to generating.

### 2.3.1 Analysis of magnetically linear operation

Linear analysis is centred on the voltage and torque equations. The terminal voltage generated across one phase is related to the change in magnetic flux in the winding according to Faraday's law. The following simplifying assumptions are made:

- hysteresis and eddy current losses are neglected in the analysis of the magnetic circuit
- there is negligible mutual coupling between phases
- the winding resistance is constant and independent of the current waveform and frequency

The terminal voltage generated across one phase is:

$$
\begin{equation*}
v_{p h}=i_{p h} R_{p h}+v_{L p h} \tag{2.1}
\end{equation*}
$$

Where:

$$
\begin{array}{ll}
v_{p h} & =\text { the applied phase voltage } \\
i_{p h} & =\text { the phase current } \\
R_{p h} & =\text { the phase winding resistance } \\
v_{L p h} & =\text { the induced voltage on the phase inductance }
\end{array}
$$

Subscript ' $p h$ ' is left out for clarity, from here on.

The induced voltage $v_{L}$ is defined by the magnetic flux linkage, $\psi$, that varies as a function of the phase current, $i$, and the rotor position, $\theta$.

$$
\begin{equation*}
v_{L}=\frac{d \psi(i, \theta)}{d t}=\frac{\partial \psi(i, \theta)}{\partial i} \frac{d i}{d t}+\frac{\partial \psi(i, \theta)}{\partial \theta} \frac{d \theta}{d t} \tag{2.2}
\end{equation*}
$$

Therefore

$$
\begin{equation*}
v=i R+\frac{\partial \psi(i, \theta)}{\partial i} \frac{d i}{d t}+\frac{\partial \psi(i, \theta)}{\partial \theta} \frac{d \theta}{d t} \tag{2.3}
\end{equation*}
$$

Where, $d \theta / d t$ is the angular velocity, $\omega$, in $\mathrm{rad} / \mathrm{s}$, and $\partial \psi(i, \theta) / \partial i$ represents the instantaneous inductance $L(i, \theta)$. For simplicity, it is assumed that there is no magnetic saturation, which means that the phase inductance is unaffected by variations in phase current, then $L(\theta)=\psi(\theta) / i$. Equation (2.3) can be further expanded using linear analysis to yield:

$$
\begin{equation*}
v=i R+L(\theta) \frac{d i}{d t}+i \omega \frac{d L(\theta)}{d \theta} \tag{2.4}
\end{equation*}
$$

Thus, the applied phase voltage is equal to the sum of the voltage drops on the right hand side of Equation (2.4), the resistive voltage drop, the inductive voltage, and the induced emf or 'back-emf'. The back-emf, $e$, is equivalent to:

$$
\begin{equation*}
e=i \omega \frac{d L(\theta)}{d \theta} \tag{2.5}
\end{equation*}
$$

The instantaneous electrical power, $v i$, is

$$
\begin{equation*}
v i=i^{2} R+L(\theta) i \frac{d i}{d t}+i^{2} \omega \frac{d L(\theta)}{d \theta} \tag{2.6}
\end{equation*}
$$

The time derivative of magnetic stored energy at any instant is given by

$$
\begin{equation*}
\frac{d}{d t}\left(\frac{1}{2} L(\theta) i^{2}\right)=\frac{1}{2} i^{2} \frac{d L(\theta)}{d t}+L(\theta) i \frac{d i}{d t}=\frac{1}{2} i^{2} \omega \frac{d L(\theta)}{d \theta}+L(\theta) i \frac{d i}{d t} \tag{2.7}
\end{equation*}
$$

Assuming no losses other than $i^{2} R$ and in order to agree with the law of conservation of energy, the mechanical power must equal to the electrical input power less the resistive power losses $\left(i^{2} R\right)$ and the rate of change in the magnetic stored energy. Therefore, the instantaneous mechanical power, which is equivalent to $\omega T$, where $T$ is the instantaneous electromagnetic torque, can be written as:

$$
\begin{equation*}
\omega T=\frac{1}{2} i^{2} \omega \frac{d L(\theta)}{d \theta} \tag{2.8}
\end{equation*}
$$

Therefore the expression for electromagnetic torque ( $T$ ) is:

$$
\begin{equation*}
T=\frac{1}{2} i^{2} \frac{d L(\theta)}{d \theta} \tag{2.9}
\end{equation*}
$$

Equation (2.9) indicates that the torque is independent of the sign of the phase current and is instead determined by the sign of the $d L / d \theta$, where the absolute value of $d L / d \theta$ contributes to the amount of torque produced. For this reason, SRMs are generally designed to have a large ratio between the aligned and unaligned inductance in order to attain high torque levels. Large air gaps between the stator and rotor pole at the unaligned position increases the inductance ratio (Miller 1993). Typically, an SRM with a low phase number and therefore a low rotor and stator pole count has larger air gaps.


Figure 2.9: Equivalent circuit for a single phase of the SRM

From the perspective of the phase winding terminals of the SRM, equation (2.4) appears to indicate the equivalent circuit shown in Figure 2.9 comprising of a resistance $(R)$, an inductance $(L)$ and a back-emf ( $e$ ) that is proportional to speed. However, with $L$ and $e$ varying with both rotor position and current, the torque cannot be calculated from a
simple equivalent circuit but requires direct solution of equations (2.1) and (2.9). A method to directly solve these equations requires non-linear analysis of the SRM.

### 2.3.2 Analysis of magnetically nonlinear region

The practical SRM operates most effectively and efficiently in the magnetically saturated region. Operating the machine in the magnetically linear region leads to inefficient operation of the drive. Nonlinear analysis takes into account the saturation of the magnetic circuit in the SRM and this allows a full understanding of the electromechanical energy conversion for both motoring and generating operation. One type of analysis is based on the magnetization curve shown in Figure 2.10; this is a sample of the flux linkage $(\psi)$ versus phase current $(i)$ characteristic at a particular rotor position.


Figure 2.10: Magnetization curve indicating magnetic field stored energy $\left(W_{f}\right)$ and the magnetic field co-energy $\left(W_{c}\right)$

The energy stored in a magnetic field is

$$
\begin{equation*}
W_{f}=\int_{0}^{\psi} i(\psi, \theta) d \psi \tag{2.10}
\end{equation*}
$$

It is more desirable to express torque in terms of current instead of magnetic flux and this is achieved using the term of co-energy $\left(W_{c}\right)$ instead of energy. Magnetic field coenergy is defined as

$$
\begin{equation*}
W_{c}=\int_{0}^{i} \psi(i, \theta) d i \tag{2.11}
\end{equation*}
$$

The relationship between field energy and co-energy is illustrated in Figure 2.10 and defined as

$$
\begin{equation*}
W_{f}+W_{c}=i \psi \tag{2.12}
\end{equation*}
$$



Figure 2.11: Magnetization curve showing the effect of the rotor moving from position A to position B

A rotor movement from its original position at A to a new position at B through an angular displacement $\Delta \theta$ yields the magnetization curves for both positions shown in Figure 2.11. Assuming that the current remains constant during this rotor rotation, the electrical energy $\left(W_{e}\right)$ exchanged with the supply is

$$
\begin{equation*}
\Delta W_{e}=\int i v d t=\int i \frac{d \psi}{d t} d t=\int i d \psi=A B C D \tag{2.13}
\end{equation*}
$$

The change in stored field energy is

$$
\begin{equation*}
\Delta W_{f}=\mathrm{OBC}-\mathrm{OAD} \tag{2.14}
\end{equation*}
$$

Therefore, the mechanical work is the change in electrical energy minus the change in magnetic field energy is expressed as:

$$
\begin{align*}
& \Delta W_{m}=\Delta W_{e}-\Delta W_{f} \\
& \Delta W_{m}=\mathrm{ABCD}-(\mathrm{OBC}-\mathrm{OAD}) \\
& \Delta W_{m}=\mathrm{OABCD}-\mathrm{OBC} \\
& \Delta W_{m}=\mathrm{OAB} \quad \quad \text { (shaded in Figure 2.11) } \tag{2.16}
\end{align*}
$$

This value corresponds to the increase in the magnetic field co-energy, $\Delta W_{m}=\Delta W_{c}$. The mechanical work done during the displacement $\Delta \theta$, from A to B , can be expressed as:

$$
\begin{equation*}
\Delta W_{m}=T \Delta \theta=\Delta W_{c} \tag{2.17}
\end{equation*}
$$

Therefore, in the limit, when $\Delta \theta \rightarrow 0$, the instantaneous torque $(T)$ is the partial derivative in co-energy with respect to angular displacement.

$$
\begin{equation*}
T=\left[\frac{\partial W_{C}}{\partial \theta}\right]_{i=\text { cons } \tan t} \tag{2.18}
\end{equation*}
$$

In a motor with no saturation all the magnetization curves would be straight lines and the stored magnetic field energy would equal the magnetic field co-energy at all times to yield:

$$
\begin{equation*}
W_{f}=W_{c}=\frac{1}{2} L(\theta) i^{2} \tag{2.19}
\end{equation*}
$$

This expression for $W_{c}$ implies that equation (2.18) for electromagnetic torque reduces to:

$$
\begin{equation*}
T=\frac{1}{2} i^{2} \frac{d L(\theta)}{d \theta} \tag{2.20}
\end{equation*}
$$

This is identical to equation (2.9) from linear analysis.

For a multi-phase SRM, the instantaneous torque equation becomes the summation of the individual torque values for each phase and is of the form:

$$
\begin{equation*}
T=\sum_{n=1}^{k} T_{n} \tag{2.21}
\end{equation*}
$$

where $T_{n}$ is the torque produced by the $n^{\text {th }}$ phase and $k$ is the total number of phases.

### 2.3.3 Analysis of generator operation

In the description of the generating operation provided earlier, the firing angles are selected so that the current flows in the phase winding immediately after the rotor and stator poles have passed alignment when the phase inductance is decreasing. The rotor produces negative or braking torque opposing the direction of rotation. A negative voltage is then applied to the phase winding and the mechanical energy expended by a prime mover in pulling the rotor pole away from the excited stator pole is converted to electrical energy to yield a generating current.

The circuit diagram for the SRM to operate as a generator is shown in Figure 2.12. An example of the generator current and the idealised inductance is shown in Figure 2.13


Figure 2.12: Switched reluctance generator for single phase


Figure 2.13: Switched reluctance generator phase currents and idealised inductance

The instantaneous current flowing in the phase winding is defined as $i_{p h}$. As illustrated in Figure 2.12 and 2.13 at the angle $\theta_{\text {on }}$, the voltage $\left(V_{S}\right)$ is applied to the phase winding and current $\left(i_{p h}=i_{i n}\right)$ begins to flow. Negative voltage $\left(-V_{S}\right)$ is applied at $\theta_{\text {off }}$ and current $\left(i_{p h}=i_{\text {out }}\right)$ continues to flow due to the generating action until the end of the rotor and stator pole overlap at which point the current in the phase winding decays to zero at $\theta_{\text {ext }}$. The current flow in the phase winding between $\theta_{\text {on }}$ and $\theta_{\text {off }}$ is called the excitation current $\left(i_{i n}\right)$, while the current flowing between $\theta_{\text {off }}$ and $\theta_{\text {ext }}$ is defined as the generated current ( $i_{\text {out }}$ ).

The average of the excitation current, $I_{i n}$, over a single stroke is determined as follows:

$$
\begin{equation*}
I_{i n}=\frac{1}{\theta_{\text {off }}-\theta_{\text {on }}} \int_{\theta_{\text {on }}}^{\theta_{\text {off }}} i_{p h} d \theta \tag{2.22}
\end{equation*}
$$

The average of the generated current, $I_{\text {out }}$, over a single stroke is determined as follows:

$$
\begin{equation*}
I_{\text {out }}=\frac{1}{\theta_{\text {ext }}-\theta_{\text {off }}} \int_{\theta_{\text {off }}}^{\theta_{\text {ext }}} i_{\text {ph }} d \theta \tag{2.23}
\end{equation*}
$$

The net generated average current, $I_{o}$, over a single stroke is expressed as:

$$
\begin{equation*}
I_{o}=I_{\text {out }}-I_{\text {in }} \tag{2.24}
\end{equation*}
$$

The power conversion in the SRM when operating as a generator can be characterized by the excitation penalty, $\xi$, (Miller 2001) and is expressed as:

$$
\begin{equation*}
\xi=\frac{P_{\text {ext }}}{P_{\text {out }}}=\frac{I_{\text {in }}}{I_{\text {out }}}=\frac{I_{\text {in }}}{I_{o}+I_{\text {in }}} \tag{2.25}
\end{equation*}
$$

where $P_{\text {ext }}$ is the mean electrical excitation power and $P_{\text {out }}$ is the mean electrical output power. An excitation penalty that is as small as possible is desired in order to minimise losses.

### 2.4 Dynamic operation of SRM

The continuous operation of the SRM requires the switching of current pulses from phase to phase during shaft rotation. For motoring operation, this can be defined for low speed and high speed ranges. The generating mode of operation is analysed at low speed, base speed and high speed. The classic or asymmetric half-bridge converter shown in Figure 2.14 is the converter topology used to assist in the description of all the dynamic modes of operation of the SRM.


Figure 2.14: (a) Static view of the converter. (b) Magnetization mode. (c) Freewheeling mode. (d) Forced demagnetization mode

### 2.4.1 Low speed motoring

The current pulses must be regulated at low speed as back-emf is insufficient to limit the current. There are two main methods of current regulation at low speed: voltage- $P W M$ and current hysteresis. The regulation of the phase current is implemented by chopping, which is the switching on and off the power switches in Figure 2.14 at a frequency that is much higher than the fundamental frequency of the current waveform (Miller 1993). There are two types of chopping schemes: soft chopping and hard chopping.

The soft-switching strategy has three modes of operation as illustrated in Figure 2.14b, c and $d$. The first mode is called the energization mode or magnetization mode or positive-voltage loop (PVL) as indicated in Figure 2.14b. During this time both switches $\left(\mathrm{Q}_{1}\right.$ and $\left.\mathrm{Q}_{2}\right)$ are on and the current rises rapidly in the phase winding as indicated in Figure 2.15a (I). During the second mode, the freewheeling state or zero-voltage loop, only one switch and one diode $\left(Q_{2}\right.$ and $\left.D_{1}\right)$ are on as illustrated in Figure 2.14c. There is zero volts applied across the phase winding and the current continues to flow through the switch and the diode, although it is gradually decaying as indicated in Figure 2.15a (II). No energy is transferred to or from the supply during this period. The third mode, the demagnetization state or the negative-voltage loop, occurs when both switches are off and the energy returned to the supply via the freewheeling diodes $\left(D_{1}\right.$ and $\left.D_{2}\right)$ as shown in Figure 2.14c. Both diodes are forward biased and a negative voltage is applied across the phase winding, forcing the current to rapidly decay to zero as indicated in Figure 2.15a (III).

The hard-switching strategy has only two modes of operation, the magnetization and demagnetization states. The magnetization and demagnetizations waveform for the hard-switching scheme is illustrated in Figure 2.15b (IV) and Figure 2.15b (V) respectively. During demagnetization, the decay in the current waveform is greater leading to greater current ripple but reduced dynamic response time.

During the zero-volt period of the soft chopping operation the change in the phase current is very small, which allows for a reduced switching frequency and current ripple rating for the converter filter capacitor (Miller 2001). Additionally the soft chopping scheme produces lower acoustic noise and lower EMI levels (Miller 1993).


Figure 2.15: Low speed motor of operation for both (a) soft switching - (I) energization, (II) freewheeling and (III) demagnetization and (b) hard switching - (IV) Energization and (V) Demagnetization

The energy conversion process starts when the power switches are turned on and current begins to flow in the phase winding at $\theta_{\text {on }}$, the current increases rapidly to the required value before rotor and stator pole overlap at $\theta_{1}$. Torque production begins as the rotor and stator poles approach overlap and it then rises rapidly to the required value. By maintaining a constant current value between the beginning $\left(\theta_{1}\right)$ and end of overlap $\left(\theta_{2}\right)$,
a constant torque value can be maintained over this period. The power switches are turned off at $\theta_{2}$ and the phase voltage has a negative polarity, which leads to the current freewheeling through the diodes. The current falls rapidly to zero and must be at zero before $\theta_{3}$, in order to prevent the production of a negative torque. The process is illustrated in what is called the energy conversion loop illustrated in Figure 2.16 for low speed operation. The maximum energy conversion area, $W$, is bounded by the aligned and unaligned magnetization curves and is traversed in a counter clockwise direction from the unaligned to the aligned position. A single cycle of the loop is achieved during each stroke.


Figure 2.16: Low speed motoring energy conversion loop

As noted previously, there are two main methods of current regulation at low speed: voltage-PWM and current hysteresis. Voltage-PWM implementation requires that one or both of the power switches are turned on and off at a fixed frequency, while the duty cycle varies depending on the current requirements. This method can be implemented with either hard or soft chopping switching schemes. Under soft chopping operation, one of the power switches are turned on and off and the other power switch remains on during the conduction period, while with hard chopping both of the power switches are turned on and off together.

Current hysteresis necessitates that one of the power switches be switched off when the current exceeds a particular set point value and switches back on again the current fall below a second level. The range between the current limits is referred to as the hysteresis-band. The switching frequency varies, which can lead to unwanted audible noise and current harmonics. Both soft and hard chopping switching are possible with this type of current regulation. Delta modulation is a variation of current hysteresis in
which the current is sampled at a fixed frequency. When the phase current exceeds a reference current value one of the power switches is turned off and when the current drops below the reference value, the power switch is turned on again. The switching frequency can vary up to the fixed sampling frequency value. Soft and hard chopping schemes are also possible with this type of current regulation.

### 2.4.2 High speed motoring

At high speed, no current regulation is required as the back-emf is large enough to limit the current. The torque is controlled only by varying the firing angles of a single pulse of current to yield what is called the single pulse mode of operation. The single pulse mode waveforms for the idealised inductance profile, the phase voltage, the single pulse current and the resultant torque are provided in Figure 2.17


Figure 2.17: Single pulse control for single phase motoring at high speed

The energy conversion process starts when both power switches are turned on after passing the unaligned position of the previous stroke at $\theta_{4}$ and current rises rapidly in the phase winding due to the low value of inductance and no back-emf. At $\theta_{1}$ the inductance begins to increase and the back-emf quickly exceeds the supply voltage and forces the $d i / d t$ to become negative. The greater the speed, the faster the drop off in current in this region and only an increase in the supply voltage can counteract this effect. The dwell angle must be increased linearly with speed above the base speed in order to maintain a reasonable torque output although it will be decaying in value. The energy conversion loop for high speed operation is illustrated in Figure 2.18 and is traversed in the counter clockwise direction.


Figure 2.18: High speed motoring energy conversion loop

### 2.4.3 Low speed generating

Generating at low speed is similar to motoring at low speed except the firing angles are retarded in order for the current pulse to coincide with the region of decreasing inductance. Current regulation is required during the low speed generating cycle, as the magnitude of the back-emf is smaller than the combined magnitude of the applied voltage and the resistive voltage drop. Hard chopping is the preferred switching strategy as energy is returned every switching cycle whereas no energy is returned during the zero-voltage cycle of the soft switching strategy. Voltage-PWM control can be used to regulate the current when generating at low speeds by varying the average applied voltage in the SRM (Miller 2001). The excitation and generation waveform at low speed
is illustrated in Figure 2.19. It is assumed that the inductance is linear and that the current reaches its set point before $\theta_{3}$ and the conduction cycle ends at $\theta_{4}$.


Figure 2.19: Voltage-PWM current regulation at low speed

In one PWM period the excitation current corresponds to the area $A_{l}$ and the generated current corresponds to the area $A_{2}$ in Figure 2.19. Assuming that the duty cycle $d$ is constant over a conduction period and the current ripple due to PWM is negligible compared to its average peak value $i_{p}$, then

$$
\begin{align*}
& A_{l}=D_{l} t_{p w m} i_{p} \\
& A_{2}=D_{2} t_{p w m} i_{p} \tag{2.26}
\end{align*}
$$

Where $D_{l}=d$ and $D_{2}=1-d$ and $t_{p w m}$ is the PWM period $\left(t_{p w m}=1 / f_{p w m}\right)$. The net generated current in one PWM period ( $I_{o, p w m}$ ) is:

$$
\begin{align*}
I_{o, p w m} & =A_{2}-A_{l} \\
& =\left(D_{2}-D_{1}\right) t_{p w m} i_{p} \tag{2.27}
\end{align*}
$$

In the analysis, the initial excitation current in the area indicated (1) in Figure 2.19 and the generated current after the turn-off angle at $\theta_{4}$ in the area indicated (2) are neglected.

The ratio between excitation power and the generated power yields the excitation penalty, $\xi$, (Miller 2001) for the current regulated with PWM is defined as:

$$
\begin{equation*}
\xi=\frac{D_{1}}{D_{2}-D_{1}}=\frac{d}{1-2 d} \tag{2.28}
\end{equation*}
$$

During the excitation period, the terminal voltage of the phase winding is expressed as follows:

$$
\begin{equation*}
v_{p h}=L(\theta) \frac{d i}{d t}-e \tag{2.29}
\end{equation*}
$$

where the voltage drop $(i R)$ due to the resistance of the coil is neglected and the backemf, $e$, is equivalent to:

$$
\begin{equation*}
e=i \omega\left|\frac{d L(\theta)}{d \theta}\right| \tag{2.30}
\end{equation*}
$$

where $\omega$ is the rotor speed, $d L / d \theta$ is always negative under generating operation and the negative sign is placed alongside $e$ for clarity. For effective PWM control at low speeds the condition $|e|<\left|V_{s}\right|$ must always be true, otherwise the generating current is uncontrollable and increases during the demagnetization period. During the excitation period the equation is:

$$
\begin{equation*}
L(\theta) \frac{d i_{e x c}}{d t}=V_{S}+e>0 \tag{2.31}
\end{equation*}
$$

During the generating period, the equation is:

$$
\begin{equation*}
L(\theta) \frac{d i_{g e n}}{d t}=-V_{S}+e<0 \tag{2.32}
\end{equation*}
$$

Assuming that the change in $L$ over the PWM period is small and can be neglected, in order to keep the average current constant over a PWM period, then

$$
\begin{align*}
& \left|\frac{d i_{e x c}}{d t} D_{1} t_{p w m}\right|=\left|\frac{d i_{g e n}}{d t} D_{2} t_{p w m}\right|  \tag{2.33}\\
& \left|V_{S}+e\right| D_{1}=\left|V_{S}-e\right| D_{2}
\end{align*}
$$

Rearranging the above equation and substituting $D_{1}=d$ and $D_{2}=1-d$ yields the expression:

$$
\begin{equation*}
d=\frac{1}{2}\left(1-\frac{e}{V_{S}}\right) \tag{2.34}
\end{equation*}
$$

From equation (2.28), in order to generate net energy which is greater than the excitation power, the condition of $\mathrm{d}<0.333$ must be satisfied. Substituting this condition into equation (2.34) gives the condition required in order to generate net power greater than the power consumed during the excitation of the phase winding with voltage-PWM is:

$$
\begin{equation*}
0.333 \mathrm{~V}_{\mathrm{DC}}<\mathrm{e}<\mathrm{V}_{\mathrm{DC}} \tag{2.35}
\end{equation*}
$$

and

$$
\begin{equation*}
0.333 \omega_{\mathrm{b}}<\mathrm{e}<\omega_{\mathrm{b}} \tag{2.36}
\end{equation*}
$$

where $\omega_{\mathrm{b}}$ is the base speed. It therefore can be concluded for net power generation at low speed using voltage-PWM is possible between one third of the base speed and the base speed. The energy conversion loop for low speed generating operation is illustrated in Figure 2.20 and is traversed in the clockwise direction.


Figure 2.20: Low speed generating energy conversion loop

### 2.4.4 High speed generating

Generating at high speed can be defined for two regions: (a) at the base speed and (b) above the base speed. The power switches turn on at $\theta_{\text {on }}$ and excitation power is applied to the phase winding and magnetic energy is built up in the air gap and at $\theta_{\text {off }}$ the power switches are turned off and regenerated current flows through the freewheeling path until the current goes to zero at $\theta_{\text {ext }}$.


Figure 2.21: Single pulse control for single phase generating at high speed

At the base speed, the magnitude of the back-emf and the combined magnitude of the applied voltage plus the resistive voltage drop in the phase winding are in balance and this yields current that remains constant without the need for current regulation (Torrey 2002) until the overlap of the poles at $\theta_{4}$ and then decays to zero by $\theta_{\text {ext }}$ as indicated in Figure 2.21 (a). Above the base speed, the back-emf in the phase winding has a larger magnitude than the combined magnitude of the applied voltage plus the resistive voltage
drop of the phase winding, and the current increases after the power switches turn off at $\theta_{\text {off }}$ and the current increases until pole overlap at $\theta_{4}$ where it decays to zero at $\theta_{\text {ext }}$ as indicated in Figure 2.21(b).

On method of implementing generator operation at high speed is to regulate the applied voltage with speed in order to use the condition $|e|>\left|V_{s}-\mathrm{i} R\right|$, as indicated in Figure 2.21(b), to allow the generating current to reach a set point value, and then implement and regulate the condition $|e|=\left|V_{s}-\mathrm{iR}\right|$, as indicated in Figure 2.21(a), to maintain constant generator current (Miller 2001).

The energy conversion loop for high speed generating operation is illustrated in Figure 2.22 and is traversed in the clockwise direction.


Figure 2.22: High speed generating energy conversion loop

### 2.5 Summary

The SRM has gone through significant developments since its beginnings in the early 1800s to the present day. The evolution in high speed computers and magnetic analysis software has allowed significant developments in the design of the SRM. Since the 1980s, significant developments in semiconductor technologies have led to greater power handling capabilities for power switching devices, particularly the MOSFET and the IGBT. These devices have allowed for converter operation with forced commutating
schemes and for current regulation schemes to operate at much higher frequencies. The development of powerful microprocessors and in particular low cost digital signal processors (DSP) in recent years has allowed for the implementation of complex control algorithms for the SRM. This has increased the application potential of the SRM in many commercial arenas from starter/generator for articulated vehicle and mild hybridelectric powertrain to washing machines and hand dryers.

For the implementation of the SRM in an automotive application as both a motor and a generator, it is desirable to have high torque capability to drive loads (starting an engine or actual propulsion assistance) or to operate as a generator, particularly under regenerative conditions where high braking torque may be beneficial. A two-phase SRM would be the most suitable for these applications if operating in only one direction. This SRM configuration would minimise the complexity of the power converter. The larger areas around the stator poles of a two-phase SRM allow for phase windings with copper of larger cross section. This enables lower copper losses at higher current operation. The larger iron sections of the rotor and stator poles keep core losses low and maintain good mechanical stiffness which is important in minimising acoustic noise (Miller 1993). The core losses are also reduced by the lower commutation frequency of the two-phase SRM. The larger air gap, higher current handling capability and reduced core losses all contribute to the increased torque capability of the two-phase SRM as discussed in Section 2.3.

From the review and the analysis of the SRM, the converter in this application should operate under voltage-PWM for both low speed motoring and generating conditions and single-pulse operation under high speed conditions. Variation in the source voltage would be desirable under high speed generating to maintain the condition $|e|=\left|V_{s}-\mathrm{iR}\right|$, in order to maintain constant generator current.

## Chapter 3 Converter topologies

Significant research effort has been invested in the design of electronic power converters for the SRM. A review of a cross section of the numerous converter topologies that are available is presented in this chapter before finalizing the configuration that is most suitable for this application. The general requirements are defined for the converter in order to determine the most suitable choice. The converters are grouped into various classifications, which are based on the predominant feature of the converter. Each converter from a topology group is described under the heading of its predominant features, the modes of operation and the main benefits and limitations. On review of all the groups, the most suitable converter configuration is selected for preliminary analysis.

### 3.1 Selection criteria and topology groups

The fundamental selection criteria to determine the most suitable converter for this application include the following:

- Independent phase operation with respect to the operating modes for the energization or magnetization, freewheeling and demagnetisation for both motoring and generating modes of operation.
- Soft chopping switching capability or the ability for the application to implement freewheeling operation.
- Unidirectional current and bidirectional voltage for all phases.
- Maximum efficiency capability in both motoring and generation modes of operation.
- Minimum complexity in order to minimise converter costs

The converter topologies are divided into two primary classifications: hard- switching and soft-switching. The fundamental converter configurations are illustrated in Figure 3.1. The hard-switching classification contains five subgroups: bridge, capacitive energy recovery, magnetic, dissipative and single phase. The soft-switching classification contains a single subgroup: self-commutating There are four bridge converters topologies: the asymmetrical half-bridge, the shared winding converter, the shared switch converter and the full-bridge converter. The capacitive energy recovery group has five fundamental configurations but there are variations within each
configuration. The configurations are: C-dump converter, voltage boosting converter, the split dc converter and the Sood converter. The magnetic energy recovery group have two basic converter schemes: the bifilar converter and the auxiliary commutation winding converter. The dissipative group has a single elementary configuration called the R-dump but there are variations defined as the decay converters. The selfcommutating group has four essential configurations but there are some derivatives. They are: series resonant, zero-voltage transition (ZVT) PWM converter, auxiliary quasi-resonant dc-link (AQRDCL) converter and the H -bridge converter. The single phase converter topology is included here for completeness but is not discussed here as the application requires a minimum of a two phase SRM to implement unidirectional starting capability.


Figure 3.1: Classification of power converters for switched reluctance motor

### 3.2 Bridge Converters

Four fundamental bridge converter topologies are addressed in this section and these are the asymmetrical half-bridge converter, the shared phase winding converter, the shared switch converter and the full-bridge converter. A brief description is provided for each converter topology that includes a discussion on the possible modes of operation together with an illustration. The main benefits and limitations are outlined for each topology.

### 3.2.1 Asymmetrical Half-Bridge Converter

This converter is also known as the classic converter and is a widely documented (Lawrenson 1980), (Ray 1979), (Vukosavic 1990) converter topology using a single rail power supply as shown in Figure 3.2a. It is defined as a 2 N active switch configuration, where N is the number of phases.


Figure 3.2: The asymmetrical half-bridge or classic converter. (a) Static view of converter. (b) Energization mode. (c) Freewheeling mode. (d) Forced demagnetization mode

This converter has two possible switching strategies, soft-switching and hard-switching. The soft-switching strategy has three modes of operation as illustrated in Figure 3.2 b, c and d. The first mode is called the energization mode or magnetization mode as indicated in Figure 3.2b. During this time both switches $\left(\mathrm{Q}_{1}\right.$ and $\left.\mathrm{Q}_{2}\right)$ are on and the current rises rapidly in the phase winding as indicated in Figure 3.3a (I). During the second mode, the freewheeling state, only one switch and one diode are on as illustrated in Figure 3.2c. There is zero volts applied across the phase winding and the current continues to flow through one switch and one diode, although it is gradually decaying as indicated in Figure 3.3a (II). No energy is transferred to or from the supply. The third mode, demagnetization, occurs when both switches are off and the energy in the phase winding is returned to the supply via the freewheeling diodes as shown in Figure 3.2c. The voltage is reversed across the phase winding which forces the current to rapidly decay to zero as indicated in Figure 3.3a (III).


Figure 3.3: Half-bridge converter modes of operation for both (a) soft switching - (I) energization, (II) freewheeling and (III) demagnetization and (b) hard switching - (IV) energization and (V) demagnetization

The hard-switching strategy has only two modes of operation, the magnetization state and the demagnetization states. The magnetization and demagnetizations waveform for the hard-switching scheme is illustrated in Figure 3.3b (IV) and Figure 3.3b (V) respectively. During demagnetization, the decay in the current waveform is greater leading to greater current ripple but reduced dynamic response time.

The most significant advantages of this circuit are (i) the possibility to independently control the upper and lower switched for maximum flexibility, (ii) all possible firing angles can be implemented with soft-switching allowing for maximum regenerative braking capability and (iii) equal performance in forward and reverse directions. The main limitation is the high power semiconductor count per phase, which can become expensive with switched reluctance drives with a large number of phase windings. Other disadvantages are the relatively low demagnetization voltage at high speeds due to the fixed voltage supply and the requirement for a large capacitor on the supply voltage in order to filter the voltage ripple associated with the magnetization and demagnetization of the phase winding. Demagnetization during generator mode of operation could yield significant power losses through the freewheeling diodes due to the large forward voltage drop across the diode coupled with the large operating current.

### 3.2.2 Shared phase winding converter

This scheme allows for two phase winding to be shared in a modified asymmetrical half-bridge converter (Krishnan, 2001) as shown in Figure 3.4a. This increases the utilization of the power devices by increasing the component duty cycles. An SRM with an even number of phases is required to take advantage of this scheme. A siliconcontrolled rectifier (SCR) is used to steer the current through the desired phase winding. Only one power switch and one diode are required per phase winding compared to two power switches and two diodes in the asymmetrical converter. Alternate phase windings are grouped together to allow for independent control with overlapping currents that do not exceed one phase cycle duration.

This converter can also be operated with soft-switching and hard-switching strategies. Soft-switching again has three modes of operation: magnetization, freewheeling and demagnetization, while hard-switching has only magnetization and demagnetization as discussed previously with the asymmetrical converter. The main difference is that the
desired phase winding becomes active when the SCR is turned on (Phase 1 by $\mathrm{SCR}_{1}$ and Phase 2 by $\mathrm{SCR}_{2}$ as illustrated in Figure 3.4). The operation of Phase 1 is illustrated graphically in Figure 3.4 and Phase 2 operates in the same manner when $\mathrm{SCR}_{2}$ becomes active.


Figure 3.4: The shared-phase winding converter. (a) Static view of converter. (b)
Energization mode. (c) Freewheeling mode. (d) Forced demagnetization mode

The main advantages of this configuration include:

- Only one power switch, one SCR and one diode are required per phase winding.
- Greater utilization of power switches and diodes in the modified asymmetrical converter as the power devices are now used for two phase windings instead of one thereby reducing cost in the SRM drive.
- The converter is capable of positive, negative and zero voltage output, which allows for greater current control flexibility.
- Independent control of phase current is possible with this configuration The main disadvantages of this configuration are:
- The SCR is always in the conduction path, which can lead to significant losses during high power applications. This would require a larger heat sink for cooling thereby reducing the efficiency of the system and increasing system costs.
- SCR gate drive circuits would increase the component count and therefore drive costs, while also increasing complexity with the requirement for gate drive circuit isolation.
- Current overlap is not possible between phase winding within the same halfbridge.


### 3.2.3 Shared switch converter

This converter is also known as the Miller converter when implemented with a three phase SRM (Pollock 1990) and (Vukosavic 1990). A two phase implementation is illustrated in Figure 3.5a. The switches and diodes are shared between more than one phase-winding that yields an $\mathrm{N}+1$ active switch configuration. This is particularly useful when the SRM has two or more phase windings as it reduces the number of power device.


Figure 3.5: The shared switch converter. (a) Static view of converter. (b) Energization mode. (c) Freewheeling mode. (d) Forced demagnetization mode

This converter can also implement soft-switching and hard-switching strategies in the same fashion as with the asymmetrical half-bridge converter. The operation of phase 1 is illustrated in Figure 3.5, while phase 2 operated in the same way except the $\mathrm{Q}_{3}$ and $\mathrm{D}_{3}$ are now active devices instead of $\mathrm{Q}_{1}$ and $\mathrm{D}_{1}$.

The benefits of this converter are greater utilization of the power switches due to the shared switch operation and the topology is applicable to two or more phases and has fewer constraints on phase current overlap when the phase number is greater than four.

The main limitations of this topology are that there are restrictions on the current control options during current overlap conditions. For phase count greater than or equal to four, two or more phases can be operated independently but not all the phases can be operated independently.

### 3.2.4 Full-bridge synchronous rectifier converter

This configuration offers the potential to reduce conduction and switching losses during freewheeling and demagnetization mode of operation by replacing the diodes in the half-bridge circuit with MOSFETs power switches as indicated in Figure 3.6a.


Figure 3.6: The full-bridge converter. (a) Static view of converter. (b) Energization mode. (c) Freewheeling mode. (d) Forced demagnetization mode

It also provides utmost flexibility in motoring and generating modes of operation (Krishnamurthy 2005). This converter also has the capability to operate in either soft or hard switching strategy. The soft-switching incorporates the two modes of operation of hard-switching, so only soft-switching is discussed here. The magnetization mode begins when both $Q_{1}$ and $Q_{2}$ turn on and both $Q_{3}$ and $Q_{4}$ are off as illustrated in Figure3.6b. Throughout freewheeling, $\mathrm{Q}_{3}$ and $\mathrm{Q}_{2}$ turn on and both $\mathrm{Q}_{1}$ and $\mathrm{Q}_{4}$ are off as
indicated in Figure 3.6c. During demagnetization, $\mathrm{Q}_{3}$ and $\mathrm{Q}_{4}$ turn on and both $\mathrm{Q}_{1}$ and $\mathrm{Q}_{2}$ are off as shown in Figure 3.6d. During magnetization and freewheeling modes, $\mathrm{Q}_{3}$ operates as a synchronous rectifier, (Mohan 1995c) while both $\mathrm{Q}_{3}$ and $\mathrm{Q}_{4}$ operate as synchronous rectifiers during demagnetization cycle of operation. The idealized waveforms of control signals for all the switches in magnetization, freewheeling and demagnetization modes of operation and phase winding voltage and current waveforms are illustrated in Figure 3.7a for soft-switching and Figure 3.7b for hard-switching strategies.


Figure 3.7: Full-bridge converter modes of operation for both (a) soft switching - (I) energization, (II) freewheeling and (III) demagnetization and (b) hard switching - (IV) energization and (V) demagnetization

A delay period, called blanking time, is required between the switching on and off of $\mathrm{Q}_{1}$ and $Q_{2}$ pair and $Q_{3}$ and $Q_{4}$ pair in order to prevent a short circuit of the power supply. During the blanking period the diode in parallel with the switch conducts until the power switch turns on.

The main advantages are the same as with the half-bridge converter but with improved operational efficiency during freewheeling and demagnetization modes of operation using synchronous rectification scheme, which is especially beneficial during generator mode of operation. The mail limitation is again the same as with the half-bridge with under utilization of the power switches being further exacerbated in the full-bridge with the additional power switches. The additional cost of the extra gate drive circuits for the additional power switches must be taken into account.

### 3.3 Capacitive energy recovery converters

Four capacitive energy recovery converters are addressed in this section and they are the C-dump converter, the split dc converter, the Sood converter and the voltage boosting (buck-boost) converter. A brief description is provided for each converter topology that includes a discussion on the possible modes of operation together with illustration and the main benefits and limitations of the circuits. Voltage boosting can be achieved by a number of different schemes, some of which are highlighted briefly. A detailed discussion is provided on the buck-boost converter.

### 3.3.1 C-dump converter

The defining characteristic of the C -dump converter is the sharing of the freewheeling circuit with the SRM phase (Bass 1985) and (Miller 1993) as indicated in Figure 3.8a. During freewheeling the charge builds up in the dump capacitor, $\mathrm{C}_{\mathrm{d}}$, and is typically controlled by a step down circuit, consisting of $\mathrm{Q}_{\mathrm{r}}, \mathrm{D}_{\mathrm{r}}$ and $\mathrm{L}_{\mathrm{r}}$, to maintain an average value of $2 \mathrm{~V}_{\mathrm{s}}$ across the capacitor. This defines the converter as a dual-rail circuit. The step down circuit operates like a large snubber with energy recovery to the supply.


Figure 3.8: The parallel C-dump converter. (a) Static view of converter. (b) Magnetization mode (c) and (d) Freewheeling with energy recovery mode. (e) and (f) Demagnetization with energy recovery mode

There are three distinct mode of operation: magnetization, freewheeling with energy recovery and demagnetization with energy recovery. During magnetization, the supply voltage is applied to the phase winding when $\mathrm{Q}_{1}$ is turned on as indicated in Figure 3.8b. When the phase winding current exceeds a predetermined threshold, switch $\mathrm{Q}_{1}$ turns off and forward biasing diode $\mathrm{D}_{1}$ to allow the current to freewheel and charge the capacitor, $\mathrm{C}_{\mathrm{d}}$ as indicated in Figure 3.8c. This has the effect of reducing the phase winding current below the reference value. During the next magnetization cycle of the switch, $\mathrm{Q}_{1}$, a feedback control circuit varies the duty cycle of the energy recovery switch, $\mathrm{Q}_{\mathrm{r}}$, to regulate the voltage across the dump capacitor by transferring energy from the capacitor to the dc source and the inductor, $\mathrm{L}_{\mathrm{r}}$, as indicated Figure 3.8d. This cycle of energization, freewheeling and energy recovery is repeated during the conduction period of the phase winding. At commutation, the demagnetization begins when the switch, $\mathrm{Q}_{1}$, turns off and the energy in the machine is partially transferred to the dump capacitor as indicated in Figure 3.8e and the voltage across the capacitor increases. The voltage difference between $\mathrm{V}_{\mathrm{o}}$ and $\mathrm{V}_{\mathrm{s}}$ is impressed across the phase winding and the current decays rapidly to zero. The voltage across the dump capacitor is regulated by controlling the duty cycle of the energy recovery switch, $\mathrm{Q}_{\mathrm{r}}$, as indicated in Figure 3.8f. The waveforms for the C-dump converter during the complete cycle of operation are shown in Figure 3.9.


Figure 3.9: Waveforms for the C-dump converter with energy recovery circuit

The main advantage of this converter is the ability to have independent phase control with the minimum number of switches. The main disadvantage is that demagnetization voltage is limited due to it being the difference in the voltage across the dump capacitor and the supply voltage. Additional losses are incurred in the energy recovery circuit resulting in a decrease in the efficiency of the motor drive. Failure of the energy recovery circuit can lead to uncontrollable charging of the dump capacitor yielding catastrophic results. The circuit shown in Figure 3.8 is a parallel C-dump converter, while it is also possible to have a series C-dump converter as illustrated in Figure 3.10a and this circuit allows for the dump capacitor to be rated at the demagnetization voltage and not the demagnetization voltage plus the supply voltage as is the case with the parallel C-dump. A further modification of the C-dump circuit is provided in Figure 3.10b (Mir 1997). This revised circuit reduces the VA rating of the power switches and the voltage rating of the dump capacitor. A freewheeling mode of operation is possible with this revised configuration.


Figure 3.10: Variations of the C-dump converter circuit, (a) the series C-dump converter, (b) the modified C-dump converter

### 3.3.2 Buck-boost converter

For a buck-boost converter, $\mathrm{Q}_{\mathrm{a}}, \mathrm{D}_{\mathrm{a}}$ and $\mathrm{L}_{\mathrm{a}}$ and the output capacitor, $\mathrm{C}_{\mathrm{b}}$ form a buckboost front end stage (Barnes 1998), (Krishnan, 2001) and (Vukosavic 1990) as illustrated in Figure 3.11a. This dual-rail voltage boosting circuit offers added flexibility in the SRM control capabilities by separating the magnetization and demagnetizing voltage and providing a variable supply voltage. The converters operation can be divided into four possible states.

- Magnetization commences when the switch, $\mathrm{Q}_{1}$, turns on and impresses the voltage, $\mathrm{V}_{\mathrm{Cb}}$, across the phase winding as indicated in Figure 3.11b.
- The second state is forced demagnetization: it occurs when $\mathrm{Q}_{1}$ is off and the diode, $\mathrm{D}_{1}$, conducts transferring the energy from the phase winding to the capacitor, $\mathrm{C}_{\mathrm{S}}$ as indicated in Figure 3.11c.
- The third stage is the charging of capacitor, $C_{b}$, with $Q_{a}$ turned on. When the switch, $\mathrm{Q}_{\mathrm{a}}$, turns on, and assuming the voltage drop across $\mathrm{Q}_{\mathrm{a}}$ is negligible, then the voltage across the inductor, $\mathrm{L}_{\mathrm{a}}$, is equal to the source voltage as indicated in Figure 3.11d.
- The fourth and final stage is the charging of capacitor, $C_{b}$, with $Q_{a}$ turned off. During this stage, $\mathrm{Q}_{\mathrm{a}}$ turns off and the diode, $\mathrm{D}_{\mathrm{a}}$, conducts transferring the energy stored in $L_{a}$ to $C_{b}$ as indicated in Figure 3.11e.


Figure 3.11: The buck-boost converter. (a) Static view of converter. (b) Magnetization (c) Demagnetization (d) Charging of $C_{b}$ with $Q_{a}$ turned on (e) Charging of $C_{b}$ with $Q_{a}$ turned off

The most significant advantage of the buck front end allows for the input voltage to be greater than the dc source voltage to accelerate current buildup in the phase winding, which is especially useful in generator mode as rapid current build up is required in the phase winding near rotor and stator pole alignment. Another advantage is the each phase can be controlled independently of the other even though there is only one switch per machine phase. The main disadvantages are extra circuit complexity and the higher voltage rating requirement for the power switches, the voltage across $Q_{1}$ is $V_{C b}$, while the voltage across $\mathrm{Q}_{\mathrm{a}}$ is $\mathrm{V}_{\mathrm{Cs}}$ plus $\mathrm{V}_{\mathrm{Cb}}$.

There are a number of other voltage boosting circuits including: (a) parallel dc-link voltage-boosting converter (top) and series dc-link voltage-boosting converter (bottom), are shown in Figure 3.12a (Barnes 1998). The boost capacitor in the dc-link voltageboosting converters increases the turn on and turn-off voltage applied for part of the motoring stroke. The auxiliary rail boost converter is shown in Figure 3.12b (Hava 1992), parallel (top) and series (bottom). In these circuit the auxiliary voltage boost capacitor, $\mathrm{C}_{\mathrm{b}}$, is switched in and out of the energization cycle using the switch, $\mathrm{Q}_{\mathrm{b}}$, and diode, $\mathrm{D}_{\mathrm{b}}$. The sequential boost converter is shown in Figure 3.12c (Le-Huy 1990). This circuit is similar to the series auxiliary rail boost converter but has a boost capacitor and blocking diode per phase winding. The variable dc-link converter is illustrated in Figure 3.12d (Krishnan, 2001). Here the switch, $\mathrm{Q}_{\mathrm{c}}$, the diode, $\mathrm{D}_{\mathrm{c}}$, the inductor, $L_{c}$, and the capacitor, $C_{c}$, form a step-down switching power stage. This stage
varies the input dc source voltage to obtain the desirable input voltage to the machine windings.


Figure 3.12: (a) Parallel dc-link voltage-boosting converter(top) and series dc-link voltage-boosting converter (bottom), (b) Auxiliary rail boost converter, parallel (top) and series (bottom) (c) Sequential boost converter (d) Variable dc-link converter

### 3.3.3 Split DC Converter

In this circuit, the single dc link capacitor is replaced with two capacitors connected in series as illustrated in Figure 3.13a. This converter is also known as the Oulton converter circuit (Miller 1993). This circuit has two possible modes of operation: magnetization and demagnetization, which fundamentally is a hard-switching format. The operation for a single phase is as follows:

- Magnetization commences when $\mathrm{Q}_{1}$ is closed. Current circulates through $\mathrm{Q}_{1}$, phase 1 , and the capacitor $\mathrm{C}_{1}$. The voltage across the capacitor is applied to the winding as shown in Figure 3.13b.
- When the switch, $\mathrm{Q}_{1}$, is open at demagnetization, the current freewheels through the diode, $\mathrm{D}_{1}$, and the voltage across the capacitor, $\mathrm{C}_{2}$, is applied to the phase winding. The charging of the capacitor, $\mathrm{C}_{2}$, quickly depletes the phase winding current as illustrated in Figure 3.13c.


Figure 3.13: The Split dc converter. (a) Static view of converter. (b) Magnetization mode. (c) Demagnetization mode

The waveforms illustrating the magnetization and demagnetization modes of operation are illustrated in Figure 3.14.


Figure 3.14: Waveforms for the split dc converter circuit

The main advantage is this circuit achieves the capability of having one switch per phase without adding extraneous passive components and still achieves significant control flexibility and efficiency. The main limitation is the requirement for balancing the charge across the dc link capacitors, $\mathrm{C}_{1}$ and $\mathrm{C}_{2}$, which requires an even number of machine phases. Additionally, the balancing of energy flow in the capacitors results in some loss in the independent control of the phase windings. Another disadvantage to this configuration is that only half of the supply voltage is applied to the phase winding during magnetization and demagnetization, decreasing dynamic response of the current control loop and reducing the maximum motoring speed capability.

### 3.3.4 Sood converter

This converter does without a dc-link capacitor and instead uses the boost capacitor as a dump capacitor as indicated in Figure 3.15a. It is also considered to be a dual rail topology and its configuration is similar to the C-dump and buck-boost circuits but the Sood converter has primarily different modes of operation (Vukosavic 1990). This converter has four possible operating states:

- The first state is magnetization from dc supply, $V_{s}$. The switch, $\mathrm{Q}_{1}$, turns on and the phase winding is connected to the supply voltage as indicated in Figure 3.15b
- The magnetization from the capacitor, $\mathrm{C}_{\mathrm{b}}$, is the second state. Here both $\mathrm{Q}_{1}$ and $\mathrm{Q}_{\mathrm{a}}$ are on, the capacitor voltage, $\mathrm{V}_{\mathrm{c}}$, is larger than the supply voltage, $\mathrm{V}_{\mathrm{s}}$ and the energy flows from the capacitor to the phase winding as shown in Figure 3.15c. If the capacitor voltage is smaller than the supply voltage the magnetization reverts to the first state.
- Demagnetization through freewheeling is defined as the third state. In this state, $Q_{a}$ is on and $D_{1}$ and $D_{a}$ are on providing a freewheeling path for the phase winding current as indicated in Figure 3.15d. This allows the phase winding to demagnetize slowly. $\mathrm{S}_{1}$ must withstand the boost voltage, $\mathrm{V}_{\mathrm{c}}$, during this period.
- Demagnetization by charging the boost capacitor, $\mathrm{C}_{\mathrm{b}}$, is defined as the fourth and final state. During this period, both $\mathrm{Q}_{1}$ and $\mathrm{Q}_{\mathrm{a}}$ are off and the diode, D 1 , turns on and the phase winding is demagnetized through $\mathrm{D}_{1}$, the boost capacitor, $\mathrm{C}_{\mathrm{b}}$, and the supply voltage as shown in Figure 3.15e. The boost capacitor is charged by the demagnetization energy for the phase winding and the supply voltage.

The boost capacitor voltage must be kept within a narrow band. The minimum voltage is determined by the demagnetization requirements and this value also determines all switch and boost capacitor voltage ratings. Low speed operation requires PWM current control and alternates between state one and state four. State three is only implemented at very low speed when time is not critical. During state four, the switch, $\mathrm{Q}_{\mathrm{a}}$, must remain off until the phase winding current has decayed to zero. The main advantage of this configuration is the low component count and that the four possible states allow additional motor control freedom. The main limitation is the complex control required to implement the four states. There are also additional power losses through the energy recovery circuit.


Figure 3.15: The Sood converter. (a) Static view of converter. (b) Magnetization from Vs. (c) Magnetization from boost capacitor (d) Demagnetization through freewheeling (e) Demagnetization by charging the boost capacitor

### 3.4 Magnetic Energy Recovery Converters

These circuits exploit the fact that the energy stored in the magnetic field of the phase winding can be transferred to a closely coupled second winding that can be either returned to the voltage supply or used to energize another phase winding (Barnes 1998) and (Miller 1993). Two converter configurations are examined in this section: the bifilar converter and the auxiliary winding converter. A brief description is provided for each converter topology that includes a discussion on the possible modes of operation together with illustration and the main benefits and limitations of the circuits.

### 3.4.1 Bifilar Converter

This configuration uses one switch and one diode per phase and using a bifilar-wound SRM with closely coupled primary and secondary windings to regenerate the stored magnetic energy to the source [(Krishnan 2001) and (Ray 1979)]. The switch is in series with the primary winding, while the diode is in series with the secondary winding as illustrated in Figure 3.16a.


Figure 3.16: The bifilar converter. (a) Static view of converter. (b) Magnetization state (c) Demagnetization state

There are two operating states: magnetization and demagnetization.

- Magnetization commences with the switch, $\mathrm{Q}_{1}$, turns on allowing current, $\mathrm{i}_{\mathrm{pr}}$, to build up in the primary phase winding; during this period the diode is reversed biased as illustrated in Figure 3.16b.
- At commutation the switch turns off and the polarity of the induced emf in the secondary winding is such to forward bias the diode, $\mathrm{D}_{1}$. This allows the current, $\mathrm{i}_{\text {sec }}$, to circulate through the diode, the secondary winding and the source, which leads to the demagnetization of the primary as illustrated in Figure 3.16c.

The waveforms illustrating the magnetization and demagnetization modes of operation are illustrated in Figure 3.17.


Figure 3.17: Waveforms for the bifilar converter circuit

The main advantage is the component count is low due the use of the magnetic recovery winding. The main drawback is that the bifilar winding is not economical for large motors. The voltage across $Q_{1}$ at turn off is $V_{S}+a V_{S}$, where ' $a$ ' is the turns ratio between the primary and secondary winding, requiring the switch to have a higher voltage rating that consequently results in greater power losses. Another limitation is that the coupling is never perfect and snubber circuits are required to limit the transient voltages. This adds cost and complexity to what is otherwise a simple configuration. The bifilar winding also decreases the efficiency of the system due to the poor copper utilization from the reduced winding area available for the main winding. Soft-switching is not possible as there is no freewheeling condition.

### 3.4.2 Auxiliary Commutation Winding Converter

This converter also requires that the motor must have an auxiliary winding (Liang 1994) as illustrated in Figure 3.18a. This circuit has four possible states: energization and freewheeling of the main winding are the first two states. The next state is the demagnetization of the main winding to the auxiliary winding and the final state is
demagnetization of the excess energy in the main winding to the source. The magnetization and freewheeling of the main winding is implemented using a conventional converter like an asymmetrical half bridge, which facilitates switching between positive and zero voltage loops as illustrated in Figure 3.18b and Figure 3.18c respectively. The demagnetization of the main winding to the auxiliary winding is implemented through magnetic coupling as illustrated in Figure 3.18d. During the negative voltage loop the diode, $\mathrm{D}_{2}$, is forward biased, which allows current to circulate in the auxiliary winding. The demagnetization of the excess energy the main winding to the source is illustrated in Figure 3.18d, while during this period the current freewheels in the auxiliary winding. During the magnetization of the next phase winding, the positive voltage loop allows the magnetic energy of the auxiliary winding to couple to the main winding to allow the current to build up rapidly.


Figure 3.18: The auxiliary winding converter. (a) Static view of converter. (b) Magnetization state (c) Freewheeling state (d) Demagnetization to auxiliary winding and to dc-link

The main advantages are that the magnetic energy is recovered in the auxiliary winding and therefore increases the performance of the system. Another benefit is that current is allowed to rapidly build up in the phase winding using the stored magnetic energy of the auxiliary winding. This circuit also allows for soft-switching capability. The main disadvantage is the extra cost for an SRM with the auxiliary winding.

### 3.5 Dissipative Converters

As the name suggests, these converters do not recover the magnetic stored energy in the phase winding, but instead dispel all the energy. The most fundamental type of dissipative converter is the R-dump converter (Barnes 1998) (Krishnan, 1990). It has two variants known as the decay type converter and a modified version of the decay converter.

### 3.5.1 R dump converter

This converter configuration consists of a single switch and single diode per phase winding in the SRM as indicated in Figure 3.19a (Krishnan 1990). It can only operate in hard-switching mode with the capability for only two states: magnetization and demagnetization.


Figure 3.19: The R-dump converter. (a) Static view of converter. (b) Magnetization state (c) Demagnetization to the dump resistor, $\mathrm{R}_{\mathrm{d}}$

During magnetization, the switch, $\mathrm{Q}_{1}$, turns on and current flows in the phase winding as illustrated in Figure 3.19b. The demagnetization commences when $\mathrm{Q}_{1}$ turns off and the phase current freewheels through the diode, $\mathrm{D}_{1}$, charging the capacitor, $\mathrm{C}_{1}$, and later flows through the dump resistor, $\mathrm{R}_{\mathrm{d}}$ as shown in Figure 3.19c. The detailed waveforms for the circuit operation are provided in Figure 3.20.


Figure 3.20: Waveforms for the R-dump converter circuit

At low power levels, the simplicity, low cost and low semiconductor component count of the converter may outweigh the loss in drive efficiency. Another advantage is that only grounded gate drive circuits are required, which further reducing converter costs. The main limitation is that this type of converter is impractical for high power applications as the dissipation of stored energy would substantially reduce the drive efficiency. Other limitations are that the negative voltage drop tends to decrease as current decreases, and the inability to apply zero volts across the voltage winding during current conduction.

There are two variations on the R -dump circuit; the first provides a switch, $\mathrm{Q}_{\mathrm{a}}$, in parallel the dump resistor as illustrated in Figure 3.21a (Barnes 1998). This circuit is called the decay converter and it provides for a zero-voltage loop and therefore the possibility of soft-switching operation. Another version of the decay circuit adds another switch, $\mathrm{Q}_{\mathrm{b}}$, and diode, $\mathrm{D}_{\mathrm{b}}$, and this allows for one voltage loop to operate in
freewheeling mode, while another phase is in demagnetization mode as shown in Figure 3.21b (Barnes 1998).


Figure 3.21: (a) Static view of the decay converter. (b) The modified version of a dual decay converter

### 3.6 Self-Commutating Converters

These converters use various techniques to commutate between the phase-windings of the SRM. There are a number of different converter schemes to implement self commutation that include: the series resonant converter, the zero-voltage transition (ZVT) PWM converter, the auxiliary quasi-resonant dc-link (AQRDCL) converter, the current source converter and the H -bridge converter. Even though these designs are old they are included for completeness of this review.

### 3.6.1 Series resonant converter

The semiconductor devices switch at zero in this converter due to the partially resonating nature of the circuit (Park 1992) as illustrated in Figure 3.22a. This circuit has two fundamental modes of operation: magnetization and demagnetization. During energization of the phase winding, $\mathrm{SCR}_{1}, \mathrm{SCR}_{2}$ and $\mathrm{S}_{1}$ are turned on and this causes the capacitor, $\mathrm{C}_{1}$, to overcharge, which in turn forces the current in the inductor, $\mathrm{L}_{\mathrm{a}}$, to zero as illustrated in Figure 3.22b. Then $\mathrm{SCR}_{1}, \mathrm{SCR}_{2}$ and $\mathrm{S}_{1}$ turn off and the phase current continues to flow, until $\mathrm{C}_{1}$ is negatively charged. Then $\mathrm{S}_{1}$ turns on and the demagnetization current flows via the diodes, $\mathrm{D}_{1}$ and $\mathrm{D}_{1}$, to return energy to the dc link. The main advantage is that switching at zero volts reduces the losses and the stresses in the switching components. The main limitation is that the component count is high, increasing overall system cost.


Figure 3.22: The series resonant converter. (a) Static view of converter. (b) Magnetization state (c) Demagnetization to the dump resistor, $\mathrm{R}_{\mathrm{d}}$

Additional resonant converters include the zero-voltage transition (ZVT) PWM converter (Park 1992) illustrated in Figure 3.23a and the auxiliary quasi-resonant dclink (AQRDCL) (De Doncker 1991) illustrated in Figure 3.23b. The dc link voltage in the ZVT PWM converter is regulated using a chopping switch, $\mathrm{S}_{\mathrm{a}}$, that is commutated at zero voltage through the action of a sub circuit comprising of a resonant tank, $L_{r}$ and $C_{r}$, and an auxiliary switch, $\mathrm{S}_{\mathrm{b}}$, that is hard switched. There are conduction losses due to the chopping switch and some limitations on independent current control of the phase windings.


Figure 3.23: (a) The ZVT PWM converter, (b) and the AQRDCL converter

The AQRDCL converter uses a resonant circuit to allow for the transition of the main switches to occur at zero volts to further reduce switching losses. The main limitations are the additional conduction losses in the resonant circuit switches and limitations in independent control of the phases due to the zero voltage switching.

### 3.6.2 H-Bridge Converter

In the H-bridge circuit, two phases must always carry current. The circuit is configured as illustrated in Figure 3.24a (Corda 1991). There are three stages of operation. In the first state, the top left switch, $\mathrm{Q}_{1}$, and the bottom-left switch, $\mathrm{Q}_{3}$, turn on and current conducts through the top-left (phase 1) and bottom-left (phase 3) phase windings as seen in Figure 3.24b. In the second stage, when $\mathrm{Q}_{1}$ turns off, the bottom-left diode, $\mathrm{D}_{3}$, and the top-right switch, $\mathrm{Q}_{2}$, turns on so that the sum of the current flowing in the top two phase winding remains at a constant value as indicated in Figure 3.24c. The third stage consists of the $\mathrm{Q}_{3}$ turning off and $\mathrm{Q}_{4}$ turning on to maintain a constant current through phase 2 and phase 4 , while $D_{1}$ and $D_{3}$ becomes forward bias to demagnetize phase 1 and phase 3 as illustrated in Figure 3.24d. The fourth stage consists of $\mathrm{Q}_{2}$ turning off, while the diode, $\mathrm{D}_{4}$, and the switch, $\mathrm{Q}_{1}$, turns on so that the sum of the currents flowing in the top two phase winding remains at a constant value as indicated in Figure 3.24e. The final stage consists of $\mathrm{Q}_{4}$ turning off and $\mathrm{Q}_{3}$ turning on again to maintain a constant current through phase 1 and phase 3 , while $D_{2}$ and $D_{4}$ becomes forward bias to demagnetize phase 2 and phase 4 as illustrated in Figure 3.24f. The main advantage is this configuration allows for one switch and one diode per phase and thereby reducing converter component costs. The main limitation is that current cannot flow in only one phase and therefore prevents independent phase control. This converter configuration requires that the machine design must consist of multiples of four phases.


Figure 3.24: The H -bridge converter. (a) Static view of converter. (b) Stage 1 (c) Stage 2 (d) Stage3 (e) Stage 4 (f) Stage5

### 3.7 Converter selection

In this application where the SRM is implementing automotive starter and alternator functions, there is a requirement for maximum flexibility of converter topology design to achieve those key objectives, converter efficiency is of critical importance, as is independence of converter phase operation in order to maximise control strategy options. Circuit complexity and consequently cost is another key consideration.

The magnetic energy recovery converters that require an SRM with a bifilar or auxiliary winding can be eliminated as the SRM that is used in this application is not of this type. As efficiency is of critical importance, the dissipation converter topologies are not suitable as the power requirements for the SRM are quite large. Of the bridge converter topologies, the shared switch converter is also unsuitable as the conduction losses in the switching device in series with the phase winding would have a significant effect on efficiency. Independent control of phase windings during motoring and generating
modes of operation prohibits the use of the shared winding, the shared switch, the splitdc , and the H -bridge converters.

Minimising circuit complexity and therefore the converter cost is also an important consideration, so the resonant converters, the auxiliary and the sequential converters are eliminated for this reason, as the component count is high in these converters. The series and parallel dc-link converters are also eliminated due to the circuit complexity, as these circuits have essentially a voltage boost front end on a bridge converter. The AQRDCL converter is also be ignored for the same reasons as the dc-link converters above but also due to the reduced efficiency incurred by the passive components in the resonant circuit outweighing the theoretical zero switching losses under resonant operation The C-dump is discarded mainly on the grounds of circuit complexity contributing to extra converter costs and there are additional losses due to energy recovery circuit. The Sood converter is discarded due to the potential costs of implementing the complex control may outweigh the reduced component count.

The buck-boost converter potentially offers significant advantages under generating operation with the capability of provide magnetization voltages greater the supply voltage. This and the reduced number of switching components per phase must be weighed against the potential inefficiency of using switching devices with a higher voltage rating and the additional losses incurred by the passive components in the chopper circuit. This leaves the asymmetrical half-bridge and full-bridge converters as the circuits that provide maximum flexibility, potentially high efficiency levels, and provides full independence over all ranges of operation. These converters are analysed in the next chapter to determine the most suitable circuit to carry to the final converter design stage. If variable input voltage is necessary for improved range of operation in the SRM drive, a buck-boost front end can be added to the circuit at a later stage.

## Chapter 4 - Preliminary Analyses

In order to design an efficient converter for SRM motoring and generating modes of operation, power switching components were selected and evaluated to maximise efficiency and reliability and minimise cost. To identify suitable components to evaluate, the operating conditions were first defined in which these devices needed to function. The efficiency of the components and the converter configuration options were then determined through power analysis. The components were first evaluated on the half-bridge converter and then on the full-bridge converter. The MOSFET reverse recovery times were evaluated through simulation and experimental analysis in order to evaluate worse-case operation for implementation as synchronous rectifiers in the fullbridge converter. The most efficient converter configuration was determined during this assessment and the final selection was matched with the optimum components for this application.

### 4.1 Operating Conditions

The operating conditions for the SRM converter are determined by the specifications of the SRM and the application (i.e. it must function as an automotive ISG). The SRM specification defined the peak power and peak current requirements. The application specifications include: the performance conditions for the ISG, the operating environment of the ISG in which the converter must function, the worst case conduction periods and duty cycles for motoring and generating, and automotive electrical parameter limits.

The performance conditions in this situation are the modes and speeds at which the SRM operates as an automotive ISG; these modes are: starting, low speed motoring, low speed generating and high speed generating. The speed range for each mode determines the conducting periods and the duty cycles of operation for the switching devices, and the voltage and current requirements.

The application also determines the operating environment that is encountered by the converter and therefore by the switching devices, which includes temperature extremes and cycles and varying levels of vibration.

The automotive electrical parameter limits defined the voltage and current limits used to specify and completely evaluate the switching components. Safety margins were defined for the voltage and current ratings. Limits were provided for other parameters including MOSFET on-resistance, diode forward voltage, reverse recovery time, $\mathrm{t}_{\mathrm{rr}}$, of diodes and synchronous rectifier MOSFETs, and finally, for the case and junction temperature limits. This allowed for the evaluation of different switching devices and converter configurations in order to achieve the most efficient solution, and consequently defined the requirements for the heat sinks, gate drive circuitry, filter capacitors and the choice and configuration of the high current conductors.

### 4.1.1 SRM Specifications

Initially a two phase machine was proposed for the ISG but unfortunately it proved impossible to obtain and no alternative vendors could be found to supply an equivalent off-the-shelf 2-phase unit. The SRM that is used in this application is a four phase unit with eight stator poles and six rotor poles as this satisfies the required voltage and power rating A summary of the specifications for the machine is provided in Table 4.1 [(Motion System Tech 2002) and (Chapmore Controls Ltd. 2007)].

| Phases | 4 | Aligned inductance $\left(\mathrm{L}_{\mathrm{a}}\right)(\mu \mathrm{H})$ | 334 |
| :--- | :---: | :--- | :---: |
| Stator poles | 8 | Phase winding resistance $(\mathrm{m} \Omega)$ | 8 |
| Rotor poles | 6 | Maximum speed (rpm) | 15000 |
| Power rating $(\mathrm{W})$ | 3500 | Base speed (rpm) | 6000 |
| Rated voltage $(\mathrm{V})$ | 48 | Rated torque $(\mathrm{Nm})$ | 5.48 |
| Rated Current $(\operatorname{Avg})(\mathrm{A})$ | 84 | Peak torque $(\mathrm{Nm})$ | 10.7 |
| Unaligned inductance $\left(\mathrm{L}_{\mathrm{u}}\right)(\mu \mathrm{H})$ | 47 | Weight $(\mathrm{kg})$ | 15 |

Table 4.1: SRM specifications

### 4.1.2 Performance Conditions

The ISG operates in four possible modes: starting, low speed motoring, low speed generating and high speed generating. Typical starter motor and alternator specifications in standard automobiles are illustrated in Table 4.2 for starter motors [(Visteon 2005a), (Visteon 2005b) and (Visteon 2005c)] and Table 4.3 for alternators [(Bosch 2008)].

| Type | Power range | Stall torque | Current | Efficiency | Mass |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | $0.8-1.0 \mathrm{~kW}$ | 11 Nm | 175A @ 5Nm | 61\% @ 5Nm | 3.5 kg |
| 2 | $1.0-1.7 \mathrm{~kW}$ | $15-28 \mathrm{Nm}$ | 160-220A @ 5Nm | 71\% @ 5Nm | $2.6-3.2 \mathrm{~kg}$ |
| 3 | $1.7-2.5 \mathrm{~kW}$ | 36-42Nm | 400A @ 15Nm | 70\% @ 15Nm | $3.9-4.1 \mathrm{~kg}$ |
| Note |  |  |  |  |  |
| Type 1 s Type 2 s Type 3 | er for 4-cylind er for 4 to 8 cy er for 4-cylind | r petrol (1.0L inder petrol ( r diesel (up to | o 1.6 L$)$ and diesel 4L to 4.0 L$)$ and die $2.5 \mathrm{~L})$ engines | el (to 1.4 L ) eng | ngines |

Table 4.2: Typical starter motor specifications for standard automobile

| Power range | Min Current | Max. Current | Mass |
| :--- | :---: | :---: | :---: |
| $1.1-2.1 \mathrm{~kW}$ | $45-82 \mathrm{~A}$ | $80-155 \mathrm{~A}$ | $4.7-6.4 \mathrm{~kg}$ |
| Note <br> Minimum current available @ 1800 RPM <br> Maximum current available @ 6000 RPM |  |  |  |
| $l$ |  |  |  |

Table 4.3: Typical alternator specifications for standard automobile

Starting is the primary motoring mode of operation for the ISG, typically in the engine speed range of $100-200 \mathrm{rpm}$ for current vehicle engines with equivalent power capabilities in the range of 0.8-2.5kW [(Bosch 2000), (Visteon 2005a), (Visteon 2005b) and (Visteon 2005c)]. Low speed motoring applies to start-stop or idle-stop mode of operation that would be in the range of 500-1000 rpm [(Service Tech Magazine 2001) and (Albertoni, L et al 2003)]. Generating at low speed provides a reduced power output, equivalent to the maximum power of $1.1 \mathrm{~kW}-2.1 \mathrm{~kW}$ for current generators, and operates at engine speeds in the region of $1000 \mathrm{rpm}-2000 \mathrm{rpm}$ (Bosch 2008). High speed generating is defined for an engine speed range of $2000-3000 \mathrm{rpm}$ and is capable of providing up to 3.5 kW as a standard generator or through regenerative braking. At very high speeds, $3000-6000 \mathrm{rpm}$, the ISG would be disabled to provide maximum vehicle acceleration. It was assumed that the SRM rotor would rotate twice for each engine revolution as this would utilize almost the full SRM speed range and provide increased torque handling capability for the given ISG package size. The operating speeds of the SRM for each mode of operation are illustrated in Table 4.4. An illustration of a potential implementation of the ISG in an automotive environment is shown in Figure 4.1 and a description of each mode of operation is provided in Figure 4.2.

| Specification |  | Starting | Low speed | Low speed | High speed |
| :--- | :---: | :---: | :---: | :---: | :---: |
|  |  |  | motoring | generating | generating |
| Min. speed | $(\mathrm{rpm})$ | 200 | 1000 | 2000 | 4500 |
| Max. speed | $(\mathrm{rpm})$ | 400 | 2000 | 4500 | 6000 |

Table 4.4: Worst case ISG operating speeds


Figure 4.1: ISG automobile layout


Figure 4.2: ISG operation

The ISG implementation would use a belt drive coupling system as illustrated in Figure 4.1 and the configuration is similar to systems what has been implemented by a number of manufacturers [(Delphi 2008), (Visteon 2003) and (Teratani et al 2003)]. The ISG would be part of a 42 V power supply system that uses a 36 V battery (Teratani et al 2003). This system would easily integrate into existing powertrain and would still achieve the benefits of stop/start mode, regenerative braking and potentially launch assistance. A solenoid clutch would be connected between the engine crankshaft and crank pulley and would engage and disengage on command when the various operating modes were implemented as illustrated in Figure 4.2.

### 4.1.3 Operating Environment

The automotive engine compartment represents a particularly harsh environment for automotive electronics (Myers 2003). This includes extreme temperature variations leading to thermal cycle or thermal shock (>1000 cycles), vibration (up to 10 Grms ), exposure to dirt, moisture, chemicals and gases, external noises and electrostatic discharge. The extremes in ambient temperature $\left(-40^{\circ} \mathrm{C}\right.$ to $\left.150^{\circ} \mathrm{C}\right)$ are perhaps the most difficult challenge to address. Figure 4.3 shows a typical automotive operating environment (Myers 2003).


Figure 4.3: Automotive Operating Environment

Applications that have high power dissipation represent the greatest challenge to electronic cooling systems design. Motor control electronic modules must be able to operate in ambient temperatures up to $150^{\circ} \mathrm{C}$. This provides a significant challenge to the reliability of the design, especially considering the requirement for faultless operation in all weather conditions for 10 years or more (Myers 2003).

The ambient temperature requirements for the converter in this application are defined as $-40^{\circ} \mathrm{C}$ to $100^{\circ} \mathrm{C}$ by locating the converter low down and at the front of the engine to maximise cool airflow or use water cooling to maximise heat transfer. The ambient temperature experienced by the ISG during cold starting is defined to be $-40^{\circ} \mathrm{C}$ to $45^{\circ} \mathrm{C}$, while during other modes of operation would experience the full temperature range. For power analysis, the upper temperature is of greatest importance. The proposed worstcase temperatures to be experienced by the converter under the different modes of operation of the ISG are shown in Table 4.5 (at the end of section 4.1)

### 4.1.4 Conduction Periods and Duty Cycles

A detailed analysis used to determine the conduction intervals during starting, low speed motoring, and low and high speed generating operation is presented in the following sections, and the details for each speed is provided in Table 4.5 (at the end of section 4.1). It is assumed that the worst case speed of operation for the ISG would be 200 rpm for starting, 1000rpm for low speed motoring, 2000rpm for low speed generating and 4500rpm for high speed generating. These speeds yield the maximum conduction intervals for each mode of operation of the ISG.

A typical circuit schematic for a single phase SRM converter is shown in Figure 4.4. The duration over which a phase winding becomes active and repeats the cycle again is defined in this application to be the conduction period. The active interval is then defined to be the conduction duty cycle, $D_{C}$. These definitions are illustrated for starting and low speed motoring, low speed generating and finally high speed generating in Figures $4.5 \mathrm{a}, 4.5 \mathrm{~b}$ and 4.6 , respectively.


Figure 4.4: Single Phase SRM Converter

### 4.1.4.1 Starting and low speed motoring

During starting and low speed motoring, it is assumed that current is flowing just before and during the entire motoring cycle (region of positive $d L / d \theta$ ) and for a short period after alignment for demagnetisation as indicated by the interval $\theta_{\text {on }}, \theta_{1}, \theta_{2}$ and $\theta_{\text {ext }}$ in Figure 4.5 a . An ISG starting speed of 200 rpm implies that one revolution takes approximately 300 ms . Since the SRM has 6 rotor poles, each phase is energised six times for one complete revolution, which yields a conduction period of 50 ms for each SRM phase.


Figure 4.5: PWM current control for single phase operating at low speed.
(a) Motoring - Soft chopping (b) Generating - Hard chopping

It is assumed there is a maximum conduction duty cycle for motoring mode of $50 \%$. Therefore, the MOSFET, Q2, is on for 25 ms with the switching frequency of the device determined by the SRM operating speed, which under starting conditions is 20 Hz ( 50 ms ). The MOSFET, Q1, is pulse width modulated (PWM) at $25 \mathrm{kHz}-50 \mathrm{kHz}$, depending on audible noise and allowable levels of component switching losses during the commutation duty cycle in order to maintain the phase winding current at its set point value. The PWM duty cycle varies in order to maintain the maximum phase current and here it is assumed an average duty cycle value of $50 \%$, which yields an overall duty cycle for Q1 of $25 \%$. The diode, D1, is on when Q1 is off, and vice versa as part of the freewheeling cycle, yielding an overall duty cycle of $25 \%$, but this device also conducts during the demagnetisation cycle, which is assumed to be $10 \%$ duty cycle at 20 Hz . The diode D2 is only on during the demagnetisation of the phase winding and therefore a $10 \%$ duty cycle at 20 Hz can be assumed. These would be deemed as the worst-case conduction duty cycles for the converter during starting operation. Low speed motoring assumes the same duty cycles as starting but for a speed of 1000 rpm . The specific duty cycles and switching frequencies for each device are provided in Table 4.5 (at the end of section 4.1) and a detailed graphical representation of the current and voltage waveforms for each device is provided in Appendix A.

### 4.1.4.2 Low speed generating

During low speed generating, the worst case scenario would be that conduction would commence in the end of the dead zone (region of zero $d L / d \theta$ ) prior to the generating region (region of negative $d L / d \theta$ ) to allow the current reach a set point and then the generating current regulation would take place during the entire generating region and allowed to extinguish in the following dead zone area as indicated by the interval $\theta_{\mathrm{on}}, \theta_{3}$, $\theta_{4}$ and $\theta_{\text {ext }}$ in Figure 4.5 b. This would result in the worse case duty cycle of approximately $10 \%$ at the end of the previous motoring mode and dead zone, approximately $40 \%$ for generating mode of operation and $10 \%$ during final demagnetisation.

Low speed generating requires current regulation as the magnitude of the back-emf is smaller than the combined magnitude of the applied voltage and resistive voltage drop below the base speed. The SRM low speed generating range is defined where back emf is greater than 0.333 of the DC link voltage and less than the value of the DC link
voltage and therefore the rotor speed is greater than 0.333 of the base speed but less than the base speed (Miller 2001).

Low speed generating uses hard-chopping PWM current regulation and that implies that all devices are operating at the same PWM frequency with the average duty cycle assumed to be $50 \%$. This points to an overall duty cycle of $25 \%$ for all the devices over the conduction period. D1 and D2 are on for an additional $10 \%$ for demagnetization. The specific duty cycles and switching frequencies for each device are provided in Table 4.5 (at the end of section 4.1) and a detailed graphical representation of the current and voltage waveforms for each device is provided in Appendix A.

### 4.1.4.3 High speed generating

High speed generating is implemented through single pulse operation and conduction commences in the motoring mode of operation to allow the current in the phase winding to reach the desired value. It remains constant through the generating region until overlap occurs at minimum inductance at which point it tails off to zero in the dead zone as illustrated by the interval $\theta_{\text {on }}, \theta_{2}, \theta_{3}, \theta_{\text {off }}, \theta_{4}$ and $\theta_{\text {ext }}$ in Figure 4.6.

At the base-speed, the generating current is approximately constant due to the source voltage being approximately equal to the back-emf. The source voltage is 42 Vdc during generating at an ISG operating speed range of 4500rpm - 6000rpm and consequently provides maximum generating power capability over normal automotive engine cruising speed. The generator output is assumed to be disabled above 6000rpm.

The worst case high speed generating occurs for 42 Vdc at 4500 rpm and the worst case duty cycles are $40 \%$ in motoring mode and $30 \%$ in generating mode and a further $10 \%$ for demagnetisation. The switching frequencies and associated duty cycles for the switching devices at 4500rpm are provided in Table 4.5 (at the end of section 4.1) and a detailed graphical representation of the current and voltage waveforms for each device is provided in Appendix A .


Figure 4.6: Single pulse control for single phase generating at high speed

### 4.1.5 Automotive Electrical Parameter Limits

As noted previously, a 36 Vdc battery is used in this 42 Vdc power supply system [(Service Tech Magazine 2001) and (Teratani et al 2003)]. According to the SRM specifications [(Motion System Tech 2002) and (Chapmore Controls Ltd. 2007)], the peak power capability is 5900 W at 6000 rpm at the rated voltage of 42 Vdc , which implies a peak current, $\mathrm{I}_{\mathrm{m}}$, of 140A.

Based on the above criteria, it is possible to define the electrical requirements at the various engine speeds. Under cold starting conditions the available battery voltage is 36 Vdc , which assuming a peak current capability of 140A available to the SRM phase winding during initial engine start-up. During SRM low speed motoring for start-stop operation, it is assumed that up to 42 Vdc is available and the current values are the same as start-up. During low and high speed generating, the peak voltage and peak current are assumed to be 42 Vdc and 140 A , respectively.

A safety margin was assumed for all specifications. With an operating voltage of 42 Vdc , and assuming a safety margin of $50 \%$, a minimum voltage rating of 63 Vdc is required for the power semiconductors. The peak operating current rating is 140 A , and assuming a safety margin of $25 \%$, this yields a peak current rating of 175 A . The onresistance of all MOSFETs and the forward voltage of the diodes must be as low as possible in order to maximise efficiency. The reverse recovery time, $\mathrm{t}_{\mathrm{rr}}$, specification of 120 ns is based on the average value from the ten most suitable diodes available that meet the voltage and current specifications [(Microsemi 2004), (International Rectifier 1997), (IXYS 2003), (STMicroelectronics 2004), (Fairchild 2002b)]. The case temperature of a power semiconductor can range from $90^{\circ} \mathrm{C}$ to $110^{\circ} \mathrm{C}$ in practice (International Rectifier 2005a). An upper value of case temperature was used in this application. A summary of the electrical requirements is given in Table 4.5.


Table 4.5: SRM Worst Case Operating Conditions

### 4.2 Switching Component Analysis

Evaluation of the most efficient component options was central to determining the final converter configuration for motoring and generating operation. A number of suitable component options were selected from the vendor documentation. A power analysis was implemented with each converter configuration using what is deemed to be the most efficient devices from the specifications. The final converter configuration was selected from this analysis and then devices from a number of vendors were evaluated in order to determine the most efficient device and converter combination.

Since the SRM is capable of efficiency levels greater than $90 \%$ (Chapmore Controls Ltd. 2007), it is imperative that the converter circuit be equally efficient in order to maximise the advantages of this motor configuration. The analysis was conducted on three converter configurations: asymmetric half-bridge converter, the full-bridge synchronous rectifier converter with single components and the same full-bridge configuration with a number of switching components mounted in parallel, as illustrated in Figure 4.7(a), (b) and (c) respectively. The first case for analysis consists of two MOSFETs and two diodes per phase winding, while in the second case the diodes are replaced with MOSFETs to implement synchronous rectification. In the third and final case each MOSFET is replaced with a number of lower current rated MOSFETs connected in parallel and is defined as the parallel configuration.


Figure 4.7: (a) Asymmetric half-bridge converter, (b) full-bridge synchronous rectifier converter with single components and (c) full-bridge synchronous rectifier with switching components mounted in parallel

The power analysis was implemented for motoring operation at two speeds, 200rpm and 1000 rpm , and for generating operation at two speeds, 2000rpm and 6000 rpm . Detailed
power calculations are presented for the starting speed (200rpm) of the asymmetrical half-bridge converter, while the power calculations for the other speeds were implemented using spreadsheet program. Appendix A provides a complete analysis of the switching waveforms for each component of the asymmetrical half-bridge converter and the full-bridge synchronous rectification converter for each converter mode (magnetisation, freewheeling or demagnetisation) and at each ISG mode of operation (starting, low speed motoring, low and high speed generating) and was used to select the relevant equations for the power calculations, while the parameter values for each component is provided in Table 4.5 at the end of section 4.1. A summary of the efficiency calculations for all three converter configurations and suitable component options for all ISG modes of operation is provided in Table 4.9 (at the end of section 4.2) and the full power analysis results are provided in Appendix B. The most efficient components were then evaluated for reverse recover time specification under simulated conditions. Short-listed components from the simulation study were electrically tested in order to determine final selection.

### 4.2.1 Asymmetric Half-bridge Converter

The most suitable MOSFET (Q1 and Q2) and diode (D1 and D2) for this application was the Advanced Power Technology APT20M11JFLL (Advanced Power Technology 2004) and the ST Microelectronics STTH20002TV (ST Microelectronics 2004) respectively. The power calculations were implemented according to the analysis for conduction and switching losses that is provided in Appendix A. The procedure for the power analysis was divided into three stages, (i) the power calculations for each power semiconductor, (ii) the total power dissipation was implemented for a single phase converter and (iii) the efficiency was evaluated to determine if it was $\geq 90 \%$. A detailed set of calculations is presented for the SRM starting speed, to illustrate the process and a summary is provided for the other operating speeds. The power analysis calculations were generated using a spreadsheet program to evaluate the various operating conditions and the efficiency results are provided in Table 4.9 at the end of section 4.2.

The power dissipation of the MOSFET, Q1, consists of conduction losses and switching losses. The conduction losses depends on the value of its on-resistance ( $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ ) and this value must be derated by the on-resistance temperature coefficient. The onresistance temperature coefficient for maximum junction temperature was assumed to be the worst-case condition. A summary of the relevant data from the component
specifications (Advanced Power Technology 2004) and operating conditions to implement the power analysis that follows is provided in Table 4.6. It was assumed that the worst case rise $\left(\mathrm{t}_{\mathrm{r}}\right)$ and fall $\left(\mathrm{t}_{\mathrm{f}}\right)$ times of the MOSFET to be 10 times greater than the value in the specifications as a rule of thumb (Sweeney 2002). The power analysis for Q1 and Q2 under ISG starting mode of operation is implemented according to the analysis described in section A3 of Appendix A.

| $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ | 11 mW |
| :---: | :---: |
| thermal coefficient for $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ at $\mathrm{T}_{\mathrm{J}}=150^{\circ} \mathrm{C}$ | 2.25 |
| $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ at $\mathrm{T}_{\mathrm{J}}=150^{\circ} \mathrm{C}, \mathrm{R}_{\mathrm{DS}(\mathrm{ON}) \mathrm{HOT}}$ | $25 \mathrm{~m} \Omega$ |
| $\mathrm{t}_{\mathrm{r}}$ | 50 ns |
| $\mathrm{t}_{\mathrm{f}}$ | 100 ns |
| Worst case $\mathrm{t}_{\mathrm{r}}, \mathrm{t}_{\mathrm{r}(\mathrm{wc})}$ | $0.5 \mu \mathrm{~s}$ |
| Worst case $\mathrm{t}_{\mathrm{f}}, \mathrm{t}_{\mathrm{f}(\mathrm{wc})}$ | $1 \mu \mathrm{~S}$ |
| $\mathrm{t}_{\mathrm{rr}}$ | 500 ns |
| Peak current, $\mathrm{I}_{\mathrm{m}}$ | 140 A |
| Minimum switching frequency, $\mathrm{f}_{\mathrm{s}(\mathrm{Q} 1)}$ | 25 kHz |
| Switching duty cycle $\left(\mathrm{D}_{\mathrm{SW}}\right)$ | $25 \%$ |
| Commutation duty cycle $\left(\mathrm{D}_{\mathrm{COM}}\right)$ | $50 \%$ |
| Commutation frequency $($ Starting $), \mathrm{f}_{\mathrm{s}(\mathrm{Q} 2)}$ | 20 Hz |
| Demagnetisation duty cycle $\left(\mathrm{D}_{\mathrm{DM}}\right)$ | $10 \%$ |
| $\mathrm{~V}_{\mathrm{DS}(\mathrm{Q} 1)}=\mathrm{V}_{\mathrm{DS}(\mathrm{Q} 2)}=\mathrm{V}_{\mathrm{DC}}$ | 36 V |
| $\mathrm{~V}_{(\mathrm{D} 1)}=\mathrm{V}_{(\mathrm{D} 2)}=\mathrm{V}_{\mathrm{F}}$ | 1.8 V |

Table 4.6: Component specifications and operating conditions for power analysis

The conduction power losses are determined as follows:

$$
\begin{equation*}
P_{C\left(Q_{1}\right)}=\left(I_{R M S\left(Q_{1}\right)}\right)^{2} * R_{d s(O N) H O T} \tag{4.3}
\end{equation*}
$$

where

$$
\begin{align*}
& I_{R M S(Q 1)}=I_{m} \sqrt{D_{S W}}  \tag{4.4}\\
& I_{R M S(Q 1)}=70 \mathrm{~A}
\end{align*}
$$

Therefore:

$$
P_{C(Q 1)}=121 \mathrm{~W}
$$

The switching transition power losses are:

$$
\begin{align*}
& P_{S(Q 1)}=\frac{V_{D S(Q 1)} * I_{m}}{2} *\left(t_{r(w c)}+t_{f(w c)}\right) * f_{s(Q 1)}  \tag{4.5}\\
& P_{S(Q 1)}=95 W
\end{align*}
$$

Total power dissipation for this device, $\mathrm{P}_{\mathrm{T}(\mathrm{Q})}$, is the sum of the conduction losses, $\mathrm{P}_{\mathrm{C}_{(\mathrm{Q} 1)}}$, and the switching losses, $\mathrm{P}_{\mathrm{S}(\mathrm{Q} 1)}$.

$$
\begin{align*}
& \mathrm{P}_{\mathrm{T}(\mathrm{Q} 1)}=\mathrm{P}_{\mathrm{C}(\mathrm{Q} 1)}+\mathrm{P}_{\mathrm{S}(\mathrm{Q} 1)}  \tag{4.6}\\
& \mathrm{P}_{\mathrm{T}(\mathrm{Q} 1)}=216 \mathrm{~W}
\end{align*}
$$

The power dissipation of the MOSFET, Q2, consists of conduction losses and switching losses. In this case, the commutation duty cycle, $\mathrm{D}_{\mathrm{C}}$, is $50 \%$ and the switching losses also occur at the commutation frequency, $\mathrm{f}_{\mathrm{s}(\mathrm{Q} 2)}$, of 20 Hz , otherwise the component data is the as in Table 4.4. The conduction power losses are determined as follows:

$$
I_{R M S(Q 2)}=99 A
$$

Therefore:

$$
P_{C(Q 2)}=243 \mathrm{~W}
$$

The switching transition power losses are:

$$
P_{S_{(Q 2)}}=76 \mathrm{~mW} \text { (negligible) }
$$

Total power dissipation for this device, $\mathrm{P}_{\mathrm{T}(\mathrm{Q} 2)}$, is the sum of the conduction losses, $\mathrm{P}_{\mathrm{C}(\mathrm{Q} 2)}$, and the switching losses, $\mathrm{P}_{\mathrm{S}(\mathrm{Q} 2)}$.

$$
\mathrm{P}_{\mathrm{T}\left(\mathrm{Q}_{2}\right)}=243 \mathrm{~W}
$$

The losses of the diode, D1, occur in two regions: (I) freewheeling and (II) demagnetisation. A summary of the relevant data from the specifications (ST Microelectronics 2004) and the operating conditions to implement the power calculations is provided in Table 4.7. The power analysis for D1 and D2 under starting speed of operation was implemented according to the analysis from Appendix A.

| Worst case forward voltage drop $\left(\mathrm{V}_{\mathrm{F}}\right)$ | 1.8 V |
| :---: | :---: |
| Peak current, $\mathrm{I}_{m}$ | 140 A |
| $\mathrm{~V}_{\mathrm{R}}=\mathrm{V}_{\mathrm{S}}$ | 36 V |
| $\mathrm{Q}_{\mathrm{rr}} @ \mathrm{~T}_{\mathrm{J}}=125^{\circ} \mathrm{C}$ and $@ \mathrm{di}_{\mathrm{F}} / \mathrm{dt}=100 \mathrm{~A} / \mathrm{uS}$ | 275 nC |
| $\mathrm{t}_{\mathrm{rr}}$ | 85 nS |
| Minimum switching frequency, $\mathrm{f}_{\mathrm{sw}}$ | 25 kHz |
| Freewheeling duty cycle $\left(\mathrm{D}_{\mathrm{F}}\right)$ | $25 \%$ |
| Commutation frequency $($ Starting $), \mathrm{f}_{\mathrm{c}}$ | 20 Hz |
| Demagnetisation duty cycle $\left(\mathrm{D}_{\mathrm{DM}}\right)$ | $10 \%$ |

Table 4.7: Component specifications and operating conditions for power analysis
(I) Freewheeling

The conduction power losses during freewheeling, $\mathrm{P}_{\mathrm{CF}(\mathrm{D} 1)}$, are determined as follows:

$$
\begin{align*}
& P_{C F(D 1)}=I_{m(D 1)} * V_{F} * D_{S W}  \tag{4.7}\\
& P_{C F(D 1)}=63 \mathrm{~W}
\end{align*}
$$

The switching transition power losses during freewheeling, $\mathrm{P}_{\mathrm{SWF}(\mathrm{D}) \text {, }}$, are determined as follows:

$$
\begin{align*}
& P_{S F(D 1)}=Q_{r r(D 1)} * V_{R} * f_{s w}  \tag{4.8}\\
& \left.P_{S F(D 1)}=250 m W \quad \text { (negligible }\right)
\end{align*}
$$

(I) Demagnetisation

The conduction power losses during demagnetisation, $\mathrm{P}_{\mathrm{CDM}(\mathrm{D} 1) \text {, are determined as }}$ follows:

$$
\begin{equation*}
I_{m(D 1)}=0.5 * I_{m} \tag{4.9}
\end{equation*}
$$

The current waveform during demagnetisation is of a triangular shape; therefore the output current is approximately half during this interval.

$$
I_{m(D)}=70 \mathrm{~A}
$$

Therefore:

$$
P_{C D M(D 1)}=13 \mathrm{~W}
$$

The switching transition power losses during demagnetisation, $\mathrm{P}_{\text {SWDM(Dl) }}$, are determined as follows:

$$
P_{S D M(D 1)}=200 u W \text { (negligible) }
$$

Total power dissipation for this device, $\mathrm{P}_{\mathrm{T}(\mathrm{D} 1)}$, is the sum of the conduction losses, $\mathrm{P}_{\mathrm{CF}(\mathrm{D} 1)}$, and switching losses, $\mathrm{P}_{\mathrm{SWF}(\mathrm{D} 1)}$, during freewheeling, and the conduction losses $\mathrm{P}_{\mathrm{CDM}(\mathrm{D1})}$, and switching losses, $\mathrm{P}_{\mathrm{SWDM}(\mathrm{Dl} 1)}$, during demagnetisation.

$$
\begin{align*}
& \mathrm{P}_{\mathrm{T}(\mathrm{D} 1)}=\mathrm{P}_{\mathrm{CF}(\mathrm{D} 1)}+\mathrm{P}_{\mathrm{SF}(\mathrm{D} 1)+}+\mathrm{P}_{\mathrm{CDM}(\mathrm{D} 1)}+\mathrm{P}_{\mathrm{SDM}(\mathrm{D} 1)}  \tag{4.10}\\
& \mathrm{P}_{\mathrm{T}(\mathrm{D} 1)}=76 \mathrm{~W}
\end{align*}
$$

The power dissipation of the diode, D 2 , only occurs during demagnetisation, which is be the same as for the D1 during demagnetisation. Therefore the total power loss for this device is:

$$
\mathrm{P}_{\mathrm{T}(\mathrm{D} 2)}=13 \mathrm{~W}
$$

The power loss for the single phase, $\mathrm{P}_{\mathrm{T}(\mathrm{SP})}$, during starting is the sum of the total power losses incurred by each device.

$$
\begin{align*}
& \mathrm{P}_{\mathrm{T}(\mathrm{SP})}=\mathrm{P}_{\mathrm{T}(\mathrm{Q} 1)}+\mathrm{P}_{\mathrm{T}(\mathrm{Q} 2)}+\mathrm{P}_{\mathrm{T}(\mathrm{D} 1)}+\mathrm{P}_{\mathrm{T}(\mathrm{D} 2)}  \tag{4.11}\\
& \mathrm{P}_{\mathrm{T}(\mathrm{SP})}=550 \mathrm{~W}
\end{align*}
$$

### 4.2.1.1 Efficiency during starting mode

The efficiency during starting mode of operation is implemented as described in A2 of Appendix A. The power transfer occurs in two regions (I) magnetisation and (II) demagnetisation as indicated in Figure 4.8.


Figure 4.8: Phase winding voltage and current waveforms during starting and low speed motoring
(I) Magnetisation

During the interval $t_{0}-t_{1}$, the current is constant with a peak value, $\mathrm{I}_{\mathrm{m}}$, of 140 A and the voltage is a square wave and has a peak value, $V_{S}$, of 36 Vdc and a duty cycle, $\mathrm{D}_{1}$, of $50 \%$. The equation for the average power during demagnetisation $\left(P_{M}\right)$ that was determined in Appendix A is defined as:

$$
\begin{equation*}
P_{M}=0.5 I_{m} V_{S} D_{1} \tag{4.12}
\end{equation*}
$$

The output power during magnetisation is

$$
P_{M}=1260 \mathrm{~W}
$$

(II) Demagnetisation

In the interval $t_{l}-t_{2}$, the voltage is constant with a peak value, $-V_{S}$, of -36 Vdc the current is approximated by a triangular wave and has a peak value, $I_{m}$, of 140 A and a duty cycle, $\mathrm{D}_{2}$, of $10 \%$. The equation for the average power during demagnetisation ( $P_{D M}$ ) is:

$$
\begin{equation*}
P_{D M}=-0.5 V_{S} I_{m} D_{2} \tag{4.13}
\end{equation*}
$$

The power transfer is from the phase winding to the battery so the average power during demagnetisation is:

$$
\begin{equation*}
P_{D M}=-1\left(-0.5 V_{S} I_{m} D_{2}\right)=0.5 V_{S} I_{m} D_{2} \tag{4.14}
\end{equation*}
$$

The output power during magnetisation is

$$
P_{D M}=252 \mathrm{~W}
$$

The total power transfer during staring mode of operation is

$$
\begin{align*}
& P_{\text {phase }}=P_{M}+P_{D M}  \tag{4.15}\\
& P_{\text {phase }}=1512 \mathrm{~W}
\end{align*}
$$

Therefore the efficiency for the converter phase during starting mode of operation is

$$
\begin{align*}
& \eta=\frac{P_{\text {phase }}}{P_{\text {phase }}+P_{T(S P)}}  \tag{4.16}\\
& \eta=73 \%
\end{align*}
$$

The power analysis calculations were repeated for low speed motoring, low speed generating and high speed generating as described in A. 2 of Appendix A and the results generated using a spreadsheet program and the efficiency results for each speed of operation are provided in Table 4.9 at the end of section 4.2, while the detailed power
analysis calculations are provided in Appendix B. From the results, it can be seen that the efficiency for this configuration was $<90 \%$ and was therefore not suitable for the application.

### 4.2.2 Full-bridge Synchronous Rectifier Configuration

The full-bridge synchronous rectification allows for the use of MOSFETs instead of the freewheeling and demagnetisation diodes, which was a large source of power loss [(Mohan 1995a), (STMicroelectronics 2001) and (Excelsys Technologies Ltd 2004)]. The schematic for the converter circuit is shown in Figure 4.9. This scheme reduces the resistive losses during freewheeling and generating modes of operation. Another important characteristic when implementing this configuration is that the reverse recovery time of the MOSFET must be approximately equivalent to that of the diode. The components that are used as synchronous rectifiers are the same devices used in the asymmetric half-bridge converter configuration (Advanced Power Technology 2004). A summary of the specifications for a number of diodes that is tabulated in Table 4.10 in section 4.3 indicates that the reverse recovery time needed to be $\leq 130$ ns. It can also be seen from Table 4.6 that the MOSFET had a reverse recover time of 500 ns and therefore this device would not be suitable for this application.


Figure 4.9: Full-Bridge Synchronous Rectifier

For the sack of completeness, a power analysis study was implemented on this configuration. The power calculations follow the procedure described in A. 3 of Appendix A. The efficiency calculations are provided for each speed of operation in Table 4.9, while the detailed power analysis is provided in Appendix B. As can be seen from the results in Table 4.9, this implementation is less efficient than the asymmetric half-bridge configuration. This is due to Q3 having significant conduction power losses
that do not occur with the diodes in the asymmetric half-bridge configuration. Therefore this scheme is not suitable on two counts, poor efficiency and reverse recovery time.

### 4.2.3 Parallel Configuration

This circuit is a derivative of the full-bridge synchronous rectifier scheme but the individual MOSFET are replaced with a number of lower power devices connected in parallel as illustrated in Figure 4.10,. The lower power devices have much lower reverse recovery time and on-resistance values than the single high power device as can be seen in Table 4.8. The derating for all MOSFETs was taken at the worst-case junction temperature $\left(\mathrm{T}_{\mathrm{J}}\right)$ of $175^{\circ} \mathrm{C}$.


Figure 4.10: Full-Bridge Synchronous Rectifier parallel configuration

The analysis follows the same procedure as the full-bridge synchronous rectification configuration for the $\mathrm{Q}_{1}, \mathrm{Q}_{2}, \mathrm{Q}_{3}$ and $\mathrm{Q}_{4}$ as described in A .3 of Appendix A . The current through each device was evaluated for different numbers of devices in parallel. The power loss for the single-phase converter is the sum of the component power losses multiplied by the number of devices in parallel. The number of devices evaluated in parallel was two and four in order to determine the minimum quantity required to meet the efficiency specification of $\geq 90 \%$. The specifications for the most suitable devices [(Fairchild 2002a), (Fairchild 2003), (Fairchild 2004), (Infineon 2003), (Philips 2002) and (Philips 1999)] are provided in Table 4.8 and a detailed summary of the efficiency results for each component is provided in Table 4.9. There were no suitable components from International rectifier, On Semiconductor, ST Microelectronics, IXYS, APT, Toshiba and Vishay. The complete analysis for each component is presented in Appendix B.

| Make \& Model | $\mathrm{V}_{\text {ds }}$ | $\mathrm{I}_{\text {ds }}$ | $\mathbf{R}_{\text {ds(on) }}$ | $\mathbf{R}_{\text {ds(on) }}$ | $\mathbf{R}_{\text {thetaJc }}$ | $\mathrm{t}_{\text {rise }}$ | $\mathrm{t}_{\text {fall }}$ | $\mathrm{t}_{\mathrm{rr}}$ | Package |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Fairchild | (Vdc) | (A) | (mOhm) | Derating | $\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$ | (nS) | (nS) | (nS) |  |
| FDP047AN08A0 | 75 | 80 | 4.7 | 2.34 | 0.48 | 88 | 45 | 53 | TO-220 |
| FDH038AN08A1 | 75 | 80 | 3.8 | 2.67 | 0.33 | 141 | 126 | 50 | TO-247 |
| FDP060AN08A0 | 75 | 80 | 6 | 2.17 | 0.58 | 79 | 38 | 37 | TO-220AB |
| Infineon |  |  |  |  |  |  |  |  |  |
| SSP80N08S2L-07 | 75 | 80 | 7.1 | 1.83 | 0.5 | 81 | 78 | 100 | TO-220 |
| Philips |  |  |  |  |  |  |  |  |  |
| BUK7506-75B | 75 | 75 | 5.6 | 2.1 | 0.5 | 56 | 48 | 86 | TO-220AB |
| PSMN009-100W | 100 | 100 | 9 | 2.78 | 0.5 | 100 | 100 | 80 | TO-247 |

Table 4.8: MOSFET Specifications

It can be seen from the results that only the Philips BUK7506-75B can satisfy the specification ( $\geq 90 \%$ efficiency) for all ISG modes when 4 devices are used in parallel, while the Fairchild FDP047AN08A0 and FDP060AN08A0 are marginal. The Fairchild FDH038AN08A1, the Infineon SPP80N08S2L-07 and the Philips PSMN009-100W failed for all device numbers and therefore this device was eliminated from further evaluation. The actual number of switching devices that were implemented in parallel was a trade off between efficiency, cost, heatsink capabilities, gate drive complexity and cost. Two devices in parallel were deemed as sufficient to achieve the efficiency specification and still retain a reasonably low level of circuit complexity and cost. The selected components were then evaluated for reverse recovery time capabilities in order to finalize the most suitable candidates.

| Power Analysis | Starting | Low speed motoring | Low speed generating | High speed generating |
| :---: | :---: | :---: | :---: | :---: |
| Speed (RPM) | 200 | 1000 | 2000 | 4500 |
| Classic Configuration |  |  |  |  |
| Efficiency (\%) |  |  |  |  |
| SynchronousRectifier Configuration |  |  |  |  |
| Efficiency (\%) | 71 | 74 | 79 | 87 |
| Parallel Configuration |  |  |  |  |
| Fairchild FDP047AN08A0 |  |  |  |  |
| Efficiency (\%)-2 devices | 86 | 87 | 87 | 97 |
| Efficiency (\%)-4 devices | 89 | 89 | 89 | 98 |
| Fairchild FDH038AN08A1 |  |  |  |  |
| Efficiency (\%)-2 devices | 80 | 81 | 80 | 97 |
| Efficiency (\%)-4 devices | 82 | 82 | 81 | 98 |
| Fairchild FDP060AN08A0 |  |  |  |  |
| Efficiency (\%)-2 devices | 86 | 87 | 88 | 96 |
| Efficiency (\%)-4 devices | 89 | 89 | 89 | 98 |
| Infineon SPP80N08S2L-7 |  |  |  |  |
| Efficiency (\%)-2 devices | 79 | 80 | 80 | 95 |
| Efficiency (\%)-4 devices | 82 | 82 | 82 | 97 |
| Phillips BUK7506-76B |  |  |  |  |
| Efficiency (\%)-2 devices | 87 | 88 | 89 | 97 |
| Efficiency (\%)-4 devices | 90 | 91 | 91 | 98 |
| Phillips PSMN009-100W |  |  |  |  |
| Efficiency (\%)-2 devices | 78 | 79 | 81 | 93 |
| Efficiency (\%)-4 devices | 82 | 83 | 83 | 96 |

Table 4.9: Component Efficiency Comparison (\%)

### 4.3 Reverse Recovery Analysis

A simulation study was implemented on the most suitable devices to evaluate the reverse recovery time, $\mathrm{t}_{\mathrm{rr}}$, of each component. This time needed to be as low as possible in order to minimise shoot through currents during freewheeling operation of the converter. An electrical test was preformed on each of the approved components to verify simulation accuracy and finalize the component selection.

### 4.3.1 Simulation Analysis

The reverse recovery time, $\mathrm{t}_{\mathrm{r}}$, is the period of time that the current conducts in the reverse direction at turn off of a diode (Mohan 1995b). It is measured from the zero crossing where the diode current goes from forward bias to reverse bias, to the point at which a straight line through the maximum reverse recovery current ( $\mathrm{I}_{\mathrm{RM}}$ or $\mathrm{I}_{\mathrm{RRM}}$ ) and $0.25 * \mathrm{I}_{\text {RM }}$ passes through zero as illustrated in Figure 4.11 [(Microsemi 2004) and (Fairchild 2002b)]. The reverse recover time of the intrinsic diode in the MOSFET that is used this application must limit the amount of shoot through current experienced by the circuit. A time of $\leq 130 \mathrm{~ns}$ was chosen in order to compare favourably with the average value of the diodes that could be used in the asymmetric half-bridge configuration [(Microsemi 2004), (International Rectifier 1997), (IXYS 2003), (STMicroelectronics 2004), (Fairchild 2002b)] as indicated in Table 4.10. The reverse recovery time of the candidate MOSFETs was initially evaluated under simulated conditions and successful devices were then evaluated in an experimental test circuit to verify actual device operation.

| Manufacturer | Microsemi | IRF | IXYS | ST | Fairchild |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Component | APT2X101_100DQ60J | 80 EPF02 | DSEP $2 \times 101-04 \mathrm{~A}$ | STTH20002TV | RURG8060 |
| $\mathbf{t}_{\text {rr }}(\mathbf{n S})$ | 160 | 195 | 120 | 85 | 85 |

Table 4.10: Diode reverse recovery times


Figure 4.11: Diode Reverse Recovery Waveform

The test circuit for reverse recovery simulation is illustrated in Figure 4.12. The pulse period was adjusted in order to obtain a forward current $\left(\mathrm{I}_{\mathrm{F}}\right)$ through the diode of 20A and once the desired forward current is achieved, a reading was obtained for the reverse recovery time ( $\mathrm{t}_{\mathrm{rr}}$ ) and the maximum reverse recovery current ( $\mathrm{I}_{\mathrm{RM}}$ ). The resultant waveforms $\mathrm{t}_{\mathrm{rr}}$ and $\mathrm{di}_{\mathrm{f}} / \mathrm{dt}$ are illustrated in Figure 4.13, respectively. The simulation results for all the candidate devices are tabulated in Table 4.11.


Figure 4.12: Reverse Recovery Simulation Test Circuit


Figure 4.13: Reverse Recovery Electrical Test Waveform $-t_{\mathrm{rr}}, \mathrm{I}_{\mathrm{RM}}$

### 4.3.2 Experimental Analysis

The test circuit for the reverse recovery electrical test is illustrated in Figure 4.14. The pulse period was adjusted for a forward current $\left(\mathrm{I}_{\mathrm{F}}\right)$ of up to 20A and the readings taken for forward current $\left(\mathrm{I}_{\mathrm{F}}\right)$, $\mathrm{di}_{\mathrm{F}} / \mathrm{dt}$, reverse recovery time $\left(\mathrm{t}_{\mathrm{rr}}\right)$ and current $\left(\mathrm{I}_{\mathrm{RM}}\right)$ are tabulated in Table 4.11. Examples of the reverse recovery time waveforms are included in Figure 4.15 for forward current $\left(\mathrm{I}_{\mathrm{F}}\right)$ and $\mathrm{di}_{\mathrm{F}} / \mathrm{dt}$ and in Figure 4.16 for reverse recovery time ( $\mathrm{t}_{\mathrm{rr}}$ ) and current ( $\mathrm{I}_{\mathrm{RM}}$ ). From the results, it can be seen that all of the devices from Fairchild Semiconductor are suitable for implementation in the converter. The reverse recovery time of Infinion device is too high, while there was no simulation file available to test the device from Philips Semiconductor. The Fairchild Semiconductor FDP047AN08A0 was selected for the circuit implementation due to component availability.


Figure 4.14: Reverse Recovery Electrical Test Circuit


Figure 4.15: Reverse Recovery Electrical Test Waveform - $\mathrm{I}_{\mathrm{F}}$


Figure 4.16: Reverse Recovery Electrical Test Waveform - $\mathrm{t}_{\mathrm{r}}$, $\mathrm{I}_{\mathrm{RM}}$

| Reverse Recovery <br> Analysis | Data Sheet | Simulation Study |  |  |  |  | Electrical Test |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\mathbf{t}_{\mathbf{r r}}$ | $\mathbf{t}_{\mathbf{r r}}$ | $\mathbf{I}_{\mathbf{F}}$ | $\mathbf{I}_{\mathbf{R M}}$ | $\mathbf{t}_{\mathbf{r r}}$ | $\mathbf{I}_{\mathbf{F}}$ | $\mathbf{I}_{\mathbf{R M}}$ |  |  |  |
| Parallel Configuration | $(\mathrm{nS})$ | $(\mathrm{nS})$ | $(\mathrm{A})$ | $(\mathrm{A})$ | $(\mathrm{nS})$ | $(\mathrm{A})$ | $(\mathrm{A})$ |  |  |  |
| Fairchild |  |  |  |  |  |  |  |  |  |  |
| FDP047AN08A0 | 53 | 95 | 43.4 | 0.56 | 67 | 10 | 2.5 |  |  |  |
| FDP060AN08A0 | 37 | 87 | 43.4 | 0.46 | 58 | 10 | 3 |  |  |  |
| Phillips |  |  |  |  |  |  |  |  |  |  |
| BUK7506-76B | 86 | No Pspice model file | No Samples Available |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |

Table 4.11: Reverse Recovery Analysis

### 4.4 Summary

Component cost and efficiency are essential aspects of the converter design. The switched reluctance motor has an efficiency value of over ninety percent, so the converter must also operate at an equivalent level. The key element in the converter design is keeping the switching component losses to a minimum. Significant developments in MOSFET technology have enabled conduction losses to be reduced significantly. The choice of switching frequency has a significant bearing on the component losses to the point where these are the dominant losses. Therefore, component power analysis is essential in determining if single components or multiple components in parallel provide the optimum solution. From the implementation of the power analysis, simulation study and electrical tests, the full bridge synchronous rectifier converter with parallel switching devices offers the most efficient solution for both motoring and generating operation. The implementation of a number of switching devices in parallel requires careful consideration in order to obtain efficient and reliable operation of the converter.

To evaluate the converters configurations and the associated switching components, the operating conditions were defined in order to set limits for the converter operation. The operating conditions were determined by the SRM specification and the application of the machine as an ISG. The application specific conditions included the performance conditions and operating environment for the ISG, the conduction periods and duty cycles experienced by all the switching components under all converter modes (magnetisation, freewheeling and demagnetisation) and ISG modes (starting, low speed motoring, low and high speed generating), and the specific automotive electrical parameter limits.

The full-bridge synchronous rectifier with two MOSFETs mounted in parallel provided the best compromise of efficiency, cost and complexity for implementation with the ISG under motoring and generating operation. The most efficient MOSFETs were evaluated for reverse recovery time capability in order to minimise the possibility of current shoot through during freewheeling mode of operation. The analysis was implemented under simulated and experimental conditions and a device from Philips (BUK7506-75B) was deemed the most acceptable component for this application and
two devices from Fairchild (FDP047AN08A0 and FDP060AN08A0) were deemed as marginal.
As can be seen from the power analysis computations in Appendix B, the power dissipation of the switching devices during low speed generating is excessive. As low speed generating occurs in the region from engine idle speed (1000rpm) up to engine cruising speed (2000rpm), it would represent only a small contribution to the total generating requirements. Generating at around engine idle speed would be rare when the vehicle is operating in start/stop mode. Eliminating generating operation between engine idle speed and engine cruising speed would be more efficient as this would represent the region where vehicle acceleration would occur. Low speed generating is therefore not considered beyond this preliminary analysis even though it is a theoretically possible mode of operation.

## Chapter 5 Converter Design

The previous chapter addressed the power losses in the switching components and determined that a parallel component configuration is the most effective solution. This chapter addresses the detailed design process for the converter. A detailed discussion is presented on the implementation of the parallel component configuration and its associated requirements. The heat sink design to determine the most appropriate heat sink configuration for this application is described. Gate drive design is then addressed incorporating the issues of blanking time and circuit isolation. The selection of the appropriate value of filter capacitor is explained and a discussion on the high current conductor configuration is included. Current sensor requirements are addressed and finally the specifications for the prototype circuit layout are outlined.

### 5.1 MOSFETs in Parallel

When discrete MOSFETs are configured in parallel, the current handling capability of the circuit can be increased significantly. However, the actual implementation is more complex than using single high power modules. Numerous issues need to be addressed, including thermal coupling, stray inductances, circuit layout, gate drive circuitry and parasitic oscillations, in order to maximise current balancing between the parallel devices.

Careful attention needs to be given to the thermal coupling when MOSFETs are connected in parallel. Under steady state conditions the positive temperature coefficient of the MOSFET on-resistance tends to equalize the current in parallel devices (International Rectifier 2004a), (Gauen 1984) and (Mohan 1995). Although, this has less of an effect under dynamic operation, it is still essential to have close thermal coupling between devices to maintain junction temperature equilibrium (Gauen 1984) and (Pelly 2004). Parallel devices should be mounted on the same heat sink and a current derating of $20 \%$ is also required to account for variation in device characteristics. The requirement for tight thermal coupling weighs against electrical isolation and when a thermal barrier is placed between the individual devices it tends to decouple the individual junction temperatures. Therefore, thermally conductive insulator pads, placed directly at the cooling surface of a TO-220 or TO-247 device or electrically isolated TO-220 and TO247 packages, are not ideal for parallel device configuration (Pelly 2004). From this observation, the Fairchild Semiconductor device,

FDH038AN08A1, with its TO247 electrically isolated package was deemed unsuitable for this application. The parallel devices should be mounted on a common heatsink. If electrical isolation is required, the parallel devices can be mounted on a common heatspreader to thermally couple the junctions. The isolation barrier is placed between the heatspreader and the main heatsink as illustrated in Figure 5.1.


Figure 5.1: Using a heatspreader to provide thermal coupling between parallel devices and electrical isolation with main heatsink.

The effect of stray collector, source and gate inductances can be significant when the devices are connected in parallel. Stray collector inductance can lead to voltage imbalance and overshoot conditions but it can be tolerated so long as it does not exceed device ratings (International Rectifier 2004a). It can also affect the turn-on times by dropping voltage at the collector. Stray source inductance must be balanced, especially at high frequencies of operation, as it affects device turn-on times due to the counteractive voltage drop slowing the rise of the gate voltage (International Rectifier 2004a). It can also lead to different turn-off times in devices causing excessive current in some devices. Any significant levels of stray gate inductance can lead to dv/dt induced device turn-on (International Rectifier 2004b).

Circuit layout is of critical importance when implementing a parallel MOSFETs configuration. Minimising conducting path lengths can significantly reduce stray inductance, while symmetrical layout of components and routing of connections equalizes the stray inductance (International Rectifier 2004a), (Forsythe 1981), (Gauen 1984) and (Mohan 1995). The most significant effect of non-symmetrical layout is current imbalance during switching intervals and consequently unbalanced switching losses. The stray source inductance is the most critical element to balance. An ideal layout for balancing the source inductance and the switching losses is the circular layout
illustrated in Figure 5.2a (Pelly 2004). Where switching losses are low due to switching frequency and/or switching voltage is relatively low, the simple in-line layout illustrated in Figure 5.2b can be used even though it is not electrically symmetrical.


Figure 5.2: (a) Circular layout, (b) in-line layout

Special attention also needs to be given to the gate drive circuitry implementation and layout and to the prevention of parasitic oscillations. The gate drive circuit must represent a stiff voltage source for rapid device turn-on and it must provide very low impedance for fast device turn off in order to help negate some circuit imbalance (International Rectifier 2004a), (Forsythe 1981), (Fairchild 1993) and (Gauen 1984). It is also extremely important that the gate drive impedance is matched through careful layout (Gauen 1984). Close symmetrical layout assists in matching the gate drive impedances and minimising stray inductances (Gauen 1984). With the low impedance paths created when using MOSFETs in parallel, parasitic oscillations can become a significant problem. Individual gate decoupling resistors ( $10 \Omega-20 \Omega$ ) or ferrite beads provide damping to prevent oscillations (International Rectifier 2004a), (Forsythe 1981), (Gauen 1984) and (Mohan 1995). Zenor diodes to protect the MOSFET gate should be placed on the drive side of the gate resistor to prevent oscillations, while any capacitors in the gate drive circuit can also lead to oscillations (International Rectifier 2004a).

The following are the key areas that need to be addressed when implementing MOSFETs in parallel:

- Close thermal coupling of parallel MOSFETs to prevent junction temperature imbalance.
- Symmetrical component placement and layout with minimum length connection paths in order to balance and minimise any stray circuit inductance.
- Gate drive circuit that represents a stiff voltage and has very low impedance.
- Individual decoupling resistors or ferrite beads on the MOSFET gates to prevent oscillations.


### 5.2 Heatsink Design

Thermal design must be considered at an early stage when designing power electronic equipment to operate at high ambient temperature conditions (Mohan 1995). It is critical to maintain the lowest possible junction temperature as the failure rate doubles for every $10^{\circ} \mathrm{C}$ rise in junction temperature (Mohan 1995) and (Hill 2004). It is difficult to keep power semiconductor case temperature below $90^{\circ} \mathrm{C}$ without using a water-cooled heatsink (International Rectifier 2004c). This discussion reviews the fundamentals of heat sink design and the specific requirements for this application. The step-by-step procedure for the heat sink design is then discussed for the starting mode of operation and the process concludes with the selection of the most suitable heat sink configuration for this application.

### 5.2.1 Fundamentals

Three factors affect junction temperature: the sum of all thermal resistance from the junction to the ambient environment (air, oil or water), the amount of heat to be dissipated and finally the ambient temperature (Hill 2004). A schematic (Hill 2004) and (Polyfet 2005) of the "equivalent circuit" for the thermal resistances is given in Figure 5.3.


Figure 5.3: Schematic for thermal resistances

Thermal resistance, $\mathrm{R}_{\theta}$, is derived from the equation for energy flow from the higher temperature end to the lower temperature end of a material as illustrated in Figure 5.4 and is determined from the formula (Mohan 1995)

$$
\begin{align*}
& P_{\text {cond }}=\frac{\lambda A \Delta T}{d}  \tag{5.1}\\
& R_{\theta}=\frac{\Delta T}{P_{\text {cond }}}=\frac{d}{\lambda A} \tag{5.2}
\end{align*}
$$

Where $P_{\text {cond }}$ is the energy flow per unit time (W), $\lambda$ is thermal conductivity $\left(\mathrm{Wm}^{-1 \mathrm{o}} \mathrm{C}^{-1}\right)$, A is the cross sectional area $\left(\mathrm{m}^{2}\right), \Delta \mathrm{T}$ is the temperature difference, $\mathrm{T}_{2}-\mathrm{T}_{1}\left({ }^{\circ} \mathrm{C}\right), \mathrm{d}$ is the length of material (m) and $\mathrm{R}_{\theta}$ is defined as the thermal resistance. The units of thermal resistance $\left(\mathrm{R}_{\theta}\right)$ is degrees centigrade per watt $\left({ }^{\circ} \mathrm{CW}^{-1}\right)$.Aluminium is typically used in heatsinks and has a thermal conductivity of approximate $220 \mathrm{Wm}^{-1}-{ }^{\circ} \mathrm{C}^{-1}$ when $90 \%$ pure (Mohan 1995), (Tillmann Steinbrecher 2005) and (Electrocomp 2003).


Figure 5.4: Conduction of heat energy per unit time, $P_{\text {cond }}$, in a material

The type and size of heatsink can be determined from the following equation (Mohan 1995), (Hill 2004), (Wakefield 2005) and (Polyfet 2005):

$$
\begin{equation*}
\mathbf{R}_{\theta-a}=\frac{\mathrm{T}_{\mathrm{j}}-\mathrm{T}_{\mathrm{a}}}{\mathrm{P}_{\mathrm{cond}}}-\left(\mathrm{R}_{\theta j-c}+\mathrm{R}_{\theta c-s}\right) \tag{5.3}
\end{equation*}
$$

The above expression can also be used to determine the temperature at the different locations in the heat flow path.

The predominant types of cooling strategies for power electronics are air (forced or natural) or liquid. Air is favoured over liquid due to the complexities of the hardware required to control and circulate liquid and the extra design effort and cost (Soule 2005). The use of a fan with the heatsink provides additional cooling but valuable space is used for the fan, fan mount, and air flow entry and exit. As fan speed increases the airflow at
higher speed generates two sources of noise: the moving fan and the friction of the air moving between the cooling fins.

Heat dissipation is proportional to surface area of the device and the volume of fluid (air or liquid) moving along the heat transfer surface (Bertrand 2003). A liquid cooled heat sink can dissipate more heat with considerable less flow volume, maintain better temperature consistency and generate less local acoustic noise (Soule 2005). Liquid cooled heatsinks are also unaffected by elevation, which would be an important consideration in the automotive environment. The surface area required for liquid cooled heatsinks is much smaller than that required for air-cooled heatsinks.

There are a number of different schemes for implementing liquid cooled heatsinks (Bertrand 2003) and these includes: embedded or pressed tube in aluminium plate, expanded copper tube, gun-drilled plate, one-piece castings, direct cooling, bolted cold plate and brazed cold plate. The embedded copper tube in aluminium cold plate illustrated in Figure 5.5a (Aavid Thermalloy 2007a) provides the most cost effective solution in a light package but with a possible lack of uniformity across the surface of the plate and differences in thermal characteristics in double sided applications. The brazed cold plate illustrated in Figure 5.5b (Aavid Thermalloy 2007b) provides the highest performance and the most uniform cooling across the entire plate and can have a very compact footprint that can facilitate double sided cooling.


Figure 5.5: (a) The embedded copper tube in aluminium cold plate, (b) brazed cold plate

### 5.2.2 System Description

The implementation of the converter in this application using MOSFETs in parallel necessitates that the junction temperature of the devices also be equalised so good thermal coupling is vital. In order to achieve this, the devices must be mounted on a common heat sink and, if electrical isolation is required, a heat spreader or bus bar can be used to thermally couple the junctions. An isolation barrier, called an electrically isolated thermal conductor, can then be placed between the heat spreader and the main heatsink (Pelly 2004). Illustrations of the side view and the top view for a possible configuration are provided in Figure 5.6 and Figure 5.7, respectively.

As mentioned previously, it is critical for reliability to maintain the lowest possible junction temperature. The MOSFET case temperature, $\mathrm{T}_{\mathrm{c}}$, is defined to be equal to $100^{\circ} \mathrm{C}$, as typically the temperature would range from $90^{\circ} \mathrm{C}$ to $110^{\circ} \mathrm{C}$ (International Rectifier 2004c). The automotive engine compartment ambient temperature can range from $-40^{\circ} \mathrm{C}$ to $150{ }^{\circ} \mathrm{C}$ (Myers 2003) and (DuPont 2005). Operating in this environment necessitates locating the converter assembly low down on the engine and using watercooling to limit the ambient temperature of the heatsink to approximately $90^{\circ} \mathrm{C}$. For implementation in an automotive environment it is assumed that a double-sided heat sink is used for the converter, while for implementation in the laboratory a single force air cooled heatsink is used for each converter phase. This allows for a simplified heat sink configuration for the prototype converter as the ambient temperature was assumed to have a maximum value of $45^{\circ} \mathrm{C}$ to compare with the maximum ambient temperature experienced by the ISG during cold starting conditions as defined in section 4.1.3.

The final selection on the number of devices to be implemented in parallel was determined as part of the heat sink analysis. The fewer devices that can be used, the more compact the single-phase converter can be, thereby minimising stray inductance. The number of devices in parallel also dictates the size of the heat spreader and therefore the thermal conductor. The heat sink analysis describes the step-by-step process used to determine the thermal resistance requirement for the heat sink during ISG start mode. A spreadsheet program was then used to evaluate the different combinations of devices number in parallel, heat spreader and thermal conductor size, case and ambient temperatures, in order to determine the most suitable configuration.


Figure 5.6: Side view of air cooled converter mechanical assembly


Figure 5.7: Top view of air cooled converter mechanical assembly


Figure 5.8: Heat Flow Path for a Single Phase Converter

### 5.2.3 Determination of $\mathbf{R}_{\theta s-\mathrm{a}}$

In order to determine the thermal resistance requirement for heat sink-to-ambient path, one needs to calculate the sum of thermal resistances from the junction-to-sink. The heat flow path from junction-to-ambient for a single-phase converter, $\mathrm{R}_{\mathrm{\theta j}^{2}-\mathrm{a}}$, (assuming device number equals two) is shown in Figure 5.8. As there are parallel paths for heat flow, the thermal resistance combine like electrical resistors in parallel (Mohan 1995). First, the thermal resistance from the junction-to-heat spreader is determined for each component from the sum of the thermal resistance junction-to-case, $\mathrm{R}_{\mathrm{\theta j}-\mathrm{c}}$, and case-to-heat spreader, $\mathrm{R}_{\theta c \text {-hs. }}$. Then the parallel sum of these thermal resistances is calculated for the selected number of devices. The total thermal resistance in parallel is the thermal resistance for the individual component divided by the number of devices in parallel $(N)$ since the thermal resistances are the same value (Mohan 1995) and (Fowler 1989). Next, this value of thermal resistance is added to the value of thermal resistance for the heat spreader-to-thermal conductor, $\mathrm{R}_{\theta \text { ens-t }}$, and the thermal conductor to the heat sink, $\mathrm{R}_{\theta \mathrm{tc}-\mathrm{s}}$, and this yields the thermal resistance junction-to-sink, $\mathrm{R}_{\mathrm{\theta j}_{\mathrm{j}} \mathrm{s}}$, for each component group (e.g. $\left.\mathrm{R}_{\theta \mathrm{jj}-\mathrm{s}(\mathrm{Q} 1)}\right)$. Finally, this step needs to be repeated for the other three component groups $\left(\mathrm{Q}_{2}, \mathrm{Q}_{3}\right.$ and $\left.\mathrm{Q}_{4}\right)$ and the parallel sum of the thermal resistances for the four groups of components yields the converter phase thermal resistance junction-to-sink, $\mathrm{R}_{\text {0j-s(Phase) }}$, when using a single heat sink for each phase. The thermal resistance sink-toambient, $\mathrm{R}_{\theta s \mathrm{~s}-\mathrm{a}}$, is then determined using equation 5.3. The revised equation to determine the thermal resistance sink-to-ambient, $\mathrm{R}_{\theta s-\mathrm{a}}$, is:

$$
\begin{equation*}
R_{\theta s-a}=\left(\frac{T_{j(\max )}-T_{a}}{P_{T(S P)}}\right)-\left[\frac{\left(\frac{R_{\theta j-c(\text { Device })}+R_{\theta c-h s}}{N}\right)+\left(R_{\theta h s-c c}+R_{\theta t c-s}\right)}{4}\right] \tag{5.4}
\end{equation*}
$$

where $P_{T(S P)}$ is the total power dissipation of the MOSFETs from the single converter phase, $T_{a}$, is the maximum ambient temperature of $45^{\circ} \mathrm{C}$ during ISG cold starting conditions and $T_{j(\max )}$ is the maximum junction temperature experienced by the MOSFETs $\left(\mathrm{Q}_{1}-\mathrm{Q}_{4}\right)$ during that particular ISG mode of operation (starting, low speed motoring and high speed generating).

The junction temperature, $T_{j}$, determined from the following equation.

$$
\begin{equation*}
T_{j}=T_{c}+\left(R_{\theta j-c} P_{T(d e v i c e)}\right) \tag{5.5}
\end{equation*}
$$

where $P_{T(d e v i c e)}$ is the total power dissipation for each of the MOSFETs devices $\left(\mathrm{Q}_{1}-\mathrm{Q}_{4}\right)$ from the single converter phase, $R_{\theta j-c}$ is the thermal resistance for the TO-220 package and $T_{c}$ is the case temperature of $100^{\circ} \mathrm{C}$. (Polyfet 2005)

In order to determine the thermal resistance sink-to-ambient, $\mathrm{R}_{\theta s-a}$, the values of thermal resistance had to be determined for the heat spreader and the electrically conductive thermal conductor. The step-by-step process of calculating the thermal resistance values under starting mode of operation is illustrated in section 5.2.4 and the results for this and the other speeds during motoring and generating modes of operation are included in Table 5.3. The table also includes results for different numbers of devices in parallel for each component group and the effects of different ambient temperatures on the heat sink selection process. The calculations were implemented using a spreadsheet program to automate the heat sink analysis in order to evaluate the effects of different device numbers in parallel (2 and 4), variations in ambient temperatures $\left(45^{\circ} \mathrm{C}\right.$ and $\left.90^{\circ} \mathrm{C}\right)$, using alternative types of thermal conductor materials and different sizes of heat spreader. These calculations were implemented for each ISG mode of operation (starting, low speed motoring and high speed generating). The specific objective of the analysis was to determine the optimum heat sink selection ( $\mathrm{R}_{\theta s-\mathrm{a}}$ value). The detailed analysis for each component is provided in Appendix C, while a summary of the results is provided in Table 5.4.

### 5.2.3.1 Determination of $\boldsymbol{R}_{\theta}$ for Heat Spreader

The heat spreader is constructed from aluminium ( $\lambda=$ approximately $220 \mathrm{Wm}^{-1}-{ }^{\circ} \mathrm{C}^{-1}$ ). The worse case situation assumes that only two devices are used in parallel and therefore this defines the smallest size of heat spreader. The MOSFET dimensions were determined from the device data sheet for a TO-220 package (Fairchild 1999) (approximately 17 mm long by 11 mm wide) and the two parallel devices are mounted side by side on the heat spreader that is 50 mm long by 25 mm wide. There are four heat spreaders, one for each component group $\left(\mathrm{Q}_{1}, \mathrm{Q}_{2}, \mathrm{Q}_{3}\right.$ and $\left.\mathrm{Q}_{4}\right)$ as illustrated in Figure 5.4. The maximum thickness (d) of the heat spreader is assumed to be 16 mm in order to allow ample material depth for the mounting screws to attach the MOSFETs and to
allow sufficient area to attach electrical connections to the heatspreader/bus bar in order to complete the connections for the full-bridge converter. These dimensions provide the worse case sizing of the heat spreader to be used in this application. The thermal resistance of the heat spreader, $\mathrm{R}_{\text {日hs-tc }}$, is:

$$
\begin{equation*}
R_{\theta h s-c c}=\frac{d}{\lambda A}=0.058^{\circ} \mathrm{CW}^{-1} \tag{5.6}
\end{equation*}
$$

### 5.2.3.2 Determination of $\boldsymbol{R}_{\theta}$ for the electrically isolated thermal conductor

Elastomers are used for the thermal conductor in this application. They are made from an elastomer-binding agent, usually silicone, in conjunction with thermally conductive filler, typically aluminium-oxide or boron nitrate (Electrocomp 2003). The material is easy to cut to size at room temperature, has high tensile strength and does not require thermal grease. A list of products and relevant specifications is given in Table 5.1. The size of the thermal conductor is dependent on the size of heat spreader determined in the previous section. The worst case sizing assumes that the insulator has the same area as the heat spreader but the material was extended beyond the edges of the heat spreader by 5 mm in order to provide sufficient insulation. The worst-case thermal resistance, $\mathrm{R}_{\theta \text { tc- }- \text {, }}$ for the Warth K200 thermal conductor product is:

$$
\begin{equation*}
R_{\theta t c-s}=\frac{d}{\lambda A}=0.135^{\circ} \mathrm{CW}^{-1} \tag{5.7}
\end{equation*}
$$

The thermal resistance values for each product (Bergquist 2005), (Bergquist 2004) and (Warth 2004) are given in Table 5.1. The Bergquist Sil-Pad 2000 provides the best solution $\left(\mathrm{R}_{\text {өtc-s }}=0.058^{\circ} \mathrm{CW}^{-1}\right)$ for this application.

| Vendor | Product | Construction | $\boldsymbol{\lambda}\left(\mathbf{W m}^{-\mathbf{1}} \mathbf{- 0}^{\mathbf{0}} \mathbf{C}^{\mathbf{- 1}}\right)$ | $\mathbf{d}_{(\text {max })}(\mathbf{m m})$ | $\mathbf{R}_{\text {өtc-s }}\left({ }^{\mathbf{0}} \mathbf{C W}^{\mathbf{- 1}}\right)$ |
| :--- | :--- | :--- | :---: | :---: | :---: |
| Bergquist | Sil-Pad 2000 | Silicon/fiberglas | 3.5 | 0.254 | 0.058 |
| Bergquist | Sil-Pad K10 | Silicon/film | 1.3 | 0.152 | 0.094 |
| Warth | K200 | Silicon/fiberglas | 1.3 | 0.22 | 0.135 |

Table 5.1: Sources of Thermally Conductive Insulators

### 5.2.3.3 Determination of junction temperature, $\boldsymbol{T}_{\boldsymbol{j}}$

The value of the junction temperature for $\mathrm{Q}_{1}$ during starting mode when using the Fairchild Semiconductor FDP047AN08A0 is

$$
\begin{equation*}
T_{j}=T_{c}+\left(R_{\theta j-c} P_{T\left(Q_{1}\right)}\right)=127^{\circ} \mathrm{C} \tag{5.8}
\end{equation*}
$$

where $P_{T(Q l)}=55 \mathrm{~W}$ during ISG starting mode, $T_{c}=100^{\circ} \mathrm{C}$ and $R_{\theta j-c}=0.48^{\circ} \mathrm{CW}^{-1}$. The junction temperature determined for each device $\left(\mathrm{Q}_{1}-\mathrm{Q}_{4}\right)$ is provided in Table 5.2.

| Device | $\mathbf{Q}_{\mathbf{1}}$ | $\mathbf{Q}_{\mathbf{2}}$ | $\mathbf{Q}_{\mathbf{3}}$ | $\mathbf{Q}_{\mathbf{4}}$ |
| :---: | :---: | :---: | :---: | :---: |
| $\mathbf{T}_{\mathbf{j}}\left({ }^{\circ} \mathbf{C}\right)$ | 127 | 113 | 127 | 101 |
| $\mathbf{P}_{\mathbf{T} \text { (deice) })}(\mathbf{W})$ | 55 | 27 | 57 | 2 |

Table 5.2: Calculated junction temperatures for each MOSFET (Q- Q4) during ISG starting mode

### 5.2.4 Step-by-Step Determination of $\mathbf{R}_{\theta s-\mathrm{a}}$ - Starting Mode

The calculation of the thermal resistance sink-to-ambient, $\mathrm{R}_{\theta s \mathrm{~s} \text { a }}$, discussed here illustrates the step-by-step process that is involved to determine the thermal resistance value under ISG starting mode of operation of the SRM. The value of thermal resistance sink-to-ambient for the single phase converter is calculated using equation 5.4. The following are the operating conditions when using the Fairchild Semiconductor FDP047AN08A0 (Fairchild 2004):

| $\mathbf{R}_{\mathbf{0 j - c}}\left({ }^{( } \mathrm{CW}^{-1}\right)$ | $\mathbf{R}_{\text {өc-hs }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | $\mathbf{R}_{\text {日hs-tc }}\left({ }^{( } \mathrm{CW}^{-1}\right)$ | $\mathbf{R}_{\text {өtc-s }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | $\left.\mathrm{T}_{\mathrm{j} \text { (max) }}{ }^{( }{ }^{\text {a }} \mathrm{C}\right)$ | $\mathrm{T}_{\mathrm{c}}\left({ }^{\text {a }} \mathrm{C}\right)$ | $\mathrm{T}_{\mathrm{a}}\left({ }^{\circ} \mathrm{C}\right)$ | N | $\mathbf{P}_{\text {T(SP) }}(\mathbf{W})$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0.48 | 0.1 | 0.058 | 0.058 | 127 | 100 | 45 | 2 | 283 |

Table 5.3: Operating conditions
$R_{\theta j-c}$ is the thermal resistance of the TO-220 package provided in the device data sheet (Fairchild 1999), $R_{\theta c-h s}$ is the thermal resistance of the heat sink compound (Wakefield 2008), $R_{\text {日hs-tc }}$ is the thermal resistance of the heat spreader determined in section 5.2.3.1, $R_{\text {etc-s }}$ is the thermal resistance of the thermal conductor determined in section 5.2.3.2, $T_{c}$ is the maximum case temperature of the $\operatorname{MOSFET}, T_{a}$ is the maximum ambient temperature, and $T_{j(\max )}$ is the maximum junction temperature experienced by the MOSFETs $\left(\mathrm{Q}_{1}-\mathrm{Q}_{4}\right)$ during ISG starting mode, $N$ is the number of devices connected in
parallel and $P_{T(S P)}$ is the total power dissipation of the single phase converter in ISG starting mode. The thermal resistance sink-to-ambient, $R_{\theta_{s-}-a}$, is:

$$
\begin{align*}
R_{\theta s-a} & =\left(\frac{T_{j(\max )}-T_{a}}{P_{T(S P)}}\right)-\left[\frac{\left(\frac{R_{\theta j-c(\text { Device })}+R_{\theta c-h s}}{N}\right)+\left(R_{\theta t s-t c}+R_{\theta c-s}\right)}{4}\right]  \tag{5.9}\\
& =0.19^{\circ} C W^{-1}
\end{align*}
$$

The thermal resistance sink-to-ambient, $\mathrm{R}_{\theta_{s-\mathrm{a}} \text {, }}$ for the different initial conditions were calculated in the automated spreadsheet program and a summary of the results is shown in Table 5.4, while the detailed results for the thermal analysis calculations are provided in Appendix C.

| Thermal Analysis | Starting | Low speed motoring | High speed generating |
| :---: | :---: | :---: | :---: |
| $\mathrm{T}_{\mathrm{c}}=100^{\circ} \mathrm{C}$ | 200RPM | 1000RPM | 4500RPM |
| Fairchild FDP047AN08A0 |  |  |  |
| 2 Devices @ $T_{\mathrm{a}}=45^{\circ} \mathrm{C}$ | 0.19 | 0.17 | 0.48 |
| 4 Devices @ $\mathrm{T}_{\mathrm{a}}=45^{\circ} \mathrm{C}$ | 0.23 | 0.20 | 0.88 |
| 2 Devices @ $\mathrm{T}_{\mathrm{a}}=90^{\circ} \mathrm{C}$ | 0.031 | 0.030 | 0.074 |
| 4 Devices @ $\mathrm{T}_{\mathrm{a}}=90^{\circ} \mathrm{C}$ | 0.032 | 0.028 | 0.14 |
| Fairchild FDP060AN08A0 |  |  |  |
| 2 Devices @ $T_{\mathrm{a}}=45^{\circ} \mathrm{C}$ | 0.18 | 0.17 | 0.41 |
| 4 Devices @ $\mathrm{T}_{\mathrm{a}}=45^{\circ} \mathrm{C}$ | 0.24 | 0.21 | 0.77 |
| 2 Devices @ $\mathrm{T}_{\mathrm{a}}=90^{\circ} \mathrm{C}$ | 0.026 | 0.026 | 0.061 |
| 4 Devices @ $\mathrm{T}_{\mathrm{a}}=90^{\circ} \mathrm{C}$ | 0.032 | 0.028 | 0.12 |
| Phillips BUK7506-76B |  |  |  |
| 2 Devices @ $\mathrm{T}_{\mathrm{a}}=45^{\circ} \mathrm{C}$ | 0.21 | 0.19 | 0.46 |
| 4 Devices @ $\mathrm{T}_{\mathrm{a}}=45^{\circ} \mathrm{C}$ | 0.27 | 0.24 | 0.86 |
| 2 Devices @ $\mathrm{T}_{\mathrm{a}}=90^{\circ} \mathrm{C}$ | 0.031 | 0.029 | 0.070 |
| 4 Devices @ $\mathrm{T}_{\mathrm{a}}=90^{\circ} \mathrm{C}$ | 0.038 | 0.033 | 0.14 |

Table 5.4: Thermal analysis to determine $\mathrm{R}_{\theta \mathrm{s}-\mathrm{a}}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$

From Table 5.4, it can be seen that the Philips BUK7506-76B provides the most suitable solution for this application but the Fairchild Semiconductor FDP047AN08A0 and FDP060AN08A0 are also acceptable. For the FDP047AN08A0, the worst-case thermal resistance sink-to-ambient is $0.03{ }^{\circ} \mathrm{CW}^{-1}$ at $\mathrm{T}_{\mathrm{a}}=90^{\circ} \mathrm{C}$ and $0.17^{\circ} \mathrm{CW}^{-1}$ at $\mathrm{T}_{\mathrm{a}}=$ $45^{\circ} \mathrm{C}$. It is possible to use a forced air-cooled heatsink for implementation in a laboratory environment as $\mathrm{T}_{\mathrm{a}}<45^{\circ} \mathrm{C}$. A suitable heatsink would be the HS Marston

890SP-01000-A-100 (HS Marston 2001), which provides a thermal resistance of $0.12^{\circ} \mathrm{CW}^{-1}$ when using an airflow rate of $22.21 \mathrm{~s}^{-1}$.

A water-cooled configuration would be used in the automotive environment due to the high ambient air temperature of $100^{\circ} \mathrm{C}-150^{\circ} \mathrm{C}$ in the engine compartment, while it is assumed that the cooling fluid has a maximum $\mathrm{T}_{\mathrm{a}}<90^{\circ} \mathrm{C}$.. A possible configuration is an aluminium plate with embedded copper tubing where each converter phase would be attached to a plate. A possible candidate for the heatsink is the Aavid Thermolly six pass model 416101U00000G liquid cooled cold plate (Aavid Thermalloy 2007a). The plate has a thermal resistance of $0.012^{\circ} \mathrm{CW}^{-1}$, with a coolant flow rate of $0.06 \mathrm{ls}^{-1}$. The use of a brazed cold plate would provide a more significant improvement in thermal resistance and more uniform cooling. It would also be more applicable to a mass production environment, as custom plates can be designed for this application. An illustration of a possible water cooled heatsink layout is given in Figure 5.9.

It can be seen in the detailed analysis provided in Appendix C that when using 2 devices in parallel that the $\mathrm{T}_{\mathrm{j}} \approx 130^{\circ} \mathrm{C}$ during starting and low speed motoring while the $\mathrm{T}_{\mathrm{j}}<$ $115^{\circ} \mathrm{C}$ when using 4 devices in parallel. The heat sink requirement is almost the same for 2 or 4 devices in parallel under starting and lower speed motoring conditions but is significantly lower for 4 devices under high speed generating conditions. Using 2 devices in parallel reduces cost and complexity but leads to a compromise of reduced reliability for the components due to the higher junction temperatures experienced by the devices.


Figure 5.9: Side view of water cooled heat sink

### 5.3 Gate Drive Design

The full-bridge synchronous rectifier with two MOSFETs mounted in parallel was used in this application and is illustrated in Figure 5.10. It utilizes a high side switch configuration (with the MOSFET drain connected to the voltage supply and the MOSFETs source connected to the load) and this places specific requirements on the gate drive circuit. To fully turn on the high side switch, the gate voltage must be higher than the voltage supply, which is frequently the highest voltage in the system. The gate voltage must be controllable from logic circuits which are normally referenced to ground. The control signals need to be level shifted to the source of the high side device, which in most cases swings between positive and negative voltage supplies. The power absorbed by the gate drive circuitry should not significantly affect the overall efficiency of the converter.


Figure 5.10: Full-Bridge Synchronous Rectifier parallel configuration

When implementing MOSFETs in parallel, large source currents must be provided by the gate drive circuit to enable rapid MOSFET turn-on and also provide very low impedance for fast device turn-off in order to negate circuit imbalance in the circuit. There are numerous techniques for implementing high side gate drive and some of these include floating gate drive supply, pulse transformer, charge pump, boot strip, carrier drive and gate drive integrated circuit (or gate driver IC). A brief review of these techniques to implement these gate drive configurations is summarized in the following section. The gate driver IC, or more simply called the 'gate driver', was selected for this application as it integrated most of the capabilities (level shifting of the logic signals, gate voltage higher than the supply voltage and operation in a wide range of duty cycles and switching frequencies) for high side gate drive operation in a compact package).

The gate driver can provide large peak output current that is acceptable for most applications. However, when driving MOSFETs in parallel a current buffer may be required to facilitate the necessary peak current levels. The implementation of a current buffer is determined by the peak gate drive current requirement of the parallel MOSFETs configuration.

A dead time period or blanking time needs to be provided between switching states of a high and low side switch (e.g. Q1 and Q2 in Figure 5.10) in order to prevent current cross conduction or shoot through condition. The gate driver provides almost no dead time period (Clemente 1990), so a resistor diode network was placed on the gate driver output to implement the additional dead time requirement.

Isolation of the logic control signals is required to protect the low voltage control logic circuitry from the power switching circuits in the event of a fault condition. Isolation in this application is achieved using optical isolators. The output of the optical isolators and the gate drivers for all the switching groups $\left(\mathrm{Q}_{1}-\mathrm{Q}_{4}\right)$ for all converter phases would be powered by a single isolated power supply.

### 5.3.1 Gate Drive Configuration

As noted previously, there are a number of techniques for implementing high side gate drive and some of these include floating gate drive supply, pulse transformer, charge pump, boot strip, carrier drive and gate drive integrated circuit or 'gate driver'. An outline of each technique is provided in Table 5.5 (Clemente 1990). The main limitation of the floating gate supply is the requirement for an isolated supply for each high side MOSFET which would be prohibitive in this application requiring multiple high side MOSFETs. The pulse transformer is a simple and inexpensive solution for high side drive but has limited switching frequency range. The transformer is designed for operation in a specific frequency range whereas the MOSFETs in this application operate at frequencies from 20 Hz up to 25 kHz . Slow turn-on time's factor against selecting charge pump for this application. While simple and inexpensive, limitations in the range of duty cycles provided using bootstrap capacitor circuit negate this configurations selection. The gate driver was selected for this application as it provides level shifting, gate voltage higher than the supply voltage and operation in a wide range of duty cycles and switching frequencies in a single compact package.

| Method | Basic Circuit | Main Features |
| :---: | :---: | :---: |
| Floating Gate Drive Supply |  | - Full gate control for infinite periods of time. <br> - One isolated supply required for each high side MOSFET => significant cost. <br> - Level shifting required for ground referenced signal $=>$ must sustain full voltage and switch fast with low power consumption <br> - Opto isolators expensive with limited bandwidth and noise sensitive |
| Pulse <br> Transformer |  | - Simple and cost effective but has limitations. <br> - Operation over a wide duty cycles requires additional circuitry. <br> - Transformer size increases significantly as frequency decreases. <br> - Significant parasitics create less than ideal operation with fast switching waveforms. |
| Charge Pump |  | - Can be used to generate a gate voltage higher than the supply voltage $\left(\mathrm{V}_{\mathrm{s}}\right)$ controlled by a level shifter or to "pump" the gate when device is on. <br> - Requires level shifting circuitry and turn on times too long for fast switching applications. <br> - Gate can be turned on for an infinite time period. <br> - Inefficiencies in voltage pumping circuit may require more that two stages of pumping |
| Bootstrap |  | - Simple and inexpensive to implement but has same limitations as pulse transformer, in that duty cycle and on-time are constrained by bootstrap capacitor refresh rate. <br> - Power dissipation can be significant when capacitor charged from high voltage supply. <br> - Requires level shifting circuitry |
| Carrier <br> Drive |  | - Gives full gate control for infinite period of time. <br> - Improved switching performance requires additional circuitry. |
| Gate drive integrated circuit <br> (IC) <br> or <br> Gate driver |  | - Provides level shifting referenced to ground signal in a compact package that requires only a few addition components <br> - Is able to sustain full voltage applied to MOSFET and provide very fast switching speeds with low power consumption. <br> - Operate in bootstrap mode or with floating supply. <br> - It can operate over a wide range of frequencies and duty cycles. |

Table 5.5: Gate drive configurations

The specific device selected for use in this application is the International Rectifier IR2110 gate driver (International Rectifier 2005b) is illustrated in Figure 5.11 (functional block diagram) and Figure 5.12 (typical connection diagram). This device is a high voltage and high speed gate driver with independent high and low side referenced output channels. The floating high side channel is designed for bootstrap operation and
can drive a MOSFET that operates up to 600V. The input logic is TTL/CMOS compatible down to 3.3 V logic. The signals from the input logic are coupled to the individual channels through high noise immunity level translators. The high side channel is built into what is defined as an "isolation tub" that is capable of floating from 600 V to -5 V with respect to ground. This 'tub' floats at a potential of $\mathrm{V}_{\mathrm{S}}$, which is established by the voltage applied to $\mathrm{V}_{\mathrm{B}}$. The gate charge for the high side MOSFET is provided by the bootstrap capacitor, $\mathrm{C}_{\mathrm{B}}$, which is charged by the $\mathrm{V}_{\mathrm{CC}}$ supply through the bootstrap diode during the time when the device is off (assuming that $\mathrm{V}_{\mathrm{S}}$ swings to ground during that time, which generally is always the case). As the capacitor is charged from a low voltage source the power consumed to drive the gate is small.


Figure 5.11: Functional block diagram with lead definitions for the IR2110 gate driver


Figure 5.12: Typical connection diagram when using IR2110 gate driver

A number of issues need to be addressed when using the IR2110 gate driver including, the selection of the bootstrap components (capacitor, $\mathrm{C}_{\mathrm{B}}$, and diode, $\mathrm{D}_{\mathrm{B}}$ ) and minimising negative spikes at the high side floating supply pin, $\mathrm{V}_{\mathrm{S}}$. Negative spikes are minimised by reducing parasitic inductances through careful layout, discussed in section 5.7.2, improved local decoupling by using low ESR capacitors in parallel with $C_{B}$ and capacitor at low side supply ( $\mathrm{V}_{\mathrm{CC}}$ to COM ), selecting the gate resistor value to minimise the amplitude to the negative spike.

### 5.3.2 Determination of Peak Gate Drive Current

Power MOSFETs have a large gate capacitance that must be charged to achieve device turn on. The gate drive circuit must provide sufficient current to charge the equivalent gate capacitance in the required time interval. The total gate charge is the key specification in determining gate drive requirements as it brings together all device charge values and accounts for the "Miller effect" [(Dunn 2003), (Dunn 2004), (Supertex 2001), (Barkondarian 2000) and (Andreycak 1999)].

The process of charging the gate is defined in three stages as illustrated in Figure 5.13 [(Dunn 2003) and (Barkondarian 2000)]. The first stage is the charging of the gatesource capacitance, $\mathrm{C}_{\mathrm{GS}}$, the gate-drain capacitance, $\mathrm{C}_{\mathrm{GD}}$, or the Miller capacitance is also charging but it is very low. Once $\mathrm{C}_{\mathrm{GS}}$ is charged up to the gate threshold voltage, the device begins to turn on and the current ramps up to its full value. On reaching the full current value, the drain-to-source voltage begins to collapse. It is at this point that the gate voltage levels out due to the Miller capacitance being charged as the drain voltage falls. When the drain voltage has fallen to its final level, the gate capacitance (both $\mathrm{C}_{\mathrm{GS}}$ and $\mathrm{C}_{\mathrm{GD}}$ ) is charged the rest of the way to the gate drive voltage.


Figure 5.13: (a) Gate capacitance model for MOSFET and (b) gate charge waveform

The gate charge value simplifies the calculation of the current required from the gate drive circuit to turn on and turn off the MOSFET, as illustrated in equation 5.10 [(Dunn 2003), (Dunn 2004), (Barkondarian 2000), (Hussain 2002), (Dorf 1999), (Winters 2002) and (Andreycak 1999)].

$$
\begin{equation*}
I_{G}=\frac{Q_{G(t o t)}}{\Delta t} \tag{5.10}
\end{equation*}
$$

where $I_{G}$ is the gate drive current, $Q_{G(t o t)}$ is the total gate charge for the MOSFET and $\Delta \mathrm{t}$ is either the turn on or rise time, $t_{r}$, or the turn off or fall time, $t_{f}$, for the MOSFET, which are specified in the device data sheet. The rise and fall times and the total gate charge specifications for the output devices determine the amount of gate drive current to source or sink. The relevant specifications for all suitable MOSFETs for the converter are provided in Table 5.5.

The power dissipated by the IR2110 gate driver is typically < 500 mW (Clemente 1990) and this would have a negligible effect on the overall converter efficiency. The power dissipated to charge the device gate capacitance $Q_{g(t o t)}$ whenever a capacitor is charged or discharged through a resistor is defined by equation 5.11, [(Dunn 2003), (Dunn 2004), (Supertex 2001) and (Andreycak 1999)].

$$
\begin{equation*}
P_{G}=Q_{g(t o t)} V_{G} f \tag{5.11}
\end{equation*}
$$

where $Q_{g(t o t)}$ is the total gate charge, $V_{G}$ is the gate voltage and $f$ is the switching frequency of 25 kHz . The step by step calculation of the peak source and sink currents for the Fairchild FDP047AN08A0 are provided in detail in the following section and the results for all the devices are included in the Table 5.5. The gate voltage of 12 V is sufficient, as a greater value has little effect on reducing the on-resistance of the MOSFET (Andreycak 1999).The peak source current and peak sink current are determined as follows:

$$
\begin{aligned}
& I_{G(\text { turn on })}=3.14 \mathrm{~A} \\
& I_{G(\text { turn off })}=6.13 \mathrm{~A}
\end{aligned}
$$

The power dissipated to charge the device gate and consumed by the gate drive circuitry are determined as follows:

$$
P_{G}=41.4 \mathrm{~mW}
$$

where $Q_{g(t o t)}$ is the total gate charge provided in Table $5.5, V_{G}$ is the gate voltage of 12 V and $f$ is the switching frequency of 25 kHz .

| Gate Drive | Data |  |  | Results |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\boldsymbol{V}_{\boldsymbol{G}}=\mathbf{1 2 V}$ | $\boldsymbol{t}_{\boldsymbol{r}}$ | $\boldsymbol{t}_{\boldsymbol{f}}$ | $\boldsymbol{Q}_{\boldsymbol{G} \text { (tot) }}$ | $\boldsymbol{I}_{\boldsymbol{G} \text { (turn on })}$ | $\boldsymbol{I}_{\boldsymbol{G} \text { (turn off) }}$ | $\boldsymbol{P}_{\boldsymbol{G}}$ |  |
| Device No. $=\mathbf{2}$ | $(\mathrm{ns})$ | $(\mathrm{ns})$ | $(\mathrm{nC})$ | $(\mathrm{A})$ | $(\mathrm{A})$ | $(\mathrm{mW})$ |  |
| Fairchild |  |  |  |  |  |  |  |
| FDP047AN08A0 | 88 | 45 | 138 | 3.14 | 6.13 | 41.4 |  |
| FDP060AN08A0 | 79 | 38 | 95 | 2.41 | 5 | 28.5 |  |
| Philips |  |  |  |  |  |  |  |
| BUK7506-76B | 56 | 48 | 91 | 3.25 | 3.79 | 27.3 |  |

Table 5.5: MOSFET data and gate drive calculations

As can be seen from the results in Table 5.5, the current requirement for the MOSFETs in parallel is significantly more than the IR2110 gate driver can provide so a high current buffer was a requirement in this application.

### 5.3.3 High Current Buffer

The high current gate drive buffer circuit used in this application is described in [(Clemente 1990) and (Kiraly 2004)] and is illustrated in Figure 5.14.


Figure 5.14: High current gate drive buffer circuit

This circuit can deliver 8A peak output current, has high input impedance and low output impedance. When the input changes states the resistor, $\mathrm{R}_{1}$, limits the current
through $\mathrm{Q}_{1}$ and $\mathrm{Q}_{2}$ when both transistors are on for a few ns. The output stage formed by $\mathrm{Q}_{3}$ and $\mathrm{Q}_{4}$ can be sized to suit the peak current demand and also corrects the logic flow from the gate drive input to output. The truth table for the input, output and transistor states is provided in Table 5.6.

| Input | Q1 | Q2 | Q3 | Q4 | Output |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $H$ | Off | On | On | Off | $H$ |
| L | On | Off | Off | On | L |

Table 5.6: Truth table for gate drive buffer

There is a delay in the turn on, due to the RC time constant formed by $\mathrm{R}_{1}$ and the input capacitance of the output transistor, which is beneficial in providing a dead time in the overall converter operation. The configuration as it is implemented in this application is shown in Figure 5.15.


Figure 5.15: High and low side gate drive using the IR2110 gate driver and high current buffer circuits

### 5.3.4 Determination of peak current for the buffer gate drive circuit

The calculation of the peak input gate drive current for the buffer circuit determines the gate driver selection. When $12 \mathrm{~V}\left(V_{G}\right)$ is applied to the buffer input, the p-channel device $\left(\mathrm{Q}_{1}\right)$ turns off, the n -channel device $\left(\mathrm{Q}_{2}\right)$ turns on and $\mathrm{Q}_{3}$ turns on and current flows into
the gate and thereby charges the gate capacitance. Therefore peak current requirement is determined using the combined gate charge values for $\mathrm{Q}_{1}$ and $\mathrm{Q}_{2}$, and using either the fall time of $\mathrm{Q}_{1}$ or the rise time of $\mathrm{Q}_{2}$, which ever is greater. The power dissipation is determined from the following device data as illustrated in Table 5.7 [(Fairchild 2002a, 2004) and (Philips 2002)].

| MOSFET | $\mathbf{Q}_{\mathbf{G}(\text { (tot) }} \mathbf{( n C )}$ | $\mathbf{t}_{\mathbf{r}}(\mathbf{n s})$ | $\mathbf{t}_{\mathbf{f}}(\mathbf{n s})$ |
| :---: | :---: | :---: | :---: |
| Philips BUK 7506-76B | 91 | 56 | 48 |
| Fairchild FDP047AN08A0 | 138 | 88 | 45 |
| Fairchild FDP060AN08A0 | 95 | 79 | 38 |
| IRF IRFD9110 | 8.7 | 27 | 17 |
| IRF IRFD110 | 8.3 | 16 | 9.4 |

Table 5.7: MOSFET specification data

The peak source and sink current are determined using equation 5.10 , while the power dissipated to charge the gate drive capacitance is determined by equation 5.11. The results are given in Table 5.8.

| $\mathbf{I}_{\mathbf{G} \text { (turn on) }}(\mathbf{A})$ | $\mathbf{I}_{\mathbf{G}_{\text {turn off }}(\mathbf{A})}$ | $\mathbf{P}_{\mathbf{G}}(\mathbf{m W})$ |
| :---: | :---: | :---: |
| 1 | 0.63 | 5.1 |

Table 5.8: Buffer circuit calculations

The gate driver circuit must source up to 1 A and it must be capable of sinking 0.63 A . The IR2110 (International Rectifier 2005b) can sink and source 2A, so is suitable for use in this application. The total power dissipation for the gate driver is $\approx 500 \mathrm{~mW}$ (IR2110 < 500 mW and buffer < 5mW) and therefore has negligible contribution to the overall converter power losses.

### 5.3.5 Bootstrap Components

As noted in section 5.3.1, the voltage between the $\mathrm{V}_{\mathrm{b}}$ and $\mathrm{V}_{\mathrm{s}}$ pins ( $\mathrm{V}_{\mathrm{bs}}$ ) of the IR2110 gate driver supplies the high side gate driver circuitry and should remain between 10 15 V in order to fully turn on the MOSFET. This requires the selection of the appropriate bootstrap capacitor and diode values.

### 5.3.5.1 Calculating the bootstrap capacitor value

The minimum charge, $Q_{b s}$, that needs to be supplied by the bootstrap capacitor, $C_{b s}$, is determined by the equation (Adams 2004):

$$
\begin{equation*}
Q_{b s}=2 Q_{g}+\frac{I_{q b s(\max )}}{f}+Q_{L S}+\frac{I_{C b s(l e a k)}}{f} \tag{5.12}
\end{equation*}
$$

where $Q_{g}$ is the gate charge of high side MOSFETs, $f$ is the frequency of operation, $I_{\text {Cbs(leak) }}$ is the bootstrap capacitor leakage current and $Q_{L S}$ is the level shift charge required per cycle which equals 5 nC for the IR2110 (International Rectifier 2005b). In order to minimise the amount of ripple on the high side gate voltage $\left(\mathrm{V}_{\mathrm{BS}}\right)$, the minimum charge in the bootstrap was multiplied by a factor of 15 (rule of thumb) (Adams 2004). The capacitor value is determined by the equation (Adams 2004):

$$
\begin{equation*}
\mathrm{C}_{\mathrm{bs}} \geq 15\left[\frac{2 Q_{b s}}{V_{C C}-V_{f}-V_{L S}-V_{M i n}}\right] \tag{5.13}
\end{equation*}
$$

where $V_{f}$ is the forward voltage drop across the bootstrap diode, $V_{L S}$ is the voltage drop across the low side MOSFET (or load for the high side driver) and $V_{\text {Min }}$ is the minimum voltage between $\mathrm{V}_{\mathrm{B}}$ and $\mathrm{V}_{\mathrm{S}}$ of the IR2110 gate driver.

The calculation for the bootstrap components is implemented step-by-step for the Fairchild FDP047AN08A0 and the results are tabulated in Table 5.9. The gate charge for the high side MOSFET was determined from the combination of the high side buffer circuit and the two high side MOSFETs of the converter. The total gate charge values for the devices are given in Table 5.7. On high side circuit activation, the charge ( $Q_{g}$ ) must be supplied to the gates of $\mathrm{Q}_{2}$ and $\mathrm{Q}_{3}$ of the buffer circuit and the two parallel high side MOSFETs of the converter and on deactivation, charge is only supplied to $\mathrm{Q}_{1}$ and Q4.

| $Q_{g}(\mathbf{n C})$ | $I_{\text {Cbs (leak })}(\mu \mathrm{A})$ | $Q_{L S}(\mathrm{nC})$ | $f(\mathrm{kHz})$ | $V_{f}(\mathbf{V})$ | $V_{\text {Min }}(\mathrm{V})$ | $V_{L S}(\mathrm{~V})$ | $V_{C C}(\mathrm{~V}$ | $I_{\text {gbs }(\max )}(\mathbf{n A})$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 293 | 3 | - 5 | 25 | 0.875 | 13 | 0.5 | 15 | 230 |
| ${ }^{1}$ IR2110 |  |  |  |  |  |  |  |  |

Table 5.9: Bootstrap capacitor operating conditions

The minimum charge that needs to be supplied by the bootstrap capacitor is determined from equation 5.12.

$$
Q_{b s}=590 \mathrm{nC}
$$

The bootstrap capacitor value is determined from equation 5.13. A $47 \mu \mathrm{~F} 100 \mathrm{~V}$ capacitor was used in order to provide sufficient margin.

$$
C_{b s} \geq 28 \mu \mathrm{~F}
$$

### 5.3.5.2 Selecting the Bootstrap Diode

The diode, $D_{b s}$, must be able to block the full supply voltage of 42 V when the high side device is switched on. It must have a fast recovery time to minimise the amount of charge that is fed back to the voltage supply, $V_{C C}$, of the IR2110 gate driver. The high temperature reverse leakage current is important if the capacitor has to store charge for long periods of time. The current rating for the diode is the product of the charge, $Q_{b s}$, and the switching frequency, $f$, (Adams 2004). The relevant component data and current calculation data is provided in Table 5.10. The diode that meets these requirements is the MUR120 (ON Semiconductor 2005). It has a worst-case forward voltage, $V_{f}$, drop of 0.875 V .

$$
\begin{align*}
& I_{f}=Q_{b s} f  \tag{5.14}\\
& I_{f}=15 \mathrm{~mA}
\end{align*}
$$

| $V_{r r m}(\mathbf{V})$ | $\boldsymbol{t}_{\text {rr(max) }}(\mathbf{n s})$ | $\boldsymbol{I}_{\boldsymbol{f}}(\mathbf{A})$ | $\boldsymbol{V}_{\boldsymbol{f}}(\mathbf{V})$ | $\boldsymbol{f}(\mathbf{k H z})$ |
| :---: | :---: | :---: | :---: | :---: |
| 42 | 100 | 15 | 0.875 | 25 |

Table 5.10: Bootstrap diode data

### 5.3.5.3 Gate resistor selection

Increasing the value of the series gate resistance rapidly reduces the amplitude of the negative spikes due to stray inductance (e.g. track length, component lead length above the circuit board) at the high side return $\left(\mathrm{V}_{\mathrm{s}}\right)$. The value of the series gate resistor reduces the switching speed and therefore the value of $d v / d t$ and is based on the graph of turn-off time versus series gate resistance shown in Figure 5.16 (Clemente 1990). Selecting a resistor value just on the "knee" provides a good trade-off between the spike amplitude and the turn-off speed. The gate resistor dampens any oscillations in the gate circuit caused by a resonant tank formed by parasitic inductances and capacitances inherent in the MOSFET and contributed by circuit connections (Fairchild Semiconductor 1998). A $22 \Omega$ gate resistance was selected for the input to the gate drive
buffer circuit, while a $4.7 \Omega$ gate resistor was placed on each MOSFET in a parallel configuration and was located as close as physically possible to the gate of the device.


Figure 5.16: Gate resistance vs. negative voltage spike amplitude and turn-off time

### 5.3.6 Blanking Time Delay

A time delay needed to be provided between the switching states of the high and low side switches in order to prevent a current shoot through condition. This time delay is defined as the blanking time. There are a number of elements contributing to the blanking time. There is a 25 ns difference between the turn-on and turn-off propagation delay times of the IR2110 gate driver (International Rectifier 2005b), to ensure no conduction overlap of the converter power devices. A resistor diode network was placed at the input to the buffer circuit to provide additional margin of safety as illustrated in Figure 5.17. The diode would be reversed biased at turn-on thereby generating a delay corresponding to the RC time constant of the gate resistor and the input capacitance of the buffer circuit. The diode would be forward bias at turn-off to provide a low impedance path for fast turn-off. A 1N4148 (Fairchild 2007) diode was used for this application.

### 5.3.7 Electrical isolation

Electrical isolation for the control logic signal for the gate drive circuit was provided using HPCL-263A optocouplers (Agilent Technologies 1999a). This device provides high $\mathrm{dv} / \mathrm{dt}$ rating up to $1000 \mathrm{~V} / \mu \mathrm{s}$ and can operate at speeds up to $10 \mathrm{Mbit} \mathrm{s}^{-1}$. The implementation of this device required an isolated power supply for the optocoupler output and the gate drive circuit. The optocouplers were mounted on an interface board or the microcontroller board to further reduce susceptibility to common-mode noise generated by the full-bridge converter circuit (Agilent Technologies 1999b).


Figure 5.17: Full Bridge Converter

### 5.4 DC Source Capacitor Analysis

Essentially during magnetization and demagnetization, the full-bridge circuit mimics the operation of a boost converter, while during freewheeling mode, it operates like a buck converter during freewheeling operation. The dc source needs to have low internal impedance for the instantaneous current and a large capacitor can provide this low impedance path (Mohan 1995). It provides the regulated dc connection between the dc source and the inverter (Krein 1998) and (Lander 1981). Selecting the dc source capacitor requires knowledge of the general capacitor parameters, the specific application requirements in order to determine the correct value for the application.

### 5.4.1 Capacitor Parameters

Capacitors are selected based on the required capacitance, the rated operating voltage, the RMS current, and frequency, (Mohan 1995), (Vishay 2004), (Nichicon 2004) and (BHC 2004). Aluminium electrolytic capacitors provide large capacitance per unit volume and high ripple current capability (Mohan 1995) and (BHC 2004). The rated voltage is the peak value of pulsed voltage that is applied continuously to the capacitor. Any pulsating voltage across a capacitor yields an alternating current flowing through the capacitor and the RMS value of this alternating current is called the ripple current. The heat generated by the ripple current is an important factor in determining the useful life of the capacitor and higher frequency operation yields greater reactive power dissipation and temperature rise in the capacitor (Vishay 2004).

### 5.4.2 Specific Application Requirements

DC source capacitors supply high currents when there are peak requirements, so they tend to be abruptly charged and discharged and they need to have a high thermal rating to handle the relatively high reactive power dissipation (Siemens Matsushita 2004). Under the proposed 42 -Volt electrical system, electrical components, including capacitors, must withstand higher operating temperatures of $150^{\circ} \mathrm{C}$ and above (Epcos 2003). The requirement for large capacitance values can necessitate that the capacitors be connected in parallel to achieve the correct value. Individual protection may be required against sudden discharge of the entire capacitor bank into a defective capacitor (Vishay 2004) and (BHC 2004). It is also important that there is a balance of the current distribution in all capacitor branches (Nichicon 2004) and (Power Designers 2004).

### 5.4.3 Determining Capacitance Value

The percentage voltage ripple on the dc source capacitor, $\mathrm{C}_{\mathrm{S}}$, determines the actual capacitor value. High speed generating defines the worst case cycle of operation for the voltage ripple as the switching period is determined by the speed of the machine. It has a minimum value of 2.2 ms at 4500 rpm . It is assumed that the capacitor voltage is maintained at 42 V maximum and that excess current is directed to the battery voltage supply by $\mathrm{Q}_{\mathrm{G}}$ as illustrated in Figure 5.18. All the ripple current through $\mathrm{Q}_{4}$ flows through the capacitor. The shaded area in Figure 5.19 represents the charge $\Delta \mathrm{Q}$. Therefore the peak-to-peak voltage ripple is represented by equation 5.15 , which when rearranged allows for the calculation of the capacitor as illustrated in equation 5.16 (Hart 1997).

$$
\begin{gather*}
\Delta V_{S}=\frac{\Delta Q}{C_{S}}=\frac{I_{S} D T_{s}}{C_{S}}=\frac{V_{S} D T_{s}}{R C}  \tag{5.15}\\
C_{S}=\frac{V_{S} D T_{s}}{\Delta V_{S} R} \tag{5.16}
\end{gather*}
$$

The peak-to-peak voltage ripple in this application is assumed to be the dip in the dc source voltage, $V_{S}$. The percentage ripple, $\Delta V_{S} / V_{S}$, on the dc source capacitor is defined to be $10 \%$, the duty cycle, $D$, for the magnetization period during high speed generating is $40 \%$, and the period, $T_{s}$, is 2.2 ms . The resistance value, $R$, is determine from the series resistance, ESR, of the electrolytic capacitor (typically > 25m $\Omega$ ) (Epcos 2006), the phase winding resistance of the SRM (typically $0.8 \mathrm{~m} \Omega$ ) (Motion System Tech 2002), and the on-resistance of the MOSFETs (typically $4 \mathrm{~m} \Omega$ ) (Fairchild 2004). Using the above data, the value of dc source capacitor is determined to be 0.3 F . This is quite a large capacitor value and would add excessive cost to the overall system. As the capacitor requires a voltage rating of 100 Vdc (double the maximum power supply value), the most cost effective device would be the $10,000 \mathrm{uF}$ capacitor. In order to implement the converter with this device, the magnetisation duty cycles needed to be limited at each speed of operation. Table 5.11 illustrates the magnetisation duty cycles and percentage voltage ripple values for the various generating speeds of operation when using this capacitor value. Ultimately, the capacitor selection is a compromise between cost and acceptable performance limits.


Figure 5.18: Full-Bridge Converter with charging circuit


Figure 5.19: Voltage ripple on the dc source capacitor, $\mathrm{C}_{\mathrm{S}}$

| $\Delta \boldsymbol{V}_{\boldsymbol{S}} / \boldsymbol{V}_{\boldsymbol{S}}(\%)$ | $\boldsymbol{D}(\%)$ | $\boldsymbol{T}_{\boldsymbol{s}}(\mathrm{ms})$ | Speed (rpm) |
| :---: | :---: | :---: | :---: |
| 5 | 25 | 0.04 | 2000 |
| 10 | 1 | 2.22 | 4500 |
| 20 | 3 | 2.22 | 4500 |
| 50 | 7 | 2.22 | 4500 |
| 10 | 2 | 1.67 | 6000 |
| 20 | 4 | 1.67 | 6000 |
| 50 | 10 | 1.67 | 6000 |

Table 5.11: Magnetization duty cycles and percentage voltage ripple values at various generating speeds of operation when using a $10,000 \mathrm{uF}$ capacitor

### 5.5 Bus Bar Analysis

Two types of power distribution technologies are used in modern equipment: wiring harness and bus bars. Wiring harnesses are suitable for low current low volume applications while bus bars are more suitable to high current that require low inductance (Hill Technical Sales 2004). Large di/dt and leakage inductances can be a significant problem in the power supply leads of circuits. When stray inductance are reduced in the leads so to are the transient voltage spikes and noise that lead to significant EMI and parasitic oscillations (Mohan 1995), (Hanley 2003) and (Hill Technical Sales 2004). Bus bars have many advantages and with the correct layout out can provide an ideal solution for high current applications.

### 5.5.1 Bus bar implementation

The use of bus bars allows for the reduction in conductor losses, reduce stray inductance and simplify power bus assembly and routing. Bus bars provide a greater surface area so can handle more current with reduced losses (Dossert 2004) and (Hanley 2003). They yield an increase in circuit reliability due to fewer connections, as would be the case with cabling (Hanley 2003). Rectangular bus-bars reduce the self-inductance by $1 / 3$ to $1 / 2$ when compared to round conductors of equal length and cross sectional area (Hanley 2003) and (Hill Technical Sales 2004). A laminated structure helps to control both self and mutual inductance (Hill Technical Sales 2004). It consists of interleaving layers of ground planes and voltage layers of different polarities. Bus-bars can simplify routing of power conductors and can reduce probability of errors in assembly due to their rigid structure (Hanley 2003). Conductors can be made from a variety of metals, including copper, nickel, gold or aluminium, but cost and weight are the deciding factors in an application (Mohan 1995), (Hanley 2003) and (Eldre 2004). While more aluminium may be needed in a conductor than copper, 1.66 times more cross sectional area is required to conduct the same amount of current, it has $55 \%$ less weight when compared
with copper and is less expensive (Hanley 2003) and (States Department of the Interior 2000).

### 5.5.2 General bus bar structure

The structure of the bus bar is critical for the reduction of stray inductance, elimination of noise and arcing, improving current distribution in parallel capacitors and reducing the need for snubber circuits for the power devices. A laminated structure with large plates in a sandwich with thin insulators is the most space efficient bus bar structure (Mohan 1995), (Power Designers 2004), (Hanley 2003) and (Eldre 2004). The large plates create the interleaving layers which minimise mutual inductances (Hill Technical Sales 2004). Traditionally bare bus bars do not suppress noise, are bulky, have potential to arc between the plates and are costly to assemble (Eldre 2004). The laminated structure reduces noise due to the interleaving layers (Hanley 2003). Creepage and arcing is eliminated by increasing the distance the insulator protrudes past the plates (Mohan 1995). Laminated bus bars allow for equal current distribution to parallel capacitors (Mohan 1995) and (Power Designers 2004). The structure must be as compact as possible as long interconnection distances between switching devices increases bus inductance, which requires complex snubber circuits for protection, adding to system cost (Hill Technical Sales 2004).

### 5.6 Current Sensors

In order to implement precise current regulation in a power converter design, the choice of current sensor is critical. When implementing current regulation, consideration needs to be given to the type of current being measured, the operating range of the current, the required output signal, measurement accuracy, available power supply and the working voltage. Additionally, dynamic operating parameters need to be considered, which includes frequency range, di/dt and dv/dt. Finally, consideration must be given to the environmental variables - temperature, vibration and shock, and the presence of external fields. Three current sensing schemes - shunt resistor, current transformer and Hall effect - were evaluated for suitability in this particular application.

### 5.6.1 Shunt Resistor

With this scheme, the voltage drop across the shunt resistor is proportional to the current flowing in the circuit (Dickinson 2002) and additional circuitry is required to improve signal quality (Lepkowski 2003). This measurement can be implemented in
either high side or low side configuration as illustrated in Figure 5.20. The high side measurement is the preferred method, as it is less intrusive as long as the sense resistor is small. The low side measurement is easier to implement but disrupts the ground path of the load and this can cause noise problems in the system. In either case, the load current, $I_{L}$, is determined using the equation (Lepkowski 2003).

$$
\begin{equation*}
I_{L}=\frac{V_{M}}{R_{M}} \tag{5.17}
\end{equation*}
$$

The shunt resistor measurement scheme is inexpensive to implement but it requires additional circuitry to improve signal quality and it has no electrical isolation (Mohan 1995) and (Lepkowski 2003). This scheme is impractical for use in circuits where the current measurements are above 20A and has poor accuracy over a wide temperature range (Dickinson 2002) and (Lepkowski 2003).


Figure 5.20: Shunt resistor measurement schemes, (a) High-side and (b) low-side

### 5.6.2 Current Transformer

These sensors use the principle of transformers where the ratio of the primary current, $I_{P}$, to the secondary current, $I_{S}$, is a function of the turns ratio, $N$, as illustrated in Figure 5.21 and described using equation 5.18 (Lepkowski 2003). They are simple to implement and have no drive circuits. The scheme provides galvanic isolation but an AC signal is required to prevent the transformer from saturating (Mohan 1995), (Dickinson 2002) and (Lepkowski 2003).

$$
\begin{equation*}
I_{S}=\frac{I_{P}}{N} \tag{5.18}
\end{equation*}
$$




Figure 5.21: Current sensing transformer

### 5.6.3 Hall Effect Transducer

Hall effect is based on the principle that a voltage, $\mathrm{V}_{\mathrm{H}}$, is developed when current flows, $\mathrm{I}_{\mathrm{C}}$, in a direction perpendicular to a magnetic field, B, as illustrated in Figure 5.22 (Melexis 1997) and (Lepkowski 2003).


Figure 5.22: The Hall Effect principle

There are two main techniques: open loop and closed loop (Dickinson 2002) and (Lepkowski 2003). The open loop scheme amplifies the Hall generator voltage to provide an output signal as illustrated in Figure 5.23a. Closed loop transducers uses the output voltage of the Hall element to develop a secondary or compensation current in a secondary coil as illustrated in Figure 5.23b. This secondary current in conjunction with the secondary ratio generates a magnetic flux that is equal in magnitude but opposite in polarity to the flux created in the primary current to yield a total flux of zero (Lepkowski 2003).

Both techniques are suitable for measurement of dc, ac and complex current waveforms in power applications that need galvanic isolation (Melexis 1997) and (LEM Components 2004). The two schemes provide a robust solution to environmental disturbances, including vibration, moisture and dirt or oil film (Gilbert 2002). The closed loop design has the advantage of very good accuracy and linearity, low gain drift,
wide bandwidth ( $0 \mathrm{~Hz}-200 \mathrm{kHz}$ ), and fast response time, but the current measurement is limited due to the finite compensation current (Mohan 1995), (Dickinson 2002), (Melexis 1997), (Lepkowski 2003) and (LEM Components 2004). Closed loop transducers have very good reaction times (less than $1 \mu \mathrm{~S}$ ) and are able to measure $\mathrm{di} / \mathrm{dt}$ of $50-500 \mathrm{~A}^{-1}$ and greater, which makes them suitable for short circuit protection (LEM Components 2004).


Figure 5.23: (a) Open loop Hall Effect transducer, (b) closed loop Hall Effect transducer

Recently, a hybrid scheme (LEM Components 2004) has being developed that works like an open loop Hall Effect transducer up to 10 kHz and like a current transformer at higher frequencies. Both Hall effect and current transformer signals are electronically added to form a common output signal as illustrated in Figure 5.24.


Figure 5.24: Combined Open loop and closed loop Hall effect transducer

This scheme is similar to closed loop Hall effect transducers but only requires a small secondary power supply (LEM Components 2004). At higher frequencies, the current transformer yields high bandwidth and fast response. Open loop at low frequencies
implies that there are gain and offset drifts with temperature and a moderate level of accuracy. Low frequency open loop operation requires more expensive construction when compared with the closed loop scheme (LEM Components 2004). Bandwidth, response time and di/dt behaviour are similar to closed loop transducers although it is slightly less efficient at high frequencies (LEM Components 2004).

### 5.6.4 Sensor Selection and Implementation

The closed loop Hall effect sensor provides the most suitable option for this application for the reason that the sensor provides electrical isolation, has large bandwidth, fast response time and is therefore able to provide the response times necessary for current overload protection. The specific device selected for this application is the LA 100P/SP13 (LEM Components 2005). This device allows the bus bar connection to the motor phase terminal to pass through the sensor aperture as illustrated in Figure 5.25(a).

In order to implement the current sensor in this application, the following items had to be addressed: the layout of the power conductors and the sensor output signals, the power supply requirements, the determination of the measurement resistor and finally any signal conditioning requirements for the transducer output signals. The specific layout issues are discussed in section 5.7.6. The closed loop sensor requires a bipolar power supply (LEM Components 2005) $\pm 15 \mathrm{~V}$ power supply provides the power requirement.

The appropriate measurement resistor, $\mathrm{R}_{\mathrm{M}}$ is determined based on the range provided in the data sheet, and depends on the maximum ambient temperature. The maximum measured voltage, $\mathrm{V}_{\mathrm{M}}$, is determined using equations 5.19 and 5.20

$$
\begin{align*}
& \mathrm{I}_{\mathrm{S}}=\mathrm{I}_{\mathrm{P}}\left(\mathrm{~N}_{\mathrm{P}} / \mathrm{N}_{\mathrm{S}}\right)  \tag{5.19}\\
& \mathrm{V}_{\mathrm{M}}=\mathrm{R}_{\mathrm{M}} \mathrm{I}_{\mathrm{S}} \tag{5.20}
\end{align*}
$$

where $I_{S}$ is the secondary current, $I_{P}$ is the primary peak current, $\mathrm{N}_{\mathrm{P}}$ is the number of primary turns and $\mathrm{N}_{\mathrm{S}}$ is the number of secondary turns (LEM Components 2004).The connections to the current sensor are implemented as shown in Figure 5.25b (LEM Components 2005).


Figure 5.25: (a) Current sensor physical layout, (b) current sensor connections

### 5.7 Circuit Layout Considerations

### 5.7.1 Full Bridge Circuit

In a typical bridge circuit, the critical stray inductances that need to be reduced are in the high current path of the circuit. Stray inductances in the "dc path" are due to the wiring inductances between the MOSFETs and the decoupling capacitors (dc source capacitor), while stray inductances in the "ac path" are due to the wiring inductances between the MOSFETs (Clemente 1990). Stray inductance was reduced by using a laminated bus structure to minimise connection lengths (input connections from the source capacitor, MOSFETs interconnections and output connections to the SRM). Parallel MOSFETs were mounted in a symmetrical pattern in order to further minimise stray circuit inductance and they were mounted to a common heat spreader as this provided close thermal coupling between devices. The detailed layout of the full bridge circuit can be seen in Figure 5.26a (top view), 5.26b (side view) and Figure 5.26c (circuit schematic). The MOSFET drains were connected directly to the heat spreader, while the sources were connected to the printed circuit board mounted above the MOSFETs (Murray 2001). The source connections were connected symmetrically using copper bus conductor. The laminated bus bar was mounted centrally to maximise symmetry and is described in detail in section 5.7.5.


Figure 5.26: Complete converter illustrations (a) top view (b) side view and (c) circuit schematic

### 5.7.2 MOSFET gate driver

Negative voltage spikes are generated at the $\mathrm{V}_{\mathrm{s}}$ pin of the IR2110 gate driver due to $\mathrm{di} / \mathrm{dt}$ in the stray inductance in the ac path (Clemente 1990). Once stray inductance was reduced in the ac path, decreasing switching speed with a gate resistor further reduced the di/dt-induced spikes. The circuit layout minimised the stray inductance on the gate drive charge/discharge loop by minimising track lengths. This reduces oscillations and improves switching speed and noise immunity to prevent dv/dt turn-on (Clemente 1990). The connections went directly from the gate driver pins to the MOSFET pins using parallel tracks in a PCB layout. The IR2110 gate driver was placed as close as possible to the power switches and local decoupling was improved by using one lowESR capacitor for the bootstrap capacitance and in the $\mathrm{V}_{\mathrm{CC}}-\mathrm{COM}$ and $\mathrm{V}_{\mathrm{DD}}-\mathrm{V}_{\mathrm{SS}}$ pin locations of the IR2110. The low side capacitance, $\mathrm{V}_{\mathrm{CC}}-\mathrm{COM}$ pins, was ten times greater than the bootstrap capacitor (Clemente 1990). A ceramic capacitor was placed as close as possible to the $\mathrm{V}_{\mathrm{B}}$ and $\mathrm{V}_{\mathrm{S}}$ pins of the gate driver when using an aluminium electrolytic capacitor for the bootstrap capacitor, as the low-ESR capacitor provided good de-coupling.

### 5.7.3 Gate drive buffer circuit

A $10 \mu \mathrm{~F}$ electrolytic and a $0.1 \mu \mathrm{~F}$ ceramic decoupling capacitors were mounted physically close to the buffer output to nullify the effects of stray inductance (Kiraly 2004). Short parallel tracks in a PCB layout were used to connect the buffer output to the parallel MOSFETs. A single point ground (ground plane of the centrally located laminated bus bar) was used to connect the sources of the low side power devices to a common point, which defined the common ground. A low-ESR decoupling capacitor was selected for use in the power stage, typically $10 \mu \mathrm{~F}$ to $1000 \mu \mathrm{~F}$ depending on the layout and switching current.

### 5.7.4 Optocoupler electrical isolation

A $0.1 \mu \mathrm{~F}$ ceramic disc bypass capacitor was placed on the power supply line and it needed to be placed within 10 mm of the IC (Agilent Technologies 1999a). The recommended layout for the optocoupler provided by the manufacturer is illustrated in Figure 5.27 (Agilent Technologies 1999a).


Figure 5.27: Manufacturers recommended layout for optocoupler

### 5.7.5 Bus bars

The bus bars were mounted centrally on the converter as shown in Figure 5.17a. The bus bars are separated into four layers: positive motor phase layer, $A+$, negative motor phase layer, $A$-, positive power layer, $+V_{S}$, and negative power layer, $-V_{S}$, with an insulating material separating each layer The bus bars are approximately a half-inch wide. The specific interconnections to the MOSFETs are as follows:

- The negative motor phase plane, $A$-, is connected to the drain of $\mathrm{Q}_{2}$ via the heat spreader and the source of $\mathrm{Q}_{4}$ via the stud connection located between the two parallel devices.
- The positive motor phase plane, $A+$, is coupled to the drain of $\mathrm{Q}_{3}$ and to the source of $\mathrm{Q}_{1}$ using the same scheme as the negative motor phase layer.
- The negative power plane, $-V_{S}$, is connected to the source terminals of $\mathrm{Q}_{3}$ and $\mathrm{Q}_{2}$ the stud connection located between the two parallel devices.
- The positive power plane, $+V_{S}$, is attached to the drains of $\mathrm{Q}_{1}$ and $\mathrm{Q}_{4}$ via the heat spreader.

This format equalizes the dimensions and provides symmetry to the layout, which further reduces stray inductance; the bus bar layers are stacked in the following configuration: the bottom layer of the bus bar is the positive power plane, $+V_{S}$, next is the negative power plane, $-V_{S}$, then the positive motor phase plane, $A+$, and finally the negative motor phase layer, $A$-. A thin layer of insulation is placed between each motor and power plane to implement a laminated bus bar construction. This configuration minimises mutual inductance due to the close association of opposite polarity currents.

The symmetrical connections between MOSFET and the source stud were implemented using copper tined conductor as illustrated in Figure 5.26a.

### 5.7.6 Current sensor

The layout of the current carrying conductor through the sensor aperture provides maximum separation from the return conductor or other high current conductors and the conductor completely fills the sensor aperture (LEM Components 2004), (Besnier 2004) and (LEM Components 2005) as illustrated in Figure 5.26a and 5.26b, respectively. The transducer output wiring must have minimum loop area and also must have minimum length traces separated from power leads (LEM Components 2004). The current sensor is mounted in the top corner of the PCB as illustrated in Figure 5.26a. Copper trace material was cleaned away from around the circuit to provide isolation from the high power circuitry and all signal and power connections were brought to the circuit through a dedicated connector. Power and ground planes for the current sensor power supply were implemented to minimise noise interference.

### 5.8 Final Converter Assembly

The complete single phase full-bridge converter assembly incorporating all the requirements previously discussed and illustrated in Figure 5.26 can be seen in its complete form in the images shown in Figure 5.28-5.31. The overall final assembly is shown in Figure 5.28, the top view is provided in Figure 5.29, the side view is provided in Figure 5.30 and the end view can be seen in Figure 5.31.


Figure 5.28: Single phase full-bridge converter final assembly


Figure 5.29: Top view of the single phase full-bridge converter


Figure 5.30: Side view of the single phase full-bridge converter


Figure 5.31: End view of the single phase full-bridge converter

### 5.9 Summary

The full-bridge converter with synchronous rectification using two MOSFETs in parallel provides the best compromise of efficiency, cost and complexity for implementation with the ISG under motoring and generating operation. Using MOSFETs connected in parallel improved the current handling capability of the circuit but the implementation was more complex than using individual modules. To finalize the converter design, a thermal analysis was conducted in order to determine the most suitable heat sink configuration. When using MOSFETs in parallel, the gate drive circuit needs particular consideration in order to provide sufficient current to charge the gates of the MOSFETs and effective operate the high side devices of the full-bridge configuration. The provision for blanking time was addressed in order to provide prevent current shoot-through conditions and electrical isolation was implemented using optoisolators as part of the gate drive configuration, in order to protect the control logic circuitry. A source capacitor value was selected in order to provide instantaneous current for motor drive and act as a filter capacitor to reduce ripple during generating operation. The main converter interconnections and power conductors in this application were provided by a laminated bus bar structure in order to minimise stray inductance in the circuit. A closed loop Hall effect current sensor was selected for this application in order to implement current regulation during converter operations and allow for the potential inclusion of short circuit protection. Specific layout conditions needed to be addressed for the full bridge converter, the gate drive circuit with electrical isolation, the bus bar configuration and the current sensor in order to achieve the most efficient operation of the circuit in this application.

## Chapter 6 - System Implementation

Practical implementation in this application involves both hardware and software. The issues discussed range from the experimental setup for converter evaluation through to the development of control strategies to provide precise operation of the converter under motoring and generating modes. Two experimental setups were developed, one consisting of the SRM and a load/drive motor with a torque measurement system and a second setup comprising of a bench load to model the resistive and inductive characteristics of a single phase the SRM. Experiments were only carried out on the bench load.

### 6.1 Hardware

The experimental setup comprising of the SRM and load/drive motor with a torque measurement system was developed to provide a load or facilitate drive under motoring and generating operating modes of the ISG, respectively. The experimental set-up for the converter evaluation and the development of the current control strategy under bench conditions consists of a resistive-inductive load to model the SRM phase winding, a 1 kW power supply, a low voltage power supply and interface circuit, the full-bridge converter and the digital signal processing development board (DSP controller) as illustrated in Figure 6.1. The development of the converter prototype included the converter layout, mechanical component considerations, converter assembly and preliminary evaluation of the converter to verify that it satisfies functional tests.


Figure 6.1: The complete experimental setup for converter evaluation

### 6.1.1 The SRM

The project initially involved developing an electronic drive for a 2-phase SRM. The use of a 2-phase SRM is suitable for applications with high initial starting torques and where the cost of the converter needs to be minimised. The large peak torque capability also yields a significant regenerative braking capability, which can be highly advantageous. Unfortunately, the original project plan for the 2-phase SRM to be designed and constructed by a project partner was not fulfilled so an alternative SRM was sourced for the project application. An SRM of equivalent power rating was sourced commercially but since switched reluctance motors have a limited availability in off-the-shelf configurations, compromises had to be made in order to meet the desired power requirements. The SRM that most closely matched the specifications was a 3.5 kW , 48 V , 4-phase, $8 / 6$ SRM (Motion System Tech 2002). While an SRM could be custom designed to the project specifications (Motorsoft 2007), this direction was deemed to be prohibitively expensive and time consuming for this single application, so the commercially available SRM was selected instead, in order to prove the validity of the hardware application. The nominal parameters for the 4-phase SRM are provided in Table 6.1.

| Manufacturer <br> Model | Motion System Tech <br> RA165L |
| :--- | :--- |
| Parameters | Value |
| $\mathrm{R}_{\text {phase }}$ | $8 \mathrm{~m} \Omega$ |
| $\mathrm{~L}_{\text {aligned }}$ | $334 \mu \mathrm{H}$ |
| $\mathrm{L}_{\text {unaligned }}$ | $47 \mu \mathrm{H}$ |
| Moment of Inertia | 127 kg cm |
| Rated current | 100 A |
| Rated voltage | 48 V |
| Stator/rotor poles | $8 / 6$ |
| Phases | 4 |
| Rated torque | $5.68 \mathrm{~N}-\mathrm{m}$ |
| Rated speed | 6000 rpm |

Table 6.1: Nominal parameters of the SRM

### 6.1.2 The Digital torque measurement system

The digital torque measurement system consists of a dc-machine (MV 1042) attached via ball bearing at each end of the machine to the machine housing, a machine bed (MV1004) and a control unit (MV 1041) (Terco 2003). The machine bed aligns and secures the dc machine to the test machines. Torque measurement is achieved using a torque arm attached beneath the machine on which is mounted a strain gauge transducer and this constitutes the signal source for the torque measurement. The machine also contains a speed indicator, which generates a pulse train proportional to speed. The control unit consists of digital instruments for torque, speed, and field and armature currents, while the front panel of the control unit also contains a potentiometer for control of the field rectifier for load tests. The field can also be supplied by an external source by removing the jumpers and there are terminals on the front panel for connecting the armature winding to an external power source (motor drive) or to a load resistor (generator drive). There are analogue outputs for speed and torque and an analogue input for control of load torque.

An interface chassis was developed to align and connect the SRM with the dc machine and machine bed. A suitable coupler was acquired to interface the SRM with the dcmachine. It is a general-purpose coupler with a flexible rubber insert for flexibility and shock resistance. It is capable of accommodating accidental misalignments and has a torque range of up to 90 Nm (Fenner 2006). The digital torque measurement system is illustrated in Figure 6.2.


Figure 6.2: The digital torque measurement system

### 6.1.3 Experimental RL load setup and 1 kW Power Supply

The RL load setup consisted of an inductor that modelled the worse case phase inductance and winding resistance when the SRM was in the unaligned position and the inductance was at the minimum value. It was used as part of the bench test setup to test the converter operation and develop the current regulation strategy. The experimental RL load setup with converter is illustrated in Figure 6.3.


Figure 6.3: Schematic of converter with RL load

A 1 kW power supply was used for the dc link power supply for the converter. It provides dc power up to 1 kW over a wide range of voltage and current combinations. The power supply has a voltage range of $0-60 \mathrm{~V}$ and a current range of $0-50 \mathrm{~A}$.

### 6.1.4 The LV power supply and interface unit

This unit provides all the low voltage power supplies and signal interfacing for the converter and the DSP controller. This unit was developed as part of a prototype assembly that was designed and built for a 3phase SRM (described in the report (Murphy 2002)). A detailed schematic of the power supply circuit is included in Appendix D. The power supply provides the following voltages:

- isolated +5 V supply for the optical isolators output stage on the interface circuit
- $\pm 5 \mathrm{~V}$ supplies for the DSP controller
- +3.3 V supply for the CMOS logic circuits and the optical isolator inputs on the interface circuit to provide logic level compatibility with signals to and from the DSP controller
- $\pm 12 \mathrm{~V}$ supplies for the current sensing circuit on the converter hardware
- +15 V for the converter gate drive circuit.
- $+12 \mathrm{~V}, 2 \mathrm{~A}$ power supply for cooling fans on the converter

The interface circuit's primary purpose is to provide optical isolation for the SRM gate drive signals from the DSP controller circuit. This reduces the risk of damage to the DSP controller circuit in the event of an electrical failure on the converter. The circuit also provides a distribution point for the power supply voltages for the converter and DSP controller circuits. Finally, this circuit provides an interface for signals being routed to and form the DSP controller circuit, i.e. current sensing signals and the output enable switch. A detailed schematic of the interface circuit is provided in Appendix D. A bock diagram of the interface circuit and the low voltage power supply is given in Figure 6.4; while a detailed interconnection schematic for this system is included in Appendix D.


Figure 6.4: Block diagram of interface and low voltage power supply

### 6.1.5 DSP controller

An Analog Devices digital signal processor (ADSP21992) was employed in the experimental implementation of the current control strategy. It was suitable for this application, as it had a three-phase PWM generator unit and dual auxiliary PWM outputs, which allowed the implementation of current regulation using PWM for a four phase SRM. Additionally, using this hardware allowed for integration of the converter current controller with the SRM motor and generator control strategies developed on the same hardware.

The ADSP21992 is a mixed signal DSP controller that integrates the fixed point ADSP219x family base architecture (Analog Devices 2003a). A functional block diagram of the DSP controller is provided in Figure 6.5 and the key features are listed in Table 6.2. (The ADSP21992 costs approximately $€ 19$ when ordered in quantities of between 1000
and 5000). The ADSP-21992 EZ-KIT Lite development board was employed in the experimental set-up for evaluation of the converter and development and test of the current regulation scheme (Analog Devices 2003b). The integrated special purpose and motor control peripherals (the analog-to-digital conversion (ADC), the pulse-width modulation (PWM), the programmable interrupts and the programmable Flag I/O pins) were employed in the converter evaluation and in the current controller implementation. An overview description of the development board and how these specific peripherals are setup are provided in Appendix E.

- ADSP-219x DSP core, 160 MHz
- 14-bit, 8-channel, 20 MSPS ADC with on-chip voltage reference
- 16 K data memory, 32 K program RAM
- Three-phase PWM generation unit, with additional dual auxiliary PWM outputs
- 16-bit general purpose flag I/O port
- Incremental encoder interface unit
- Three 32-bit, general purpose timers
- External memory interface
- Peripheral interrupt controller
- Synchronous serial (SPORT) and SPI communications port
- Integrated controlled area network (CAN) interface

Table 6.2: Key features of ADSP-21992

In order to implement the numerous capabilities of the ADSP-21992 DSP, a full understanding of the software development environment called VisualDSP++ was required (Analog Devices 2002).. It provided a single, integrated project management and debugging environment for advanced code development and debug. VisualDSP++ 3.0 has a number of built in or intrinsic functions designed to make programming a DSP in a C environment even more user-friendly. The specific software requirements to setup and use the required peripherals in this application are provided in Appendix F.


Figure 6.5: Functional block diagram of ADSP-21992

### 6.1.6 Converter prototyping

The prototyping of the converter is discussed under four specific headings: electronic circuit layout, mechanical layout, converter assembly and preliminary converter evaluation. As image of the complete converter assemble is shown in Figure 6.6.


Figure 6.6: Single phase full-bridge converter final assembly

### 6.1.6.1 Circuit layout

The converter circuit schematic was initially drawn in a CAD software schematic capture package and a netlist was generated in order to create a prototype printed circuit board (PCB) layout for test and evaluation. The central aspect of the layout is the MOSFET positioning that defines source and drain layout to minimise stray inductance and maximise symmetry and maximise circuit balance (through equal track lengths) between the parallel devices. After much iteration a final layout compromise was achieved for the parallel switching component layout. Significant attention was focused on addressing the gate drive circuit layout for the gate driver and the buffer circuit where the layout was optimised for minimal stray inductance and maximum circuit balance. All gate drive signal groups used ground planes in order to minimise noise and stray inductance and maximise gate drive signal quality. The layout for the current sensor required that the device was located as far as possible from the high current switching signals and their corresponding switching emissions. The laminated bus bar connection to the SRM (A+ and A-) separated a sufficient distance from the current sensor to minimise sensor signal interference and maximise signal quality as illustrated
in Figure 6.10a. A dedicated ground plane was placed in the sensor circuitry area to minimise noise contamination of the sensor signal. The printed circuit board layout illustrating the various ground planes is illustrated in Figure 6.7. The complete converter circuit schematic is illustrated in Figure 6.8.


Figure 6.7: Printed circuit board layout illustrating the various ground planes


Figure 6.8: Converter circuit schematic

### 6.1.6.2 Mechanical layout

The mechanical outlines of all the major components were defined during the PCB layout. This allowed for detailed sizing of all mechanical components (heat spreaders heatsink, cooling fan and bus bars) to be finalized including determination of the exact locations of all the components. There were interactions between the various mechanical components and the PCB, which included the bus bar drain connections (heat spreader), locating the sources studs on the PCB to attach the bus bar source connections, attaching the PCB to the heat sink while electrically isolating the heat spreader, routing the bus bar through the current sensor and locating of the cooling fan was also finalized during the PCB layout. The specific hole sizes and locations for all the mechanical components (heat spreader, heatsink and bus bar) and the PCB were also defined during the layout. An illustration of the converter assembly with the heat spreader, thermally conductive insulators and the heatsink is shown in Figure 6.9, while a detailed drawing of the complete converter assembly is provided in Figure 6.10.

A number of templates were created as part of the PCB layout process that would allow marking of the exact hole locations on the heat spreader (both top and sides), the exact size and mounting hole locations for the thermally conductive insulator and the exact mounting hole locations on the heat sink to attach the heat spreaders and the cooling fan. A number of template outline drawings were also created for the bus bars to specify the exact size and mounting hole locations for each bus bar layer and insulator layer.

The holes drilled in the top of the heat spreader were through-holes for the mounting bolts to attach the PCB heat spreader assembly to the heat sink. The hole diameter needed to be sufficient to accommodate the mounting bolt and an insulating spacer. Holes were drilled on the side of the heat spreader and tapped for M4 bolts to attach the relevant laminated bus bar connections. The thermally conductive insulators were cut to a sufficient dimension so as to allow four millimetres of the electrically insulating material to protrude all around the heat spreader as illustrated in Figure 6.9. Throughholes were punched to just allow the PCB heatspreader to heat sink mounting bolts to pass through in order to maximise electrical isolation.


Figure 6.9: Converter assembly with heat spreaders and heatsink

### 6.1.6.3 Converter assembly

The assembly of the converter was divided into various stages: the PCB assembly, the heat spreader with MOSFET assembly, the installation of the bus bar assembly, the heat sink been put in place and finally the fitting of the heatsink cooling fan. The PCB assembly involved the installation of all the circuit components except for the power MOSFETs. Two MOSFETs were installed to each of the four heat spreaders and the each assembly was then attached to the printed circuit board at the four locations for Q1, Q2, Q3 and Q4. Insulating spacers were placed between the heat spreader and the PCB and additional insulating spacers were placed in the through-holes for the bolts attaching the PCB heat spreader assembly to the heat sink as illustrated in Figure 6.10b. This provided electrical isolation between each head spreader MOSFET drain connection that would otherwise be compromised when the PCB heat spreader assembly was bolted to the heat sink. The bus bar lamination was routed through the current sensor and then affixed to the appropriate drain and source locations as described in section 5.7.5 of chapter 5 and filler strips were inserted to the bus bar at the current sensor to improve signal strength as illustrated in Figures 6.10a and 6.10b. The remaining bus bar layers were attached to the appropriate drain and source connections together with appropriate thin insulator separating each layer as illustrated in Figures 6.10a and 6.10b. The thermally conductive insulators were placed at the appropriate locations on the heat sink and the PCB - heat spreaders assembly was aligned with the heat sink and bolted in place. The PCB - heat spreader assembly to heat sink mounting bolts were tightened to a torque value of 15 Nm following a diagonal pattern to provide uniform pressure on all the heatsink, thermal conductive insulator and heat spreader junctions in order to achieve the best possible thermal equilibrium between the power switching devices. The heatsink cooling fan was then attached to the heatsink. The complete converter assembly drawings are shown in Figure 6.10.


Figure 6.10: Complete converter assembly (a) top view (b) side view and (c) approximate 3 D view

### 6.1.6.4 Preliminary converter evaluation

The initial evaluation of the converter involved visual inspection of the converter and the electrical test of the converter in incremental stages through to full converter switching operation on a load resistance. The first area to be addressed was the visual inspection of all components to determine if the values and device orientations were correct. The gate driver IC was removed and power is applied to the circuit to verify no short or open circuits and that all power supply levels were available. The output pins of the gate driver were shorted to their respective common pins to prevent a floating input to the buffer circuit. A square wave test signal was then applied to verify that the input signal lines were functional. The gate drive IC was then inserted but with the output pins floating and the test signal was again applied to verify the output gate drive signal was available. A differential probe was used to verify the all-high side gate drive signals. The gate drive IC was then completely inserted and the test signal applied once more to verify the outputs of the gate drive buffer circuit, in order to verify that the correct signals were present and at the correct levels. Finally a low voltage and low current power supply was applied once more to the dc link without the presence of the dc source capacitor and the test signal was applied to verify the output switching signal of the converter across a large value resistor in order to evaluate that the converter was functional. The converter was then ready for full operation and for the development and test of current control strategies.

### 6.2 Software

Precise control is required for the SRM and the full-bridge converter to operate efficiently. The level and timing of the current that enters each phase winding of the SRM is extremely important to ensure smooth torque generation. In order to evaluate a converter design, the first area of control to be addressed tends to be current regulation. Initially, this can be achieved using an open loop scheme at very small duty cycles, but is really only suitable for functional tests. The operation of the converter precisely over a wide range requires closed loop current control as shown in Figure 6.11. In this project, it was implemented using voltage-PWM with a Proportional-Integral (PI) controller to determine the duty-cycle values


Figure 6.11: Converter current control scheme

The converter was only implemented as a single-phase unit and a resistive-inductive (RL) load was used to replicate the phase winding resistance and inductance in the unaligned position. This provided the worst case conditions to evaluate both the converter and the current control strategy. The control source code was developed such that it could be ported for implementation with a 4-phase SRM.

The overall control structure was first defined in order to achieve precise step-by-step operation of the converter and following this the precise implementation of current regulation was then addressed. The control strategy was then implemented on the ADSP-21992 DSP evaluation board using the C programming language through the VisualDSP++ application. The central function in the project source code was the interrupt service routine (ISR) for the PWM duty-cycle update. A number of experiments were conducted to evaluate the fundamental operation and the worst-case performance of the converter and the current control strategy.

### 6.2.1 Control Structure

Current control was implemented using a voltage-PWM as described in Chapter 2, section 2.4.1, and the duty-cycles were determined using a PI controller. PWM provides fixed switching frequency operation, which allows for a constant level of switching losses and therefore improves converter efficiency. Additionally the use of a PWM current controller reduces the current harmonics, which yields a reduction in acoustic noise during SRM operation (Miller 2001). The current controller design was based on the scheme of designing the controller for the unaligned phase inductance value that results in a stable design for all rotor positions (DiRenzo 2000).

The implementation of the switching strategies for precise converter operation was addressed prior to the design of the current controller. These switching strategies control the operation of the individual converter MOSFETs in order to execute the four modes of operation (magnetisation, freewheeling, demagnetisation and shut-down) of the converter as shown in Figure 6.12 and described in Chapter 2. The PWM output signals were connected to the MOSFETs, $\mathrm{Q}_{1}$ and $\mathrm{Q}_{3}$, and $\mathrm{I} / \mathrm{O}$ logic level signals were MOSFETs, $\mathrm{Q}_{2}$ and $\mathrm{Q}_{4}$.


Figure 6.12: The full-bridge converter. (a) Static view of converter in shut down mode,
(b) magnetization mode, (c) freewheeling mode, and (d) demagnetization mode

SRM control requires precise rotor position information in order to determine the correct turn-on and turn-off angles, which in turn defines the conduction interval over which the current flows into and out of the phase winding of the SRM. For operation as a single-phase unit with an RL load, signal pulses were generated to simulate the turnon and turn-off angles instead of reading and decoding the actual rotor position information. The position information allowed for the establishment of control signals to precisely implement switching strategies as shown in Table 6.3.

There are five distinct cycles that happened during the conduction interval for the converter: start-up PWM, PI voltage-PWM, freewheel PWM, demagnetisation PWM and shut-down. Start-up PWM and PI voltage-PWM implements magnetisation and freewheeling operation as shown in Table 6.3. At the turn-on angle, there is a start-up
routine using PWM operation but at fixed duty-cycles in order to allow the current in the SRM phase winding to rise quickly and controllably to a threshold current ( $\mathrm{I}_{\mathrm{th}}$ ) value. The current is then controlled by PI voltage-PWM operation and regulated at the reference current ( $\mathrm{I}_{\mathrm{ref}}$ ) value and this requires PWM operation with variable duty-cycle values determined by a PI controller. If the current exceeds an upper limit current ( $\mathrm{I}_{\text {high }}$ ), assigned to be $10 \%$ above $\mathrm{I}_{\text {ref }}$, then freewheel PWM operation is required to allow the current to decrease sufficiently. This mode applies $0 \%$ duty cycle to $\mathrm{Q}_{1}$ and $100 \%$ duty cycle to $\mathrm{Q}_{3}$.

At the turn-off angle, demagnetisation of the phase winding commences and when the value of the current is above the threshold level the MOSFETs, $\mathrm{Q}_{3}$ and $\mathrm{Q}_{4}$, are turned on. $\mathrm{Q}_{3}$ requires PWM operation and is implemented at 100 kHz with $100 \%$ duty cycle. This higher frequency operation allows more frequent current measurement to determine if the minimum current threshold has being reached. Finally, demagnetisation at low current and shut-down requires that all MOSFETs are turned off and the remaining current conducted through the intrinsic diodes of the MOSFETs. Shut down also signals the end of close loop control for that particular phase.

| Position logic |  | $\begin{array}{\|c} \hline \text { Modes } \\ \text { of } \\ \text { Operation } \\ \hline \end{array}$ | Full bridge converter |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Q1 | Q3 |  |  | Q2 | Q4 |
| A | B |  | $\mathrm{I}_{\text {meas }}<\mathrm{I}_{\text {th }}$ | $\mathrm{I}_{\text {meas }} \leq \mathrm{I}_{\text {th }}<\mathrm{I}_{\text {high }}$ | $\mathrm{I}_{\text {meas }}>\mathrm{I}_{\text {high }}$ |  |  | $\mathrm{I}_{\text {meas }}<\mathrm{I}_{\text {th }}$ | $\mathrm{I}_{\text {meas }}<\mathrm{I}_{\text {th }}<\mathrm{I}_{\text {high }}$ | $\mathrm{I}_{\text {meas }}>\mathrm{I}_{\text {high }}$ |
| 1 | 1 |  | Mag/free | Start PWM | PI PWM | Free PWM | Start PWM | PIPWM | Free PWM | On | Off |
| 1 | 0 | Demag | 0\% |  |  | Shutdown | Demag PWM (100\%) |  | Off | On |
| X | 0 | Shutdown | Off |  |  |  |  |  |  |  |

Table 6.3: Rotor position logic and converter switching cycles

The angle data and current measurement ( $\mathrm{I}_{\text {meas }}$ ) data determine the transition points between the different cycles. The current measurement defines the point to toggle between start-up PWM and PI voltage-PWM (PI PWM) and the changeover between demagnetisation at high current (demag PWM) and shut-down if the shut-down angle has not yet being reached. The angle data defines when PWM (start-up and PI) commences and when demagnetisation commenced.

The PI controller determines the new duty-cycle value required to regulate the current at a predetermined reference value. The control law used for the PI controller is shown in equation 6.1 (Dorf 1998).

$$
\begin{equation*}
u(t)=K_{p} e(t)+K_{i} \int_{0}^{T} e(t) d t \tag{6.1}
\end{equation*}
$$

In this application, $u(t)$ is the new duty-cycle value, $\mathrm{K}_{\mathrm{p}}$ the value of gain applied to the error signal, $e(t)$. The error signal, $e(t)$, is the difference between the reference current, $\mathrm{I}_{\mathrm{ref}}$, and the actual measured current, $\mathrm{I}_{\text {meas }} . \mathrm{K}_{\mathrm{i}}$ is the value of gain applied to the integral of the error signal. The time increment, dt, is the PWM period ( $40 \mu \mathrm{~s}$ for 25 kHz switching frequency), as the integral of the error is determined at a fixed time interval during the ISR for the PWM update.

The PI controller was tuned manually. The resultant values of $K_{p}$ and $K_{i}$, were $K_{p}=$ 0.015 and $\mathrm{K}_{\mathrm{i}}=0.1$.

### 6.2.2 Control Implementation

The source code was structured for the implantation with a four-phase SRM. Since the converter was only evaluated as a single-phase on an RL load, only the source code for a single-phase (phase A) was fully developed and tested. The ISR for the PWM was only developed for a single-phase (phase A) but could easily be expanded for phases B and C. Phase D would require the implementation of an ISR for auxiliary PWM but was not developed further than the initialization stage in order to verify it was capable of matching the operation of the other three phases. The source code contains six functions: read_rotor_angle(), commutation_four_phase(), motor_control_a(), pwm_isr(), Initialization(), and the main function.

A tutorial on how to implement the configuration requirements for the DSP modules (ADC, PWM, Auxiliary PWM, Program sequencer and Peripheral interrupt controller, and Flag I/O) used in this project are documented in Appendix E and tutorial on using the VisualDSP++ development suite to create the source code is provided in Appendix F. The complete source code is documented in Appendix G

The main function calls the functions in the appropriate sequence for successful program operation for the PWM current control update. A number of DSP modules (Clock speed, Interrupts, ADC, PWM, Aux PWM and FIO) registers needs to be configured before program execution. These setup requirements are grouped together in
a single initialization function, initialization().The flowchart for the overall structure of the program source code is shown in Figure 6.13.


Figure 6.13: Overall source code structure

The central function in the project source code is the ISR for the PWM update. A number of other functions are required for the ISR implementation and to provide structure in the execution of the source code. In order to implement the PWM successfully, the exact rotor position is required so a function, read_rotor_angle(), was developed to provide rotor angle information. As the converter was only evaluated as a single phase with a RL load, the function only provided the angle output data needed to test the converter operation. The angle information is used by the commutation function, commutation_four_phase(), to generate the appropriate control signals to implement the various modes of operation for each phase and disable the other phases at the same time as illustrated in the flowchart shown in Figure 6.14.


Figure 6.14: The commutation function to determine the control signals

The control signal information is then used by the motor control function, motor_control_a(), to configure and enable the PWM outputs and the FIO outputs for phase A, as illustrated in the flowchart shown in Figure 6.15. This implements each of the five distinct cycles (startup PWM, PI PWM, freewheel PWM, demag PWM and shutdown) that occur during the conduction interval of the converter. A duty cycle update control variable is then set to allow the ISR to be called.

The steps involved to implement the ISR function for the PWM, PWM_ISR(), are illustrated in the flowchart shown in Figure 6.16. The first step in the ISR is to clear the interrupt and then check if in the $2^{\text {nd }}$ half-cycle of the PWM signal as an update is only implemented at this time. This provides a half PWM period between the ADC reading and the duty-cycle update. The ISR then reads the ADC value and calculates the current value, and then using this information calculates the duty-cycle value from the PI difference equation. Then depending on the control signal for the converter mode of
operation (magnetisation, freewheeling and demagnetisation) and the level of current, the final duty-cycle update codes are determined and assigned to the appropriate registers. The duty cycle update control variable is then cleared before exiting the ISR.


Figure 6.15: The motor control function to initial the appropriate converter cycle


Figure 6.16: The ISR for the PWM duty-cycle update

### 6.2.3 Design Verification

As noted previously, the control strategy was implemented on an ADSP-21992 DSP development board. Only a single phase converter was evaluated and an RL load was used to model the phase winding resistance and inductance at the unaligned position. This provided the worst-case condition to evaluate both the converter operation and the current control strategy. Initially the elementary converter and source code operation was evaluated under three separate conditions: the gate drive operation, the gate drive switching operation under the different cycles of operation and finally the current measurement capability. The current control algorithm was then evaluated at different current levels in order to verify the converter operation and current control accuracy.

### 6.2.3.1 Preliminary Converter and source code evaluation

The initial assessment of the converter necessitated that the gate drive switching signals be evaluated from the DSP evaluation board output through to the power MOSFETs $\left(\mathrm{Q}_{1}-\mathrm{Q}_{4}\right)$ inputs in order to verify that signal levels were correct at each stage The switching signal chain from the DSP output through the gate drive buffer circuit output of the converter is shown in Figure 6.17.


Figure 6.17: Gate drive signal path for $\mathrm{Q}_{1}$ at DSP 3.3V output (Channel 1), at the IR2110 gate driver 5 V input (Channel $21 \mathrm{~V}=50 \mathrm{mV}$ ) and at buffer circuit 15 V output (Channel $31 \mathrm{~V}=20 \mathrm{mV}$ )

The current measurement by the DSP was verified in conjunction with the basic MOSFET switching operation using the setup illustrated in Figure 6.18. The MOSFET switching signals for start-up PWM, PI PWM, demagnetisation or demag PWM and shutdown were evaluated at this time. The signals for the transition between start-up PWM and PI PWM, and between PI PWM and demag PWM are shown in Figures 6.19 -6.20 , respectively.


Figure 6.18: Initial current measurement test setup


Figure 6.19: Transition between shutdown and start-up PWM operation, $Q_{1}$ (Channel 1), $\mathrm{Q}_{2}$ (Channel 2), $\mathrm{Q}_{3}$ (Channel 3) and $\mathrm{Q}_{4}$ (Channel 4). $\mathrm{Q}_{1}$ has fixed duty cycle of 2.5\% and consequently $\mathrm{Q}_{3}$ has a duty-cycle of $97.5 \%$ during start-up, while Q2 is on and Q4 is off


Figure 6.20: Transition between PI PWM and demag PWM operation, $\mathrm{Q}_{1}$ (Channel 1), $\mathrm{Q}_{2}$ (Channel 2), $\mathrm{Q}_{3}$ (Channel 3) and $\mathrm{Q}_{4}$ (Channel 4). The $\mathrm{Q}_{3}$ PWM gate signal operated at 100 KHz and $100 \%$ duty cycle during demagnetisation.

As can be seen from Figure 6.20, unstable PWM operation occurred during the transition between PI PWM and demag PWM. During this interval of approximately 10 $-20 \mu \mathrm{~s}, \mathrm{Q}_{1}$ turned on while $\mathrm{Q}_{3}$ was on leading to a shoot through current condition. A number of attempts were made to prevent this glitch from occurring including adding a delay in the angle reading source code to shut down the converter between transitions, but a solution could not be found. As this occurred at the reference current, which could be up to 100 A and as the result of one board failure at much lower current, it was decided to disable this feature and go directly to shutdown from PI PWM as illustrated in Figure 6.21. While demag PWM is possible, this glitch would need to be resolved in order to implement both demagnetisation mode at high motor speed and generator mode at high efficiency and achieve the maximum advantage of this converter design. As the converter was designed for operation with a duty cycle of $10 \%$ during demagnetisation mode and the value experienced during testing as $<1 \%$ at ISG starting speed (200rpm), the demag PWM mode was disabled to achieve stable software operation. Therefore, during shutdown the demagnetisation current would flow through the intrinsic diodes of $\mathrm{Q}_{3}$ and $\mathrm{Q}_{4}$.


Figure 6.21: Transition between PI PWM and shutdown operation, $\mathrm{Q}_{1}$ (Channel 1), $\mathrm{Q}_{2}$ (Channel 2), $\mathrm{Q}_{3}$ (Channel 3) and $\mathrm{Q}_{4}$ (Channel 4).

Once the current measurement and MOSFET switching operation was verified, the PI current controller was developed for operation at 5A, initially. The controller was tuned heuristically with the test results shown in Table 6.4 for proportional gain, $\mathrm{K}_{\mathrm{p}}$, integral gain, $\mathrm{K}_{\mathrm{i}}, 5 \mathrm{~A}$ reference current, $\mathrm{I}_{\text {ref }}$, peak current, $\mathrm{I}_{\text {peak }}$, steady state current, $\mathrm{I}_{\mathrm{ss}}$, percentage overshoot, OS\%, rise time, $\mathrm{t}_{\mathrm{r}}$, settling time, $\mathrm{t}_{\mathrm{s}}$, and steady state error, $\mathrm{e}_{\mathrm{ss}}$, to illustrate the transient and steady state response of the system. The resultant values of $\mathrm{K}_{\mathrm{p}}$ and $\mathrm{K}_{\mathrm{i}}$, that yielded the best performance characteristics were $\mathrm{K}_{\mathrm{p}}=0.015$ and $\mathrm{K}_{\mathrm{i}}=0.1$.

| $\mathbf{K}_{\mathbf{p}}$ | $\mathbf{K}_{\mathbf{i}}$ | $\mathbf{I}_{\text {peak }}(\mathbf{A})$ | $\mathbf{I}_{\mathbf{s s}}(\mathbf{A})$ | $\mathbf{O S} \%$ | $\mathbf{t}_{\mathbf{r}}(\boldsymbol{\mu s})$ | $\mathbf{t}_{\mathbf{s}} \mathbf{( \mu \mathbf { s } )}$ | $\mathbf{e}_{\mathbf{s}}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0.001 | 0 | 2.8 | 2.5 | -44 | 270 | 960 | -2.5 |
| 0.01 | 0 | 4.6 | 4.3 | -8 | 430 | 810 | -0.7 |
| 0.1 | 0 | 16.3 | 4.9 | 226 | 640 | 5680 | -0.1 |
| 0.05 | 0 | 8.5 | 4.7 | 70 | 700 | 3180 | -0.3 |
| 0.02 | 0 | 5.3 | 4.5 | 6 | 680 | 1500 | -0.5 |
| 0.015 | 0 | 4.9 | 4.4 | -2 | 700 | 1100 | -0.6 |
| 0.015 | 0.001 | 5 | 4.5 | 0 | 700 | 1100 | -0.5 |
| 0.015 | 0.01 | 5.3 | 4.8 | 6 | 700 | 1160 | -0.2 |
| 0.015 | 0.1 | 5.3 | 4.9 | 6 | 7200 | 1100 | -0.1 |
| 0.015 | 1 | 5.4 | 4.9 | 8 | 700 | 1100 | -0.1 |
| 0.015 | 10 | 6 | 4.9 | 20 | 700 | 1840 | -0.1 |
| 0.015 | 0.5 | 5.3 | 4.9 | 6 | 700 | 1260 | -0.1 |

Table 6.4: Results from heuristic tuning of the PI current controller

A comparison between the measured current of 5 A in the RL load and the value calculated in the source code and plotted by the VisualDSP++ application is shown in Figures 6.22 and 6.23 , respectively. This verified the converter current sensor operation and measurement accuracy using the source code calculation.


Figure 6.22: Measured current in the RL load at 5 A (Channel $31 \mathrm{~A}=10 \mathrm{mV} / \mathrm{div}$ )


Figure 6.23: Current of 5A calculated during source code execution and plotted by the VisualDSP++ application. Current measured by current sensor on the converter

### 6.2.3.2 Current controller evaluation

The performance was then evaluated under the different operating cycles (start-up PWM, PI PWM, demagnetisation PWM and finally shut-down). Figure 6.24 illustrates the full-bridge converter modes of operation for soft switching to provide a reference for comparison with the actual results. Operation under start-up PWM conditions is shown in Figure 6.25, while the transition between start-up PWM and PI PWM conditions is shown in Figure 6.26. The current ramped up with a fixed duty cycle value until the threshold current, $\mathrm{I}_{\mathrm{th}}$, was reached and then continued under PI PWM operation until the reference value, $\mathrm{I}_{\mathrm{ref}}$, of 5 A was reached. Once at the reference current, the PI PWM control strategy regulated the current at the reference value. At demagnetisation, all the MOSFETs $\left(\mathrm{Q}_{1}-\mathrm{Q}_{4}\right)$ were turned off and the transition between PI PWM and shut-down is shown in Figure 6.27. The current handling capability was then evaluated at three different current levels, 20A, 40A and 100A, and are shown in Figures 6.28-6.30, respectively


Figure 6.24: Full-bridge converter modes of operation for soft switching (I) magnetisation, (II) freewheeling and (III) demagnetisation


Figure 6.25: Start-up operation at transition period between shutdown, start-up PWM and PI PWM, $\mathrm{Q}_{1}$ (Channel 1), $\mathrm{Q}_{3}$ (Channel 2), RL voltage (Channel 3) and RL current (Channel 4 - 5A/div).


Figure 6.26: Current waveform and control signals at transition period between start-up PWM and PI PWM, Q ${ }_{1}$ (Channel 1), $\mathrm{Q}_{3}$ (Channel 2), RL voltage (Channel 3) and RL current (Channel $4-5 \mathrm{~A} /$ div ).


Figure 6.27: Current waveform and control signals at transition period between PI PWM and shut-down, $\mathrm{Q}_{1}$ switching signals (Channel 1), $\mathrm{Q}_{2}$ switching signal (Channel 2) and RL load voltage (Channel 3), Current (Channel 4 -5A/div)


Figure 6.28: Current and voltage waveform and control signals for 20A RL load current. $\mathrm{Q}_{1}$ switching signals (Channel 1), $\mathrm{Q}_{2}$ switching signal (Channel 2) and RL load voltage (Channel 3), Current (Channel 4 - 10A/div)


Figure 6.29: Current and voltage waveform and control signals for 40A RL load current. $\mathrm{Q}_{1}$ switching signals (Channel 1), $\mathrm{Q}_{2}$ switching signal (Channel 2) and RL load voltage (Channel 3), Current (Channel 4 - 20A/div)


Figure 6.30: Current and voltage waveform and control signals for 100A RL load current $\mathrm{Q}_{1}$ switching signals (Channel 1), $\mathrm{Q}_{2}$ switching signal (Channel 2) and RL load voltage (Channel 3), Current (Channel 4 - 50A/div)

### 6.3 Summary

The system implementation consisted of both hardware and software. The hardware included two experimental setups and the full-bridge converter prototyping. One experimental setup consisted of the SRM and a load/drive motor with a torque measurement system and a second setup comprising of a bench load to model a single phase winding of the SRM. Experiments were only carried out on the bench load. The full-bridge converter prototyping included the electronic circuit layout, the mechanical layout, the converter assembly and the preliminary converter evaluation.

The software operation centred on the switching strategies to control the operation of the individual converter MOSFETs and the implementation of the PWM current regulation strategy. The execution of precise current control required an understanding of the DSP evaluation board used in this application. The specific areas included the ADC , the PWM, and the auxiliary PWM, the program sequencer, the peripheral interrupt controller and the flag I/O. An understanding of the software development environment, used in conjunction with the DSP evaluation board, was required in order to implement all the DSP functions required in this application.

The design was evaluated under a range of operation from initial functional testing through to full power operation and the limitations and the results are presented to illustrate each level of operation.

## Chapter 7-Conclusion and Recommendations

### 7.1 Conclusions

In this thesis a number of converter topologies for implementation with the SRM were presented. The full-bridge converter with synchronous rectification using two MOSFETs mounted in parallel was chosen for the design that would be used as part of integrated starter generator (ISG). Control strategies were designed to provide precise control of the full-bridge converter switching devices and implement current regulation using voltage PWM with a proportional-integral controller.

The opening chapters presented a review of the SRM and a number of converter topologies. This provided the criteria to define the operating conditions when operating the SRM as an integrated starter generator and narrowed the converter selection to the half-bridge asymmetrical converter and the full-bridge converter. Preliminary analysis on the switching devices and the converter topologies determined the most efficient configuration for operation under motoring and generating conditions and also defined the limits for the converter operation under these conditions. The switching frequency was defined to be fixed at 25 kHz and the current was regulated using PWM and the duty cycle value determined using a proportional-integral controller.

Based on this analysis, the full-bridge with synchronous rectification using two MOSFETs mounted in parallel was deemed to provide the most efficient solution for SRM operation as a motor and especially when operating as a generator. MOSFETs connected in parallel improved the current handling capability of the circuit but the implementation was more complex than using individual modules. The issues that had to be addressed centred about maximising the current balance between parallel devices. This was achieved through minimising stray inductance by using symmetrical layout and using laminated bus bars for all high current connections, designing a gate drive circuit to provide the significant charge required by the parallel devices at turn on and a low impedance path for fast device turn off, and through close thermal coupling of parallel devices by mounting them on a heat spreader. Thermal analysis determined the most suitable heat sink configuration while a closed loop Hall effect transducer was selected for the current measurement.

The converter was evaluated using an experimental setup comprising of a bench load to model the characteristic of a single SRM phase winding. C code was developed to implement the switching strategy for the converter switching devices to implement magnetisation, freewheeling and demagnetisation modes of operation based on angle information data. PWM with the duty cycle updated through a proportional-integral controller as the method used to implement current regulation.

The software was implemented on a DSP evaluation board and required a comprehensive understanding of a number of key features of the DSP including ADC, PWM and interrupt implementation. The hardware and software were validated by experimental results presented in Chapter 6. The experimental results verify the switching strategies, but highlighted unstable PWM operation in the transition between PI PWM and Demag PWM. Attempts were made to resolve the problem but none were found. Demag PWM mode was disabled (the converter went straight to shutdown mode) in order to prevent a current shoot trough condition occurring that would result in a catastrophic converter failure. The experimental results verify the current measurement accuracy and the converter current handling capability up to 125 A . While the current handling capability was verified for the converter, this was due in part to an error that was occurring in the current measurement. While the current measurement was accurate up to 40 A , the error in the measurement when it had reached 125 A was $>25 \%$.

A second experimental setup was constructed consisting of a 3.5 kW 4 phase SRM and a load/drive motor with torque measurement system but only the bench load setup was used for converter testing and software development.

### 7.2 Recommendations

While software was developed and tested to implement the PWM strategies to operate the converter in start-up PWM, PI PWM and in demag PWM modes, the unstable transition between PI PWM and demag PWM need to be resolved in order to achieve stable system operation.

With full motor operation and precise position information it could be possible to apply $0 \%$ duty cycle to Q1 and $100 \%$ duty cycle before turning off Q2 and turning on Q4.

Developing a test circuit to implement precise rotor position information would be the next logical stage for prototype software development.

The 1 kW power supply was completely saturated in attaining the 125 A measurement, therefore, to operate a 3.5 kW SRM at high power levels a $3.5 \mathrm{~kW}-5 \mathrm{~kW}$ power supply would need to be obtained or designed to fully evaluate the converter with the SRM. The current measurement accuracy would need to be analysed to determine if the non linearity in the reading could be corrected in software or if an alternative current sensor would be required.

There is a possibility that the start-up PWM mode could be eliminated as this would allow faster rise time of the current waveform. Experiments would need to be conducted to verify that the current overshoot was not excessive, especially at high current levels.

Three more single phase converters would need to be constructed in order to evaluate the 4 phase converter operation with the load/drive motor. To evaluate a 4 phase converter, the low voltage power supply and interface circuit would have to be redesigned to facilitate of a four phase converter.

Further source code development would be required to implement the PWM current control of the fourth phase using the auxiliary PWM module of the DSP evaluation board. Software development would be required to implement and adapt control strategies for operating the 4 phase SRM as a motor and a generator.

From the preliminary analysis it is better to operate the SRM at a higher speed in order to reduce the losses during starting conditions and to have the majority of the generating and regenerative braking occurring at a higher speed in order to maximise converter efficiency.

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## Appendix A - Power Analysis Derivations

The detailed analysis provided in the following sections presents the relevant equations and parameter values that are used to implement the power analysis for each component in both the asymmetrical half-bridge converter and full-bridge synchronous rectification converter and to determine the overall converter efficiency. The analysis is divided into three specific ISG modes of operation: (a) starting and low speed motoring, (b) low speed generating and (c) high -speed generating. A number of equations are defined for the current, voltage and power calculations and these equations are used throughout this appendix. A method is presented to determine the efficiency for a single phase converter phase in each ISG mode of operation. The current and voltage waveforms are presented for each component (Q1, Q2, D1 and D1) of the asymmetrical half-bridge converter and the relevant equations and parameter values are then selected for at each ISG mode of operation. The same procedure is implemented for each component (Q1, Q2, Q3 and Q4) of the full-bridge synchronous rectification converter.

## A. 1 Analysis Equations

The voltage and current waveforms are assumed to be periodic during the converter operation. The specific current and voltage waveforms for each switching device in both the half-bridge and full-bridge converters configurations are illustrated in Sections A.3.


Figure A.1: Periodic square waveform

The average value of current for the periodic square wave shown in Figure A. 1 is determined from the equation (Hart 1997):

$$
\begin{equation*}
I_{A V G}=\frac{1}{T} \int_{0}^{T} i(t) d t=I_{m} D \tag{A.1}
\end{equation*}
$$

The RMS value of current for the periodic square wave is determined from the equation (Hart 1997):

$$
\begin{equation*}
I_{R M S}=\sqrt{\frac{1}{T} \int_{0}^{T} i^{2}(t) d t}=I_{m} \sqrt{D} \tag{A.2}
\end{equation*}
$$



Figure A.2: Periodic triangular waveform

The average value of current for the periodic triangular wave shown in Figure A. 2 is determined from the equation (Ness 2006):

$$
\begin{equation*}
I_{A V G}=\frac{1}{T} \int_{0}^{T} i(t) d t=0.5 I_{m} D \tag{A.3}
\end{equation*}
$$

The RMS value of current for the periodic triangular wave is determined from the equation (Ness 2006):

$$
\begin{equation*}
I_{R M S}=\sqrt{\frac{1}{T} \int_{0}^{T} i^{2}(t) d t}=I_{M} \sqrt{\frac{D}{3}} \tag{A.4}
\end{equation*}
$$

The conduction power losses for the MOSFET are determined by the equation (Williams 1987):

$$
\begin{equation*}
P_{c}=\left(I_{R M S}\right)^{2} R_{d s(\text { ON }) \text { Hот }} \tag{A.5}
\end{equation*}
$$

The hot on-resistance ( $\left.\mathrm{R}_{\mathrm{DS}(\text { (ол)нот }}\right)$ is the MOSFET drain to source resistance at the maximum allowable junction temperature.


Figure A.3: Typical voltage and current at turn-off switching transition for an inductive load. Current and voltage are interchanged at turn-on

The MOSFET switching transition power loss is determined using the equation for an inductive load as shown in Figure A. 3 (Williams 1987):

$$
\begin{equation*}
P_{s}=\frac{V_{m} I_{m}}{2}\left(t_{r}+t_{f}\right) f_{s} \tag{A.6}
\end{equation*}
$$

$V_{m}=V_{D S}=V_{S}$ (the applied voltage) for $\mathrm{Q}_{1}$ and $\mathrm{Q}_{2}$ of both the half-bridge and full-bridge converter, as shown in Figure A. 9 (page A15). $V_{m}=V_{D}=V_{S D}$ (the forward voltage of the intrinsic diode) for $\mathrm{Q}_{3}$ and $\mathrm{Q}_{4}$ of the full-bridge converter, as shown in Figure A. 22 (page A28). $I_{m}$ equals the maximum phase current, while $t_{r}$ and $t_{f}$ are the worst case rise and fall times, respectively.

The conduction losses for the diode are determined using the equation (Williams 1987):

$$
\begin{equation*}
P_{c}=I_{m} V_{D} D \tag{A.7}
\end{equation*}
$$

Where $V_{D}=V_{F}$ (the forward voltage of the diode) and $I_{m}$ is the peak current and $D$ the duty cycle of the current, an example of this is shown in Figure A. 9 (page A15).

The switching losses for the diode are determined using the equation (Williams 1987):

$$
\begin{equation*}
P_{s}=Q_{r r} V_{R} f_{s} \tag{A.8}
\end{equation*}
$$

Where, $Q_{r r}$ is the reverse recovery charge, $V_{R}=-V_{D}=V_{S}$, the reverse voltage applied to the diode just after turn-off and $f_{s}$ is the switching frequency.

The total power loss for a single phase is the sum of all the component losses, both conducting and switching losses, and is determined by the equation:

$$
\begin{equation*}
P_{T(S P)}=P_{T(Q 1)}+P_{T(Q 2)}+P_{T(D 1)}+P_{T(D 2)} \tag{A.9}
\end{equation*}
$$

## A. 2 Converter Efficiency and Power Transfer

The efficiency of a power converter is defined as the ratio of the output power to the output power plus losses (Hart 1997). In this application the converter transfers power in both directions (motoring and generating) so the output power is defined as the phase power.

$$
\begin{equation*}
\eta=\frac{P_{\text {phase }}}{P_{\text {phase }}+P_{T(S P)}} \tag{A.10}
\end{equation*}
$$

During magnetisation the power is transferred from the battery voltage source to the phase winding while during demagnetisation and generating the power transfer is from the phase winding to the battery. Power losses occur in the converter, $\mathrm{P}_{\mathrm{T}(\mathrm{SP})}$, during all stages of operation, so the total output power of the converter is the sum of all power transfers, $\mathrm{P}_{\text {phase }}$.

The current and voltage waveforms for the phase winding of the SRM are nonsinusoidal periodic waveforms as shown in Figures A. 4 (page A6), A5 (page A8) and A. 6 (page A10). The current and voltage waveforms can be represented by the Fourier series as shown in Equations A. 11 and A. 12 (Hart 1997).

$$
\begin{align*}
& v(t)=V_{0}+\sum_{n=1}^{\infty} V_{n} \cos \left(n \omega_{0} t+\theta_{n}\right)  \tag{A.11}\\
& i(t)=I_{0}+\sum_{n=1}^{\infty} I_{n} \cos \left(n \omega_{0} t+\phi_{n}\right) \tag{A.12}
\end{align*}
$$

The average power is determined using equation A. 13

$$
\begin{equation*}
P=\frac{1}{T} \int_{0}^{T} v(t) i(t) d t \tag{A.13}
\end{equation*}
$$

The average power for nonsinusoidal periodic voltage and current waveforms is expressed as

$$
\begin{equation*}
P=V_{0} I_{0}+\sum_{n=1}^{\infty}\left(\frac{V_{n, \max } I_{n, \max }}{2}\right) \cos \left(\theta_{n}-\phi_{n}\right) \tag{A.14}
\end{equation*}
$$

The total average power is the sum of the powers at the frequencies in the Fourier series. For practical analysis in order to determine the worst case power losses, the idealized periodic voltage waveforms are constructed from a sequence of square waves, while the idealized periodic current waveforms are constructed from a sequence of square waves and triangular waves. The average power losses were analysed for three specific ISG modes of operation: (a) starting and low speed motoring, (b) low speed generating and (c) high-speed generating.

The power transfer for the converter is assumed to be positive when it is from the battery to the phase winding, while during demagnetisation and generating the power transfer is assumed to be negative. The power transfers in either direction contribute to power losses by the converter components so the magnitude of all the power transfers is assumed to contribute to the output power of the converter. In order to determine the total power transfer for the converter, the power transfer during generating and demagnetisation is multiplied by -1 .

## A.2.1 Starting and Low Speed Motoring

The calculation of the average power during starting and low speed motoring is divided into two regions, (I) magnetisation and (II) demagnetisation as indicated in Figure A.4. The phase winding voltage is assumed to be square waves during the magnetisation region and constant during the demagnetisation region, while the current is assumed to be constant during magnetisation and a triangular wave shape in the demagnetisation region.


Figure A.4: Phase winding voltage and current waveforms during starting and low speed motoring

The time corresponding to the turn-on angle $\left(\theta_{o n}\right)$ is $t_{0}=0$, the turn-off angle at the alignment angle $\left(\theta_{2}\right)$ occurs at $t_{1}$, the end of demagnetisation occurs at $t_{2}$ and the end of the stroke $\left(\theta_{s}\right)$ is at $t_{3}=T_{s}$. The value of $T_{s}$ is determined from the speed of the SRM. The duty cycle for the magnetisation region (I) is $D_{l}$ and the duty cycle for the demagnetisation region (II) is $D_{2}$. The PWM square wave voltage waveform has a switching frequency of 25 kHz and has an average duty cycle of $50 \%$ as described in Chapter 4, Section 4.1.4.1. This yields an overall duty cycle for the voltage square wave of $0.5 \mathrm{D}_{1}$.

The equation for the average power $(P)$ over the stroke during starting and low speed motoring is defined as:

$$
\begin{align*}
& P=\frac{1}{T_{S}} \int_{0}^{T_{S}} v(t) i(t) d t  \tag{A.15}\\
& P=\frac{1}{T_{S}}\left(\int_{t_{0}}^{t_{1}} v(t) i(t) d t+\int_{t_{1}}^{t_{2}} v(t) i(t) d t+\int_{t_{2}}^{t_{3}} v(t) i(t) d t\right) \tag{A.16}
\end{align*}
$$

During magnetisation (I) the interval $t_{0}-t_{l}$, the current is constant $\left(I_{m}\right)$ and the voltage square wave has a peak value of $V_{S}$ as shown in Figure A. 4 The equation for the average power during magnetisation $\left(P_{M}\right)$ is defined as:

$$
\begin{equation*}
P_{M}=\frac{1}{T_{S}} \int_{t_{0}}^{t_{1}} v(t) i(t) d t=\frac{0.5 I_{m}}{T_{S}} \int_{0}^{D_{1} T_{S}} v(t) d t=0.5 I_{m} V_{S} D_{1} \tag{A.17}
\end{equation*}
$$

During demagnetisation (II) in the interval $t_{l}-t_{2}$, the voltage is constant $\left(-V_{S}\right)$ and the current is approximated by a triangular wave and has a peak value of $I_{m}$ as shown in Figure A.4. The equation for the average power during demagnetisation $\left(P_{D M}\right)$ is:

$$
\begin{equation*}
P_{D M}=\frac{1}{T_{S}} \int_{t_{1}}^{t_{2}} v(t) i(t) d t=\frac{-V_{S}}{T_{S}} \int_{D_{1} T_{S}}^{D_{2} T_{S}+D_{1} T_{S}} i(t) d t=-0.5 V_{S} I_{m} D_{2} \tag{A.18}
\end{equation*}
$$

The power transfer is from the phase winding to the battery so the average power during demagnetisation is:

$$
\begin{equation*}
P_{D M}=-1\left(-0.5 V_{S} I_{m} D_{2}\right)=0.5 V_{S} I_{m} D_{2} \tag{A.19}
\end{equation*}
$$

The average power loss during the interval $t_{2}-t_{3}$ is zero as the voltage and current is zero during the interval. Therefore, the average power $(P)$ over the stroke during starting and low speed motoring is defined as:

$$
\begin{equation*}
P=0.5 I_{m} V_{S} D_{1}+0.5 I_{m} V_{S} D_{2} \tag{A.20}
\end{equation*}
$$

## A.2.2 Low Speed Generating

The calculation of the average power during low speed generation is divided into two regions, (I) magnetisation and generating and (II) demagnetisation as indicated in Figure
A.5. The phase winding voltage waveform is assumed to be square waves during the magnetisation and generating regions and constant during the magnetisation demagnetisation region, while the current is assumed to be constant during magnetisation and generating and a triangular wave during demagnetisation.


Figure A.5: Phase winding voltage and current waveforms during low generating

The time corresponding to the turn-on angle $\left(\theta_{o n}\right)$ is $t_{0}=0$, the turn-off angle at the unaligned angle $\left(\theta_{4}\right)$ occurs is $t_{1}$, the end of demagnetisation occurs at $t_{2}$ and the end of the stroke $\left(\theta_{s}\right)$ is at $t_{3}=T_{s}$. The value of $T_{s}$ is determined from the speed of the SRM. The duty cycle for the magnetisation and generating region during the interval $t_{0}-t_{l}$ is assumed to be the same at $D_{l}$ and the duty cycle for demagnetisation during the interval $t_{1}-t_{2}$ is $D_{2}$. The PWM square wave voltage waveform has a switching frequency of 25 kHz and has an average duty cycle of $50 \%$ as described in Chapter 4, Section 4.1.4.2. This yields an overall duty cycle for the voltage square wave of $0.5 \mathrm{D}_{1}$ for magnetisation and $0.5 \mathrm{D}_{1}$ for generating.

The equation for the average power $(P)$ over the stroke during low speed generating is defined as:

$$
\begin{equation*}
P=\frac{1}{T_{S}}\left(\int_{t_{0}}^{t_{1}} v(t) i(t) d t+\int_{t_{1}}^{t_{2}} v(t) i(t) d t+\int_{t_{2}}^{t_{3}} v(t) i(t) d t\right) \tag{A.21}
\end{equation*}
$$

During magnetisation in the interval $t_{0}-t_{l}$, the current is assumed to be approximately constant $\left(I_{m}\right)$ and the voltage is a PWM square wave with a peak value of $V_{s}$ and a duty cycle of $\mathrm{D}_{1}$ as indicated in Figure A.5. The average power during demagnetisation $\left(P_{M}\right)$ is:

$$
\begin{equation*}
P_{M}=\frac{1}{T_{S}} \int_{t_{0}}^{t_{1}} v(t) i(t) d t=\frac{0.5 I_{m}}{T_{S}} \int_{0}^{D_{1} T_{s}} v(t) d t=0.5 I_{m} V_{S} D_{1} \tag{A.22}
\end{equation*}
$$

During generating in the interval $t_{0}-t_{1}$, the current is assumed to be approximately constant $\left(I_{m}\right)$ and the voltage square wave with a peak value of $-V_{s}$ and a duty cycle of $\mathrm{D}_{1}$ as indicated in Figure A.5. The average power during generating $\left(P_{G}\right)$ is:

$$
\begin{equation*}
P_{G}=\frac{1}{T_{S}} \int_{t_{0}}^{t_{1}} v(t) i(t) d t=\frac{0.5 I_{m}}{T_{S}} \int_{0}^{D_{1} T_{S}} v(t) d t=-0.5 I_{m} V_{S} D_{1} \tag{A.23}
\end{equation*}
$$

The power transfer is from the phase winding to the battery so the average power during generating $\left(P_{G}\right)$ is:

$$
\begin{equation*}
P_{G}=-1\left(-0.5 I_{m} V_{S} D_{1}\right)=0.5 I_{m} V_{S} D_{1} \tag{A.24}
\end{equation*}
$$

During demagnetisation in the interval $t_{1}-t_{2}$, the voltage is assumed to be constant $\left(-V_{s}\right)$ during the interval and the current is approximated by a triangular wave with a peak value of $I_{m}$ as indicated in Figure A.5. The average power during demagnetisation is:

$$
\begin{equation*}
P_{D M}=\frac{1}{T_{S}} \int_{t_{1}}^{t_{2}} v(t) i(t) d t=\frac{-V_{S}}{T_{S}} \int_{D_{1} T_{S}}^{D_{2} T_{S}+D_{1} T_{S}} i(t) d t=-0.5 V_{S} I_{m} D_{2} \tag{A.25}
\end{equation*}
$$

The power transfer is from the phase winding to the battery so the average power during demagnetisation is:

$$
\begin{equation*}
P_{D M}=-1\left(-0.5 V_{S} I_{m} D_{2}\right)=0.5 V_{S} I_{m} D_{2} \tag{A.26}
\end{equation*}
$$

The average power loss during the interval $t_{2}-t_{3}$ is zero as the voltage and current is zero during the interval. Therefore, the average power $(P)$ over the stroke during low speed generating is:

$$
\begin{equation*}
P=I_{m} V_{S} D_{1}+0.5 I_{m} V_{S} D_{2} \tag{A.27}
\end{equation*}
$$

## A.2.3 High Speed Generating

The calculation of average power during high speed generation is divided into three regions, (I) magnetisation, (II) generating and (III) demagnetisation as indicated in Figure A.6. The phase voltage waveform is assumed to be constant during all regions, while the current waveform is a triangular wave for both magnetisation and demagnetisation and is a constant for the generating region.


Figure A.6: Phase winding voltage and current waveforms during high speed generating

The time corresponding to the turn-on angle $\left(\theta_{o n}\right)$ is $t_{0}=0$, the magnetisation turn-off angle ( $\theta_{o f f}$ ) occurs is $t_{l}$, the end of generating occurs at the rotor and stator pole overlap $\left(\theta_{4}\right)$ occurs at $t_{2}$, the end of demagnetisation occurs at $t_{3}$ and the end of the stroke $\left(\theta_{s}\right)$ is
at $t_{4}=T_{S}$. The value of $T_{S}$ is determined from the speed of the SRM during high speed generating. The duty cycle for the magnetisation during the interval $t_{0}-t_{l}$ is $D_{l}$, the duty cycle for generating during the interval $t_{1}-t_{2}$ is $D_{2}$ and the duty cycle for demagnetisation during the interval $t_{2}-t_{3}$ is $D_{3}$.

The equation for the average power $(P)$ over the stroke during low speed generating is defined as:

$$
\begin{equation*}
\left.P=\frac{1}{T_{S}} \int_{t_{0}}^{t_{1}} v(t) i(t) d t+\int_{t_{1}}^{t_{2}} v(t) i(t) d t+\int_{t_{2}}^{t_{3}} v(t) i(t) d t+\int_{t_{3}}^{t_{4}} v(t) i(t) d t\right) \tag{A.28}
\end{equation*}
$$

During magnetisation in the interval $t_{0}-t_{1}$, the voltage is assumed to be approximately constant $\left(V_{S}\right)$ and the current is a triangular wave with a peak value of $I_{m}$ as indicated in Figure A.6. The equation for the average power during demagnetisation $\left(P_{M}\right)$ is:

$$
\begin{equation*}
P_{M}=\frac{1}{T_{S}} \int_{t_{0}}^{t_{1}} v(t) i(t) d t=\frac{V_{S}}{T_{S}} \int_{0}^{D_{1} T_{S}} i(t) d t=0.5 I_{m} V_{S} D_{1} \tag{A.29}
\end{equation*}
$$

During generating in the interval $t_{l}-t_{2}$, the current and voltage are assumed to be approximately constant at $I_{m}$ and $-V_{s}$, respectively, as indicated in Figure A.6. The average power during generating $\left(P_{G}\right)$ is:

$$
\begin{equation*}
P_{G}=\frac{1}{T_{S}} \int_{t_{1}}^{t_{2}} v(t) i(t) d t=\frac{-V_{S} I_{m}}{T_{S}} \int_{D_{1} T_{S}}^{D_{2} T_{S}+D_{1} T_{S}} d t=-V_{S} I_{m} D_{2} \tag{A.30}
\end{equation*}
$$

The power transfer is from the phase winding to the battery so the average power during generating $\left(P_{G}\right)$ is

$$
\begin{equation*}
P_{G}=-1\left(-V_{S} I_{m} D_{2}\right)=V_{S} I_{m} D_{2} \tag{A.31}
\end{equation*}
$$

During demagnetisation in the interval $t_{2}-t_{3}$, the voltage is assumed to be constant $\left(-V_{s}\right)$ during the interval and the current is approximated by a triangular wave with a peak value of $I_{m}$ as indicated in Figure A.6. The equation for the output power during demagnetisation is:

$$
\begin{equation*}
P_{D M}=\frac{1}{T_{S}} \int_{t_{2}}^{t_{3}} v(t) i(t) d t=\frac{-V_{S}}{T_{S}} \int_{D_{2} T_{s}+D_{1} T_{S}}^{D_{3} T_{S}+D_{2} T_{S}+D_{1} T_{S}} i(t) d t=-0.5 V_{S} I_{m} D_{3} \tag{A.32}
\end{equation*}
$$

The power transfer is from the phase winding to the battery so the average power during demagnetisation is:

$$
\begin{equation*}
P_{D M}=-1\left(-0.5 V_{S} I_{m} D_{3}\right)=0.5 V_{S} I_{m} D_{3} \tag{A.33}
\end{equation*}
$$

The average power loss during the interval $t_{3}-t_{4}$ is zero as the voltage and current is zero during the interval. Therefore, the average power $(P)$ over the stroke during starting and high speed generating is:

$$
\begin{equation*}
P=0.5 I_{m} V_{S} D_{1}+I_{m} V_{S} D_{2}+0.5 I_{m} V_{S} D_{3} \tag{A.34}
\end{equation*}
$$

## A. 3 Component Analysis

The analysis for each component of both the asymmetrical half-bridge and full-bridge synchronous rectification converter is divided into three specific ISG modes of operation: (a) starting and low speed motoring, (b) low speed generating and (c) high speed generating. The mechanical rotor position, inductance profile, the switching waveforms for all components (Q1, Q2, D1 and D2), and the associated phase voltage and current are illustrated in Figure A. 7 for (a) starting and low speed motoring and (b) low speed generating.


Figure A.7: Waveforms at speeds of operation (a) starting and low speed motoring (b) low speed generating

The mechanical rotor position, inductance profile, the switching waveforms for all components (Q1, Q2, D1 and D2), and the associated phase voltage and current are illustrated in Figure A. 8 for high speed generating


Figure A.8: Waveforms for high speed generating operation

## A.3.1 Asymmetrical half-bridge

The determination of the relevant equations and parameter values for evaluating each component (Q1, Q2, D1 and D1) in each ISG mode of operation (starting, low speed motoring, and low and high speed generating) for the asymmetrical half-bridge converter is presented in the following sections. The schematic of the asymmetrical half-bridge converter including the converter modes of operation (magnetisation, freewheeling and demagnetisation) are illustrated in Figure A. 9


Figure A.9: The asymmetrical half-bridge or classic converter. (a) Static view of converter. (b) Energization mode. (c) Freewheeling mode. (d) Forced demagnetization mode

## A.3.1.1 Starting and low speed motoring - $Q_{1}$


(a)

(b)

Figure A.10: (a) Converter schematic with voltage and current labelled for $\mathrm{Q}_{1}$.
(b)Voltage and current waveforms for $\mathrm{Q}_{1}$ during magnetisation

The conduction losses are determined using equation A.5. The RMS current is determined using equation A. 2 as the current waveform is assumed to be of the form of a square wave with a peak value of $I_{m}$ as shown in Figure A.10b. D is the duty cycle of continuous operation, which is determined in chapter 4 to be $25 \%$.

The switching losses are determined using equation A.6. $V_{m}=V_{S}$ (the applied voltage) for $\mathrm{Q}_{1}$ as shown in Figure A.10a and $I_{m}$ is shown in Figure A.10b. The switching frequency, $f_{s}$, is 25 kHz . The $t_{r}$ and $t_{f}$ time are obtained from the specific MOSFET data sheet.

## A.3.1.2 Starting and low speed motoring - $\mathbf{Q}_{2}$



Figure A.11: (a) Converter schematic with voltage and current labelled for $\mathrm{Q}_{2}$.
(b)Voltage and current waveforms for $\mathrm{Q}_{2}$ during magnetisation and freewheeling

The conduction losses are determined using equation A.5. The RMS current is determined using equation A. 2 as the current waveform is assumed to be a square wave with a peak value of $I_{m}$ as shown in Figure A.11b. D is the duty cycle of continuous operation, which is determined in chapter 4 to be $50 \%$.

The switching losses are determined using equation A.6. $V_{m}=V_{S}$ (the applied voltage) for $\mathrm{Q}_{2}$ as shown in Figure A.11a and $I_{m}$ is shown in Figure A.11b. The switching frequency, $f_{s}$, is determined from the speed of the SRM. From the analysis in chapter 4, starting at 200RPM yields 20 Hz and low speed motoring at 1000 RPM yields 100 Hz . The $t_{r}$ and $t_{f}$ time are obtained from the specific MOSFET data sheet.

## A.3.1.3 Starting and low speed motoring - $D_{1}$


(a)

(b)

Figure A.12: (a) Converter schematic with voltage and current labelled for $D_{1}$.
(b)Voltage and current waveforms for $\mathrm{D}_{1}$ during freewheeling and demagnetisation

The conduction and switching losses are divided into two regions of operation, (I) freewheeling and (II) demagnetization.

## (I) Freewheeling

The conduction losses are determined using equation A.7. The current waveform is assumed to be of the form of a square wave with a peak value of $I_{m}$ as shown in Figure A.12b. $V_{D}=V_{F}$ (the forward bias voltage) for $\mathrm{D}_{1}$ as shown in Figure A .12 a and D is the duty cycle of continuous operation, which is determined in chapter 4 to be $25 \%$. The switching losses are determined using equation A. 8 where $V_{D}=V_{S}$ (the reverse voltage) across $\mathrm{D}_{1}$ and $f_{s}$ is 25 kHz . $Q_{r r}$ for the specific diode is obtained for the diode data sheet.

## (II) Demagnetization

The conduction losses are determined using equation A.7. The current waveform is assumed to be of the form of a triangular wave with the peak current is assumed to be $0.5 I_{m}$. D is the duty cycle of continuous operation, which is determined in chapter 4 to be $10 \%$. The switching losses are determined using equation A. 8 where $V_{D}=V_{S}$ (the reverse voltage) across $\mathrm{D}_{1}$ and $f_{s}$ is 20 Hz for starting and 100 Hz for low speed motoring. $Q_{r r}$ for the specific diode is obtained for the diode data sheet.

## A.3.1.4 Starting and low speed motoring - $D_{2}$



Figure A.13: (a) Converter schematic with voltage and current labelled for $\mathrm{D}_{2}$.
(b)Voltage and current waveforms for $\mathrm{D}_{2}$ during demagnetisation

The conduction and switching losses are the same as for $\mathrm{D}_{1}$ in the second region of operation, (II) demagnetization.

## A.3.1.5 Low speed generating - $Q_{1}$


(a)

(b)

Figure A.14: (a) Converter schematic with voltage and current labelled for $\mathrm{Q}_{1}$. (b)Voltage and current waveforms for $\mathrm{Q}_{1}$ during magnetisation

The conduction losses are determined using equation A.5. The RMS current is determined using equation A. 2 as the current waveform is assumed to be of the form of a square wave shape with a peak value of $I_{m}$ as shown in Figure A.14b. D is the duty cycle of continuous operation, which is determined in chapter 4 to be $25 \%$.

The switching losses are determined using equation A.6. $V_{m}=V_{S}$ (the applied voltage) for $\mathrm{Q}_{1}$ as shown in Figure A.14a and $I_{m}$ is shown in Figure A.14b. The switching frequency, $f_{s}$, is 25 kHz . The $t_{r}$ and $t_{f}$ time are obtained from the specific MOSFET data sheet.

## A.3.1.6 Low speed generating - $Q_{2}$



Figure A.15: (a) Converter schematic with voltage and current labelled for $\mathrm{Q}_{2}$.
(b)Voltage and current waveforms for $\mathrm{Q}_{2}$ during magnetisation

The conduction and switching losses for both regions are the same as for $\mathrm{Q}_{1}$.

## A.3.1.7 Low speed generating - $D_{1}$



Figure A.16: (a) Converter schematic with voltage and current labelled for $D_{1}$.
(b)Voltage and current waveforms for $\mathrm{D}_{1}$ during generating and demagnetisation

The conduction and switching losses are divided into two regions of operation, (I) generating and (II) demagnetization.

## (I) Generating

The conduction losses are determined using equation A.7. The current waveform is assumed to be of a square wave with a peak value of $I_{m}$ as shown in Figure A.16b. $V_{D}=$ $V_{F}$ (the forward bias voltage) for $\mathrm{D}_{1}$ as shown in Figure A .16 a and D is the duty cycle of continuous operation, which is determined in chapter 4 to be $25 \%$. The switching losses are determined using equation A. 8 where $V_{D}=V_{S}$ (the reverse voltage) across $\mathrm{D}_{1}$ and $f_{s}$ is 25 kHz . $Q_{r r}$ for the specific diode is obtained for the diode data sheet.

## (II) Demagnetization

The conduction losses are determined using equation A.7. The current waveform is assumed to be of the form of a triangular wave with the peak current is assumed to be
$0.5 I_{m}$. D is the duty cycle of continuous operation, which is determined in chapter 4 to be $10 \%$. The switching losses are determined using equation A. 8 where $V_{D}=V_{S}$ (the reverse voltage) across $\mathrm{D}_{1}$ and $f_{s}$ is 200 Hz . $Q_{r r}$ for the specific diode is obtained for the diode data sheet.

## A.3.1.8 Low speed generating - $\mathbf{D}_{\mathbf{2}}$



Figure A.17: (a) Converter schematic with voltage and current labelled for $\mathrm{D}_{2}$. (b)Voltage and current waveforms for $\mathrm{D}_{2}$ during generating and demagnetisation

The conduction and switching losses are divided into two regions of operation, (I) generating and (II) demagnetization. The conduction and switching losses for both regions are the same as for $D_{1}$.

## A.3.1.9 High speed generating - Q1


(a)

(b)

Figure A.18: (a) Converter schematic with voltage and current labelled for $\mathrm{Q}_{1}$. (b)Voltage and current waveforms for $\mathrm{Q}_{1}$ during magnetisation

The conduction losses are determined using equation A.5. The RMS current is determined using equation A. 4 as the current waveform is assumed to be of the form of a triangular pulse shape with a peak value of $I_{m}$ as shown in Figure A.18b. D is the duty cycle of continuous operation, which is determined in chapter 4 to be $40 \%$.

The switching losses are determined using equation A.6. $V_{m}=V_{S}$ (the applied voltage) for $\mathrm{Q}_{1}$ as shown in Figure A.18a and $I_{m}$ is shown in Figure A.18b. The switching frequency, $f_{s}$, is determined from the speed of the SRM. From the analysis in chapter 4, high speed generating at 4500 RPM yields 450 Hz and 6000 RPM yields 600 Hz . The $t_{r}$ and $t_{f}$ time are obtained from the specific MOSFET data sheet.

## A.3.1.10 High speed generating - Q2


(a)

(b)

Figure A.19: (a) Converter schematic with voltage and current labelled for $\mathrm{Q}_{2}$. (b)Voltage and current waveforms for $\mathrm{Q}_{2}$ during magnetisation

The conduction and switching losses for both regions are the same as for Q 1 .

## A.3.1.11 High speed generating - D1



Figure A.20: (a) Converter schematic with voltage and current labelled for $\mathrm{D}_{1}$. (b)Voltage and current waveforms for $\mathrm{D}_{1}$ during generating and demagnetisation

The conduction and switching losses are divided into two regions of operation, (I) generating and (II) demagnetization.
(I) Generating

The conduction losses are determined using equation A.7. The current waveform is assumed to be of the form of a square pulse shape. D is the duty cycle of continuous operation, which is determined in chapter 4 to be $30 \%$. Switching losses are determined using equation A. 8 where $f_{s}$ for high speed generating at 4500 RPM yields 450 Hz and 6000 RPM yields 600 Hz .
(II) Demagnetization

The conduction losses are determined using equation A.7. The current waveform is assumed to be of the form of a triangular pulse shape with a peak current is assumed to be $0.5 * \mathrm{I}_{\mathrm{M}}$. D is the duty cycle of continuous operation, which is determined in chapter 4 to be $10 \%$. Switching losses are determined using equation A. 8 where $f_{s}$ for high speed generating at 4500RPM yields 450 Hz and 6000RPM yields 600 Hz .

## A.3.1.12 High speed generating - D2



Figure A.21: (a) Converter schematic with voltage and current labelled for $\mathrm{D}_{2}$. (b)Voltage and current waveforms for $\mathrm{D}_{2}$ during generating and demagnetisation

The conduction and switching losses are divided into two regions of operation, (I) generating and (II) demagnetization. The conduction and switching losses for both regions are the same as for $D_{1}$.

## A.3.2 Full-bridge with synchronous rectification

The determination of the relevant equations and parameter values for evaluating each component $\left(\mathrm{Q}_{1}, \mathrm{Q}_{2}, \mathrm{Q}_{3}\right.$ and $\left.\mathrm{Q}_{4}\right)$ in each mode of operation for the full-bridge with synchronous rectification is presented in the following sections. The schematic of the full-bridge synchronous rectification converter including its modes of operation are illustrated in Figure A. 22.


Figure A.22: The full-bridge converter. (a) Static view of converter. (b) Energization mode. (c) Freewheeling mode. (d) Forced demagnetization mode

## A.3.2.1 Starting and low speed motoring - $\mathbf{Q}_{1}$ and $\mathbf{Q}_{\mathbf{2}}$

The conduction and switching losses are the same as for $\mathrm{Q}_{1}$ and $\mathrm{Q}_{2}$ from the asymmetric half bridge.

## A.3.2.2 Starting and low speed motoring - Q3



(b)

Figure A.23: (a) Converter schematic with voltage and current labelled for $\mathrm{Q}_{3}$. (b)Voltage and current waveforms for $\mathrm{Q}_{3}$ during freewheeling and demagnetisation

The conduction and switching losses are divided into two regions of operation, (I) Freewheeling and (II) demagnetization.
(I) Freewheeling

The conduction losses are determined using equation A.5. The RMS current is determined using equation A. 2 as the current waveform is assumed to be of the form of a square pulse shape with a peak value of $I_{m}$ as shown in Figure A.23b. D is the duty cycle of continuous operation, which is determined in chapter 4 to be $25 \%$.

The switching losses are determined using equation A. 6 with the switching frequency, $\mathrm{f}_{\mathrm{s}}$, of 25 kHz and $\mathrm{V}_{\mathrm{m}}$ is equal to the peak voltage, $\mathrm{V}_{\mathrm{S}}$, across $\mathrm{Q}_{3}$ as shown in Figure A.23a and $I_{(Q 3)}=I_{m}$ as shown in Figure A.23b. The $t_{r}$ and $t_{f}$ time are obtained from the specific MOSFET data sheet.

## (II) Demagnetization

The conduction losses are determined using equation A.5. The RMS current is determined using equation A. 4 as the current waveform is assumed to be of the form of a triangular pulse shape with a peak value of $I_{m}$ as shown in Figure A.23b. D is the duty cycle of continuous operation, which is determined in chapter 4 to be $10 \%$.

The switching losses are determined using equation A.6. The switching frequency, $\mathrm{f}_{\mathrm{s}}$, is determined from the speed of the SRM. From the analysis in chapter 4, starting at 200RPM yields 20 Hz and low speed motoring at 1000 RPM yields $100 \mathrm{~Hz} . \mathrm{V}_{\mathrm{m}}$ is equal to the peak voltage, $\mathrm{V}_{\mathrm{S}}$, across $\mathrm{Q}_{3}$ as shown in Figure A.23a and $I_{(Q 3)}=I_{m}$ as shown in Figure A.23b. The $t_{r}$ and $t_{f}$ time are obtained from the specific MOSFET data sheet.

## A.3.2.3 Starting and low speed motoring - Q4



Figure A.24: (a) Converter schematic with voltage and current labelled for $\mathrm{Q}_{4}$. (b)Voltage and current waveforms for $\mathrm{Q}_{4}$ during demagnetisation

The conduction and switching losses are the same as for Q3 in the second region of operation, (II) demagnetization.

## A.3.2.4 Low speed generating - Q1 and Q2

The conduction and switching losses are the same as for Q1 and Q2 from the asymmetric half bridge.

## A.3.2.5 Low speed generating - Q3



Figure A.25: (a) Converter schematic with voltage and current labelled for $\mathrm{Q}_{3}$. (b)
Voltage and current waveforms for $\mathrm{Q}_{3}$ during generating and demagnetisation

The conduction and switching losses are divided into two regions of operation, (I) Generating and (II) demagnetization.
(I) Generating

The conduction losses are determined using equation A. 5 The RMS current is determined using equation A. 2 as the current waveform is assumed to be of the form of a square pulse shape with a peak value of $I_{m}$ as shown in Figure A.25b. D is the duty cycle of continuous operation, which is determined in chapter 4 to be $25 \%$.

The switching losses are determined using equation A. 6 with the switching frequency, $\mathrm{f}_{\mathrm{s}}$, of 25 kHz and $\mathrm{V}_{\mathrm{m}}$ is equal to the peak voltage, $\mathrm{V}_{\mathrm{S}}$, across $\mathrm{Q}_{3}$ as shown in Figure A .25 a and $I_{(Q 3)}=I_{m}$ as shown in Figure A.25b. The $t_{r}$ and $t_{f}$ time are obtained from the specific MOSFET data sheet.
(II) Demagnetization

The conduction losses are determined using equation A.5. The RMS current is determined using equation A. 4 as the current waveform is assumed to be of the form of a triangular pulse shape with a peak value of $I_{m}$ as shown in Figure A.25b. D is the duty cycle of continuous operation, which is determined in chapter 4 to be $10 \%$.

The switching losses are determined using equation A.6. The switching frequency, $\mathrm{f}_{\mathrm{s}}$, is determined from the speed of the SRM. From the analysis in chapter 4, low speed generating at 2000 RPM yields $200 \mathrm{~Hz} . \mathrm{V}_{\mathrm{m}}$ is equal to the peak voltage, $\mathrm{V}_{\mathrm{S}}$, across $\mathrm{Q}_{3}$ as shown in Figure A.25a and $I_{(Q 3)}=I_{m}$ as shown in Figure A.25b. The $t_{r}$ and $t_{f}$ time are obtained from the specific MOSFET data sheet.

## A.3.2.6 Low speed generating - Q4



Figure A.26: (a) Converter schematic with voltage and current labelled for $\mathrm{Q}_{4}$. (b)Voltage and current waveforms for $\mathrm{Q}_{4}$ during generating and demagnetisation

The conduction and switching losses are divided into two regions of operation, (I) generating and (II) demagnetization. The conduction and switching losses for both regions are the same as for Q3.

## A.3.2.7 High speed generating - Q1 and Q2

The conduction and switching losses are the same as for Q1 and Q2 from the asymmetric half bridge.

## A.3.2.8 High speed generating - Q3



Figure A.27: (a) Converter schematic with voltage and current labelled for $\mathrm{Q}_{3}$. (b)
Voltage and current waveforms for $\mathrm{Q}_{3}$ during generating and demagnetisation

The conduction and switching losses are divided into two regions of operation, (I) Generating and (II) demagnetization.

## (I) Generating

The conduction losses are determined using equation A.5. The RMS current is determined using equation A. 2 as the current waveform is assumed to be of the form of a square pulse shape with a peak value of $I_{m}$ as shown in Figure A.27b. D is the duty cycle of continuous operation, which is determined in chapter 4 to be $30 \%$.

The switching losses are determined using equation A.6. The switching frequency, $\mathrm{f}_{\mathrm{s}}$, is determined from the speed of the SRM. From the analysis in chapter 4, high speed generating at 4500 RPM yields 450 Hz and 6000 RPM yields $600 \mathrm{~Hz} . \mathrm{V}_{\mathrm{m}}$ is equal to the peak voltage, $\mathrm{V}_{\mathrm{S}}$, across $\mathrm{Q}_{3}$ as shown in Figure A.27a and $I_{(Q 3)}=I_{m}$ as shown in Figure A.27b. The $t_{r}$ and $t_{f}$ time are obtained from the specific MOSFET data sheet.
(II) Demagnetization

The conduction losses are determined using equation A.5. The RMS current is determined using equation A. 4 as the current waveform is assumed to be of the form of a triangular pulse shape with a peak value of $I_{m}$ as shown in Figure A.27b. D is the duty cycle of continuous operation, which is determined in chapter 4 to be $10 \%$.

The switching losses are determined using equation A.6. The switching frequency, $\mathrm{f}_{\mathrm{s}}$, is determined from the speed of the SRM. From the analysis in chapter 4, high speed generating at 4500 RPM yields 450 Hz and 6000 RPM yields $600 \mathrm{~Hz} . \mathrm{V}_{\mathrm{m}}$ is equal to the peak voltage, $\mathrm{V}_{\mathrm{S}}$, across $\mathrm{Q}_{3}$ as shown in Figure A.27a and $I_{(Q 3)}=I_{m}$ as shown in Figure A.27b. The $t_{r}$ and $t_{f}$ time are obtained from the specific MOSFET data sheet.

## A.3.2.9 High speed generating - Q4



Figure A.28: (a) Converter schematic with voltage and current labelled for $\mathrm{Q}_{4}$. (b)Voltage and current waveforms for $\mathrm{Q}_{4}$ during generating and demagnetisation

The conduction and switching losses are divided into two regions of operation, (I) generating and (II) demagnetization. The conduction and switching losses for both regions are the same as for Q3.

## Appendix B - Power Analysis Computations

In the following appendix, the complete power analysis calculation results generated by a spreadsheet program are presented for the asymmetrical half-bridge converter and full-bridge synchronous rectification converter. The specific components that were evaluated are tabulated in Table B.1, while a summary of the operating conditions are provided in section B.1. The power calculation results for the asymmetrical half-bridge converter are presented in section B. 2 and the results for the components that were evaluated for the full-bridge synchronous rectification converter are presented in sections B. 3 through B.9, respectively. A number of component configurations were evaluated for the full-bridge synchronous rectification converter and these included single device and 2 or 4 devices mounted in parallel at each switching location $\left(\mathrm{Q}_{1}, \mathrm{Q}_{2}\right.$, $\mathrm{Q}_{3}$ and $\mathrm{Q}_{4}$ ).

| Device | Manufacturer | Model Number |
| :---: | :---: | :---: |
| Mosfet | APT | APT20M11JFLL |
| Diode | ST Microelectronics | STTH20002TV |
| Mosfet | Fairchild | FDP047AN08A0 |
| Mosfet | Fairchild | FDH038AN08A1 |
| Mosfet | Fairchild | FDP060AN08A0 |
| Mosfet | Infineon | SPP80N08S2L-7 |
| Mosfet | Phillips | BUK7506-76B |
| Mosfet | Phillips | PSMN009-100W |

Table B.1: Components evaluated

## B. 1 Operating Conditions



## B. 2 Asymmetric Half-Bridge - Single Devices

## B.2.1 MOSFET- APT20M11FLL, Diode -STTH20002TV



## B. 3 Full-bridge with Synchronous Rectification

## B.3.1 MOSFETs- APT20M11FLL - Single Devices



## B.3.2 Parallel MOSFETs- FDP047AN08A0 - Two Devices



## B.3.3 Parallel MOSFETs- FDP047AN08A0 - Four Devices



## B.3.4 Parallel MOSFETs- FDH038AN08A1 - Two Devices



## B.3.5 Parallel MOSFETs- FDH038AN08A1 - Four Devices



## B.3.6 Parallel MOSFETs- FDP060AN08A0 - Two Devices



## B.3.7 Parallel MOSFETs- FDP060AN08A0 - Four Devices



## B.3.8 Parallel MOSFETs- SPP80N08S2L-07 - Two Devices


B.3.9 Parallel MOSFETs- SPP80N08S2L-07 - Four Devices

| Power Analysis |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Component | Munufacturer |  | Model |  |  |  |
| MOSFET: Q1, Q2, Q3 and Q4 | Infineon |  | SPP80N08S2L-07 |  | V 13 V |  |
| Data | 100 ns |  | Device No.: | 4 |  |  |
| $\mathrm{t}_{\mathrm{T}}$ |  |  | Max Peak Current |  |  |  |
| $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})} @ \mathrm{Tj}=175^{\circ} \mathrm{C}$ (Coeff: 1) | $0.016 \Omega$ |  | $184 \mathrm{~A}\left(\mathrm{~T}_{\mathrm{C}}=115^{\circ} \mathrm{C}\right)$ |  | $\mathrm{R}_{\text {DS(ON) }}$ Coefficient @ $\mathrm{Tj}^{\text {j }} 175^{\circ} \mathrm{C}$ |  |
| $\mathrm{t}_{\mathrm{r}}$ | 1220 ns |  | Max Cont. Current |  | Rise and Fall time assumed worse |  |
| $\mathrm{t}_{\mathrm{f}}$ | 1170 ns |  |  |  | Multiply by a factor of 10 |  |
| Power Analysis | Starting | Low speed motoring | Low speed generating | High speed generating |  |  |
| Speed (RPM) | 200 | 1000 | 2000 | 4500 |  |  |
| Q1 |  |  |  |  |  |  |
| Conduction Losses |  |  |  |  |  |  |
| $\mathrm{I}_{\text {RMS(lı) }}(\mathrm{A})$ | 18 | 18 | 18 | 13 |  |  |
| $\mathrm{P}_{\mathrm{C}(1)}$ (W) | 5 | 5 | 5 | 3 |  |  |
| Switching Losses |  |  |  | 1 |  |  |
| Total Losses |  |  |  |  |  |  |
| $\mathrm{P}_{\mathrm{T}(\text { (1) }}$ (W) | 43 | 49 | 49 | 3 |  |  |
| Q2 |  |  |  |  |  |  |
| Conduction Losses |  |  |  |  |  |  |
| $\mathrm{I}_{\text {RMS(Q2) }}$ (A) | 25 | 25 | 18 | 13 |  |  |
| $\mathrm{P}_{\mathrm{C}(\mathrm{Q} 2)}(\mathrm{W})$ | 10 | 10 | 5 | 3 |  |  |
| Switching Losses |  |  |  |  |  |  |
| $\begin{gathered} \mathrm{P}_{\mathrm{S}(2) 2}(\mathrm{~W}) \\ \text { Total Losses } \end{gathered}$ | 0 | 0 | 44 | 1 |  |  |
| $\mathrm{P}_{\mathrm{T}(2) 2}$ (W) | 10 | 10 | 49 | 3 |  |  |
| Q3 |  |  |  |  |  |  |
| Freewheeling or Generating |  |  |  |  |  |  |
| Conduction Losses |  |  |  |  |  |  |
| $\mathrm{I}_{\text {RMS(Q3) }}(\mathrm{A})$ | 18 | 18 | 18 | 19 |  |  |
| $\mathrm{P}_{\text {CF(03 }}$ ( W ) | 5 | 5 | 5 | 6 |  |  |
| Switching Losses |  |  |  |  |  |  |
| $\mathrm{P}_{\text {SF(03 }}(\mathrm{W})$ | 38 | 44 | 44 | 1 |  |  |
| Demagnetisation Losses |  |  |  |  |  |  |
| Conduction Losses |  |  |  |  |  |  |
| $\mathrm{I}_{\mathrm{RMS}(\text { Q3) }}$ ( ${ }^{\text {a }}$ | 6 | 6 | 6 | 6 |  |  |
| $\mathrm{P}_{\text {CDM (Q3) }}$ (W) | 1 | 1 | 1 | 1 |  |  |
| Switching Losses |  |  |  |  |  |  |
| $\mathrm{P}_{\text {SDM(Q3) }}(\mathrm{W})$ | 0 | 0 | 0 | 1 |  |  |
| Total Losses |  |  |  |  |  |  |
| $\mathrm{P}_{\mathrm{T}(03)}$ (W) | 43 | 50 | 50 | 8 |  |  |
| Q4 |  |  |  |  |  |  |
| Total Losses |  |  |  |  |  |  |
| $\mathrm{P}_{\mathrm{T} \text { (04) }}(\mathrm{W})$ | 1 | 1 | 50 | 8 |  |  |
| Power Loss Single Phase |  |  |  |  |  |  |
| $\mathrm{P}_{\text {T(SP) }}$ (W) | 385 | 437 | 789 | 92 |  |  |
| Power Transfer of Single Phase |  |  |  |  |  |  |
| $\mathrm{I}_{\mathrm{m}}(\mathbf{A})$ | 140 | 140 | 140 | 140 |  |  |
| $\mathrm{V}_{\mathrm{m}}(\mathrm{A})$ | 36 | 42 | 42 | 42 |  |  |
| $\mathrm{P}_{\mathrm{M}}(\mathrm{W})$ | 1260 | 1470 | 1470 | 1176 |  |  |
| $\mathbf{I m}(\mathrm{A})$ | 0 | 0 | 140 | 140 |  |  |
| Vm (A) | 0 | 0 | 42 | 42 |  |  |
| $\mathrm{P}_{\mathrm{G}}(\mathrm{W})$ | 0 | 0 | 1470 | 1764 |  |  |
| $\mathbf{I m}(\mathrm{A})$ | 140 | 140 | 140 | 140 |  |  |
| $\mathbf{V m}(\mathbf{A})$ | 36 | 42 | 42 | 42 |  |  |
| $\mathrm{P}_{\mathrm{DM}}(\mathrm{W})$ | 504 | 588 | 588 | 294 |  |  |
| Efficiency of Single Phase |  |  |  |  |  |  |
| $\mathrm{P}_{\text {phase }}(\mathrm{W})$ | 1764 | 2058 | 3528 | 3234 |  |  |
| $\mathrm{P}_{\text {phase }}+\mathrm{P}_{\text {T(Sp }}(\mathrm{W})$ | 2149 | 2495 | 4317 | 3326 |  |  |
| Efficiency (\%) | 82 | 82 | 82 | 97 |  |  |

## B.3.10 Parallel MOSFETs- BUK75/7606-75B - Two Devices



## B.3.11 Parallel MOSFETs- BUK75/7606-75B - Four Devices



## B.3.12 Parallel MOSFETs- PSMN009-100W - Two Devices



## B.3.13 Parallel MOSFETs- PSMN009-100W - Four Devices



## Appendix C - Thermal Analysis Computations

The following sections present the calculations to select the most suitable heat sink for the full-bridge synchronous rectification converter. A spreadsheet program was used to implement the thermal calculations for a number of MOSFETs (Phillips BUK7506-75B, Fairchild FDP047AN08A0 and FDP060AN08A0). Calculations were implemented in order to evaluate the effect of different number of devices in parallel (2 and 4), variation in ambient temperatures $\left(45^{\circ} \mathrm{C}\right.$ and $\left.90^{\circ} \mathrm{C}\right)$, using alternative thermal conductor materials and heat spreader sizes. These calculations were implemented for each ISG mode of operation (starting, low speed motoring and high speed generating). The specific objective of the analysis was to determine the optimum heat sink selection ( $\mathrm{R}_{\theta s-a}$ value). The detailed spreadsheet calculations for the above conditions are presented in sections C. 1 through C. 12 .

The value of sink-to-ambient thermal resistance $\left(\mathrm{R}_{\theta s-\mathrm{a}}\right)$ is determined using Equation 5.4, where $P_{T(S P)}$ is the total power dissipation of the MOSFETs from the single converter phase, $T_{j(\max )}$ is the maximum junction temperature experienced by the MOSFETs $\left(\mathrm{Q}_{1}\right.$, $\mathrm{Q}_{2}, \mathrm{Q}_{3}$ or $\mathrm{Q}_{4}$ ) in the single phase converter, $T_{a}$, is the maximum ambient temperature, $R_{\theta j-c}$ is the thermal resistance of the TO-220 package, $R_{\theta c-h s}$ is the thermal resistance of the heat sink compound, $R_{\theta h s-t c}$ is the thermal resistance of the heat spreader and $R_{\theta t c-s}$ is the thermal resistance of the thermal conductor.

The projected junction temperature experienced by the devices is determined using Equation 5.5, where $T_{c}$, is the maximum case temperature and $P_{T(d e v i c e)}$ is the total power dissipation of the each MOSFET devices $\left(\mathrm{Q}_{1}, \mathrm{Q}_{2}, \mathrm{Q}_{3}\right.$ or $\left.\mathrm{Q}_{4}\right)$.

The thermal resistance of the heat spreader $\left(R_{\text {日hs-tc }}\right)$ and the thermal resistance of the thermal conductor ( $R_{\theta t c-s}$ ) is determined using Equation 5.2, where $d$ is the thickness of the material (m), $\lambda$ is thermal conductivity $\left(\mathrm{Wm}^{-10} \mathrm{C}^{-1}\right)$ of the material and $A$ is the cross sectional area ( $\mathrm{m}^{2}$ )

The specific converter layout is illustrated in Figure C. 1 for implementing two devices in parallel and a side view of the structure illustrating the different thermal resistance
layers (case, heat spreader, thermal conductor and heat sink) is illustrated in Figure C.2. The heat flow path from junction to ambient is illustrated in Figure C.3.


Figure C.1: Top view of single phase converter layout


Figure C.2: Side view of single phase converter layout


Figure C.3: The heat flow path from junction-to-ambient for the single phase converter

## C. 1 FDP047AN08A0 - Two Devices - $\mathrm{T}_{\mathrm{a}}=45^{\circ} \mathrm{C}$

| Heatsink |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Component | Munufacturer |  | Model | Thermal conductor (tc) |  | Heat spreader (hs) |  |
| MOSFET: Q1, Q2, Q3 and Q4 | Fairchild |  | FDP047AN08A0 | $\mathrm{R}_{\text {өtc-s }}\left({ }^{\circ} \mathrm{CW}{ }^{-1}\right)$ | 0.058 |  | 0.058 |
| Data |  |  |  | A ( $\mathrm{mm}^{2}$ ) | 1250 | L (mm) | 50 |
| $\mathrm{R}_{\mathrm{ej} \mathrm{j}}\left({ }^{\left(\mathrm{CW}^{-1}\right)}\right.$ | 0.48 |  |  | $\begin{gathered} \mathrm{d}(\mathrm{~mm}) \\ \lambda\left(\mathrm{Wm}^{-10} \mathrm{C}^{-1}\right) \end{gathered}$ | 0.25 | W (mm) | 25 |
| $\mathrm{R}_{\text {日c-hs }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.1 |  |  |  | 3.5 | $\begin{array}{\|c} \mathrm{d}(\mathrm{~mm}) \\ \mathrm{A}=\mathrm{LW}\left(\mathrm{~mm}^{2}\right) \\ \lambda\left(\mathrm{Wm}^{-10} \mathrm{C}^{-1}\right) \end{array}$ | $\begin{gathered} 16 \\ 1250 \\ 220 \end{gathered}$ |
| Thermal Calculations | Starting | Low speed motoring | High speed generating |  |  |  |  |
| Q1 | 200 rpm | 1000 rpm | 4500 rpm |  |  |  |  |
| $\mathrm{R}_{0 \mathrm{j} \text {-hs(Q1) }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.29 | 0.29 | 0.29 | Operating conditions |  |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 127 | 130 | 104 | Device \# | 2 |  |  |
| Q2 |  |  |  | Tc ( ${ }^{\circ} \mathrm{C}$ ) | 100 |  |  |
| $\mathrm{R}_{0 \mathrm{j} \text {-hs(Q2) }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.29 | 0.29 | 0.29 | TA $\left({ }^{\circ} \mathrm{C}\right)$ | 45 |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 113 | 113 | 104 |  |  |  |  |
| Q3 |  |  |  | Notes: |  |  |  |
| $\mathrm{R}_{0 \mathrm{j} \text {-hs(D1) }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.29 | 0.29 | 0.29 | $\begin{aligned} & \mathrm{R}_{\theta j-\mathrm{c}}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { junction to case } \\ & \mathrm{R}_{\text {ec-hs }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { heatsink compound } \\ & \mathrm{R}_{\text {ens-ct }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { heat spreader } \\ & \mathrm{R}_{\text {etc-s }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { thermal conductor } \\ & \mathrm{R}_{\text {日s-a }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { sink to ambient } \end{aligned}$ |  |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 127 | 131 | 109 |  |  |  |  |  |  |  |
| Q4 |  |  |  |  |  |  |  |  |  |  |
| $\mathrm{R}_{\mathrm{\theta j} \text {-hs }(\mathrm{D} 2)}\left({ }^{0} \mathrm{CW}^{-1}\right)$ | 0.29 | 0.29 | 0.29 |  |  |  |  |  |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 101 | 101 | 109 |  |  |  |  |  |  |  |
| Single phase converter |  |  |  |  |  |  |  |  |  |  |
| $\mathrm{R}_{\theta \text { s-a(Single Phase) }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.19 | 0.17 | 0.48 |  |  |  |  |  |  |  |

## C. 2 FDP047AN08A0 - Four Devices - $\mathrm{T}_{\mathrm{a}}=45^{\circ} \mathrm{C}$

| Heatsink |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Component | Munufacturer |  | Model | Thermal conductor (tc) |  | Heat spreader (hs) |  |
| MOSFET: Q1, Q2, Q3 and Q4 | Fairchild |  | FDP047AN08A0 | $\mathrm{R}_{\theta \text { tc-s }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.058 | $\mathrm{R}_{\text {¢hs-tc }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.058 |
| Data |  |  |  | A ( $\mathrm{mm}^{2}$ ) | 1250 | L (mm) | 50 |
| $\mathrm{R}_{\theta \text { j-c }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.48 |  |  | $\mathrm{d} \quad(\mathrm{~mm})$ | 0.25 | W (mm) | 25 |
| $\mathrm{R}_{9} \mathrm{c}$-hs $\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.1 |  |  | $\lambda\left(\mathrm{Wm}^{-10} \mathrm{C}^{-1}\right)$ | 3.5 | d (mm) | $\begin{gathered} 16 \\ 1250 \\ 220 \end{gathered}$ |
| Thermal Calculations | Starting | Low speed motoring | High speed generating |  |  | $\begin{aligned} & \mathrm{A}=\mathrm{LW}\left(\mathrm{~mm}^{2}\right) \\ & \lambda\left(\mathrm{Wm}^{-10} \mathrm{C}^{-1}\right) \end{aligned}$ |  |
| Q1 | 200 rpm | 1000 rpm | 4500 rpm |  |  |  |  |
| $\mathrm{R}_{\text {日j-hs(Q1) }}\left({ }^{\mathrm{O}} \mathrm{CW}^{-1}\right)$ | 0.15 | 0.15 | 0.15 | Operating conditions |  |  |  |
| TJ ( ${ }^{\text {O }}$ ) | 112 | 113 | 101 | Device \# | 4 |  |  |
| Q2 |  |  |  | Tc ( ${ }^{0} \mathrm{C}$ ) | 100 |  |  |
| $\mathrm{R}_{\mathrm{\theta j} \text {-hs(Q2) }}\left({ }^{\mathrm{O}} \mathrm{CW}^{-1}\right)$ | 0.15 | 0.15 | 0.15 | $\mathrm{TA}_{\mathrm{A}}\left({ }^{\circ} \mathrm{C}\right)$ | 45 |  |  |
| $\mathrm{TJ}\left({ }^{\circ} \mathrm{C}\right)$ | 103 | 103 | 101 |  |  |  |  |
| Q3 |  |  |  | Notes: |  |  |  |
| $\mathrm{R}_{\text {日j-hs(D1) }}\left({ }^{\mathrm{O}} \mathrm{CW}^{-1}\right)$ | 0.15 | 0.15 | 0.15 | $\begin{aligned} & \mathrm{R}_{\text {ej-c }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { junction to case } \\ & \mathrm{R}_{\text {ec-hs }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { heatsink compound } \\ & \mathrm{R}_{\text {ehs-ctc }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { heat spreader } \\ & \mathrm{R}_{\text {etc-s }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { thermal conductor } \\ & \mathrm{R}_{\text {es-a }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { sink to ambient } \end{aligned}$ |  |  |  |
| $\mathrm{TJ}\left({ }^{\circ} \mathrm{C}\right)$ | 112 | 114 | 103 |  |  |  |  |  |  |
| Q4 |  |  |  |  |  |  |  |  |  |
| $\mathrm{R}_{\mathrm{\theta j} \text {-hs(D2) }}\left({ }^{\mathrm{O}} \mathrm{CW}^{-1}\right)$ | 0.15 | 0.15 | 0.15 |  |  |  |  |  |  |
| $\left.\mathrm{TJ}^{( }{ }^{\circ} \mathrm{C}\right)$ | 100 | 100 | 103 |  |  |  |  |  |  |
| Single phase converter |  |  |  |  |  |  |  |  |  |
| $\mathrm{R}_{\theta} \mathrm{s}$-a(Single Phase) $\left({ }^{\circ} \mathrm{CW}^{-1}\right.$ ) | 0.23 | 0.20 | 0.88 |  |  |  |  |  |  |

## C. 3 FDP047AN08A0 - Two Devices - $\mathrm{T}_{\mathrm{a}}=\mathbf{9 0}^{\circ} \mathrm{C}$



## C. 4 FDP047AN08A0 - Four Devices - $\mathrm{T}_{\mathrm{a}}=\mathbf{9 0}^{\circ} \mathrm{C}$

| Heatsink |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Component | Munufacturer |  | Model | Thermal conductor (tc) |  | Heat spreader (hs) |  |
| MOSFET: Q1, Q2, Q3 and Q4 | Fairchild |  | FDP047AN08A0 | $\mathrm{R}_{\text {Qta-s }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.058 |  | 0.058 |
| Data |  |  |  | A ( $\mathrm{mm}^{2}$ ) | 1250 | L (mm) | 50 |
| $\mathrm{R}_{\mathrm{\theta j} \text {-c }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.48 |  |  | $\begin{gathered} \mathrm{d}(\mathrm{~mm}) \\ \lambda\left(\mathrm{Wm}^{-10} \mathrm{C}^{-1}\right) \end{gathered}$ | 0.25 | W (mm) | 25 |
| $\mathrm{R}_{\theta \text { c-hs }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.1 |  |  |  | 3.5 | $\begin{gathered} \mathrm{d}(\mathrm{~mm}) \\ \mathrm{A}=\mathrm{LW}\left(\mathrm{~mm}^{2}\right) \\ \lambda\left(\mathrm{Wm}^{-10} \mathrm{C}^{-1}\right) \end{gathered}$ | $\begin{gathered} 16 \\ 1250 \\ 220 \end{gathered}$ |
| Thermal Calculations | Starting | Low speed motoring | High speed generating |  |  |  |  |
| Q1 | 200 rpm | 1000 rpm | 4500 rpm |  |  |  |  |
| $\mathrm{R}_{\text {¢j-hs }(\mathrm{Q} 1)}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.15 | 0.15 | 0.15 | Operating conditions |  |  |  |
| $\left.\mathrm{TJ}^{(0}{ }^{\circ} \mathrm{C}\right)$ | 112 | 113 | 101 | Device \# | 4 |  |  |
| Q2 |  |  |  | Tc ( ${ }^{\circ} \mathrm{C}$ ) | 100 |  |  |
| $\mathrm{R}_{\text {dj- hs (Q2) }}\left({ }^{0} \mathrm{CW}^{-1}\right)$ | 0.15 | 0.15 | 0.15 | $\mathrm{TA}_{\mathbf{A}}\left({ }^{\circ} \mathrm{C}\right)$ | 90 |  |  |
| TJ ( ${ }^{\text {C }}$ ) | 103 | 103 | 101 |  |  |  |  |
| Q3 |  |  |  | Notes: |  |  |  |
| $\mathrm{R}_{\mathrm{\theta j} \text {-hs }(\mathrm{Dl})\left({ }^{0} \mathrm{CW}^{-1}\right)}$ | 0.15 | 0.15 | 0.15 | $\begin{aligned} & \mathrm{R}_{\text {Qj-c }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { junction to case } \\ & \mathrm{R}_{\text {gc-hs }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { heatsink compound } \\ & \mathrm{R}_{\text {ehs-ctc }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { heat spreader } \\ & \mathrm{R}_{\text {etc-s }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { thermal conductor } \\ & \mathrm{R}_{\theta s-\mathrm{a}}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { sink to ambient } \end{aligned}$ |  |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 112 | 114 | 103 |  |  |  |  |  |  |  |
| Q4 |  |  |  |  |  |  |  |  |  |  |
| $\mathrm{R}_{\theta \mathrm{j} \text {-hs (D2) }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.15 | 0.15 | 0.15 |  |  |  |  |  |  |  |
| $\left.\mathrm{TJ}^{(0}{ }^{\circ} \mathrm{C}\right)$ | 100 | 100 | 103 |  |  |  |  |  |  |  |
| Single phase converter |  |  |  |  |  |  |  |  |  |  |
| $\mathrm{R}_{\theta \text { s-a(Single Phase) }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.032 | 0.028 | 0.141 |  |  |  |  |  |  |  |

C. 5 FDP060AN08A0- Two Devices - $\mathrm{T}_{\mathrm{a}}=45^{\circ} \mathrm{C}$

| Heatsink |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Component | Munufacturer |  | Model | Thermal conductor (tc) |  | Heat spreader (hs) |  |
| MOSFET: Q1, Q2, Q3 and Q4 | Fairchild |  | FDP060AN08A0 | $\mathrm{R}_{\text {dtass }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.058 | $\mathrm{R}_{\text {日hs-tc }}{ }^{(0} \mathrm{CW}^{-1}$ ) | 0.058 |
| Data |  | Low speed <br> motoring High speed <br> generating |  | $\begin{aligned} & \mathrm{A}\left(\mathrm{~mm}^{2}\right) \\ & \mathrm{d}(\mathrm{~mm}) \\ & \lambda\left(\mathrm{Wm}^{-10} \mathrm{C}^{-1}\right) \end{aligned}$ | $\begin{gathered} 1250 \\ 0.25 \\ 3.5 \end{gathered}$ | L (mm) | 50 |
| $\mathrm{R}_{\mathrm{\theta j} \text {-c }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.48 |  |  | W (mm) |  | 25 |
| $\mathrm{R}_{\mathrm{\theta} \text { c-hs }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.1 |  |  | $\lambda\left(\mathrm{Wm}^{-10} \mathrm{C}^{-1}\right)$ | $3.5$ | d (mm) | 16 |
| Thermal Calculations | Starting |  |  | $\begin{gathered} A=L W\left(\mathrm{~mm}^{2}\right) \\ \lambda\left(\mathrm{Wm}^{-10} \mathrm{C}^{-1}\right) \end{gathered}$ |  | $\begin{array}{r} 1250 \\ 220 \\ \hline \end{array}$ |
| Q1 | 200 rpm | 1000 rpm | 4500 rpm |  |  |  |  |  |
| $\mathrm{R}_{\text {¢j-hs }(\mathrm{Q} 1)}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.29 | 0.29 | 0.29 | Operating conditions |  |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 125 | 128 | 105 | Device \# | 2 |  |  |
| Q2 |  |  |  | Tc ( ${ }^{\circ} \mathrm{C}$ ) | 100 |  |  |
| $\mathrm{R}_{\text {¢j- hs (Q2) }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.29 | 0.29 | 0.29 | $\mathrm{TA}^{( }{ }^{\circ} \mathrm{C}$ ) | 45 |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 116 | 116 | 105 |  |  |  |  |
| Q3 |  |  |  | Notes: |  |  |  |
| $\mathrm{R}_{\text {¢ }}$-hs( $\mathrm{Dl}^{1}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.29 | 0.29 | 0.29 | $\begin{aligned} & \mathrm{R}_{\text {ficc }}\left({ }^{\circ}{ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { junction to case } \\ & \left.\mathrm{R}_{\text {ec-hs }}{ }^{\circ}{ }^{\circ} W^{-1}\right)=\text { Thermal resistance }- \text { heatsink compound } \\ & \left.\mathrm{R}_{\text {ebs-ctc }}{ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { heat spreader } \\ & \mathrm{R}_{\text {elc-s }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { thermal conductor } \\ & \left.\mathrm{R}_{\text {esa }}{ }^{\circ}{ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { sink to ambient } \end{aligned}$ |  |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 127 | 130 | 111 |  |  |  |  |  |
| Q4 |  |  |  |  |  |  |  |  |
| $\mathrm{R}_{\text {¢ }}$-hs(D2) $\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.29 | 0.29 | 0.29 |  |  |  |  |  |
| $\left.\mathrm{TJ}^{(0}{ }^{\circ} \mathrm{C}\right)$ | 101 | 101 | 111 |  |  |  |  |  |
| Single phase converter |  |  |  |  |  |  |  |  |
| $\mathrm{R}_{\theta \text { s-a(Single Phase) }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.18 | 0.17 | 0.41 |  |  |  |  |  |

## C. 6 FDP060AN08A0 - Four Devices $-\mathrm{T}_{\mathrm{a}}=\mathbf{4 5}^{\circ} \mathrm{C}$

| Heatsink |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Component | Munufacturer |  | Model | Thermal conductor (tc) |  | Heat spreader (hs) |  |
| MOSFET: Q1, Q2, Q3 and Q4 | Fairchild |  | FDP060AN08A0 | $\mathrm{R}_{\text {ftcs }}\left({ }^{\circ} \mathrm{CW}{ }^{-1}\right)$ | 0.058 | $\mathrm{R}_{\text {日hs }{ }^{\text {ctc }}{ }^{\circ} \mathrm{CW}^{-1} \text { ) }}$ | 0.058 |
| Data |  |  |  | A ( $\mathrm{mm}^{2}$ ) | 1250 | L (mm) | 50 |
| $\mathrm{R}_{\mathrm{\theta j} \text {-c }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.48 |  |  | $\begin{gathered} \mathrm{d}(\mathrm{~mm}) \\ \lambda\left(\mathrm{Wm}^{-10} \mathrm{C}^{-1}\right) \end{gathered}$ | 0.25 | W (mm) | 25 |
| $\mathrm{R}_{\theta \text { c-hs }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.1 |  |  |  | 3.5 | $\begin{gathered} \mathrm{d}(\mathrm{~mm}) \\ \mathrm{A}=\mathrm{LW}\left(\mathrm{~mm}^{2}\right) \end{gathered}$ | 16 |
| Thermal Calculations | Starting | Low speed motoring | High speed generating |  |  |  | 1250 |
| Q1 | 200 rpm | 1000 rpm | 4500 rpm |  |  |  |  |
| $\mathrm{R}_{\text {¢j-hs }(\mathrm{Q})}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.15 | 0.15 | 0.15 | Operating conditions |  |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 111 | 112 | 101 | Device \# | 4 |  |  |
| Q2 |  |  |  | Tc ( ${ }^{\circ} \mathrm{C}$ ) | 100 |  |  |
| $\mathrm{R}_{0 \mathrm{j} \text {-hs(Q2) }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.15 | 0.15 | 0.15 | TA $\left({ }^{\circ} \mathrm{C}\right)$ | 45 |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 104 | 104 | 101 |  |  |  |  |
| Q3 |  |  |  | Notes: |  |  |  |
| $\mathrm{R}_{\mathrm{\theta j}^{\text {j-hs }(\mathrm{Dl})}\left({ }^{\circ} \mathrm{CW}^{-1}\right)}$ | 0.15 | 0.15 | 0.15 |  |  |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 111 | 113 | 103 |  |  |  |  |  |  |
| Q4 |  |  |  |  |  |  |  |  |  |
| $\mathrm{R}_{\text {dj- hs }(\mathrm{D} 2)}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.15 | 0.15 | 0.15 |  |  |  |  |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 100 | 100 | 103 |  |  |  |  |  |  |
| Single phase converter |  |  |  |  |  |  |  |  |  |
| $\mathrm{R}_{\theta \text { s-a(Single }}$ Phase) $\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.24 | 0.21 | 0.77 |  |  |  |  |  |  |

C. 7 FDP060AN08A0- Two Devices - $\mathrm{T}_{\mathrm{a}}=\mathbf{9 0}^{\circ} \mathrm{C}$

| Heatsink | Munufacturer |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Component |  |  | Model | Thermal conductor (tc) |  | Heat spreader (hs) |  |
| MOSFET: Q1, Q2, Q3 and Q4 | Fairchild |  | FDP060AN08A0 | $\mathrm{R}_{\text {Qtas. }}\left({ }^{\circ} \mathrm{CW}{ }^{-1}\right)$ | 0.058 | $\mathrm{R}_{\left.\mathrm{\theta} \mathrm{hs} \text {-ct }{ }^{(0} \mathrm{CW}^{-1}\right)}$ | 0.058 |
| Data |  |  |  | A ( $\mathrm{mm}^{2}$ ) | 1250 | L (mm) | 50 |
| $\mathrm{R}_{\mathrm{\theta j} \mathrm{j}}\left({ }^{\left(\mathrm{CW}^{-1}\right)}\right.$ | 0.48 |  |  | $\begin{gathered} \mathrm{d}(\mathrm{~mm}) \\ \lambda\left(\mathrm{Wm}^{-10} \mathrm{C}^{-1}\right) \end{gathered}$ | 0.25 | W (mm) | 25 |
| $\mathrm{R}_{\mathrm{\theta} \text { c-hs }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.1 |  |  |  | 3.5 | $\begin{array}{\|c\|} \hline \mathrm{d}(\mathrm{~mm}) \\ \mathrm{A}=\mathrm{LW}\left(\mathrm{~mm}^{2}\right) \\ \lambda\left(\mathrm{Wm}^{-10} \mathrm{C}^{-1}\right) \\ \hline \end{array}$ | $\begin{gathered} 16 \\ 1250 \\ 220 \end{gathered}$ |
| Thermal Calculations | Starting | Low speed motoring | High speed generating |  |  |  |  |
| Q1 | 200 rpm | 1000 rpm | 4500 rpm |  |  |  |  |
| $\mathrm{R}_{\text {¢j-hs(Q1) }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.29 | 0.29 | 0.29 | Operating conditions |  |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 125 | 128 | 105 | Device \# | 2 |  |  |
| Q2 |  |  |  | Tc $\left({ }^{\circ} \mathrm{C}\right)$ | 100 |  |  |
| $\mathrm{R}_{\text {dj-hs(Q2) }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.29 | 0.29 | 0.29 | TA $\left({ }^{\circ} \mathrm{C}\right)$ | 90 |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 116 | 116 | 105 |  |  |  |  |
| Q3 |  |  |  | Notes: |  |  |  |
| $\mathrm{R}_{\mathrm{\theta j} \text {-hs(D1) }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.29 | 0.29 | 0.29 |  |  |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 127 | 130 | 111 |  |  |  |  |  |  |  |
| Q4 |  |  |  |  |  |  |  |  |  |  |
| $\mathrm{R}_{\text {¢j-hs }}(\mathrm{D} 2)\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.29 | 0.29 | 0.29 |  |  |  |  |  |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 101 | 101 | 111 |  |  |  |  |  |  |  |
| Single phase converter |  |  |  |  |  |  |  |  |  |  |
| $\mathrm{R}_{\theta \text { s-a(Single Phase) }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.026 | 0.026 | 0.061 |  |  |  |  |  |  |  |

## C. 8 FDP060AN08A0- Four Devices - $\mathrm{T}_{\mathrm{a}}=\mathbf{9 0}^{\circ} \mathrm{C}$

| Heatsink |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Component | Munufacturer |  | Model | Thermal conductor (tc) |  | Heat spreader (hs) |  |
| MOSFET: Q1, Q2, Q3 and Q4 | Fairchild |  | FDP060AN08A0 | $\mathrm{R}_{\text {Qtass }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.058 | $\left.\mathrm{R}_{\text {¢hs-tct }}{ }^{(0} \mathrm{CW}^{-1}\right)$ | 0.058 |
| Data |  | Low speed <br> motoring High speed <br> generating |  | $\begin{aligned} & \mathrm{A}\left(\mathrm{~mm}^{2}\right) \\ & \mathrm{d}(\mathrm{~mm}) \\ & \lambda\left(\mathrm{Wm}^{-10} \mathrm{C}^{-1}\right) \end{aligned}$ | $\begin{gathered} 1250 \\ 0.25 \\ 3.5 \end{gathered}$ | L (mm) | 50 |
| $\mathrm{R}_{\mathrm{\theta j} \text {-c }}\left({ }^{\left(\mathrm{CW}^{-1}\right)}\right.$ | 0.48 |  |  | W (mm) |  | 25 |
| $\mathrm{R}_{\mathrm{\theta} \mathrm{c} \text {-hs }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.1 |  |  | $\lambda\left(\mathrm{Wm}^{-10} \mathrm{C}^{-1}\right)$ | $3.5$ | d (mm) | 16 |
| Thermal Calculations | Starting |  |  | $\begin{gathered} A=L W\left(\mathrm{~mm}^{2}\right) \\ \lambda\left(\mathrm{Wm}^{-10} \mathrm{C}^{-1}\right) \end{gathered}$ |  | $\begin{array}{r} 1250 \\ 220 \end{array}$ |
| Q1 | 200 rpm | 1000 rpm | 4500 rpm |  |  |  |  |  |
| $\mathrm{R}_{\text {¢j-hs(Q1) }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.15 | 0.15 | 0.15 | Operating conditions |  |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 111 | 112 | 101 | Device \# | 4 |  |  |
| Q2 |  |  |  | Tc ( ${ }^{\circ} \mathrm{C}$ ) | 100 |  |  |
| $\mathrm{R}_{\text {¢j- hs (Q2) }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.15 | 0.15 | 0.15 | TA $\left({ }^{\circ} \mathrm{C}\right)$ | 90 |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 104 | 104 | 101 |  |  |  |  |
| Q3 |  |  |  | Notes: |  |  |  |
| $\mathrm{R}_{\mathrm{\theta j} \text {-hs }(\mathrm{D} 1)}\left({ }^{0} \mathrm{CW}^{-1}\right)$ | 0.15 | 0.15 | 0.15 | $\mathrm{R}_{\mathrm{\theta j-c}}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=$ Thermal resistance - junction to case <br> $\mathrm{R}_{\theta c-h s}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=$ Thermal resistance - heatsink compound <br> $\mathrm{R}_{\text {ens-tc }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=$ Thermal resistance - heat spreader <br> $\mathrm{R}_{\text {tc-s }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=$ Thermal resistance - thermal conductor <br> $\mathrm{R}_{\theta \mathrm{s} \text {-a }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=$ Thermal resistance - sink to ambient |  |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 111 | 113 | 103 |  |  |  |  |  |
| Q4 |  |  |  |  |  |  |  |  |
| $\mathrm{R}_{\text {¢ }}$-hs(D2) $\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.15 | 0.15 | 0.15 |  |  |  |  |  |
| $\mathrm{TJ}^{( }{ }^{\circ} \mathrm{C}$ ) | 100 | 100 | 103 |  |  |  |  |  |
| Single phase converter |  |  |  |  |  |  |  |  |
| $\mathrm{R}_{\theta \text { s-a(Single Phase) }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.032 | 0.028 | 0.121 |  |  |  |  |  |

## C． 9 BUK75／7606－75B－Two Devices－ $\mathrm{T}_{\mathrm{a}}=45{ }^{\circ} \mathrm{C}$

| Heatsink |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Component | Munufacturer |  | Model | Thermal conductor（tc） |  | Heat spreader（hs） |  |
| MOSFET：Q1，Q2，Q3 and Q4 | Phillips Semi |  | BUK75／7606－75B | $\mathrm{R}_{\text {ftas }}\left({ }^{\circ} \mathrm{CW}{ }^{-1}\right)$ | 0.058 | $\mathrm{R}_{\text {dhs } \mathrm{tctc}^{\circ}\left({ }^{\circ} \mathrm{CW}{ }^{-1}\right)}$ | 0.058 |
| Data |  |  |  | $\begin{aligned} & \mathrm{A}\left(\mathrm{~mm}^{2}\right) \\ & \mathrm{d}(\mathrm{~mm}) \\ & \lambda\left(\mathrm{Wm}^{-10} \mathrm{C}^{-1}\right) \end{aligned}$ | 1250 | L（mm） | 50 |
| $\mathrm{R}_{\mathrm{\theta j} \text {－c }}\left({ }^{\left(\mathrm{CW}^{-1}\right)}\right.$ | 0.48 |  |  |  | 0.25 | W（mm） | 25 |
| $\mathrm{R}_{\theta \text { c－hs }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.1 |  |  |  | 3.5 | d（mm） | 16 |
| Thermal Calculations | Starting | Low speed motoring | High speed generating |  |  | $\begin{aligned} & A=\mathrm{LW}\left(\mathrm{~mm}^{2}\right) \\ & \lambda\left(\mathrm{Wm}^{-10} \mathrm{C}^{-1}\right) \end{aligned}$ | $\begin{array}{r} 1250 \\ 220 \\ \hline \end{array}$ |
| Q1 | 200 rpm | 1000 rpm | 4500 rpm |  |  |  |  |
| $\mathrm{R}_{\text {¢j－hs }(\mathrm{Q})}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.29 | 0.29 | 0.29 | Operating conditions |  |  |  |
| TJ（ ${ }^{\circ} \mathrm{C}$ ） | 123 | 125 | 104 | Device \＃ | 2 |  |  |
| Q2 |  |  |  | Tc（ ${ }^{\circ} \mathrm{C}$ ） | 100 |  |  |
| $\mathrm{R}_{\text {®j－hs（Q2）}}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.29 | 0.29 | 0.29 | $\mathrm{TA}^{( }{ }^{\circ} \mathrm{C}$ ） | 45 |  |  |
| TJ（ ${ }^{\circ} \mathrm{C}$ ） | 114 | 114 | 104 |  |  |  |  |
| Q3 |  |  |  | Notes： |  |  |  |
| $\mathrm{R}_{\text {dj－hs（ } \mathrm{Dl})}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.29 | 0.29 | 0.29 | $\begin{aligned} & \mathrm{R}_{\text {日j-c }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { junction to case } \\ & \mathrm{R}_{\text {ec-hs }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { heatsink compound } \\ & \mathrm{R}_{\text {ehb-ct }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { heat spreader } \\ & \mathrm{R}_{\text {日lc-s }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { thermal conductor } \\ & \mathrm{R}_{\text {日s-a }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { sink to ambient } \end{aligned}$ |  |  |  |
| TJ（ ${ }^{\circ} \mathrm{C}$ ） | 124 | 126 | 110 |  |  |  |  |  |
| Q4 |  |  |  |  |  |  |  |  |
| $\mathrm{R}_{0 \mathrm{j} \text {－hs }(\mathrm{D} 2)}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.29 | 0.29 | 0.29 |  |  |  |  |  |
| TJ（ ${ }^{\circ} \mathrm{C}$ ） | 101 | 101 | 110 |  |  |  |  |  |
| Single phase converter |  |  |  |  |  |  |  |  |
| $\mathrm{R}_{\theta \text { s－a（Single Phase）}}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.21 | 0.19 | 0.46 |  |  |  |  |  |

## C. 10 BUK75/7606-75B - Four Devices - $\mathrm{T}_{\mathrm{a}}=45{ }^{\circ} \mathrm{C}$

| Heatsink | Munufacturer |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Component |  |  | Model | Thermal conductor (tc) |  | Heat spreader (hs) |  |
| MOSFET: Q1, Q2, Q3 and Q4 | Phillips Semi |  | BUK75/7606-75B | $\mathrm{R}_{\text {Qtass }}\left({ }^{\circ} \mathrm{CW}{ }^{-1}\right)$ | 0.058 | $\mathrm{R}_{\text {¢ } \mathrm{hs} \text {-tc }}{ }^{( } \mathrm{CW}^{-1}$ ) | 0.058 |
| Data |  | Low speed <br> motoring High speed <br> generating |  | A ( $\mathrm{mm}^{2}$ ) | 1250 | L (mm) | 50 |
| $\mathrm{R}_{\mathrm{ej} \mathrm{j}}\left({ }^{\left(\mathrm{CW}^{-1}\right)}\right.$ | 0.48 |  |  | $\begin{gathered} \mathrm{d}(\mathrm{~mm}) \\ \lambda\left(\mathrm{Wm}^{-1} \mathrm{C}^{-1}\right) \end{gathered}$ | $\begin{gathered} 0.25 \\ 3.5 \end{gathered}$ | W (mm) | $\begin{gathered} 25 \\ 16 \\ 1250 \\ 220 \\ \hline \end{gathered}$ |
| $\mathrm{R}_{\text {日c-hs }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.1 |  |  | $\lambda\left(\mathrm{Wm}^{-10} \mathrm{C}^{-1}\right)$ | $3.5$ | d (mm) |  |
| Thermal Calculations | Starting |  |  | $\begin{aligned} & A=L W\left(\mathrm{~mm}^{2}\right) \\ & \lambda\left(\mathrm{Wm}^{-10} \mathrm{C}^{-1}\right) \end{aligned}$ |  |  |
| Q1 | 200 rpm | 1000 rpm | 4500 rpm |  |  |  |  |  |
| $\mathrm{R}_{0 \mathrm{j} \text {-hs(Q1) }}\left({ }^{0} \mathrm{CW}^{-1}\right)$ | 0.15 | 0.15 | 0.15 | Operating conditions |  |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 110 | 111 | 101 | Device \# | 4 |  |  |
| Q2 |  |  |  | Tc ( ${ }^{\circ} \mathrm{C}$ ) | 100 |  |  |
| $\mathrm{R}_{\text {¢j-hs (Q2) }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.15 | 0.15 | 0.15 | $\mathrm{TA}^{( }{ }^{\circ} \mathrm{C}$ ) | 45 |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 103 | 103 | 101 |  |  |  |  |
| Q3 |  |  |  | Notes: |  |  |  |
| $\mathrm{R}_{\text {dj-hs( } \mathrm{Dl})}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.15 | 0.15 | 0.15 | $\begin{aligned} & \mathrm{R}_{\theta j-\mathrm{c}}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { junction to case } \\ & \mathrm{R}_{\text {ec-hs }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { heatsink compound } \\ & \mathrm{R}_{\text {ens-ct }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { heat spreader } \\ & \mathrm{R}_{\text {etc-s }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { thermal conductor } \\ & \mathrm{R}_{\text {日s-a }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { sink to ambient } \end{aligned}$ |  |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 110 | 111 | 103 |  |  |  |  |  |  |
| Q4 |  |  |  |  |  |  |  |  |  |
| $\mathrm{R}_{\text {¢ }}$-hs(D2) $\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.15 | 0.15 | 0.15 |  |  |  |  |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 100 | 100 | 103 |  |  |  |  |  |  |
| Single phase converter |  |  |  |  |  |  |  |  |  |
| $\mathrm{R}_{\theta \text { - }}$ a(Single Phase) $\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.27 | 0.24 | 0.86 |  |  |  |  |  |  |

## C. 11 BUK75/7606-75B - Two Devices - $\mathrm{T}_{\mathrm{a}}=90^{\circ} \mathrm{C}$



## C. 12 BUK75/7606-75B - Four Devices - $\mathrm{T}_{\mathrm{a}}=90^{\circ} \mathrm{C}$

| Heatsink |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Component | Munufacturer |  | Model | Thermal conductor (tc) |  | Heat spreader (hs) |  |
| MOSFET: Q1, Q2, Q3 and Q4 | Phillips Semi |  | BUK75/7606-75B | $\mathrm{R}_{\text {ftcs }}\left({ }^{\circ} \mathrm{CW}{ }^{-1}\right)$ | 0.058 | $\mathrm{R}_{\text {¢ }}$ s-tc( ${ }^{\circ}{ }^{\circ} \mathrm{CW}{ }^{-1}$ ) | 0.058 |
| Data |  |  |  |  | 1250 | L (mm) | 50 |
| $\mathrm{R}_{\mathrm{\theta j} \text {-c }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.48 |  |  | $\begin{gathered} \mathrm{d}(\mathrm{~mm}) \\ \lambda\left(\mathrm{Wm}^{-1} \mathrm{C}^{-1}\right) \end{gathered}$ | 0.25 | W (mm) | 25 |
| $\mathrm{R}_{\theta \text { c-hs }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.1 |  |  |  | 3.5 | $\begin{array}{\|c\|} \hline \text { d }(\mathrm{mm}) \\ \mathrm{A}=\mathrm{LW}\left(\mathrm{~mm}^{2}\right) \\ \lambda\left(\mathrm{Wm}^{-10} \mathrm{C}^{-1}\right) \\ \hline \end{array}$ | $\begin{gathered} 16 \\ 1250 \\ 220 \end{gathered}$ |
| Thermal Calculations | Starting | Low speed motoring | High speed generating |  |  |  |  |
| Q1 | 200 rpm | 1000 rpm | 4500 rpm |  |  |  |  |
| $\mathrm{R}_{\text {¢j-hs }(\mathrm{Q} 1)}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.15 | 0.15 | 0.15 | Operating conditions |  |  |  |
| $\left.\mathrm{TJ}^{(0}{ }^{\circ} \mathrm{C}\right)$ | 110 | 111 | 101 | Device \# | 4 |  |  |
| Q2 |  |  |  | Tc ( ${ }^{\circ} \mathrm{C}$ ) | 100 |  |  |
| $\mathrm{R}_{\text {¢j-hs(Q2) }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.15 | 0.15 | 0.15 | $\mathrm{T}_{\mathrm{A}}\left({ }^{\circ} \mathrm{C}\right)$ | 90 |  |  |
| TJ ( ${ }^{\text {C }}$ ) | 103 | 103 | 101 |  |  |  |  |
| Q3 |  |  |  | Notes: |  |  |  |
| $\mathrm{R}_{\mathrm{\theta j} \text {-hs }(\mathrm{Dl})\left({ }^{0} \mathrm{CW}^{-1}\right)}$ | 0.15 | 0.15 | 0.15 | $\begin{aligned} & \mathrm{R}_{\text {Qj-c }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { junction to case } \\ & \mathrm{R}_{\text {gc-hs }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { heatsink compound } \\ & \mathrm{R}_{\text {ehs-ctc }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { heat spreader } \\ & \mathrm{R}_{\text {etc-s }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { thermal conductor } \\ & \mathrm{R}_{\theta s-\mathrm{a}}\left({ }^{\circ} \mathrm{CW}^{-1}\right)=\text { Thermal resistance }- \text { sink to ambient } \end{aligned}$ |  |  |  |
| TJ ( ${ }^{\circ} \mathrm{C}$ ) | 110 | 111 | 103 |  |  |  |  |  |  |  |
| Q4 |  |  |  |  |  |  |  |  |  |  |
| $\mathrm{R}_{\text {¢j }-\mathrm{hs}(\mathrm{D} 2)}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.15 | 0.15 | 0.15 |  |  |  |  |  |  |  |
| $\left.\mathrm{TJ}^{(0}{ }^{\circ} \mathrm{C}\right)$ | 100 | 100 | 103 |  |  |  |  |  |  |  |
| Single phase converter |  |  |  |  |  |  |  |  |  |  |
| $\mathrm{R}_{\theta \text { s-a(Single Phase) }}\left({ }^{\circ} \mathrm{CW}^{-1}\right)$ | 0.038 | 0.033 | 0.138 |  |  |  |  |  |  |  |

## Appendix D - Experimental System

D. 1 Schematics


Figure D.1.1: Interconnect block diagram


Figure D.1.2: Interconnect block schematic


Figure D.1.3: Schematic of converter circuit


Figure D.1.4: Schematic of interface circuit (Murphy 2002)


Figure D.1.5: Schematic of power supply circuit (sheet 1 of 2) (Murphy 2002)


Figure D.1.6: Schematic of power supply circuit (sheet 2 of 2) (Murphy 2002)

## D. 2 Photographs of the experimental system



Figure D.2.1: Bench test experimental system


Figure D.2.2: Converter and RL load


Figure D.2.3: ADSP-21992 EZ-KIT Lite board


Figure D.2.4: Power supply circuitry


Figure D.2.5: Interface electronics board


Figure D.2.6: Motor rig - SRM and Terco test apparatus

# Appendix E - ADSP-21992 EZ-KIT Lite Evaluation System Board 

The ADSP-21992 EZ-KIT Lite was developed by Analog Devices in order to allow for fast and efficient system development. This board was employed in the experimental set-up for the development and test of the SRM converter operation and current control strategy. The EZ-KIT Lite development board facilitates access to all the capabilities of the ADSP-21992 digital signal processor (DSP). The board's features include (Analog Devices 2003b):

- Analog Devices ADSP-21992 160 MHz , mixed-signal DSP
- USB debugging interface
- Analog input circuitry
- 8-channel 12-bit DAC (AD5328BRU) on SPI interface
- PWM outputs interface
- External memory interface
- Encoder interface circuitry
- General-purpose I/O interface
- UART interface (RS-232)
- CAN interface circuitry
- Flash memory (512K x 8)
- External SRAM (64K x 16)
- Interface connectors
- 14-pin emulator connector for JTAG interface
- Analog inputs connector
- DAC outputs connector
- PWM outputs connector
- Encoder interface connector
- SPORT connector
- RS-232 connector
- External memory interface connector

This development board was designed for use in conjunction with the VisualDSP++ development environment. VisualDSP++ runs on a Personal Computer (PC) and provides a single, integrated project management and debugging environment for advanced code development and debugging tasks to be performed. Access to the ADSP21992 processor on the EZ-KIT Lite board from the PC is achieved through a USB port or an optional JTAG emulator. An assembly drawing for the ADSP-21992 EZ-KIT Lite development board is shown in Figure E. 1 (Analog Devices 2003b).


Figure E.1: Assembly drawing for the ADSP-21992 EZ-KIT Lite development board

The ADSP-21992 is ideal for SRM control applications because of the number of integrated special purpose and motor control peripherals. In the work described in this thesis, a number of these special purpose units were employed in the operation and control of the converter, which included the Analog-to-Digital Converter (ADC), the PWM Generation unit, the Auxiliary PWM Generation unit, the Program Sequencer and the Peripheral Interrupt Controller and the Flag I/O peripheral unit. A brief description of each of these units is included below.

## E1. Overview of the Analog-to-Digital Conversion unit

The ADC unit on the ADSP-21992 accurately converts up to eight independent analog signals, such as the signals required for high performance current regulation, into digital signals through a 14-bit pipeline flash ADC. The ADC clock rate is programmable with a maximum ADC clock rate of 20 MHz . The full conversion of a single channel takes 7.5 ADC clock cycles.

All eight analog inputs applied to the analog input connector on the EZ-KIT Lite board (Connector P4 in Figure E.1) must be in the range from -1 V to +1 V . The analog interface circuitry then converts the $\pm 1 \mathrm{~V}$ signals on the input connector to signals centred on the ADSP-21992 reference voltage level (either the internally derived 1V
level or the externally provided 1.024 V level). Effectively, the analog interface circuits offset the analog connector inputs by the reference voltage level.

A functional block diagram of the ADC unit of the ADSP-21992 is shown in Figure E. 2 (Analog Devices 2003c). As can be seen, the eight input signals are divided into two banks of four signals. VIN0-VIN3 makes up one bank while the other is comprised of the signals on VIN4-VIN7. The internal multiplexers are used to connect the various analog inputs to the ADC.


Figure E.2: Functional block diagram of the ADC unit

There are a number of different conversion modes that can be selected using bits 4-6 in the ADCCTRL register. However, during the course of this project only one mode of operation was employed: simultaneous sampling mode (selected by clearing bits 4-6). In this mode, two analog inputs (one from each four-signal bank) are sampled simultaneously. VIN0 and VIN4 are sampled first followed by the pairs VIN1/VIN5, VIN2/VIN6 and VIN3/VIN7 with two cycles of the ADC clock between the sampling of one pair of analog signals and the next. After each pair of inputs are converted, the 14-bit digital numbers are written in 2's complement, left-aligned format to a dedicated 16-bit, register i.e. the ADC register $\mathrm{ADC0}$ stores the converted result for the signal on VIN0 etc. In addition, a dedicated bit is set in the ADCSTAT register. After the ADC
has finished with all of the channels, an interrupt may be generated. Alternatively, the ADCSTAT can be polled to detect successful conversion of a given pair of inputs. There are a number of ways in which the conversion process can be started, determined by bits $0-2$ in the ADCCTRL register. For the work described in this thesis, the conversion process was started by setting bit 1 of the SOFTCONVST register (a mode selected by setting bits $0-2$ of the ADCCTRL register).

## E2. Overview of the PWM Generation Unit

The PWM generation unit is a flexible, programmable, three-phase PWM waveform generator. The unit contains special functions that simplify the generation of the required PWM switching patterns for control of the electronically commutated motor (ECM). A special mode can also be implemented for the SRM. A block diagram of the main functions of the PWM Generation Unit is given in Figure E. 3 (Analog Devices 2003c).


Figure E.3: Block diagram of the main functional units of the PWM Generator unit.

The PWM generator produces six PWM output signals that consists of three high-side drive signals ( $\mathrm{AH}, \mathrm{BH}$ and CH ) and three low-side drive signals ( $\mathrm{AL}, \mathrm{BL}$ and CL ). The polarity of the PWM signals is determined by the PWMPOL input pin of the

PWMSTAT register, so that either active HI or active LO PWM patterns can be produced by tying the PWMPOL input pin high or low. The switching frequency and the dead time of the generated PWM patterns are programmable using the PWMTM and PWMDT registers. The PWMDT is internally forced to 0 by hardware when $\overline{\text { PWMSR }}$ is low to signify that the switched reluctance mode is active. The duty-cycles of the three pairs of PWM signals are directly controlled by the three duty-cycle control registers (PWMCHA, PWMCHB and PWMCHC). On the EZ-KIT Lite board shown in Figure E.1, access to the 6 PWM output signal pins on the ADSP-21992 chip is via connector P10 (Analog Devices 2003b).

The PWMSTAT register provides status information about the PWM system. In this project, the PWM polarity is always active HI PWM outputs (this requires placing jumper JP5, on the EASY-KIT Lite board, in position 2-3 to connect the PWMPOL pin to +3.3 V ), there is no external trip (this requires placing jumper JP5, on the EASY-KIT Lite board, in position 2-3 to connect the $\overline{\text { PWMTRIP }}$ pin to +3.3 V ) and SRM mode is activated (this requires placing jumper JP6, on the EASY-KIT Lite board, in position 12 to connect the PWMSR pin to GND). The status of which half cycle is active is provided by PWMPHASE bit ( $0=1^{\text {st }}$ half and $1=2^{\text {nd }}$ half). This register also contains the interrupt bits to indicate an interrupt has occurred (TRIPIRQ bit $=1$ when interrupt has occurred from and external trip and SYNCIRQ bit $=1$ when an internal interrupt has occurred due to the PWM synchronization signal). Only the synchronization interrupt was used in this project. The source code must write a 1 to clear the interrupt bit and this is usually done during an Interrupt Service Routine (ISR). An ISR is called to update the duty-cycle values when the PWM generator unit channel is active.

The PWMCTRL register is central to activating and defining operating mode characteristics of the PWM generator unit. It is configured to enable or disable PWM generation (if PWM_EN bit is 1 or 0 ), implement double or single update mode (if PWMDBL bit is 1 or 0 ), set the operation after trip (SYNC_EN PWMSYNC bit is set to 1 to continue interrupts and this requires that the external shutdown be disabled which requires that the $\overline{\text { PWMTRIP }}$ pin is connected to a logic HI), select internal or external synchronization signal (external if EXTSYNC bit is 1). As the external synchronization signal was used in this project, the SYNCSEL bit was ignored.

A number of additional registers must be configured or status read in order to implement the PWM generator unit, including, the PWMSEG register, the PWMGATE register and the PWMLSI register. Each of the six PWM output signals can be enabled or disabled by separate output enable bits of the PWMSEG register. An additional 3 control bits on the PWMSEG register permits independent crossover of the two signals of a PWM pair but this feature was not used in this project. The PWMGATE register controls a high-frequency chopping signal that is mixed with the PWM signals to drive pulse gate-drive transformers. This feature was not used in this project. When the SRM mode is activate, the PWMLSI register is used to create the four SRM chopping modes: hard chop, alternate chop, soft chop-bottom on and soft chop-top on. The low side invert that is configured by the PWMLSI bits ( $1=$ invert ) is the only difference between hard chop mode and alternate chop mode. Soft chop-bottom on uses a $100 \%$ duty-cycle on the low side of the channel, while with the soft chop-top on it is the high side of the channel that utilizes a $100 \%$ duty-cycle. Alternate chop mode was used in this project.

The PWM switching frequency is controlled by the 16-bit PWM period register, PWMTM. The required code for the PWMTM register is determined using equation E. 1 (Analog Devices 2003c).

$$
\begin{equation*}
\mathrm{PWMTM}=\frac{\mathrm{f}_{\mathrm{CK}}}{2 \times \mathrm{f}_{\mathrm{PWM}}} \tag{E.1}
\end{equation*}
$$

The value of $\mathrm{f}_{\mathrm{CK}}$ is the same as that for the peripheral clock, HCLK, which was 64 MHz in this project and $\mathrm{f}_{\mathrm{PWM}}$ is the desired PWM switching frequency. Therefore, in this project the PWM switching frequency was 25 kHz and this yielded a PWMTM register code of 1280 . The hexadecimal value ( $0 x 0500$ ) was written to the PWMTM register.

Switched reluctance mode was selected in this project and this requires that both the high-side and low-side duty-cycle values had to be set. The high-side duty-cycle values are controlled by the six 16-bit duty-cycle registers. PWMCHA, PWMCHB and PWMCHC registers control the high-side duty-cycles, while PWMCHAL, PWMCHBL and PWMCHCL registers control the low-side duty-cycles. The high-side duty-cycles are determined using formula E. 2 (Analog Devices 2003c).

$$
\begin{equation*}
\text { PWMCHx }=\left(\left(d_{\mathrm{AH}}-0.5\right) \times \text { PWMTM }\right)+\text { PWMDT } \tag{E.2}
\end{equation*}
$$

The generic duty-cycle code PWMCHx is replaced by one of the three high-side dutycycle codes, PWMCHA, PWMCHB or PWMCHC. The PWM switching frequency code was 1280 and the desired duty-cycle value ( $\mathrm{d}_{\mathrm{AH}}$ ) ranged from $0-1$, while the dead time code (PWMDT) was 0 in this application as the switched reluctance mode was active. Therefore, a duty-cycle of $10 \%$ yielded a PWMCHx code of -512 , and the corresponding hexadecimal value ( $0 x F E 00$ ) was written to the register. The low-side duty-cycles are determined using formula E. 3 (Analog Devices 2003c).

$$
\begin{equation*}
\text { PWMCHxL }=\left(\left(0.5-d_{A H}\right) \times \text { PWMTM }\right)-\text { PWMDT } \tag{E.3}
\end{equation*}
$$

The generic duty-cycle code PWMCHxL is replaced by one of the three low-side dutycycle codes, PWMCHAL, PWMCHBL or PWMCHCL; otherwise the equation components are the same as equation E.2. Therefore, a duty-cycle of $90 \%$ yields a PWMCHxL code of -512 , which corresponding hexadecimal value ( $0 x \mathrm{FE} 00$ ) is written to the register. To save time during code execution the code for high-side channel was assigned to the low-side channel as both values were the same as can be seen in the examples. In this project, the alternate chop mode was selected and when in this configuration all the low-side channels were inverted. So when the high-side channel was on for a particular duty cycle, the corresponding low-side channel was off for the same duty-cycle.

## E3. Overview of the Auxiliary PWM Generation unit

The ADSP-21992 contains a two-channel, 16-bit, auxiliary PWM output unit that can be programmed with variable duty-cycle, variable frequency and may operate in either an independent or offset operating mode. On the EZ-KIT Lite board shown in Figure E.1, access to the 2 auxiliary PWM output signal pins on the ADSP-21992 chip is via connector P10 (Analog Devices 2003b). The switching signals can be externally shutdown using the input pin, $\overline{\text { AUXTRIP }}$. In this project, there was no external trip (this requires placing jumper JP8, on the EASY-KIT Lite board, in position 2-3 to connect the $\overline{\text { AUXTRIP }}$ pin to +3.3 V ) (Analog Devices 2003b).

The auxiliary PWM generator unit can operate in either independent or offset modes. Only offset mode was used in this project, so it is the only mode that is discussed here. In this mode, there is an offset time between the rising edge of channel one (AUX0) and channel two (AUX1) and this implements alternate chop mode for switched reluctance
mode operation. The switching frequency for the two channels is controlled by the AUXTM0 register, the duty-cycles for channel one and two are controlled by the AUXCH0 and AUXCH1 registers, respectively, and the offset time is controlled by the AUXTM1 register.

The auxiliary PWM control register (AUXCTRL) enables the auxiliary PWM output (AUX-EN bit, $1=$ enable), defines operating mode (AUX_PH bit, $1=$ independent, $0=$ offset) and enables the synchronization signal (AS_EN bit, $1=$ enable) to allow for interrupt operation. The auxiliary PWM status register (AUXSTAT) provides the interrupt or raw status. The raw status bit (AUXTRIP, $1=\mathrm{HI}, 0=\mathrm{LO}$, active trip) defines if an external trip has occurred. The synchronisation interrupt bit (AS_IRQ, $1=$ occurred) provides notification that an interrupt has occurred on the synchronisation signal while the trip interrupt bit (AT_IRQ, $1=$ occurred) signals that an interrupt has occurred due to and external trip. A 1 must be written to these interrupt bits to clear them. A synchronisation interrupt was only used in this project. An ISR is called to update the duty-cycle values when the auxiliary PWM generator unit is active. The offset time also has to be updated during his routine.

The auxiliary PWM switching frequency for both channels is controlled by the 16-bit auxiliary PWM period register, AUXTM0, in offset mode. The required AUXTM0 register code is determined using equation E. 4 (Analog Devices 2003c).

$$
\begin{equation*}
\text { AUXTM0 }=\frac{\mathrm{T}_{\mathrm{AUX} 0}}{\mathrm{t}_{\mathrm{CK}}} \tag{E.4}
\end{equation*}
$$

The value of $\mathrm{t}_{\mathrm{CK}}$ is the fundamental timing unit of the auxiliary PWM unit is the switching period of the peripheral clock, HCLK, and had a frequency 64 MHz in this project. This yields a fundamental time increment of $\mathrm{t}_{\mathrm{CK}}$ of 15.625 nS . The auxiliary PWM switching period, $\mathrm{T}_{\text {Auxo }}$, for a switching frequency of 25 kHz is $40 \mu \mathrm{~s}$ and this yields an AUXTM0 register code of 2559 . The hexadecimal value ( $0 x 09 \mathrm{FF}$ ) must be written to the AUXTM0 register.

In offset mode, the AUXTM1 register defines the offset time from the rising edge of the signal for the AUX0 output to that of AUX1 output. The required AUXTM1 register code is determined using equation E. 5 (Analog Devices 2003c).

$$
\begin{equation*}
\operatorname{AUXTM} 1=\frac{\mathrm{T}_{\mathrm{OFFSET}}}{\mathrm{t}_{\mathrm{cK}}}-1 \tag{E.5}
\end{equation*}
$$

The offset time, $\mathrm{T}_{\text {OffSET }}$, is equivalent to the on-time for the AUX0 channel, which in turn depends on the duty-cycle of the channel. Therefore, the offset is equal to the dutycycle multiplied by the auxiliary PWM switching period ( $40 \mu \mathrm{~s}$ ). For a $10 \%$ duty-cycle for the AUXO channel, this yields an AUXTM1 register code of 255. The hexadecimal value ( 0 x 00 FF ) must be written to the AUXTM1 register. The code is updated at the beginning of the next AUX0 switching period.

The duty-cycle or on-time for the AUX0 channel is controlled by the AUXCH0 register and is updated at the beginning of the next AUX0 switching period. The required AUXCH0 register code is determined using equation E. 6 (Analog Devices 2003c).

$$
\begin{equation*}
\mathrm{AUXCH} 0=\frac{\mathrm{d}_{\mathrm{AUX} 0} \times \mathrm{T}_{\mathrm{SW}}}{\mathrm{t}_{\mathrm{CK}}} \tag{E.6}
\end{equation*}
$$

For a $10 \%$ duty-cycle, $\mathrm{d}_{\mathrm{AUX} 0}$, for the AUXO channel and an auxiliary PWM switching period, $\mathrm{T}_{\mathrm{sw}}$, of $40 \mu \mathrm{~s}$, yields an AUXCH0 register code of 256 . The hexadecimal value ( $0 x 0100$ ) must be written to the register. The duty-cycle or on-time for the AUX1 channel is controlled by the AUXCH1 register and is updated at the beginning of the next AUX1 switching period. The formula to determine the register code is the same as equation E6. The duty-cycle for AUX1 is determined using equation E7 (Analog Devices 2003c).

$$
\begin{equation*}
\mathrm{d}_{\mathrm{AUX} 1}=1-\mathrm{d}_{\mathrm{AUX} 0} \tag{E.7}
\end{equation*}
$$

## E4. Overview of the Program Sequencer and the Peripheral Interrupt Controller

In order to understand how to implement interrupt service routines with the ADSP21992 DSP, a fundamental understanding of the program sequencer and the peripheral interrupt controller is required. The program sequencer of the ADSP-21992 controls program flow where it is constantly providing the address of the next instruction to be executed by other parts of the DSP. Program flow in the DSP is mostly linear yielding sequential executing of program instructions. There are non-sequential program
structures that direct the DSP to execute an instruction that is not at the next sequential address and these structures include: loops, subroutines, jumps, interrupts and idle. The program flow variations for the DSP are illustrated in Figure E. 4 (Analog Devices 2003c).


Figure E.4: Program Flow Variations for the DSP

The sequencer manages the execution of these program structures by selecting the address of the next instruction to execute. As part of this process, the sequencer handles the following tasks: Increment the fetch address, maintains stacks, evaluates conditions, decrements the loop counter, calculates new addresses, maintains an instruction cache and handles interrupts. To accomplish these tasks, the sequencer uses the blocks shown in Figure E.5. The sequencer's address multiplexer selects the value of the next fetch address from several possible sources. This address enters the instruction pipeline and ends with the program counter (PC). The pipeline contains the 24 -bit addresses of the instructions currently being fetched, decoded, and executed. The PC couples with the PC stack, which stores the return addresses.


Figure E.5: Program Sequencer Block Diagram

To manage events, the sequencer's interrupt controller handles interrupt processing, determines whether an interrupt is masked, and generates the appropriate interrupt vector address. A set of system control registers configures or provides input to the sequencer. These registers include ASTST, MSTAT, CCODE, IMASK, IRPTL and ICNTL.

Interrupts can stem from a variety of conditions, both external and external to the processor. In response to an interrupt, the sequencer processes a subroutine call to a predefined address, the interrupt vector. The DSP assigns a unique vector to each interrupt. The DSP core supports five fixed interrupt sources (Emulator, Reset, Powerdown, Loop and PC Stack and Emulation kernel Interrupts) and up to 12 user assignable interrupts. The user assignable interrupts are generated by the peripheral units of the ADSP-21992 and their connection and prioritization is managed by the Peripheral Interrupt Control Unit.

The masking of the various interrupts is controlled by the IMASK processor register and the latching of the pending interrupts is controlled by the IRPTL processor register. There are dedicated bits of these registers that are associated with the various fixed and user assignable interrupt sources. Each interrupt has a dedicated 32-bit address in the interrupt vector table. The dedicated bits and associated vector addresses for each of the ADSP-21992 five core and 12 user assignable interrupts are shown in Table E. 1 (Analog Devices 2003c).

| Interrupt Source | IRPTL/IMASK Bit | Vector Address |
| :---: | :---: | :---: |
| Emulator (non-maskable) highest priority | N/A | N/A |
| Reset (non-maskable) | 0 | 0x000000 |
| Powerdown (non-maskable) | 1 | 0x000020 |
| Loop and PC Stack | 2 | 0x000040 |
| Emulation Kernel | 3 | 0x000060 |
| USR0 - user assignable | 4 | 0x000080 |
| USR1 - user assignable | 5 | 0x0000A0 |
| USR2 - user assignable | 6 | 0x0000C0 |
| USR3 - user assignable | 7 | 0x0000E0 |
| USR4 - user assignable | 8 | 0x000100 |
| USR5 - user assignable | 9 | 0x000120 |
| USR6 - user assignable | 10 | 0x000140 |
| USR7 - user assignable | 11 | 0x000160 |
| USR8 - user assignable | 12 | 0x000180 |
| USR9 - user assignable | 13 | 0x0001A0 |
| USR10 - user assignable | 14 | 0x0001C0 |
| USR11 - user assignable lowest priority | 15 | 0x00 01E0 |

Table E.1: ADSP-21992 Interrupt Mask

| Peripheral <br> Interrupt <br> Identifier | IPR Register Bits | Interrupt Name | Interrupt Source and Description |
| :---: | :---: | :---: | :---: |
| 0 | IPR0[3:0] | SPORT0_RX_IRQ | SPORT Receive Interrupt |
| 1 | IPR0[7:4] | SPORT0_TX_IRQ | SPORT Transmit Interrupt |
| 2 | IPR0[11:8] | SPI_IRQ | SPI Receive/Transmit Interrupt |
| 3 | IPR0[15:12] |  | Reserved |
| 4 | IPR1 [3:0] |  | Reserved |
| 5 | IPR1[7:4] |  | Reserved |
| 6 | IPR1[11:8] |  | Reserved |
| 7 | IPR1[15:12] |  | Reserved |
| 8 | IPR2[3:0] | PWMSYNC_IRQ | PWM Synchronization Interrupt |
| 9 | IPR2[7:4] | PWMTRIP_IRQ | PWM Shutdown Interrupt |
| 10 | IPR2[11:8] |  | Reserved |
| 11 | IPR2[15:12] |  | Reserved |
| 12 | IPR3[3:0] | EIU0TMR_IRQ | EIU Loop Timer Interrupt |
| 13 | IPR3[7:4] | EIU0LATCH_IRQ | EIU Latch Interrupt |
| 14 | IPR3[11:8] | EIU0ERR_IRQ | EIU Error Interrupt |
| 15 | IPR3[15:12] | ADC0_IRQ | ADC End of Conversion Interrupt |
| 16 | IPR4[3:0] |  | Reserved |
| 17 | IPR4[7:4] |  | Reserved |
| 18 | IPR4[11:8] |  | Reserved |
| 19 | IPR4[15:12] |  | Reserved |
| 20 | IPR5[3:0] | TMR0_IRQ | General Purpose Timer 0 Interrupt |
| 21 | IPR5[7:4] | TMR1_IRQ | General Purpose Timer 1 Interrupt |
| 22 | IPR5[11:8] | TMR2_IRQ | General Purpose Timer 2 Interrupt |
| 23 | IPR5[15:12] | MEMDMA_IRQ | Memory DMA Interrupt |
| 24 | IPR6[3:0] | FIOA_IRQ | Flag IO Interrupt A |
| 25 | IPR6[7:4] | FIOB_IRQ | Flag IO Interrupt A |
| 26 | IPR6[11:8] | AUXSYNC_IRQ | Auxiliary PWM Synchronization Interrupt |
| 27 | IPR6[15:12] | AUXTRIP_IRQ | Auxiliary PWM Trip Interrupt |
| 28 | IPR7[3:0] |  | Reserved |
| 29 | IPR7[7:4] |  | Reserved |
| 30 | IPR7[11:8] |  | Reserved |
| 31 | IPR7[15:12] |  | Reserved |

Table E.2: Peripheral Interrupt Sources

The ADSP21992 has 32 individual peripheral interrupt sources that are tabulated and identified in Table E. 2 (Analog Devices 2003c). There is a unique 4-bit code that allows each peripheral interrupt source to be assigned to one of the 12 user-assignable interrupts of the DSP core. Four of the 4-bit codes are contained in each of the 8, 16-bit Interrupt Priority Registers (Interrupt Priority Register 0 (IPR0) to Interrupt Priority Register 7 (IRP7)).

The user may write a value between $0 x 0$ and $0 x B$ to each 4 -bit location in order to connect the particular interrupt source to the corresponding user assignable interrupt of the ADSP-21992 DSP. Writing a value of $0 x 0$ connects the peripheral interrupt to the USR0 user assignable interrupt of the DSP core, while writing a value of 0xB connects the peripheral interrupt to the USR11 user assignable interrupt. The core interrupt USR0 is the highest priority user interrupt, while USR11 is the lowest priority. Writing a value between 0 xC and 0 xF effectively disables the peripheral interrupt by not connecting it to any ADSP-21992 DSP interrupt input. The masking and interrupt flagging are controlled by the core registers IMASK and IRPTL. There are additional features and registers that are available if the user wishes to assign more than one peripheral interrupt to any given DSP interrupt but this scheme was not implemented in this project. Only two peripheral interrupts were assigned in this project, PWMSYNC_IRQ was assigned to USR0 and AUXSYNC_IRQ was assigned to USR1.

## E5. Overview of the Flag I/O peripheral unit

The Flag I/O (FIO) unit is a parallel I/O interface that supports 16 bi-directional general purpose I/O signals (PF0-PF15). Each flag bit can be individually configured as an input or output depending on the contents of the direction (DIR) register. They can also be used as a source for an interrupt (Analog Devices 2003c).

When a flag is configured as an input, the FIO can be programmed to invert the input value, latch a level or detect a signal edge (rising, falling or both) depending on the contents of the POLAR, EDGE and BOTH registers. When a flag is configured as an output, the output value is driven from the FLAG register. The 16-bit FLAG register exhibits 'sticky' behaviour; only writing a ' 1 ' to a bit can modify that bit. Writing a ' 1 ' to a bit of the FLAG register at the even address 0x0002 (FLAGC) clears the FLAG bit while writing a ' 1 ' to a bit of the FLAG register at the odd address 0x0003 (FLAGS) sets the FLAG bit. Writing a ' 0 ' to any bit in either FLAGC or FLAGS has no effect. On the EZ-KIT Lite board shown in Figure E.1, access to the 16 FIO programmable flag pins on the ADSP-21992 chip is via connector P8.

# Appendix F - VisualDSP++ 3.0 and implementing the ISR 

VisualDSP++ 3.0 has a number of built in or intrinsic functions designed to make programming a DSP in a C environment even more user-friendly. These intrinsic functions require the inclusion of a number of header files in order to access these functions and to define symbolic names for the registers of the ADSP-21992 DSP. The specific registers and functions that were accessed in this project include Flag I/O, ADC, PWM, auxiliary PWM and the various functions required to implement an interrupt service routine (ISR) to update the PWM and the auxiliary PWM duty cycles.

## F. 1 Overview of VisualDSP++ 3.0 Features

The built-in functions eliminates the need for referencing-dereferencing scheme using cast pointers $(*($ int $*))$ to access memory-mapped registers. Access to all non-memorymapped registers in C required embedded assembly source code. The intrinsic functions to access non-memory-mapped system register are sysreg_read and sysreg_write and the functions to access all the memory-mapped I/O space registers are io_space_read and io_space_write (Analog Devices 2003d). These four functions and other bit manipulation instructions are defined in the header file sysreg.h. There is also an enumerated type in this header file that provides listing of the system registers that can be accessed using sysreg_read and sysreg_write.

The io_space_read and io_space_write intrinsic functions require the inclusion of the architecture definition header files, adsp-21992.h, adsp-2199x.h, def2191.h, def219x.h when using the ADSP-21992 DSP. The definition header file, adsp-21992.h, allows access the symbolic names that are unique to the ADSP-21992, specifically the CAN system registers. The common header file, adsp-2199x.h, is required to access the registers that are common to all the ADSP-2199x DSP family, which includes I/O registers, interrupt controller registers, PWM registers, encoder interface unit register, auxiliary PWM registers, watchdog timer registers, ADC module registers. The definition file, def2191.h, is also required when using the ADSP-21992 DSP as it contains additional symbolic names including: the DMA Bus Bridge, External Access Bridge, JTAG debut, clock and system control, interrupt controller, SPORT, SPI and UART communications controllers and the timer. The definition file, def219x.h, defines
the symbolic names for all the system register bit and addresses that are common to all ASDP-219x DSP cores. The Flag I/O block defined in the header file, adsp-2199x.h, supersedes the definitions already called out in the header file, def2191.h. The definitions for the interrupt controller provided in the header file, adsp-2199x.h, results in those in header definition file, $\operatorname{def} 2191 . h$, been undefined.

## F. 2 Implementation of the intrinsic functions

An example of using the built-in functions is configuring the Flag I/O (FIO) Peripheral unit to set the general purpose I/O signal pins 0-3 (PF0-3) to be outputs (Analog Devices 2003d). This information is contained in the DIR register, where a 1 means that the particular pin is an output. The first step is to access the correct IO page for the DIR register. The sysreg_write intrinsic function is used to access the IOPG system register. The first argument is the register to be written to, sysreg_IOPG (as defined in the enumeration in sysreg.h). The second argument is the value to be written to the IOPG register, FIO_Page, which is \#defined in adsp-2199x.h to be 0x06 (the page offset required to access the FIO register set).

Once the IOPG register is set appropriately to access the FIO registers, the DIR register is accessible. The DIR register is an IO space register and is written to using the io_space_write intrinsic function. Here, the arguments are the address to be written to, FIO_DIR, which is \#defined in adsp-2199x.h to be 0x000 (the physical I/O address on IO page 6 of the DIR register) and the value to be written to that address, 0x000F, where bits $0-3$ are set to 1 to enable the corresponding PF pins $0-3$ to be outputs. The source code to implement these instructions is shown in Figure F.1. Access to the ADC, PWM, and auxiliary PWM is done in the same manner, as illustrated in the code examples shown in Figure F. 2 - F.4, respectively.

```
#include <sysreg.h>
#include <adsp-2199x.h>
main( )
{
    sysreg_write (sysreg_IOPG, FIO_Page); //Go to FlO page
    io_space_write (FIO_DIR, 0x000F); //Set DIR register for PF0-3 as outputs
}
```

Figure F.1: Configuring the Flag I/O pins 03 (PF0-3) of the FIO Peripheral Unit as outputs.

```
#include <sysreg.h>
#include <adsp-2199x.h>
main( )
{
    sysreg_write(sysreg_IOPG,ADC_Page); //Go to ADC page
    io_space_write(ADC_CTRL, 0x0FOF); //max clock, sim.samp.mode
                            //and pwmsync convert trigger (000),
                                    / /SOFTCONVST (111)
```

\}

Figure F.2: Go to ADC page, set ADC clock to maximum, implement simultaneous sampling mode, and trigger when SOFTONVST bit is active

```
#include <sysreg.h>
#include <adsp-2199x.h>
main( )
{
    sysreg_write(sysreg_IOPG, PWM0_Page);
    io_space_write(PWM0_SEG, 0x03F);
    io_space_write(PWM0_CTRL, 0x000);
    io_space_write(PWM0_TM, 0x0500); //25kHz PWM Switching Frequency
    io_space_write(PWMO_CHA, 512); //Set PWM AH Duty Cycle to 90%
    io_space_write(PWMO_CHAL, 512); // Set PWM AL Duty Cycle to 10%
    io_space_write(PWM_SI, 0x0); //No invertion of low side outputs,
                                    //SR Alternate mode
                                    //Set pwm sync signal width for 500ns
}
```

Figure F.3: Go to PWM page, disable the PWM output and generation, set the switching frequency to 25 kHz , set the duty cycle for the high-side channel to $90 \%$ and the duty-cycle of the low-side channel to $10 \%$, invert the low-side output due to switched reluctance mode and enable the PWM synchronization signal with the pulse width to 500 ns

```
#include <sysreg.h>
#include <adsp-2199x.h>
main( )
{
    sysreg_write(sysreg_IOPG, Aux_PWM_Page); //Go to AUX PWM page
    io_space_write(AUX_TMA0, 2559); //25kHz PWM Switching Frequency
    io_space_write(AUX_CHAO, 256); //10% initial high-side duty-cycle
    io_space_write(AUX_CHA1, 2304); //90% initial low-side duty-cycle
    io_space_write(AUX_TMA1, 255); //Offset for low-side duty cycle
    io_space_write(AUX_CTRL, 0x000); //Disable outputs and interrupt
}
```

Figure F.4: Go to auxiliary PWM page, set the switching frequency to 25 kHz , set the duty-cycle for the high-side channel to $90 \%$ and the duty-cycle of the low-side channel to $10 \%$, set the off-set for the low-side output, disable outputs and disable interrupts

## F. 3 Implementation of the Interrupt Service routine in C

The interrupt handling in C utilizes the header-defined interrupt(signal, subroutine) module to take care of everything [(Analog Devices 2002) and (Analog Devices 2003d)]. This function associates a specific ISR module to be run for a given signal that could be received during run-time. The list of possible signals (SIG_INT value) is detailed in the signal.h header file. The interrupt handling function also sets the correct bit in IMASK to enable servicing for that interrupt. In this project, the option to prioritize the interrupts was utilized.

When using the ADSP-21992, the peripheral interrupt sources, PWMSYNC_IRQ and AUXSYNC_IRQ, must be assigned to the user assignable core interrupts. The PWM interrupt was assigned to the highest user assignable core interrupt, USR0, and the auxiliary PWM interrupt was assigned to the second highest user assignable core interrupt, USR1 (Analog Devices 2003c). The highest user assignable core interrupt, USR0, has the signal number SIG_INT4 and the second highest user assignable interrupt, USR1, has the signal number SIG_INT5 (Analog Devices 2002).
$P W M_{-} I S R()$ and $A U X P W M_{-} I S R()$ are the ISR functions that is called to service the user assignable interrupts, USR0 and USR1, respectively. The ISR function is called to service the interrupt once the correct bit is latched in the interrupt latch (IRPTL) register. This bit must be cleared when the ISR is called. In addition to this interruptregistering scheme, all interrupts must be cleared or reset at the initial source code execution, the user must globally enable interrupts by using the intrinsic function enable_interrupt() that is defined in the sysreg.h header file. The source code instructions to clear or reset the interrupts at the initial source code execution, assign the user interrupts to the DSP core, assign the appropriate ISR to in corresponding signal number and finally to globally enable all interrupts are implemented in an initialization function in the project source code. The source code to implement these initialization steps is shown in Figure F.5.

```
#include <sysreg.h>
#include <adsp-2199x.h>
main( )
{
    //----------------------------Reset Interrupts--------------------------------------------
    //Clear/Reset All Interrupts
    sysreg_write(sysreg_IRPTL, 0x000);
    sysreg_write(sysreg_ICNTL, 0x000);
    sysreg_write(sysreg_IMASK, 0x000);
    // Assign Peripheral interrupt to the core interrupt
    sysreg_write(sysreg_IOPG, IntCtrl_Page); //Go to Peripheral Interrrupt
        //Control page
    io_space_write(IPR2, 0xF0); //Assign PWMSYNC_IRQ to highest user
                                //assignable core interrupt priority
        //(USRO)
    io_space_write(IPR6, 0xF1FF); //Assign AUXSYNC_IRQ to second highest
                                    //user assignable core interrupt priority
                                    //(USR1)
    interrupt(SIG_INT4, PWM_ISR); //INT4 is for interrupt USRO
    interrupt(SIG_INT5, AUXPWM_ISR); //INT5 is for interrupt USR1
    //---------------------------Enable Interrupts-------------------------------------------
    enable_interrupts(); //Globally Enable Interrupt
}
```

Figure F.5: The source code to initialize the ISR functions.

The ISR functions, PWM_ISR() and AUXPWM_ISR(), have a common requirement to clear the interrupt latch bit associated to that ISR. In the case of the PWM, this latch bit is the SYNCIRQ bit of the PWM status (PWMSTAT) register and for the auxiliary PWM the latch bit is the AS_IRQ bit of the auxiliary PWM control (AUXCTRL) register. Once the interrupt latch bit is cleared, the specific source code instruction for that particular ISR can be implemented. An example of the source code to clear this interrupt bit is shown in Figure F. 6

```
//-----------------------------------PWM ISR-----------------------------------------------
#pragma interrupt
void PWM_ISR()
{
    sysreg_write(sysreg_IOPG, PWMO_Page); // Go to PWM i/o page
    PWM_CycleA = io_space_read(PWMO_STAT); // Read the PWM Status Register
    io_space_write(PWMO_STAT, Ox20A); // Clear PWM Interupt Latch bit
```

Figure F.6: The source code for the ISR function to clear the interrupt latch bit.

## Appendix G - DSP Implemented Source Code

## G. 1 srm_pipwm_current_reg.c

```
// File: srm_pipwm_current_reg.c
// Date: 29/06/2008
// Author: Anthony Murphy
// Purpose: This is the source file to implement the PWM and AUXPWM Generator Unit and
// read the ADC system on the ADSP-2199x
// Ref: ADSP-2199x Mixed Signal DSP Controller Hardware Reference,
// P/N:82-000640-01 Rev. 0, 2003
// Detail: This file used to initialise the PWM Generator Unit, then in the ISR
// implements adc reading and calculate and update the pwm duty cycles and
// implement reading a switch to determine if mag/free mode or demag mode. The
// pwm controller was finally implemented in its own function,
// motor_control_a() for phase A.
/ /------------------------------------------------------------------------------------------------
//---------------------------------------------------------------------------------------------------
//Include files
//--------------------------------------------------------------------------------------------------------------
#include <signal.h>
#include <math.h>
#include<sysreg.h>
#include<adsp-21992.h>
//-
//Symbolic constants
//-
#define P 0.015 // Value of proportional gain
#define I 0.1 // Value of integral gain
//
//Function prototypes
//-------------------------
void PWM_ISR(); // PWM ISR Prototype
void AUXPWM_ISR(); // AUXPWM ISR Prototype
void motor_control_a(); // SRM Phase A current control prototype
void commutation_four_phase(); // SRM commutation of all four phases prototype
void read_rotor_angle(); // Read rotor angle
//
//Global data variables
//--
int i=0,j=0,count,loop=10;
int DutyCyleUpdateA=0, DutyCyleUpdateB=0, DutyCyleUpdateC=0, DutyCyleUpdateD=0;
int EnablePhaseA=0, EnablePhaseB=0, EnablePhaseC=0, EnablePhaseD=0;
int EnableSRM=0, MagFreeDemagA=0, MagFreeDemagB=0, MagFreeDemagC=0, MagFreeDemagD=0;
int DemagPWMA=0, DemagPWMB=0, DemagPWMC=0, DemagPWMD=0, PWM_CycleA=0;
int StartupA=1, StartupB=1, StartupC=1, StartupD=1;
int ADCStatusA, ADCValueA, DutyCycleTempA, DutyCycleAL, DutyCycleAH;
int ADCStatusB, ADCValueB, DutyCycleTempB, DutyCycleBL, DutyCycleBH;
int ADCStatusC, ADCValueC, DutyCycleTempC, DutyCycleCL, DutyCycleCH;
int ADCStatusD, ADCValueD, DutyCycleTempD, DutyCycleAUX0, DutyCycleAUX1, AUXPWMOffset;
int AngleMinA=10, AngleMaxA=80, AngleMinB=200, AngleMaxB=220, AngleMinC=230,
AngleMaxC=240;
int AngleMinD=250, AngleMaxD=260, AngleDemagA=0, AngleDemagB=0, AngleDemagC=0,
AngleDemagD=0;
int AngleDemag=20, AngleOffA=0, AngleOnA=0, RotorAngle=0;
int MagFreePeriodPWM = 1280; //25kHz = 1280, 50kHz = 640, 100kHz = 320;
int DemagPeriodPWM = 320; //200kHz= 160, 500kHz = 64, 1Mhz = 32;
float Ith=0, Ia=0, Ib=0, Ic=0, Id=0, Iref = 0;
float error=0, errorlow = 0, errorhigh =0, Da=0, integral=0, deltaT=0.00004;
float I_a[4096], Ilow = 0, Ihigh = 0;
float tempA=0, tempB=0, tempC=0, tempD=0;
```



```
//Main Program
//----------
main()
{
    initialization ();
    Iref = 90.00;
    Ith = 5.00;
    Ihigh = Iref*1.1
    Ilow = Iref*0.9;
    errorhigh = Iref-Ilow;
    errorlow = Iref-Ihigh;
        while(1) // wait for interrupts
        commutation_four_phase();
    //Activate SRM commutation
}
```

```
//Function: initialization()
//Description: To initial the DSP clock speed, interrupts, PWM, auxiliary PWM, FIO and
ADC
//Inputs:
//Returns:
-
//
void initialization (void)
{
    //Increase the dsp clock speed from 32MHz to 128Mhz
    //Bypass mode enable and PLL shutoff
    asm("iopg = 0x00;");
    asm("ax1 = 0x0120;");
    asm("io(0x200) = ax1;");
    asm("nop;");
    //Bypass mode enable and write the correct multiplier value
    asm("iopg = 0x00;");
    asm("ax1 = 0x0950;");
    asm("io(0x200) = ax1;");
    asm("nop;");
    //Bypass mode disable and maintain the same mulitplier value as before
    asm("iopg = 0x00;");
    asm("ax1 = 0x0850;");
    asm("io(0x200) = ax1;");
    asm("nop;");
    //----------------------------Reset Interrupts---------------------------------------
    //Clear/Reset All Interrupts
    sysreg_write(sysreg_IRPTL, 0x000);
    sysreg_write(sysreg_ICNTL, 0x000);
    sysreg_write(sysreg_IMASK, 0x000);
    //-----------------------Initialize Interrupts--------------------------------------
    // Assign Peripheral interrupt to the core interrupt
    sysreg_write(sysreg_IOPG, IntCtrl_Page); //Go to Peripheral Interrrupt
                                    //Control page
    io_space_write(IPR2, 0xFO); //Assign PWMSYNC_IRQ to highest user
                                //assignable core interrupt priority
                                //(USR0)
    io_space_write(IPR6, 0xF1FF); //Assign AUXSYNC_IRQ to second highest
        //user assignable core interrupt priority
        //(USR1)
    interrupt(SIG_INT4, PWM_ISR); //INT4 is for interrupt USR0
    //interrupt(SIG_INT5, AUXPWM_ISR); //INT5 is for interrupt USR1
    //--------------------------Enable Interrupts----------------------------------------
    //Globally Enable Interrupt
    enable_interrupts();
    //--------------------------Intitialize PWM-------------------------------------------
    sysreg_write(sysreg_IOPG, PWMO_Page); // Go to PWM i/o page
    io_space_write(PWMO_SEG, 0x03F); //Disable all pwm outputs 0x03F
    io_space_write(PWM0_CTRL, 0x000); //Disable PWM generation
    io_space_write(PWM_SI, 0x0); //No invertion of low side outputs,
    //SR Alternate mode
    io_space_write(PWMO_SYNCWT, 31); //Set pwm sync signal width for 500ns
    //--------------------------Intitialize AUX PWM--------------------------------------
    // Go to AUX PWM i/o page
    sysreg_write(sysreg_IOPG, Aux_PWM_Page);
    io_space_write(AUX_CTRL, 0x000); //Disable outputs and interrupt
    //--------------------------Intitialize FIO------------------------------------------------
    sysreg_write(sysreg_IOPG,FIO_Page);
    io_space_write(FIO_DIR, 0xFFFC); // set outputs except PFO and PF1
    io_space_write(FIO_EDGE, 0x0000); // PFO and PF1 are level sensitive
        io_space_write(FIO_POLAR, 0x0000); // PFO and PF1 are active high input
    //-------------------------Intitialize ADC
    sysreg_write(sysreg_IOPG,ADC_Page); //Intitialize ADC
    io_space_write(ADC_CTRL, 0x0F07); //max clock, sim.samp.mode
    //and pwmsync convert trigger (000),
    //SOFTCONVST(111)
}
```

```
//----------------------
//Description: The pwm interrupt service routine
//Inputs: -
//Returns:
-
```

```
#pragma interrupt
void PWM_ISR()
{
    sysreg_write(sysreg_IOPG, PWMO_Page); // Go to PWM i/o page
    PWM_CycleA = io_space_read(PWMO_STAT); // Read the PWM Status Register
    io_space_write(PWMO_STAT, 0x20A);
    PWM_CycleA = PWM_CycleA & 0x0001;
    if(PWM_CycleA==1)
        {
        sysreg_write(sysreg_IOPG, FIO_Page); // Go to FIO page
        io_space_write(FIO_FLAGS, 0x0020); // Activate (PF5)
        io_space_write(FIO_FLAGC, 0x0010); // Disable (PF4) =>2 for 2nd half cycle
        }
        else // If in the lst half cycle, no update of pwm
            {
            sysreg_write(sysreg_IOPG, FIO_Page); // Go to FIO page
            io_space_write(FIO_FLAGS, 0x0010); //Activate (PF4)
            io_space_write(FIO_FLAGC, 0x0020); //Disable (PF5) =>1 for 1st half cycle
                }
                if((DutyCyleUpdateA==1)&&(PWM_CycleA==1))
                    {
                //--------------------------------ADC Start
                sysreg_write(sysreg_IOPG,ADC_Page);
                    io_space_write(ADC_SOFTCONVST, 0x1); // Set the soft convert start bit
                    ADCStatusA = 1;
                    while(!(ADCStatusA & 0x0001)) //Wait till conversion of ADC4
                    ADCStatusA = io_space_read(ADC_STAT);
                            //is complete
                    ADCValueA = io_space_read(ADC_DATA4); //Read value from ADC4
                    ADCValueA=ADCValueA>>2;
                            //ADC value is leftmost }14\mathrm{ bits =>
                            //shift right 2 bits
                    tempA=(float)ADCValueA; //Cast convert to a float for
                    Ia=(tempA/0x1FFF)*90.09;
                tempB=ceilf(Ia*10);
                Ia=(tempB/10) +1.6;
    // Clear PWM Interupt Latch bit
    // If in the 2nd half cycle, update pwm
            //Acolvate (DF4)
            ion_(,
                            //calculations
                            //Determine current measurement
                            //value, divide by }8191\mathrm{ or 0x1FFF
                            //and scale 90 if 11.1ohms
                            //Current value rounded off for
                    //to one decimal place
```

                if(j<4097)
                    if
                I_a[j]=Ia; //Capture initial current data for plotting
                    if (j==4096)
                        \(j=-1\);
                        j=-1;
    $j++; ~$
\}

sysreg_write(sysreg_IOPG, PWMO_Page); // Go to PWM i/o page
io_space_write(PWMO_CHA, DutyCycleAH); //Update duty cycle for high side
io_space_write(PWMO_CHAL, DutyCycleAL); //Update duty cycle for low side
StartupA=0;
\}

```
                    else
                    {
                    if(Ia>Ihigh) //Current too high=>Freewheel
                    {
                    DutyCycleAH = (int)((0-.5)*1280); //Calculate high side duty cycle
                    DutyCycleAL = DutyCycleAH; //Due to SR mode and alt mode low and
                                    //hide side dutycycle are the same.
                    sysreg_write(sysreg_IOPG, PWM0_Page); //Go to PWM i/o page
                    io_space_write(PWMO_CHA, DutyCycleAH); //0% duty cycle for high side
                    io_space_write(PWMO_CHAL, DutyCycleAL); //100% duty cycle for low side
                    StartupA=1;
                    }
                    else
                                    //Implement Startup PWM duty cycle update
                    {
                    DutyCycleAH = (int)((0.025-.5)*1280);//Calculate high side duty cycle
                    DutyCycleAL = DutyCycleAH; //Due to SR mode and alt mode low and
                            //hide side dutycycle are the same.
                    sysreg_write(sysreg_IOPG, PWMO_Page); //Go to PWM i/o page
                    io_space_write(PWMO_CHA, DutyCycleAH); //1% duty cycle for high side
                    io_space_write(PWMO_CHAL, DutyCycleAL);//99% duty cycle for low side
                    }
    }
    }
    else
    {
    if(MagFreeDemagA==0) //Demag mode of operation
        {
        if(Ia>Ith)
            {
            Da = 0;
            DutyCycleAH = (int)((Da-.5)*320); //Calculate high side duty cycle
            DutyCycleAL = (int)((.5-Da)*320);
                //Calculate low side duty cycle
            sysreg_write(sysreg_IOPG, PWMO_Page);
                //Go to PWM i/o page
            io_space_write(PWMO_CHA, DutyCycleAH); //0% duty cycle for high side
            io_space_write(PWMO_CHAL, DutyCycleAL); //100% duty cycle for low side
            DemagPWMA=1;
            }
            else
                    {
                    Da = 0;
                    DutyCycleAH = (int)((Da-.5)*320); //Calculate high side duty cycle
                    Da = 1;
                    DutyCycleAL = (int)((.5-Da)*320); //Calculate low side duty cycle
                    sysreg_write(sysreg_IOPG, PWMO_Page); //Go to PWM i/o page
                    io_space_write(PWMO_CHA, DutyCycleAH); //0% duty cycle for high side
                    io_space_write(PWM0_CHAL, DutyCycleAL); //0% duty cycle for low side
                    DemagPWMA=0;
                    }
            }
    }
    DutyCyleUpdateA=0;
}
```

```
//Function: motor_control_a()
//Description: Implements the converter modes of operation magnetisation/freewheeling,
// demagnetisation depending on control signals
//Inputs:
//Returns:
//--------------------
{
    if ((MagFreeDemagA==1)&&(EnablePhaseA==1))//Mag/Free mode of operation - Commutation
        if(DutyCyleUpdateA==0) //Implement Mag/Free mode PWM - ISR
            {
                //--------------------------------- PWM Start -----------------------------------------
                sysreg_write(sysreg_IOPG, FIO_Page);// Go to FIO page
                io_space_write(FIO_FLAGC, 0x0100); //Disable MD2 (PF8)
                io_space_write(FIO_FLAGS, 0x0200); //Activate MQ2 (PF9)
                // Go to PWM i/o page
                sysreg_write(sysreg_IOPG, PWM0_Page);
                io_space_write(PWM0_TM, 0x0500); //25kHz PWM Switching Frequency
                io_space_write(PWM0_SEG, 0x00F); //Activate AH and AL)
                                    //Enable Phase A PWM outputs, 0 = enable,
                                    //1 = disable. Disable all pwm outputs 0x03F,
                                    //enable all pwm outputs 0x0, only enable
                                    //phase A 0x00F, only enable phase B 0x033,
            io_space_write(PWM_SI, 0x1); //Inverts low side outputs, SR Alternate
                                    //mode, disables when phase is off
                                    //Invert all=0x7, invert none = 0x0, invert
                                    //A=0x1, invert B=0x2 and invert C=0x4
                                    //Enable PWM generation with PWMSYNC signal.
                                    //double update (0x007), single update (0x003
            DutyCyleUpdateA = 1;
            }
            else;
            //Do nothing, update duty cycle next time
}
else
    {
    if ((MagFreeDemagA==0)&&(EnablePhaseA==1)) //Demag mode of operation
        {
            if(DutyCyleUpdateA==0) //Implement Demag mode PWM
            {
            if(DemagPWMA==1) //Implement Full DemagPWM mode
            {
            sysreg_write(sysreg_IOPG, FIO_Page);//Go to FIO page
            io_space_write(FIO_FLAGC, 0x0200); //Disable MQ2 (PF9) => end of commutation
            //(mag and free mode)
            io_space_write(FIO_FLAGS, 0x0100); //Activate MD2 (PF8) => demag mode
            sysreg_write(sysreg_IOPG, PWM0_Page);
            io_space_write(PWM0_TM, 0x0140); //100kHz PWM Switching Frequency
            io_space_write(PWMO_SEG, 0x00F); //Activate AH and AL)
                            //Enable Phase A PWM outputs, 0 = enable,
                            //1 = disable. only enable phase A
            io_space_write(PWM_SI, 0x0); //Inverts low side outputs, SR Alternate
                    //mode, disables when phase is off
                            //Invert none = 0x0
                io_space_write(PWM0_CTRL, 0x007); //Enable PWM generation with PWMSYNC signal.
                DutyCyleUpdateA = 1. //double update (0x007), single update (0x003
                DutyCyleUpdateA = 1;
            }
            else
            {
                if (DemagPWMA==0) //Disable Full DeMag PWM mode
                    {
                    sysreg_write(sysreg_IOPG, FIO_Page);//Go to FIO page
                    io_space_write(FIO_FLAGC, 0x0300); //Disable MQ2 (PF9) and MD2 (PF8)
                    sysreg_write(sysreg_IOPG, PWMO_Page);
                    io_space_write(PWM0_TM, 0x0140); //100kHz PWM Switching Frequency
                io_space_write(PWMO_SEG, 0x00F); //Activate AH and AL)
                    //Enable Phase A PWM outputs, 0 = enable,
                    //1 = disable. Only enable phase A 0x00F
            io_space_write(PWM_SI, 0x0); //Inverts low side outputs, SR Alternate
                    //mode, disables when phase is off
                    //Invert none = 0x0
                    //Enable PWM generation with PWMSYNC signal.
                    //double update (0x007)
```

```
            DutyCyleUpdateA = 1;
            }
        }
    }
    else; //Do nothing, update duty cycle next time
}
else
    {
        if ((MagFreeDemagA==0)&&(EnablePhaseA==0)) //Shut down Phase A operation
            {
            sysreg_write(sysreg_IOPG, FIO_Page); //Go to FIO page
            io_space_write(FIO_FLAGC, 0x0300); //Disable MQ2 (PF9) and MD2 (PF8)
            sysreg_write(sysreg_IOPG, PWM0_Page); //Go to PWM i/o page
            io_space_write(PWMO_SEG, 0x03F);
            io_space_write(PWM_SI, 0x0);
            io_space_write(PWM0_CTRL, 0x000);
                    /This allow motor control to start pwm again
            DutyCyleUpdateA=0;
            }
        }
    }
}
```

```
//----------------------------------------
//Description: Selects the converter modes of operation magnetisation/freewheeling,
// demagnetisation depending on rotor data
//Inputs:
//Returns
void commutation_four_phase()
{
read_rotor_angle(); //Read current rotor angle
if((AngleMinA<RotorAngle)&&(RotorAngle<=AngleMaxA))
    {
    AngleDemagA=AngleMaxA-AngleDemag; //60
    AngleOffA = AngleMaxA-10; //70
    AngleOnA = AngleMinA+10; //20
    EnablePhaseB=0;
    EnablePhaseC=0
    EnablePhaseD=0;
    if((AngleOnA<RotorAngle)&&(RotorAngle<=AngleDemagA))
        {
        MagFreeDemagA=1; //Implement Phase A Mag/Free mode
        EnablePhaseA=1;
        sysreg_write(sysreg_IOPG, FIO_Page);// Go to FIO page
        io space write(FIO FIAGS, 0x0040);
        io_space_write(FIO_FLAGC, 0x0080); //Disable (PF7) =>1
        }
        else
            {
            if((AngleDemagA<RotorAngle)&&(RotorAngle<AngleOffA))
            {
            MagFreeDemagA=0; //Implement Phase A Demag mode
            EnablePhaseA=1;
            sysreg_write(sysreg_IOPG, FIO_Page);// Go to FIO page
            io_space_write(FIO_FLAGC, 0x0040); //Disable (PF6)
            io_space_write(FIO_FLAGS, 0x0080); //Activate (PF7) =>2
            }
            else
                {
                    MagFreeDemagA=0;
                    EnablePhaseA=0; //Shut down Phase A
                        sysreg_write(sysreg_IOPG, FIO_Page);// Go to FIO page
                    io_space_write(FIO_FLAGS, 0x00C0); //Activate (PF6 & PF7) =>3
                    }
            }
            motor_control_a(); //Activate Phase A PWM current control
        }
}
```

```
//
//Function: read_rotor_angle()
//Description: Determines the rotor position value depending on input pulse combination.
//Inputs:
//Returns:
void read_rotor_angle()
{
    // Go to FIO page
    sysreg_write(sysreg_IOPG, FIO_Page);
    //Get value of PFO Flag
    EnableSRM = io_space_read(FIO_DATA_IN);
    if ((EnableSRM & 0x0003) ==3) //If Signal pulse is high => implement mag and free mode
        {
        RotorAngle = 40; //Constant angle in turn on angle range
        }
        else
            {
                if ((EnableSRM & 0x0003) ==1) //If Signal pulse is low => implement demag mode
                    {
                    RotorAngle = 75; //Constant angle in turn off angle range
                    j=0;
                    }
                    else
                            { //Shut down phase operation
                            RotorAngle = 75; //Constant off angle
                                j=0;
                    }
                }
}
```

